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Fundamentals of Using Cracked Film Lithography to Pattern Transparent Conductive Metal Grids for Photovoltaics

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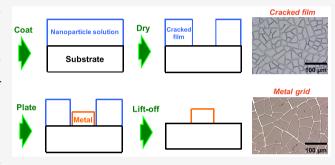
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ABSTRACT: The fundamentals of using cracked film lithography (CFL) to fabricate metal grids for transparent contacts in solar cells were studied. The underlying physics of drying-induced cracks were well-predicted by an empirical correlation relating crack spacing to capillary pressure. CFL is primarily controlled by varying the crack template thickness, which establishes a three-way tradeoff between the areal density of cracks, crack width, and spacing between cracks, which in turn determine final grid transmittance, grid sheet resistance, and the semiconductor resistance for a given solar cell. Since CFL uses a lift-off process, an additional constraint is that the metal thickness must be less than 1/3 of the crack



template thickness. The transmittance/grid sheet resistance/wire spacing tradeoffs measured in this work were used to calculate solar cell performance: CFL-patterned grids should outperform screen-printed grids for narrow cells (0.5-2 cm wide) and/or cells with high semiconductor sheet resistance ($\geq 100 \Omega/\text{sq}$), making CFL attractive for monolithically integrated thin-film photovoltaic modules.

INTRODUCTION

The transparent conduction performance of metal grids has a unique advantage over transparent conductive oxides (TCOs): Their thicknesses can be increased until grid resistance becomes negligible, without any penalty in transmittance.1 Theoretical investigations have further shown that all photovoltaic (PV) absorber technologies can benefit from improving metal grids.^{2,3} In spite of this promise, to date there is no scalable process for fabricating high-performance grids, outside of the high-temperature fired metal inks used in most Si modules. The industry-standard Ag inks suffer from low aspect ratios (height/width of 0.1-0.3) and minimum wire widths of \sim 50 μ m. Increasing the aspect ratio and decreasing the wire width stands to improve performance in Si as well as other PV absorbers. As wire width is narrowed, wire spacing can be reduced at a given transmittance, which diminishes the resistive loss in the semiconductor. Thus, there is a need for a low-cost way to fabricate metal macro- and microgrids.

First reported in 2013,5,6 cracked film lithography (CFL; see schematic in Figure 1) is a technique for patterning metal grids that have several advantages over alternative transparent conductors: (1) Metal grids are grown directly on substrates, leading to high quality semiconductor/metal interfaces, (2) metal can be solution-7 or electrodeposited8 to keep the process vacuum-free, allowing fast fabrication times (ca. 5 min) and low capital expenditure, and (3) wires down to $\sim 0.7 \mu m$ can be patterned (with $\sim 8 \mu m$ spacing), which accommodates highly resistive semiconductor substrates while avoiding the issue of accelerated degradation in nanowires. 9 In particular, metal wires with nanometer-scale diameters are known to have poor short- and long-term durability due to Joule heating, quantum-confinement-induced melting point depression, and high surface area/volume ratios that lead to failure through corrosion. 10-12 These CFL assets suggest that, despite being solution-grown, CFL-patterned grids can improve on the performance/durability of solution-synthesized Ag nanowires. 13-16 Additionally, CFL metal microgrids can act as an intermediate between TCOs and metal macrogrids, where hierarchies are a well-known route to better transparent conduction.

As mentioned above, CFL grids can be low-cost and should have durability similar to typical metal grids in PV modules. However, CFL has only been used in relatively lowperformance solar cells so far (13.8% hybrid organic-inorganic perovskite (0.09 cm²),¹⁷ 11.2% monocrystalline Si,¹⁸ 5.9% amorphous Si, 19 4.5% dye-sensitized, 20 and 2.3% organic 21). Thus, there is a gap in the knowledge base which this study has begun to fill by identifying the limits of controlling crack behavior, transferring the pattern to metal grids, and how these affect final transparent conduction performance. The following

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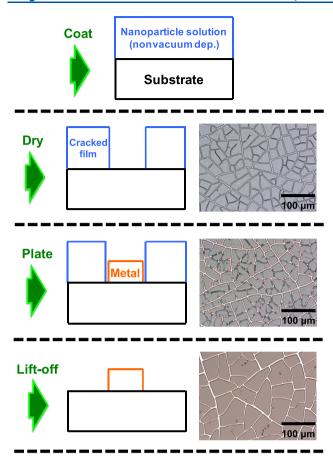


Figure 1. CFL schematic, with micrographs showing a crack template, the template after electroplating metal, and the grid after template lift-off.

features of CFL were identified as critical to limiting its performance: Crack template thickness controls the crack width, crack spacing and maximum metal thickness allowable for quality lift-off. In turn, these three parameters determine the transmittance and sheet resistance of the metal grid, as well as specifying what semiconductor resistance would be incurred between the grid lines for a given application. In this way, template thickness constrains CFL to a three-way tradeoff of transmittance/grid sheet resistance/wire spacing. In spite of this fundamental limitation, the transmittance/sheet resistance tradeoffs measured at given wire spacings in this work are still highly attractive for PV, particularly monolithically interconnected thin-film modules.

EXPERIMENTAL SECTION

 ${
m TiO_2}$ nanoparticles ("P25" or "aeroxide"; 21 nm primary particle diameter) were purchased from Fisher Scientific and mixed with deionized (DI) water to form a 30% wt/vol suspension. Surfactant-free polystyrene (PS) nanoparticle (80 \pm 20 nm diameter) suspensions were obtained from Magsphere, Inc. (Pasadena, CA). The as-purchased solutions were concentrated to 30% wt/vol by allowing the water solvent to evaporate off over the course of days. Poly(methyl methacrylate) (PMMA) nanoparticle (40–80 nm diameter 23) suspensions were purchased from Jinhua Mengni Cosmetics Co., Ltd. (Zhejiang, China). The solutions, sold as "crackle nail polish," were diluted to 30% wt/vol by adding DI water. To reduce agglomeration, TiO2 suspensions were sonicated for >20 min before using, and then used within 20 min. The polymer suspensions were not sonicated. The crack templates were blade coated, and the thickness of the final TiO2 templates was controlled

by adjusting the blade height from 50 to 350 μ m. The polymer suspensions had much lower viscosity, so final thickness was dominated by the volume of solution that was blade-coated, relative to the area of the substrate (2.6–9.0 μ L/cm²). Soda-lime glass (SLG) substrates were cleaned by sonication in warm Liquinox solution, DI water rinse, and final rinsing in a spin-rinse-dryer. Just before crack template coating, substrates were O2 plasma-cleaned for 15 min. After coating, suspensions dried in seconds. Solvent evaporation rate was estimated by measuring the evaporation rate of water from Petri dishes over the course of hours $(1.8 \times 10^{-8} - 3.9 \times 10^{-7} \text{ m/s})$. depending on air flow). Cu was deposited by e-beam evaporation (TiO2 and PMMA). For PS templates, Cu was DC sputtered to enhance pattern transfer fidelity. Lift-off was performed by immersing the samples in water (for TiO2) or tetrahydrofuran (for PS and PMMA) and sonicating for 30-60 s. These lift-off procedures were found to be the most widely successful, although rinsing with acetone was sufficient for lifting off many polymer templates. Stylus profilometry was used to determine template and metal thicknesses (Dektak 8). Ultraviolet-visible spectroscopy was used to measure transmittance of samples at 300-1350 nm (Cary 5000). The transmittance of baseline glass substrates was used to calculate the transmittance of the grids themselves $(T_{grids} = T_{measured}/T_{substrate})$. Optical micrographs were captured with a digital camera at 30-5000× magnification (Keyence) on an antivibration table. The crack/ wire width/spacing was quantified by binarizing micrographs and applying a Euclidean distance transform function to map the maximum wire and spacing width pixel by pixel. Sheet resistance was measured with a noncontact eddy current measurement system with sensitivity down to $10^5\ \Omega/\text{sq}$ (Delcom). The noncontact measurements were validated by soldering indium pads to the grids and measuring sheet resistance in a van der Pauw configuration.

For the electroplating demonstration, Tec 15 glass (with an F:SnO₂ coating; purchased from Pilkington) was coated with PMMA templates, prebaked in air at 130 °C for 5 min, ¹⁸ and then immersed in bright Cu electroplating solution (obtained from Millipore Sigma). Plating lasted 30 s at 4 V and 140 mA/cm² with a cathode-to-anode distance of 3 cm. For the substrate surface energy micrograph data, TiO₂ solutions with improved wetting (10% vol/vol dimethyl sulfoxide) were drop-cast onto substrates of SLG, SLG coated with RF sputtered Al:ZnO, and F:SnO₂ (Tec 15) that had or had not been O₂ plasma-cleaned for 15 min. For the surface energy on SLG substrates, 30 μ L of the sonicated TiO₂-water suspension was dispensed, and a goniometer was used to extract the contact angle from a digital camera image. The cracked films were coated using a blade height of 100 μ m and velocity of 16 mm/s.

■ RESULTS AND DISCUSSION

Physics of Cracking. There have been many investigations into the cracking behavior of drying films.²⁵ The concept of drying-induced cracking is relatively straightforward: Solvent evaporation contracts the film's volume, leading to stress that is relieved through the formation and growth of fractures. Nevertheless, casting the physical situation in a framework with widespread applicability and utility has proven difficult. Lee and Routh performed an analysis that scaled crack spacing and capillary pressure, finally arriving at an empirical fit to data spanning 4 orders of magnitude.²⁶ Importantly, their simple model used readily available parameters to predict crack spacing:

scaled capillary pressure =
$$\frac{20}{75} \left(\frac{3\gamma \mu_{\text{disp}}}{E} \right)^{1/2} \frac{R(1-\phi)^2}{\mu_{\text{solv}} \phi^2 H}$$
(1)

scaled crack spacing =
$$\frac{75 y \mu_{\text{solv}} \phi^2}{20R(1-\phi)^2} \left(\frac{E^3}{3\mu_{\text{disp}} \gamma^3}\right)^{1/4}$$
(2)

Here, γ is solvent surface tension, $\mu_{\rm disp}$ is dispersion viscosity (assumed to be that of the water solvent), R is particle radius, φ is final particle volume fraction (assumed to be that of close packing = 0.64), E is solvent evaporation rate, $\mu_{\rm solv}$ is solvent viscosity, H is dried film thickness, and y is crack spacing. After measuring evaporation rate and final film thickness, the scaled crack spacing and capillary pressure were calculated for this study's PS, PMMA, and TiO₂ nanoparticle suspensions. The results are compared with the empirical fit from Lee and Routh in Figure 2. Weldon et al. recently expounded on that model

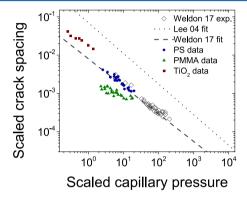


Figure 2. Scaled crack spacing as a function of scaled capillary pressure (defined in eqs 1 and 2): Previous experimental data (hollow black diamonds),²⁷ original empirical fit (dotted line),²⁶ empirical fit to two-dimensional drying fronts (dashed line),²⁷ and this study's PS (blue circles), PMMA (green triangles), and TiO₂ data (red squares).

by investigating a different cracking regime: Two-dimensional drying fronts, which have a modified characteristic fluid velocity.²⁷ That work extracted a similar empirical fit using the same dimensionless parameters. The PS data measured in this work were fit particularly well with that correlation, while the TiO₂ and PMMA data deviated somewhat. Together, these correlations fit vast data sets, suggesting that the analysis assumptions were appropriate as well as being well-suited to regimes useful for transparent conduction applications. Despite the simplicity of eqs 1 and 2, there are implicit interdependencies which are not always obvious. For instance, changing solvent affects surface tension, viscosity, and evaporation rate, but it can also affect dried film thickness and the stability of the suspension, the latter of which can alter agglomeration and the effective particle radius. Therefore, the exploitation of these correlations for more sophisticated cracking control strategies will require experimental validation.

Template Thickness and Material Control CFL. Changing the crack template thickness is the primary means of controlling CFL.^{23,28} As template thickness is increased, cracks and crack spacings get wider (Figure 3). This boosts the total crack footprint, or areal density, leading to lower transmittance and sheet resistance of the final metal grid. Transmittance of the final grid was found to correlate better with crack spacing (relative to crack width or template thickness; Figure 4). As expected, transmittance did not vary with light wavelength (Figure S1). This broadband transmittance gives the grids an advantage over TCOs, which

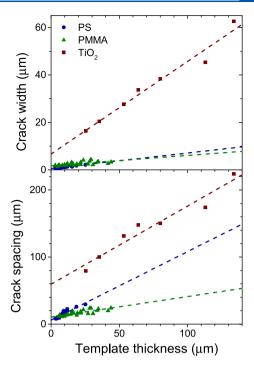


Figure 3. Crack width (top) and spacing (bottom) as a function of crack template thickness for PS (blue circles), PMMA (green triangles), and ${\rm TiO_2}$ (red squares). Dashed lines are linear least-squares fits to each material's data.

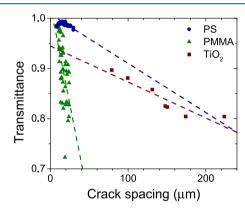


Figure 4. Transmittance (450–890 nm) of the final grids after lift-off, as a function of crack spacing in the template for PS (blue circles), PMMA (green triangles), and ${\rm TiO_2}$ (red squares). Dashed lines are linear least-squares fits to each material's data.

absorb the near-infrared wavelengths that are critical to narrow band gap PV absorbers.²⁹

Every crack template material has a critical cracking thickness, below which no cracks form. As the Young's modulus of the crack template material is increased, its critical cracking thickness increases. ^{30,31} In practice, this means that the TiO₂ suspensions (~100 GPa Young's modulus ³²) had thick crack templates (25–140 μ m) that led to less transparent grids (T=0.8-0.9) with wider spacings (80–220 μ m) and lower sheet resistance. PS and PMMA templates (3–4 GPa Young's moduli ³³) had much thinner crack templates (3–45 μ m), accessing higher transmittance grids and smaller wire spacing (8–30 μ m) at the expense of sheet resistance (Figure 5). The PS templates had slightly narrower crack widths and slightly wider crack spacings than the PMMA templates, leading to superior transmittance. This difference is also

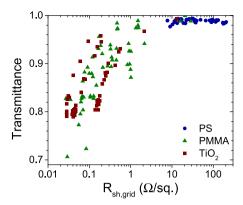


Figure 5. Transmittance (450–890 nm) as a function of grid sheet resistance for PS (blue circles), PMMA (green triangles), and TiO_2 (red squares).

observable in the shift from PS to PMMA in Figure 2 and is not predicted by eqs 1 and 2. It may relate to incorrect estimates for the equations' inputs (the PMMA solution has proprietary components) or to the particular properties of these nanoparticles (e.g., the surfactant-free PS is suspended with surface sulfate groups). Similar to crack footprint, the ratio of crack width to crack spacing is a measure of lateral strain relieved in the film. These data are in Figure S2. The lower ratio of crack width to spacing observed for PS, relative to PMMA, may trace to the former being more brittle.³⁴ Future work is needed to elucidate why PS had higher transmittance than PMMA in this work and, more generally, how crack spacing can be varied independently from crack width. The data in Figure 5 should not be directly compared to TCO transmittance/sheet resistance trade-offs because: (1) TCO transmittance depends on the substrate (unlike grids), (2) TCO transmittance has wavelength dependence, so the choice of wavelength range biases the comparison (with longer wavelengths favoring grids),³⁵ and (3) grids have nonun-iformity that induces more resistance in the contacted semiconductor (unlike TCO films).

Substrate-Template Interaction. The cracking model discussed above does not explicitly account for the template's material properties or its interaction with the substrate. As suggested by Lee and Routh, the refinement of this simple model may come from a more accurate estimate for capillary pressure.²⁶ Instead of using the maximum possible capillary

pressure, the actual yield stress, although difficult to access, would be more accurate. Indeed, it was observed in this work that substrate surface energy had a strong effect on cracking behavior. The effect was first observed for different substrates: The micrographs in Figure 6 show that moving from F:SnO₂ to Al:ZnO to SLG substrates narrowed the cracks and crack spacing (the final grid networks are shown to enhance contrast). O₂ plasma-cleaning prior to drop-casting reduced the crack width for all three substrates as well. These data suggest that the interaction between the drying film and the substrate affects cracking, possibly through altering yield stress.

Increasing the duration of a plasma clean on SLG substrates also systematically decreased crack width and spacing, increasing transmittance (Figure S3). For Figure S3, TiO, nanoparticles suspended in water were blade-coated onto SLG that had been plasma-cleaned for various durations. The plasma-clean decreased the solid-liquid interfacial energy, as evidenced by the decreasing contact angle. Combined, Figures 6 and S3 show that the template-substrate interaction effect is independent of the film deposition method. A previous investigation proved that particle-substrate interactions in drying colloidal films changed cracking behavior.³⁶ They found that more favorable interfacial energies decreased the critical stress intensity factor, making cracking more likely (increased number of cracks with narrowed widths). In the present study, improved interfacial energy also narrowed crack width and spacing, leading to greater transmittance. Therefore, to achieve similar crack templates on substrates with poor wetting, thinner films should be deposited.

The substrate—template interaction affects cracking because interfacial energy dictates the maximum shear stress between the substrate and film, which sets the lateral stress at failure. After cracking, the adhesion of the template to the substrate also sets an upper limit to how thick crack templates can be. Above a certain thickness, cracked films tend to delaminate before they can be used as templates. To correct for this, polymer templates can be subjected to heating to improve adhesion. ¹⁸

Crack Aspect Ratio. The ${\rm TiO_2}$ templates had cracks with low aspect ratios (height/width), relative to PS and PMMA (Figure S4). For a given crack width, the PS templates had higher crack aspect ratios. The combination of narrow cracks with high aspect ratios led to broken wires after lift-off when metal was evaporated. On the other hand, when metal was evaporated onto a rotating substrate or sputtered, the PS

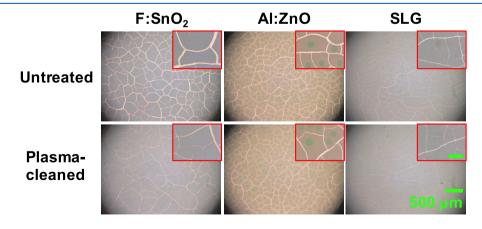


Figure 6. Metal grids patterned by TiO_2 templates, where the substrate surface (F:SnO₂, Al:ZnO, or SLG) and preparation (untreated or plasmacleaned) strongly affected the crack/wire width. Inset scale bar is 100 μ m.

cracks became more completely "filled" with metal (Figure S5). This reduced the number of broken wires and greatly enhanced conductivity. This same effect was observed on switching from stationary evaporation to evaporation onto a rotating substrate, sputtering, or electroplating, where reducing directionality of the arriving metal atoms improved PS's pattern transfer fidelity.

Metal Thickness is Constrained. For CFL to be successful, the deposited metal must be thinner than the crack template, otherwise lift-off can fail through grid delamination, incomplete lift-off or metal flagging. The former leads to holes in the grid networks and high sheet resistance,³ while the latter two behaviors reduce transmittance. To explore the practical limits of this constraint, the maximum metal thickness at which lift-off is successful was examined for PMMA and PS templates of varied thicknesses (the TiO₂ templates were too thick). In spite of the noise and nonreproducibility associated with measuring lift-off failure, the maximum metal thickness/template thickness ratio was consistently 1/3 (Figure S6). These measurements set a limit to how conductive CFL grids can ultimately be. Finally, the extra constraint's effect on the transmittance/sheet resistance/ wire spacing tradeoff is illustrated schematically in Figure S7.

CFL for Solar Cells. The architecture of a typical solar cell is in Figure S8, showing how light enters the absorber by passing through the space between grid wires, while electrical current must be transported laterally through the semiconductor to the wires for collection. The data collected in this study were used to predict transparent conduction performance in solar cells. Traditional transparent conduction figures of merit are not informative for metal grids because they are nonuniform, making more involved calculations necessary. Linear regression was used to correlate crack spacing with transmittance (Figure 4). Next, grid sheet resistance and transmittance were correlated for each material by assuming the grids had an idealized square shape, such that

$$T = \left(1 - \frac{(\rho/h_{\text{metal}})C}{R_{\text{sh,grid}}}\right)^{2}$$
(3)

Here, T is transmittance, ρ is metal resistivity $(1.68 \times 10^{-6} \ \Omega)$ cm), h_{metal} is metal thickness, C is a constant that was fit to the data to account for the actual grid geometry (1.36 for TiO2) 1.62 for PMMA, and 9.87 for PS), and $R_{\text{sh,grid}}$ is grid sheet resistance. For each material, the C constants were first fit to multiple metal thickness data sets simultaneously (Figure S9). A metal thickness was then chosen for each material such that a single function was used for all of the data (Figure S10). While the CFL grid data were imperfectly fit by the ideal square equations, they nevertheless provided the appropriate dependencies for modeling transparent conduction tradeoffs. Next, the procedure outlined by Muzzillo³ was followed to calculate resistive power loss density for lateral current transport through a semiconductor with given sheet resistance $(R_{\text{sh,semic}})$ and short-circuit current density $(J_{\text{SC}} = 40 \text{ mA/cm}^2)$ at a given wire spacing for an idealized square grid shape. The semiconductor would commonly be a highly doped emitter, contacting layer, or TCO. The same procedure was followed for a grating-shaped grid to model a baseline screen-printed grid. Resistive power loss density for lateral current transport through the metal grid was taken as³⁸

$$P_{\text{loss,Rgrid}} = \frac{R_{\text{sh,grid}} L^2 J_{\text{SC}}^2}{3} \tag{4}$$

where L is solar cell length. One strength of CFL is that it is etch-free, while a weakness is that it requires extra processing 39,40 to planarize grids—both of these features make CFL well-suited to front grids on substrate and back grids on superstrate solar cells. Therefore, a low-temperature screen-printed grating was taken as a relevant baseline: A wire width of 50 μ m, metal thickness of 12 μ m, and metal resistivity of $2.6 \times 10^{-6} \ \Omega \cdot \text{cm}$ were assumed. Finally, the power loss density due to grid shadowing was roughly estimated:

$$P_{\text{loss},T} = (1 - T)J_{\text{SC}}V_{\text{OC}}FF \tag{5}$$

 $V_{\rm OC}$ and FF are the solar cell's open-circuit voltage and fill factor, respectively (700 mV and 80%). Example power loss densities resulting from semiconductor resistance, grid resistance and shadowing are shown for the screen-printed grating baseline and ${\rm TiO_2}$ -patterned CFL grids as a function of grid transmittance in Figure S11. As can be seen, the CFL grids' narrower wires and spacings exchange negligible grid resistance for negligible semiconductor resistance, leading to lower total power loss density at high transmittances.

Next, the total power loss density was minimized with respect to transmittance. Since crack spacing and grid sheet resistance were functions of transmittance for each material (Figures 4 and S10), specifying transmittance is equivalent to specifying the transmittance/wire spacing/grid sheet resistance three-way tradeoff. The minimum total power loss density was calculated for each CFL template material and the screenprinted grating baseline as a function of solar cell length at semiconductor sheet resistances of 10, 100, and 1000 Ω/sq (Figure 7). These performance estimates show that, for narrow solar cells and high semiconductor sheet resistances, CFL grids can beat screen-printing performance. Thus, CFL grids should be useful for monolithically integrated thin-film modules: CdTe, ⁴¹ Cu(In,Ga)(Se,S)₂, ²⁹ and hybrid organic—inorganic perovskites⁴² have monolith widths of 0.6, 0.5, and 0.4-0.7 cm, respectively. Moreover, decreasing thin-film solar cells' TCO thicknesses stands to increase current density, 29 while the introduction of CFL grids would recoup the resistive losses. A schematic in Figure S12 shows how CFL can be performed after TCO deposition, followed by P3 scribing to complete monolithic integration. A typical grid-free module has a TCO with 10 Ω /sq, gridded cells/modules permit TCOs with 100 Ω/sq , while buffer layers and the thinnest possible TCOs have 1000 Ω /sq sheet resistances. Crucially, Figure 7 demonstrates that CFL can outperform traditional transparent conduction approaches in thin-film PV modules.

CONCLUSIONS

The fundamentals of using CFL to pattern metal grids for transparent conduction in solar cells were explored. Crack spacing was well-correlated with capillary pressure after proper scaling. Changing the crack template thickness is the primary means of controlling the three-way tradeoff important for PV applications: Thinner templates had lower crack footprints, narrower cracks, and narrower crack spacings, leading to higher metal grid transmittance, higher grid sheet resistance, and lower resistance induced in the contacted semiconductor. Successful lift-off required that the metal thickness be less than 1/3 of the crack template thickness, further constraining grid

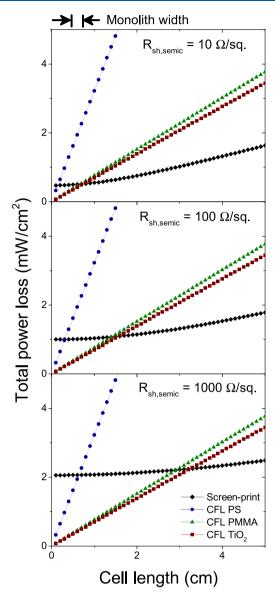


Figure 7. Total power loss density optimized with respect to grid transmittance and shown as a function of solar cell length for the screen-printed grating baseline (black diamonds) and PS- (blue circles), PMMA- (green triangles), and TiO_2 -patterned CFL grids (red squares) at a semiconductor sheet resistance of $10~\Omega/\text{sq}$ (top), $100~\Omega/\text{sq}$ (middle), and $1000~\Omega/\text{sq}$ (bottom).

sheet resistance. Grid and semiconductor resistances were calculated for solar cell applications, and the CFL-patterned grids fabricated in this work were predicted to reduce power loss, relative to screen-printed grids, for narrow solar cells (0.5–2 cm wide) and resistive semiconductors ($\geq \! 100~\Omega/\mathrm{sq}$), making them well-suited to monolithically integrated thin-film PV modules.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.langmuir.0c00276.

Wavelength-dependent transmittance, crack width to spacing ratio, grid properties as a function of contact angle, crack aspect ratio, micrographs of grids with different metal deposition processes, metal-to-template thickness ratio at which lift-off fails, schematic of CFL limitations, solar cell schematic, transmittance data as a function of sheet resistance, calculated power loss densities as a function of transmittance, and monolithic integration schematic (PDF)

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Notes

The authors declare no competing financial interest.

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