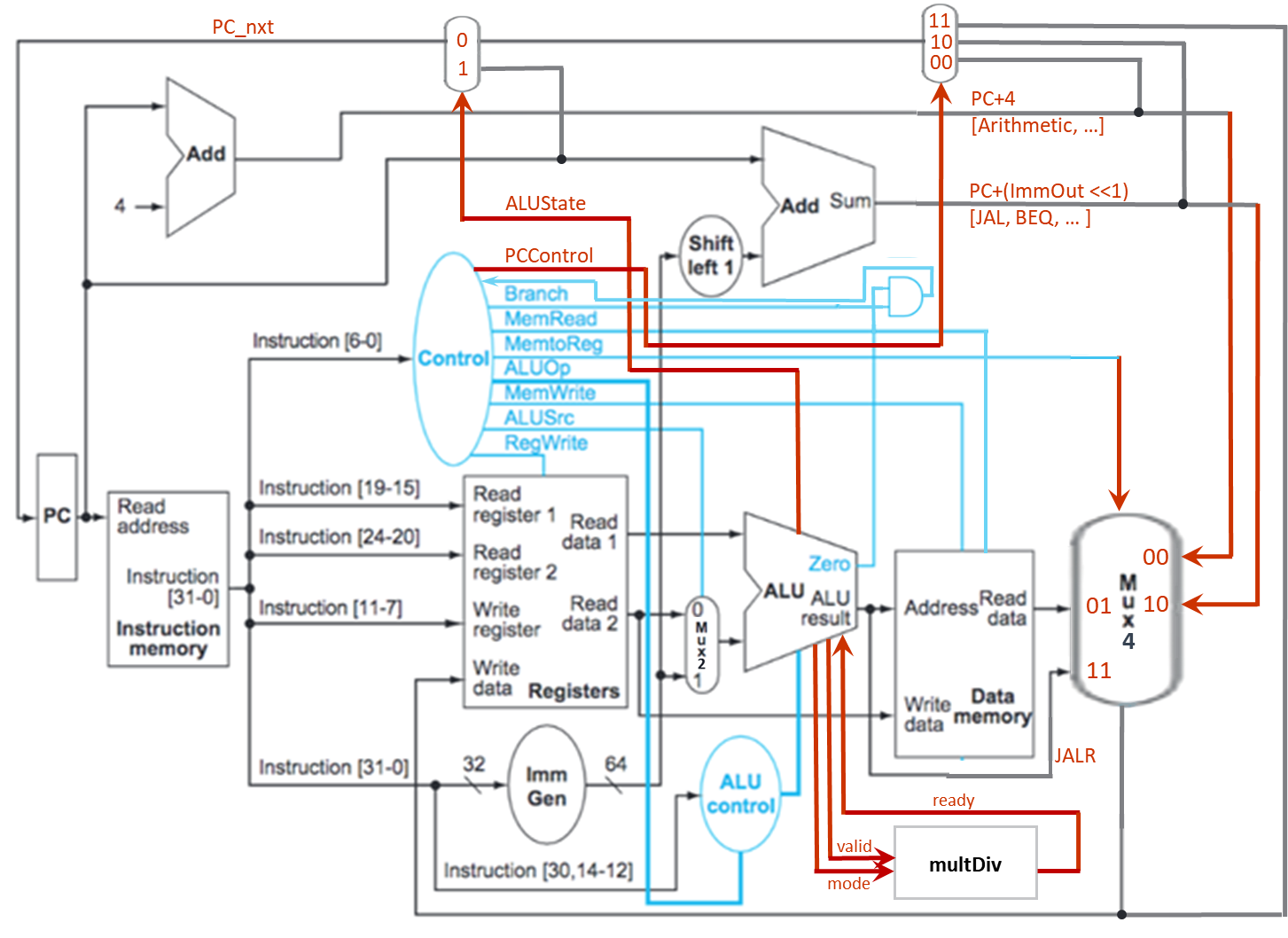
Computer Architecture

Final Project Report

2020/7/3

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1. CPU Architecture



1. Data path of instructions
2. R-TYPE

The R-TYPE instructions include ADD, SUB, SLL, SLT, SLTU, XOR, SRL, SRA, OR, and AND.

1. I-TYPE

The I-TYPE instructions include ADDI, SLTI, SRLI, SRAI, etc.

1. B-TYPE

The B-TYPE instructions include BEQ and BNE.

1. LI-TYPE

The LI-TYPE instructions are such as LW, etc.

1. S-TYPE

The S-TYPE instructions are such as SW, etc.

1. U-TYPE

The U-TYPE instructions are such as AUIPC, etc.

1. J-TYPE

The J-TYPE instructions are such as JAL, etc.

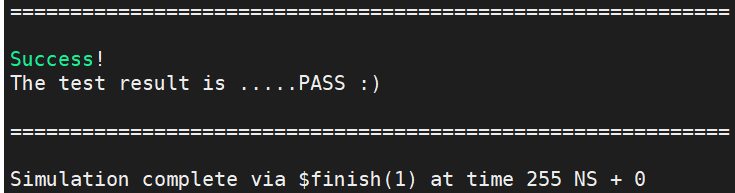
1. JI-TYPE

The JI-TYPE instructions are such as JALR, etc

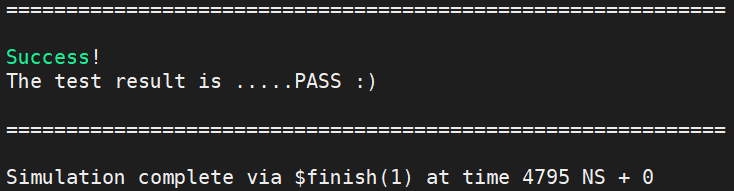
1. Multi-cycle instructions

//todo

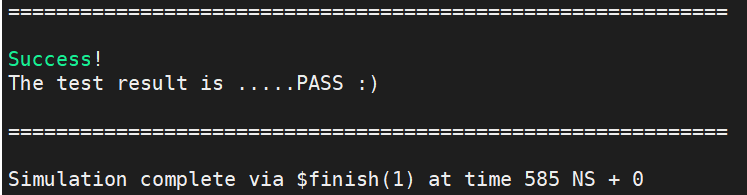
1. Total simulation time
   1. Leaf: a = 1, b = 9, c = 2, d = 2



* 1. Fact: n = 10



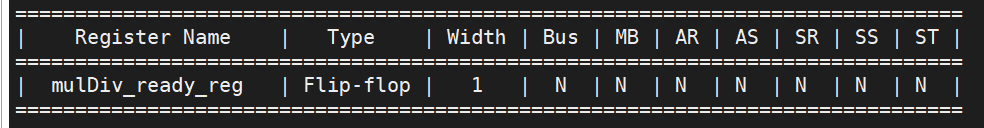
* 1. (Bonus) HW1: n = 10



1. Observation

//todo

1. Snapshot of the “Register Table”



1. Work distribution

|  |  |  |
| --- | --- | --- |
|  | 陳冠豪 | 王世全 |
| CHIP.v | V | V |
| Control.v | V | V |
| Alu\_Control.v | V | V |
| Alu.v | V | V |
| Imm\_Gen.v | V |  |
| Mux.v | V |  |
| leaf | V | V |
| fact | V | V |
| hw1 | V | V |
| Report |  | V |