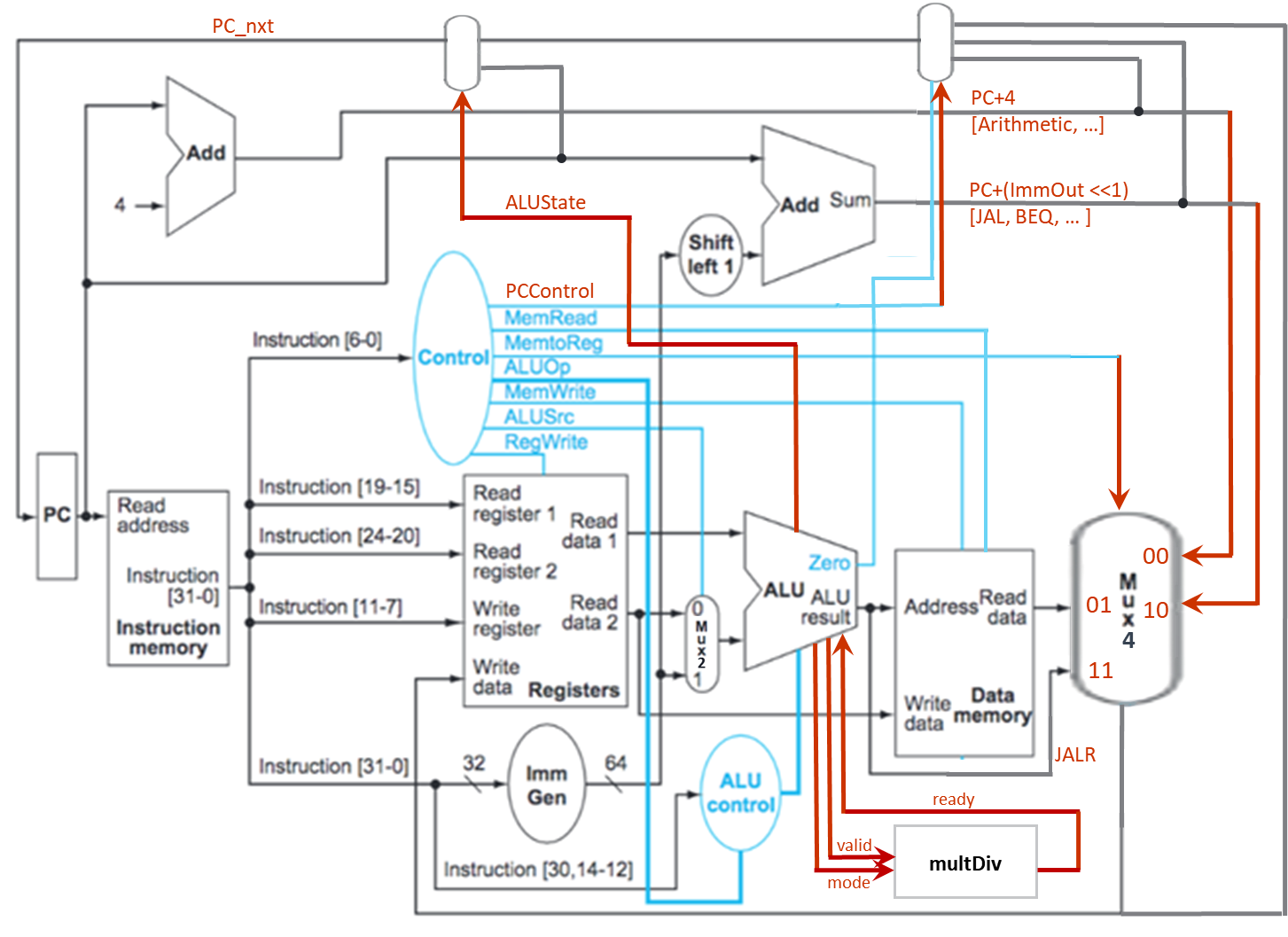
Computer Architecture

Final Project Report

2020/7/3

B05901168 陳冠豪 D07921016 王世全

1. CPU Architecture



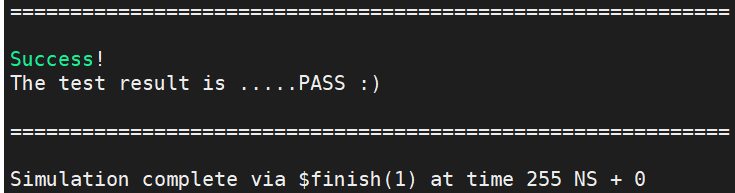
1. Data path of instructions

//todo

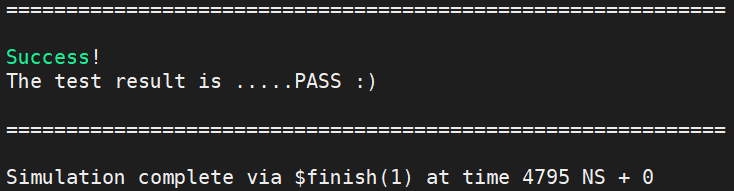
1. Multi-cycle instructions

//todo

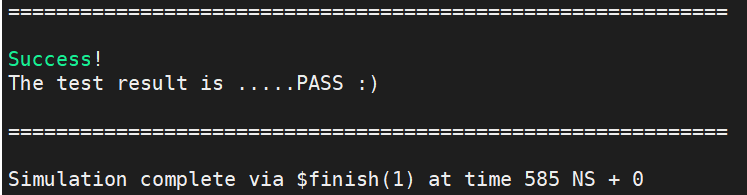
1. Total simulation time
   1. Leaf: a = 1, b = 9, c = 2, d = 2



* 1. Fact: n = 10



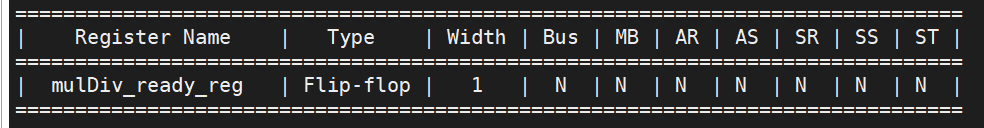
* 1. (Bonus) HW1: n = 10



1. Observation

//todo

1. Snapshot of the “Register Table”



1. Work distribution

|  |  |  |
| --- | --- | --- |
|  | 陳冠豪 | 王世全 |
| CHIP.v | V | V |
| Control.v | V | V |
| Alu\_Control.v | V | V |
| Alu.v | V | V |
| Imm\_Gen.v | V |  |
| Mux.v | V |  |
| leaf | V | V |
| fact | V | V |
| hw1 | V | V |
| Report |  | V |