Fetch Decode Execute

PC

Read address

Instruction [31–0]

Instruction memory

Add

4

Instruction [31–21]

Instruction [9-5]

Instruction [20-16]

Instruction [4-0]

Instruction [31-0]

Immediate Vals

Control

Reg2Loc
Uncondbranch
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite

Mux
0
1

Read register 1
Read register 2
Write register
Write data

Registers

Read data 1
Read data 2

32 Sign-extend 64

Instruction [31–21]

Add ALU result

Shift left 2

ALU ALU result

Zero

ALU control

Mux
0
1

Address Read data

Write data **Data memory**

Mux
1
0

Mux
0
1