Proximity Alarm System
FPGA VHDL

Tomin Mattam

Figure 1: RTL View

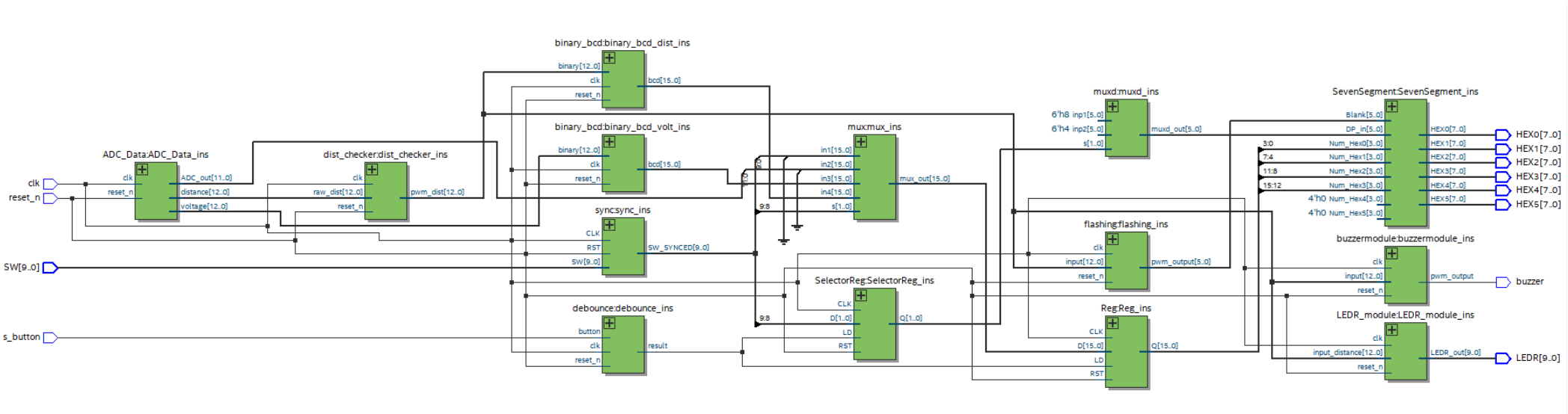

Figure 2: Timing Analysis and Fmax Summary

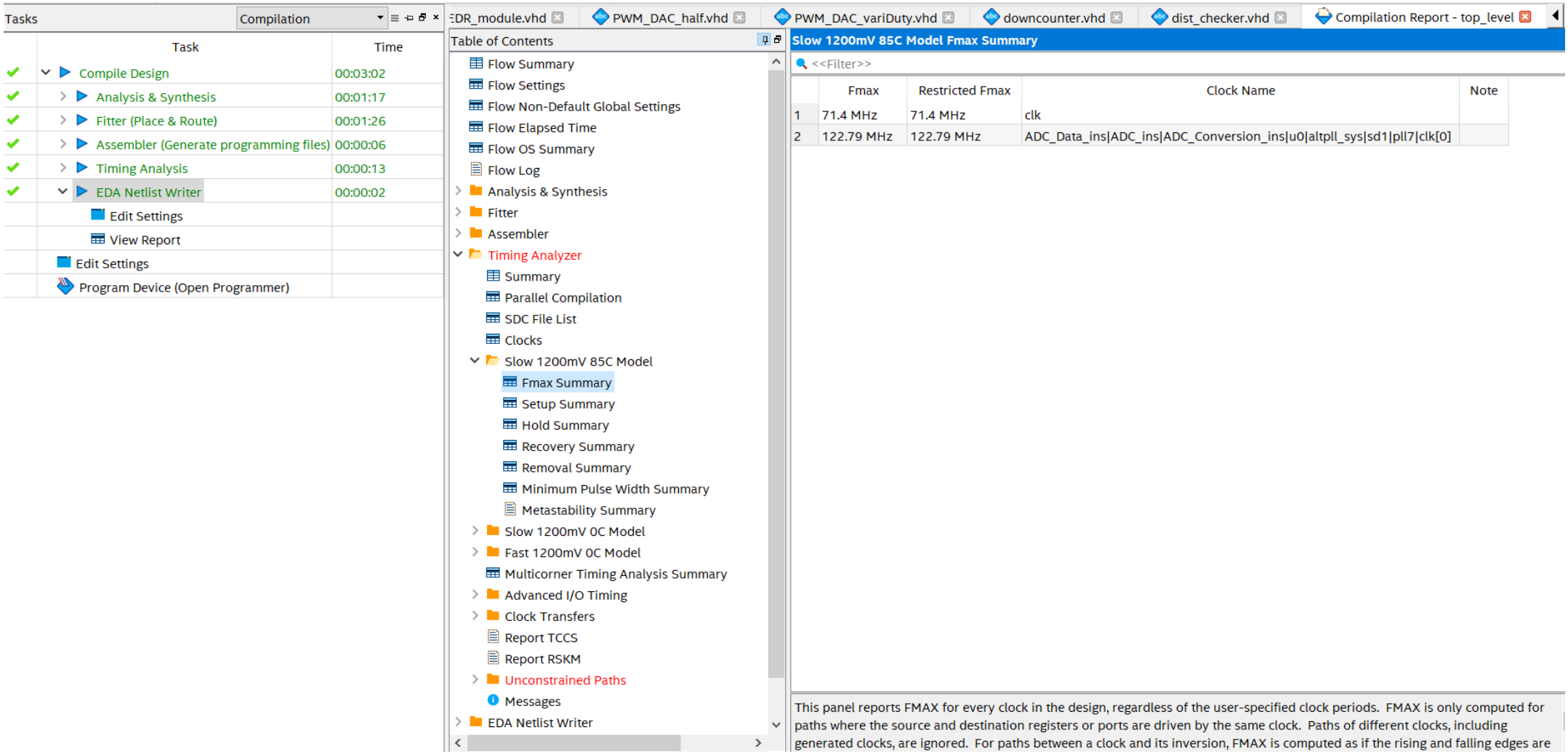

Figure 3: Warning Messages

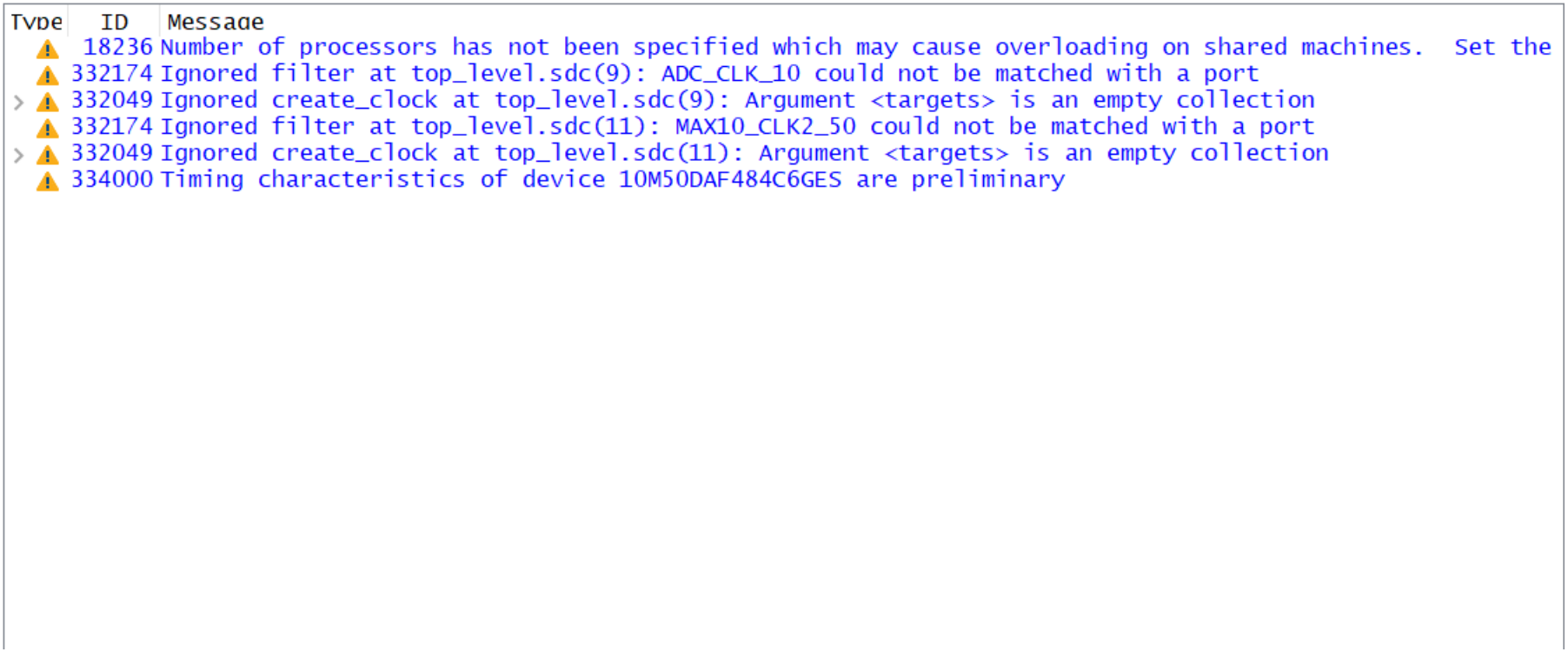

Figure 4: Top Level Simulation 1 at 24.64 cm

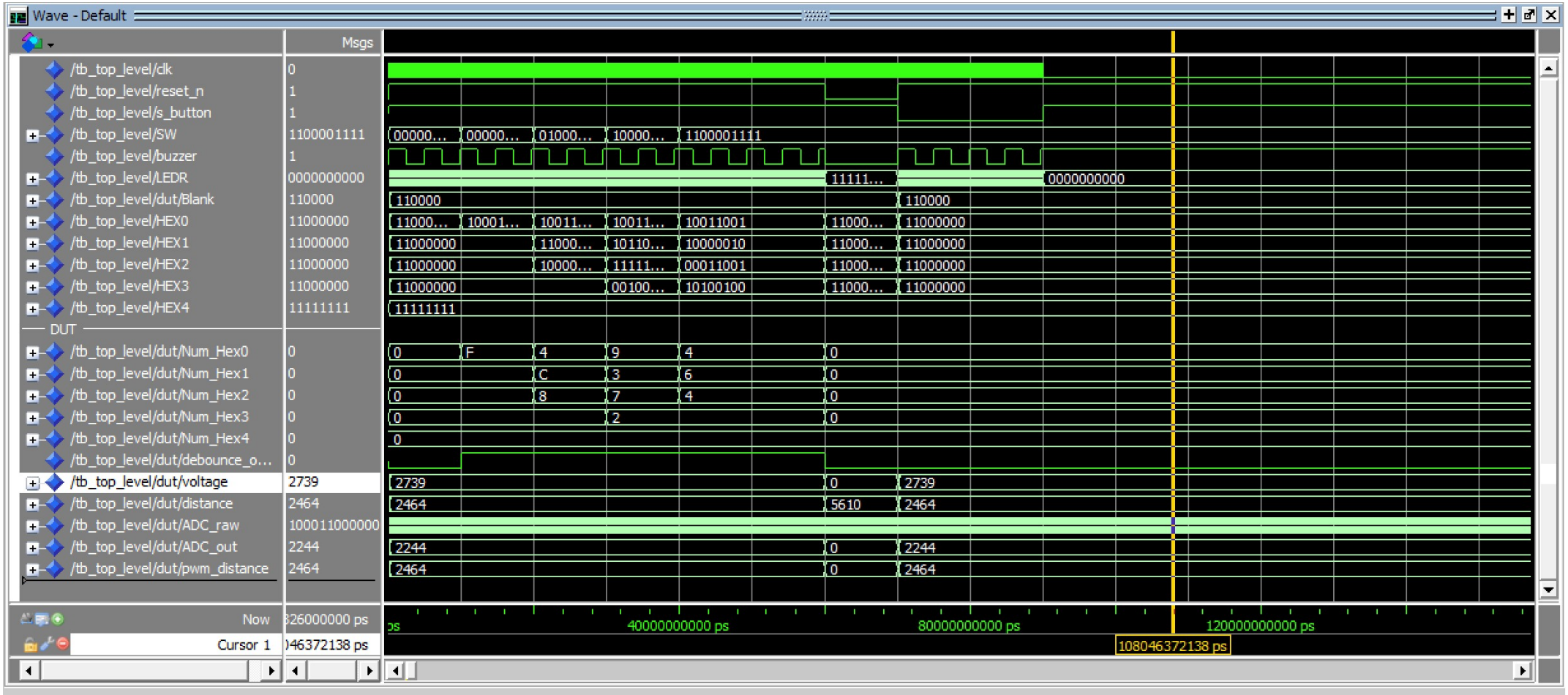

Figure 5: Top Level Simulation 2 at 7.24 cm

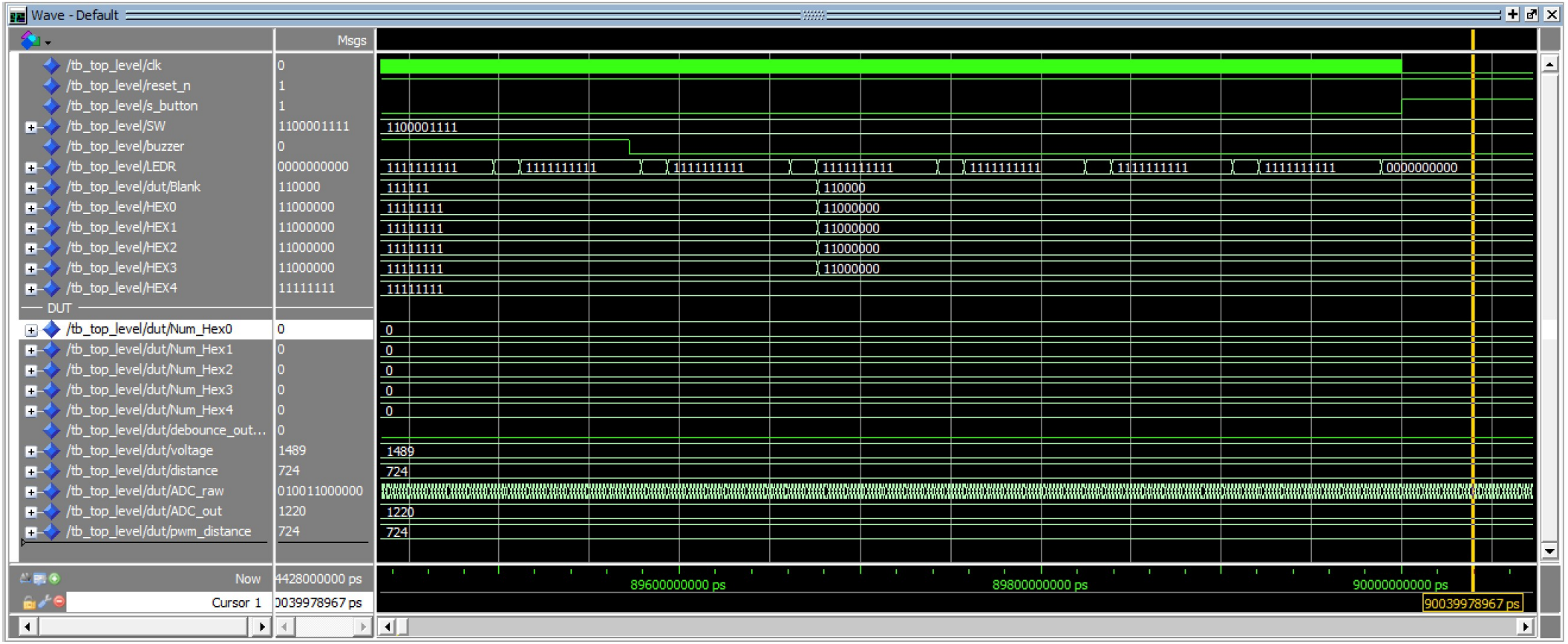

Figure 6: Top Level Simulation 3 at 66.74 cm

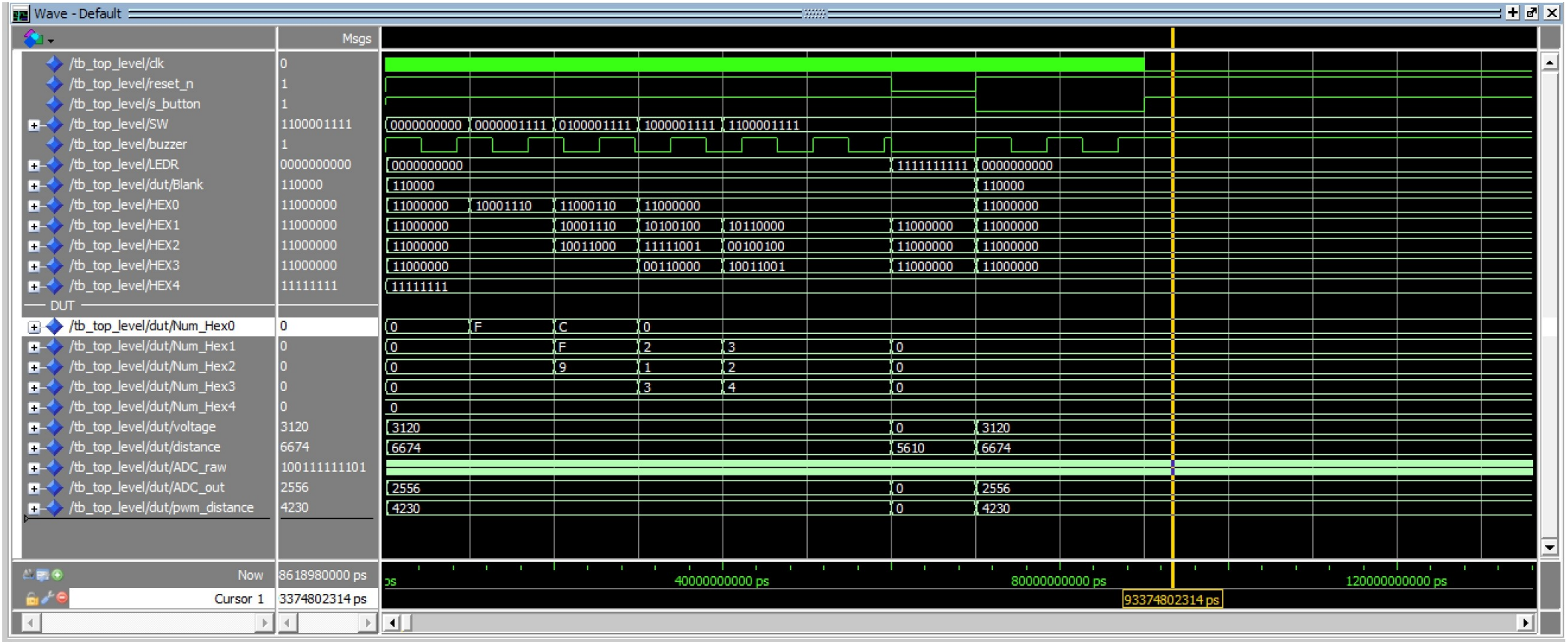

Figure 7: Pulse Width Modulation Varying Duty Cycle used for LEDR Module

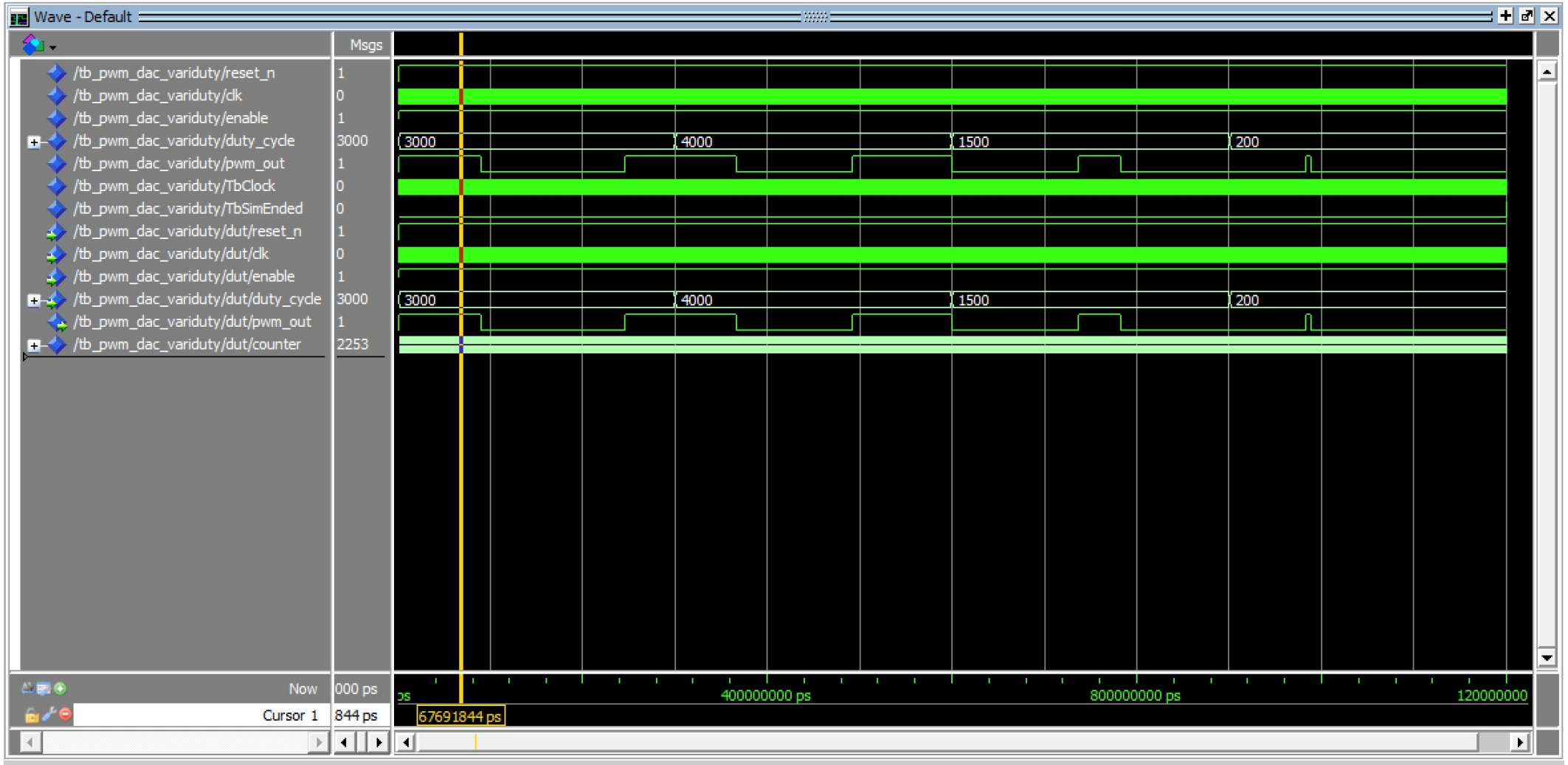

Figure 8: Pulse Width Modulation Half Duty Cycle used for Buzzer and Display Modules