

# Proximity Alarm System

## FPGA VHDL

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Figure 1: RTL View

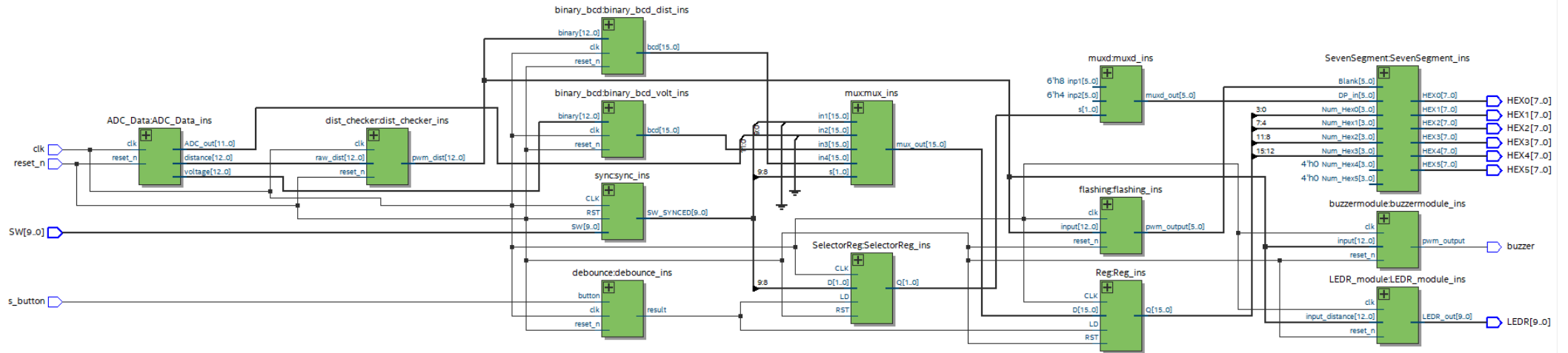


Figure 2: Timing Analysis and Fmax Summary

Tasks

Compilation

Task

Time

✓

▼ ▶ Compile Design

00:03:02

✓

▶ ▶ Analysis & Synthesis

00:01:17

✓

▶ ▶ Fitter (Place & Route)

00:01:26

✓

▶ ▶ Assembler (Generate programming files)

00:00:06

✓

▶ ▶ Timing Analysis

00:00:13

✓

▼ ▶ EDA Netlist Writer

00:00:02

Edit Settings

View Report

Edit Settings

Program Device (Open Programmer)

DR\_module.vhd

PWM\_DAC\_half.vhd

PWM\_DAC\_variDuty.vhd

downcounter.vhd

dist\_checker.vhd

Compilation Report - top\_level

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Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	71.4 MHz	71.4 MHz	clk	
2	122.79 MHz	122.79 MHz	ADC_Data_ins ADC_ins ADC_Conversion_ins u0 altpll_sys sd1 pll7 clk[0]	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are

Figure 3: Warning Messages







Type	ID	Message
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the
	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
> 	332049	Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
	332174	Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
> 	332049	Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary

Figure 4: Top Level Simulation 1 at 24.64 cm

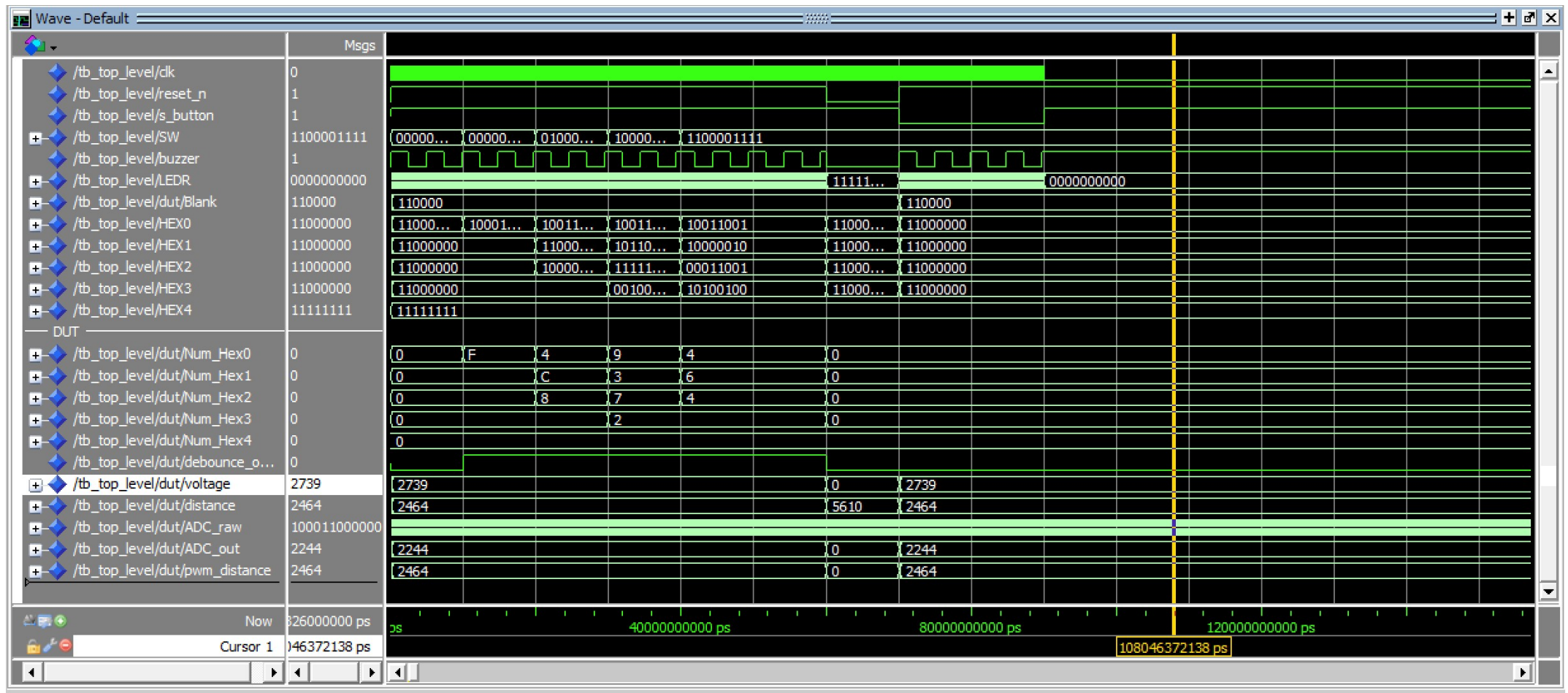


Figure 5: Top Level Simulation 2 at 7.24 cm

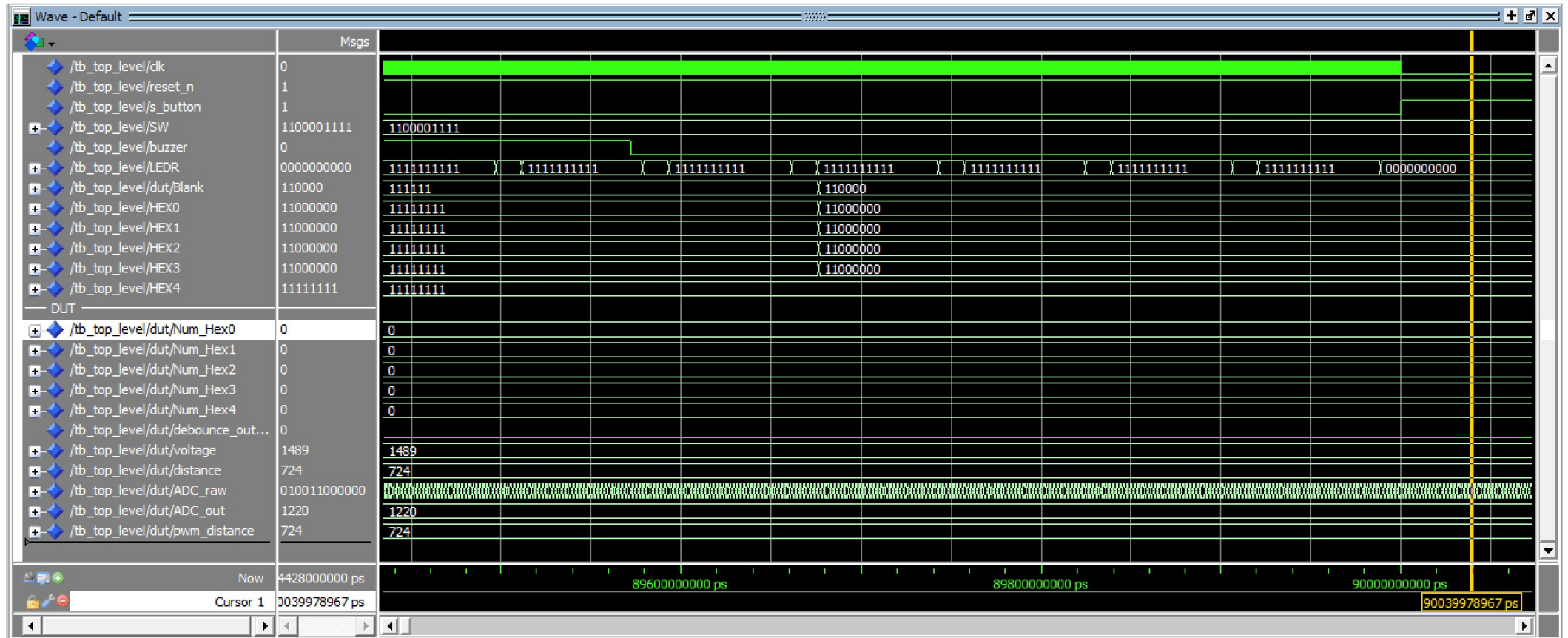


Figure 6: Top Level Simulation 3 at 66.74 cm

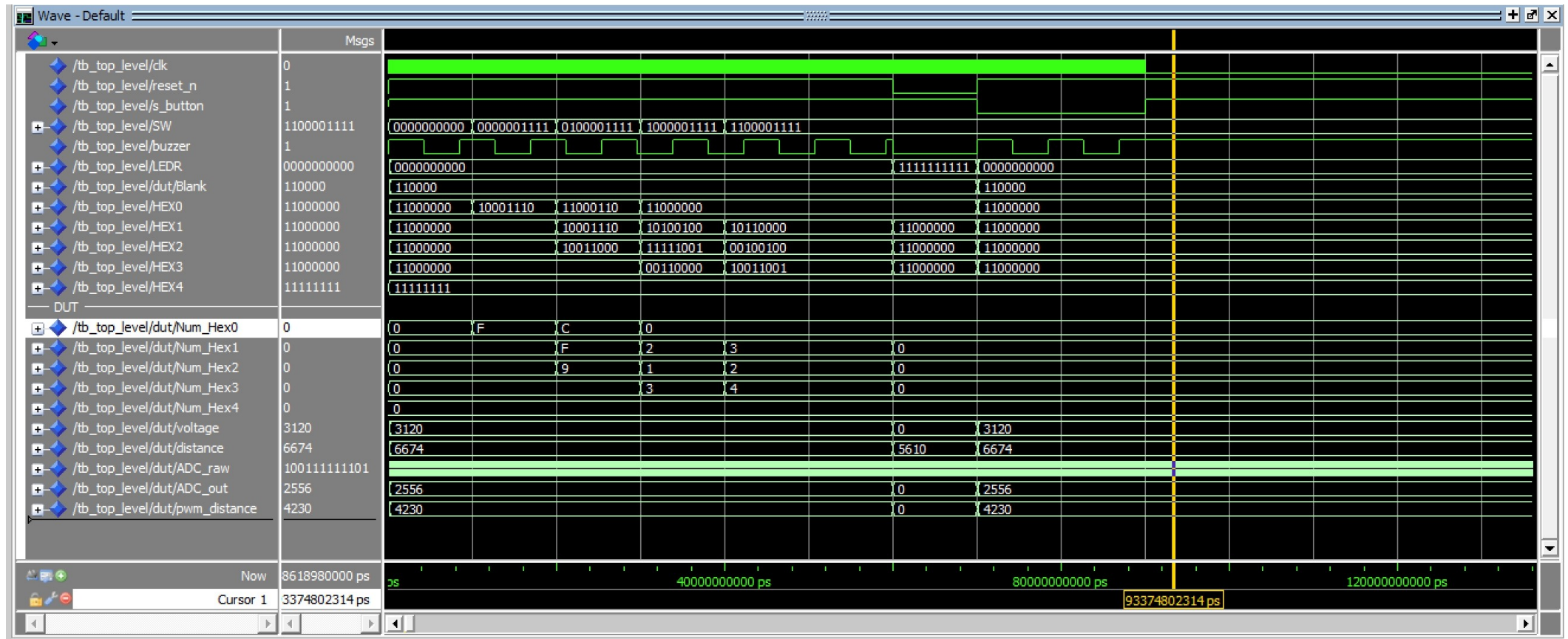


Figure 7: Pulse Width Modulation Varying Duty Cycle used for LEDR Module

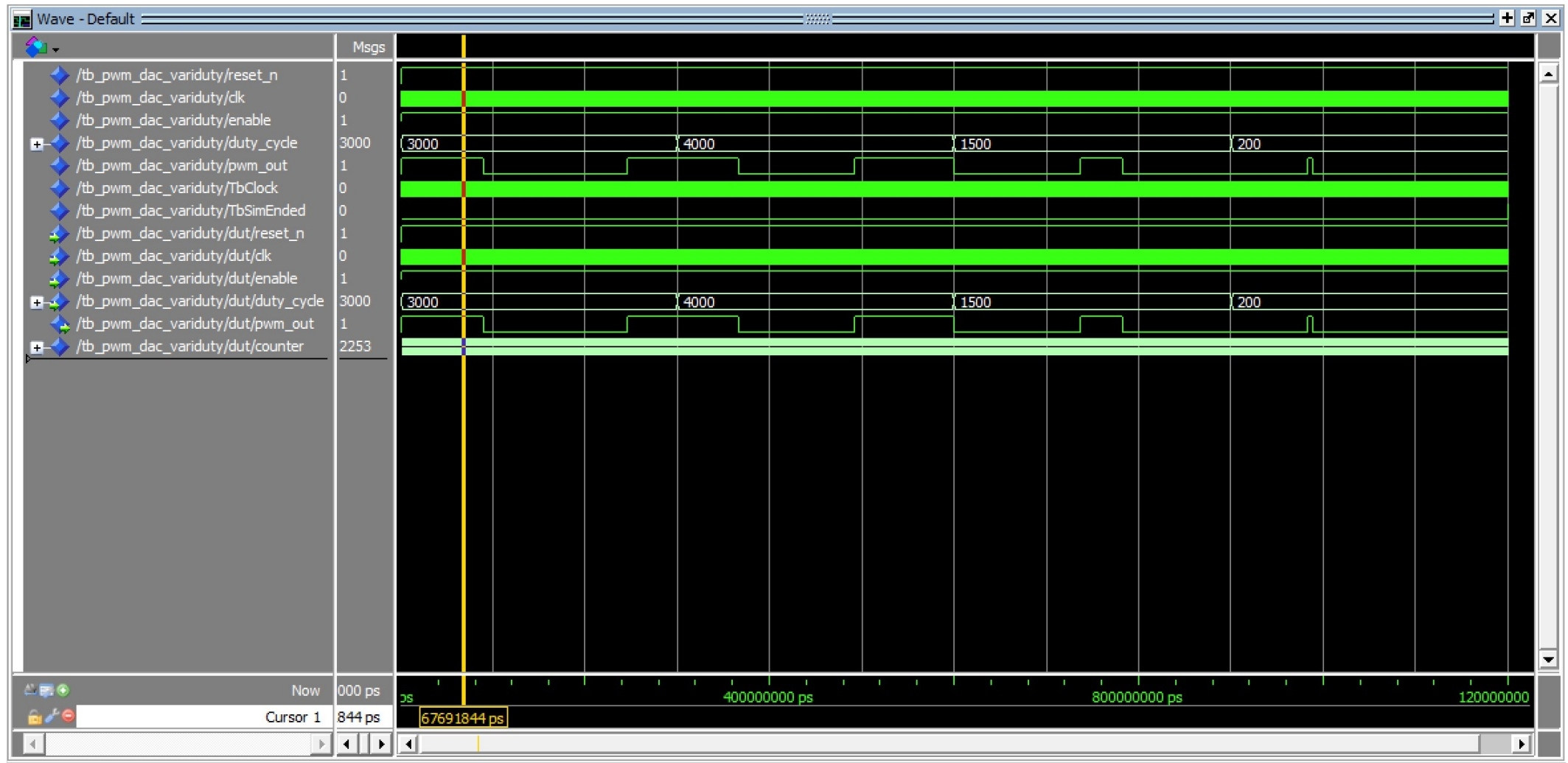




Figure 8: Pulse Width Modulation Half Duty Cycle used for Buzzer and Display Modules

