# DAVICOM Semiconductor, Inc.

# DM9051A

## SPI Fast Ethernet Controller



***Version: Internal ONLY***

***April 11, 2024***

# Content

# 1 General Description

The DM9051A is a fully integrated and cost-effective low pin count single chip Fast Ethernet controller with a Serial Peripheral Interface (SPI), a 10/100M PHY and MAC, and 16K-byte SRAM. It is designed with low power and high performance process interface that support 3.3V with 5V IO tolerance.

The PHY of the DM9051A can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX with HP Auto-MDIX.It is fully compliant with the IEEE 802.3u Spec. Its Auto-Negotiation function will automatically configure the DM9051A to take the maximum advantage of its 10M or 100M abilities.

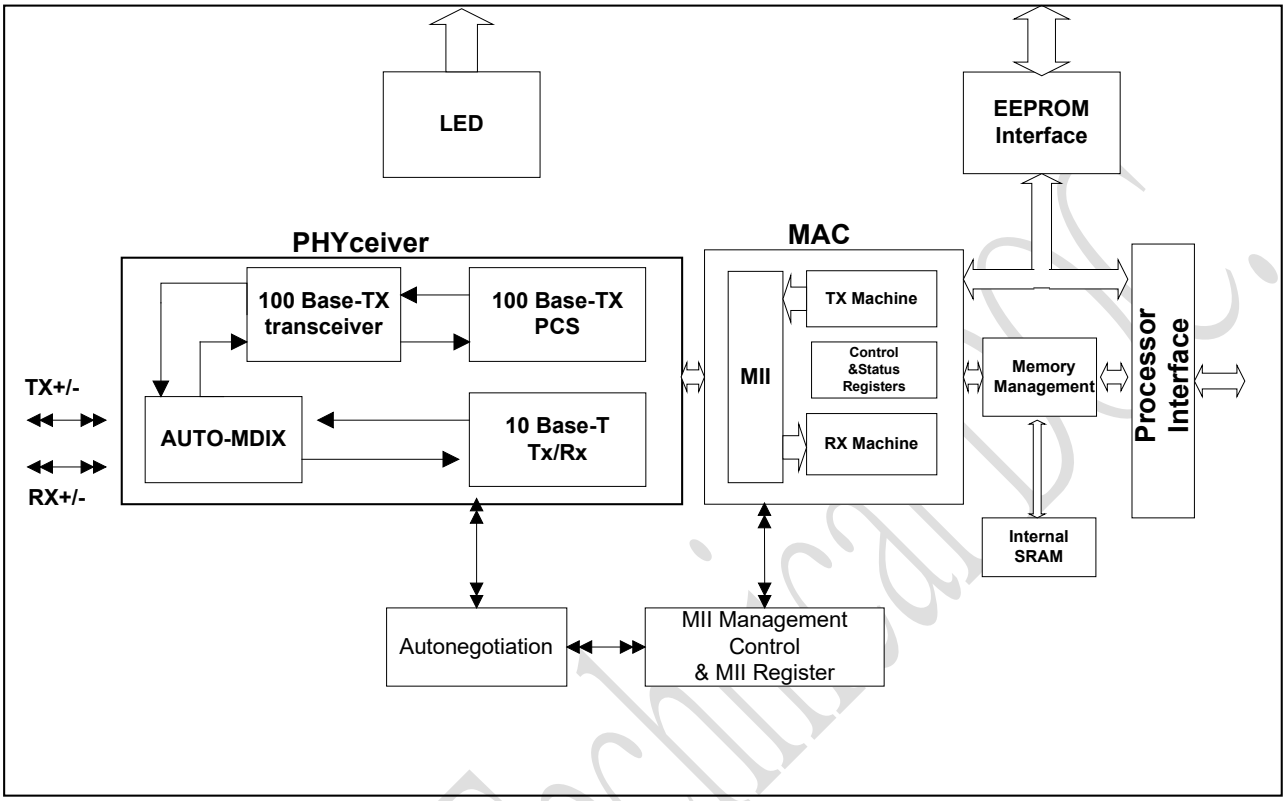
The DM9051A supports IEEE 802.3az in PHY and MAC to save power consumption when Ethernet is idle. The IEEE 802.3x Full-Duplex flow control and Half-Duplex back-pressure function also supported to avoid Ethernet packet loss with link partner.

The slave SPI interface is designed to support SPI clock mode 0 and 3 that compatible with the all master SPI interface of CPU. The clock speed can up to 50Mhz to co-operation with most high throughput master SPI. The SPI burst command format is code-effective to minimize the command overhead in access DM9051A internal registers and packet data in memory.

## 2 Features

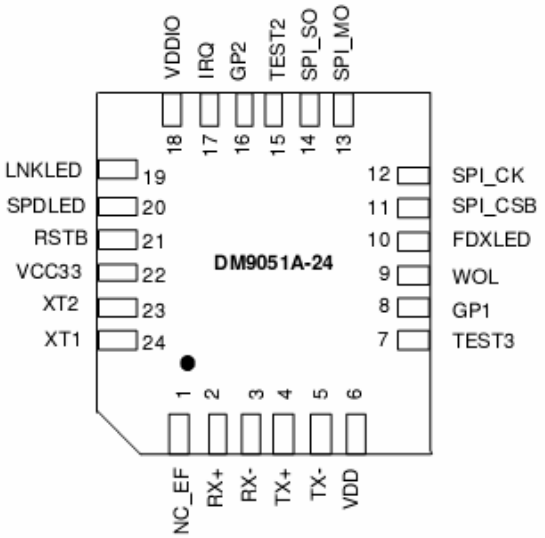
- Slave SPI Interface with clock speeds up to 50MHz for high throughput applications
- Support SPI clock mode 0 and 3
- Support 10BASE-T and 100BASE-TX and 100M Fiber interface
- Support HP Auto-MDIX crossover function in 10BASE-T and 100BASE-TX
- Support IEEE 802.3az Energy Efficient Ethernet (EEE)
- Support interface for EEPROM to configure chip settings
- Support back pressure flow control for Half-Duplex mode
- Support IEEE802.3x flow control for Full-Duplex mode
- Supports wakeup frame, link status change and magic packet events to generate remote wake on LAN (WOL) signal
- Support IPv4/ TCP / UDP checksum generation and checking
- Configurable of internal transmit/receive buffers within 16K-byte memory
- Built-in E-fuse for MAC address
- Built-in Bandgap 6.8K ohm resistor
- Fiber SD configurable source
- Support MAC data encrypt/decrypt mode
- Support TX packet buffer continued mode
- Built-in PTP clocks
- Support TimeStamp capture for TX/RX packets
- 2 GPIO pins for PTP triggers or events
- Support TX one-step TimeStamp replacement
- Built-in integrated 3.3V to 1.2V low noise regulator for core and analog blocks
- Support EMI (Class B) and HBM ESD Rating 8KV
- Support Industrial Temperature Range: –40℃ to +85℃ (DM9051AI)
- Multi-Voltage I/O
- DSP architecture PHY Transceiver
- 0.11um process

## 3 Block Diagram

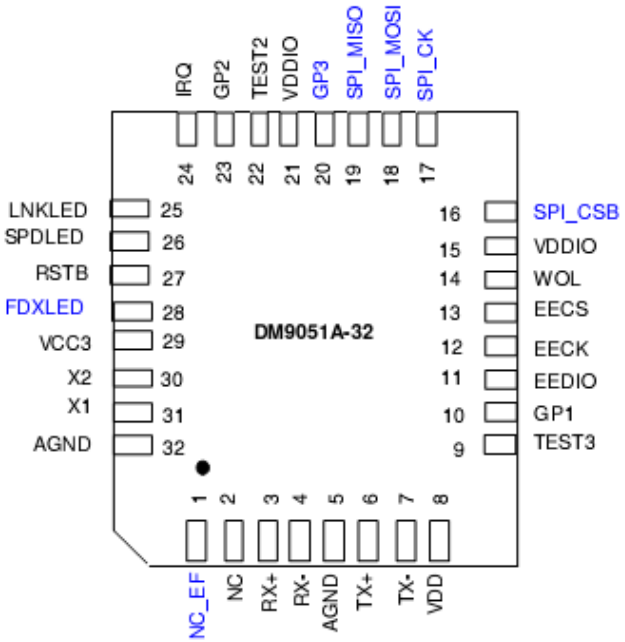


# 4 Pin Configuration

## 4.1 24-Pin QFN




## 4.2 32-Pin QFN




Note: The DM9051A IC employs a QFN package, which means the absence of a pin dedicated to ground (GND). In the QFN package, the GND is located at the bottom of the IC directly in the middle. Exposed pad (VSS) on bottom of package must be connected to ground.

# 5 Pin Description

| Buffer Type | | | |
|---|---|---|---|
| I = Input | O = Output | I/O = Input/Output | P = Power |
| O/D = Open Drain | | PD = Internal Pull-low about 60K | PU = Internal Pull-high about 60K |

## 5.1 24-QFN Pin Description

### 5.1.1 SPI Processor Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 11 | SPI_CSB | I,PU | **SPI Chip Select**<br>The low active chip select pin from master SPI. |
| 12 | SPI_CK | I,PD | **SPI Clock**<br>The SPI clock mode 0 or 3 from master SPI. |
| 13 | SPI_MOSI | I | **SPI Data In**<br>The data pin from master SPI. |
| 14 | SPI_MISO | O,PD | **SPI Data Out**<br>The data pin to master SPI. |
| 17 | IRQ | O,PD | **Interrupt Request**<br>This pin is high active at default; ? |

### 5.1.2 Clock Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 23 | XT2 | O | Crystal 25MHz Out |
| 24 | XT1 | I | Crystal 25MHz In |

### 5.1.3 LED Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 10 | FDXLED | O/D | **Full-Duplex LED**<br>In LED mode 1, its low output indicates that the internal PHY is operated in Full-Duplex mode, or it is floating for the Half-Duplex mode of the internal PHY.<br>In LED mode 0, its low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY.<br>More LED modes are controlled by MAC register 57H |
| 19 | LINKLED | O/D | **Link / Active LED**<br>In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY.<br>In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only.<br>More LED modes are controlled by MAC register 57H. |
| 20 | SPDLED | O/D | **Speed LED**<br>Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY.<br>More LED modes are controlled by MAC register 57H. |

Note: LED mode 0 or 1 is defined in MAC register 2DH or EEPROM setting.

### 5.1.4 10/100 PHY/Fiber

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 1 | NC_EF | I/O | **BGRES or FSOURCE or NC**<br>for test chip 0: this pin is connected 6.8K BGRES<br>Fir test chip 1, this pin is used for Efuse FSOURCE port<br>For test chip 2, this pin is connected 6.8K BGRES and also can be used for Efuse FSOURCE port<br>For test chip 3, this is NC pin |
| 6 | VDD | P | Connect to 0.1uF Cap. |
| 2,3 | RX+/ RX- | I/O | **RX+/-**<br>The RX input in 10BASE-T/100BASE-TX MDI mode or TX output in 10BASE-T/100BASE-TX MDIX mode.<br>In 100M Fiber mode, these pins are for RX input only. |
| 4,5 | TX+/ TX- | I/O | **TX+/-**<br>The TX output in 10BASE-T/100BASE-TX MDI mode or RX input in 10BASE-T/100BASE-TX MDIX mode.<br>In 100M Fiber mode, these pins are for TX output only. |

### 5.1.5 Miscellaneous

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 7 | TEST3 | I,PU | **Operation Mode**<br>Force to high in normal application |
| 8 | GP1 | I/O | **General Purpose Pin 1**<br>This is a general purpose pin controlled by bit 1 of MAC register 1EH/1FH. |
| 9 | WOL | O,PD | **Wake On Lan**<br>This is a control signal when wake up event occurred.<br>Its polarity and output type can be controlled by EEPROM setting. |
| 15 | TEST2 | I,PD | **Operation Mode**<br>Force to ground in normal application |
| 16 | GP2 | I/O | **General Purpose Pin 2**<br>This is a general purpose pin controlled by bit 2 of MAC register 1EH/1FH. |
| 21 | RSTB | I | **Power on Reset**<br>Active low signal to initiate the DM9051A.<br>The DM9051A is ready after 5us when this pin disserted. |

### 5.1.6 Power Pins

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 18 | VDDIO | P | **VDD for IO**<br>3.3V,2.5V,1.8V power input |
| 22 | VCC33 | P | **Analog power**<br>3.3V power input |
| 25 | VSS | P | The QFN package ground |

### 5.1.7 Strap Pins

| Pin No. | Pin Name | Description |
|---|---|---|
| 9 | WOL | **INT Output Type**<br>1 = Open-Drain<br>0 = Push-pull mode |

.

## 5.2 32-QFN Pin Description

### 5.2.1 SPI Processor Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 16 | SPI_CSB | I,PU | **SPI Chip Select**<br>The low active chip select pin from master SPI. |
| 17 | SPI_CK | I,PD | **SPI Clock**<br>The SPI clock mode 0 or 3 from master SPI. |
| 18 | SPI_MOSI | I | **SPI Data In**<br>The data pin from master SPI. |
| 19 | SPI_MISO | O,PD | **SPI Data Out**<br>The data pin to master SPI. |
| 24 | IRQ | O,PD | **Interrupt Request**<br>This pin is high active at default; its polarity can be modified by EEPROM setting or by strap pin EECK or by MAC register 39H. See the EEPROM content and MAC register 39H description for detailed. |

### 5.2.2 EEPROM Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 11 | EEDIO | I/O,PD | **EEPROM IO Data**<br>The IO data pin to or from EEPROM. |
| 12 | EECK | O,PD | **EEPROM Clock**<br>The clock pin to EEPROM.<br>This pin is also used as the strap pin of the polarity of the INT pin.<br>When this pin is pulled-high, the INT pin is low active; otherwise the INT pin is high active. |
| 13 | EECS | O,PD | **EEPROM Chip Select**<br>The high active chip select to EEPROM. |

### 5.2.3 Clock Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 30 | X2 | O | Crystal 25MHz Out |
| 31 | X1 | I | Crystal 25MHz In |

### 5.2.4 LED Interface

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 28 | FDXLED | O/D | **Full-Duplex LED**<br>In LED mode 1, its low output indicates that the internal PHY is operated in Full-Duplex mode, or it is floating for the Half-Duplex mode of the internal PHY.<br>In LED mode 0, its low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY.<br>More LED modes are controlled by MAC register 57H |
| 25 | LINKLED | O/D | **Link / Active LED**<br>In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY.<br>In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only.<br>More LED modes are controlled by MAC register 57H. |
| 26 | SPDLED | O/D | **Speed LED**<br>Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY.<br>More LED modes are controlled by MAC register 57H. |

Note: LED mode 0 or 1 is defined in MAC register 2DH or EEPROM setting.

### 5.2.5 10/100 PHY/Fiber

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 1 | NC_EF | I/O | **BGRES or FSOURCE or NC**<br>for test chip 0: this pin is connected 6.8K BGRES<br>Fir test chip 1, this pin is used for Efuse FSOURCE port<br>For test chip 2, this pin is connected 6.8K BGRES and also can be used for Efuse FSOURCE port<br>For test chip 3, this is NC pin |
| 6 | VDD | P | Connect to 0.1uF Cap. |
| 3,4 | RX+/ RX- | I/O | **RX+/-**<br>The RX input in 10BASE-T/100BASE-TX MDI mode or TX output in 10BASE-T/100BASE-TX MDIX mode.<br>In 100M Fiber mode, these pins are for RX input only. |
| 5,32 | AGND | P | Analog Ground |
| 6,7 | TX+/ TX- | I/O | **TX+/-**<br>The TX output in 10BASE-T/100BASE-TX MDI mode or RX input in 10BASE-T/100BASE-TX MDIX mode.<br>In 100M Fiber mode, these pins are for TX output only. |

### 5.2.6 Miscellaneous

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 2 | NC | | Not connected |
| 9 | TEST3 | I,PD | **Operation Mode**<br>Force to high in normal application |
| 10 | GP1 | I/O | **General Purpose Pin 1**<br>This is a general purpose pin controlled by bit 1 of MAC register 1EH/1FH. |
| 14 | WOL | O,PD | **Wake On Lan**<br>This is a control signal when wake up event occurred.<br>Its polarity and output type can be controlled by EEPROM setting. |
| 22 | TEST2 | I,PD | **Operation Mode**<br>Force to ground in normal application |
| 23 | GP2 | I/O | **General Purpose Pin 2**<br>This is a general purpose pin controlled by bit 2 of MAC register 1EH/1FH. |
| 27 | RSTB | I | **Power on Reset**<br>Active low signal to initiate the DM9051(I).<br>The DM9051A(I) is ready after 5us when this pin disserted. |
| 20 | GP3 | I/O,PD | **General Purpose Pin 3**<br>This is a general purpose pin controlled by bit 3 of MAC register 1EH/1FH. |

### 5.2.7 Power Pins

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 15,21 | VDD33 | P | **VDD for IO**<br>3.3V,2.5V,1.8V power input |
| 29 | VCC33 | P | **Analog power**<br>3.3V power input |
| 33 | VSS | P | The QFN package ground |

### 5.2.8 Strap Pins

| Pin No. | Pin Name | Description |
|---|---|---|
| 12 | EECK | **Polarity of INT**<br>1 = INT pin low active<br>0 = INT pin high active |
| 13 | EECS | **BIST Control**<br>1 = Enable BIST<br>0 = Disable BIST |
| 14 | WOL | **INT Output Type**<br>1 = Open-Drain<br>0 = Push-pull mode |

Note: If memory BIST function is enabled, the SPI interface should not active before RSTB go high 2ms.

### 5.3 Pin Test Mode

**Test Mode Table**

| Mode | Pin 41: TEST1 | Pin 14: SD3 (TEST3) | Pin 31: SD8 (TEST2) | note |
|---|---|---|---|---|
| M0: local bus (16-bit) | 0 | X | X | 48-pin |
| M1: PHY test mode | 1 | 0 | 0 | 48/32/24-pin |
| M2: SPI mode | 1 | 1 | 0 | 32/24-pin |
| M3: local bus (8-bit) | 1 | 0 | 1 | 32-pin |
| M4: ATPG test mode | 1 | 1 | 1 | 48/32/24--pin |

Note: in M3, local_bus (uP) only 8-bit mode is available.

M2 24-pin for DM9051A

M2A 32-pin for DM9051A,

M2B 32-pin for DM9051 compatible

M1/M4 32-pin: pin # X/Y, where X for DM9051A bonding( no pin 20), Y for DM9051 bonding(no pin 28)

| Pin # | M0 | M1 PHY | M2A SPI-32 | M2B SPI-32 | M2 SPI-24 | M3 uP-32 | M4 ATPG |
|---|---|---|---|---|---|---|---|
| 1/1/1 | BGRES | BGRES | BGRES | BGRES | BGRES | BGRES | --- |
| 2/2/ | - | - | - | - | - | - | --- |
| 3/3/2 | RX+ | RX+ | RX+ | RX+ | RX+ | RX+ | --- |
| 4/4/3 | RX- | RX- | RX- | RX- | RX- | RX- | --- |
| 5/5/ | GND | GND | GND | GND | GND | GND | GND |
| 6/ | - | - | - | - | - | - | --- |
| 7/ 6/ 4 | TX+ | TX+ | TX+ | TX+ | TX+ | TX+ | --- |
| 8/ 7/ 5 | TX- | TX- | TX- | TX- | TX- | TX- | --- |
| 9/ 8/ 6 | VDD12 | VDD12 | VDD12 | VDD12 | VDD12 | VDD12 | VDD12 |
| 10 | SD7 | PWRDN | --- | --- | --- | --- | --- |
| 11 | SD6 | CBSTS | --- | --- | --- | --- | --- |
| 12 | SD5 | TXER | --- | --- | --- | --- | --- |
| 13 | SD4 | TXD3 | --- | --- | --- | --- | --- |
| 14/ 9/ 7 | SD3 | TEST3=0 | TEST3=1 | TEST3=1 | TEST3=1 | TEST3=0 | TEST3=1 |
| 15 | GND | GND | GND | GND | --- | GND | GND |
| 16 | SD2 | TXD2 | --- | --- | --- | --- | --- |
| 17/ 10/ 8 | SD1 | OP2 | GP1 | GP1 | GP1 | GP1 | SO0 |
| 18 | SD0 | RXC | --- | --- | --- | --- | --- |
| 19/ 11/ | EEDIO | OP0 | EEDIO | EEDIO | --- | SD0 | --- |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 20/ 12 | EECK | TXC | EECK | EECK | --- | SD1 | --- |
| 21/ 13 | EECS | MDIX | EECS | EECS | --- | SD2 | --- |
| 22/ 14/ 9 | SD15/WOL | OP1 | WOL | WOL | WOL | SD3 | SO1 |
| 23/ 15 | VDDIO | VDDIO | VDDIO | VDDIO | VDDIO | VDDIO | VDDIO |
| 24/16/10 | SD14/FLED | TXD1 28/16 | | FDXLED | FDXLED | LNKLED | --- |
| 25/17/11 | SD13/GP6 | TXD0 16/17 | SPI_CSN/16 | SPI_CSN/17 | SPI_CSN | CMD | SI1 16/17 |
| 26/18/12 | SD12/GP5 | TXE 17/18 | SPI_CK /17 | SPI_CK/18 | SPI_CK | CSB | SI0 17/18 |
| 27/19/13 | SD11/GP4 | MDIO 18/19 | SPI_MOSI/18 | SPI_MOSI/19 | SPI_MOSI | IOR | SI2 18/19 |
| 28/20/14 | SD10/GP3 | MDC 19/20 | SPI_MISO/19 | SPI_MISO/20 | SPI_MISO | IOW | SO2 19/20 |
| | | | GP3 /20 | | | | |
| 29 | SD9/GP2 | RXD2 | | --- | --- | --- | --- |
| 30/21 | VDDIO | VDDIO | VDDIO | VDDIO | --- | VDDIO | VDDIO |
| 31/22/15 | SD8/GP1 | TEST2=0 | TEST2=0 | TEST2=0 | TEST2=0 | TEST2=1 | TEST2=1 |
| 32/23/16 | CMD | RXD1 | GP2 | GP2 | GP2 | SD4 | CK |
| 33 | GND | GND | GND | GND | GND | GND | GND |
| 34/24/17 | IRQ | RXD0 | IRQ | IRQ | IRQ | IRQ | --- |
| -/-/18 | | | | | VDDIO | | |
| 35 | IOR | CRS | --- | --- | --- | --- | --- |
| 36 | IOW | COL | --- | --- | --- | --- | --- |
| 37 | CSB | RXD3 | --- | --- | --- | --- | --- |
| 38/25/19 | LNKLED | RXDV | LNKLED | LNKLED | LNKLED | SD5 | --- |
| 39/26/20 | SPDLED | RXER | SPDLED | SPDLED | SPDLED | SD6 | DATA |
| 40/27/21 | RSTB | RSTB | RSTB | RSTB | RSTB | RSTB | SCAN_EN |
| -/28/- | | | FDXLED/28 | GP3 /28 | --- | SD7 | |
| 41// | TEST1=0 | TEST1=1 | TEST1=1 | TEST1=1 | TEST1=1 | TEST1=1 | TEST1=1 |
| 42/29/22 | VCC33 | VCC33 | VCC33 | VCC33 | VCC33 | VCC33 | VCC33 |
| 43/30/23 | X2 | X2 | X2 | X2 | X2 | X2 | --- |
| 44/31/24 | X1 | X1 | X1 | X1 | X1 | X1 | --- |
| 45 | GND | GND | GND | GND | GND | GND | GND |
| 46 | --- | --- | --- | --- | --- | --- | --- |
| 47 | RXGND | RXGND | RXGND | RXGND | RXGND | RXGND | GND |
| 48/32/ | BGGND | BGGND | BGGND | BGGND | BGGND | BGGND | GND |

## 6 MAC Control and Status Register Set

The DM9051A implements several control and status registers, which can be accessed by the host. These CSRs are byte aligned. All CSRs are set to their default values by hardware or software reset unless they are specified.

| Register | Description | Offset | Default Value after Reset |
|---|---|---|---|
| NCR | Network Control Register | 00H | 00H |
| NSR | Network Status Register | 01H | 00H |
| TCR | TX Control Register | 02H | 00H |
| TSR I | TX Status Register I | 03H | 00H |
| TSR II | TX Status Register II | 04H | 00H |
| RCR | RX Control Register | 05H | 00H |
| RSR | RX Status Register | 06H | 00H |
| ROCR | Receive Overflow Counter Register | 07H | 00H |
| BPTR | Back Pressure Threshold Register | 08H | 37H |
| FCTR | Flow Control Threshold Register | 09H | 38H |
| FCR | RX/TX Flow Control Register | 0AH | 00H |
| EPCR | EEPROM & PHY Control Register | 0BH | 00H |
| EPAR | EEPROM & PHY Address Register | 0CH | 40H |
| EPDRL | EEPROM & PHY Low Byte Data Register | 0DH | XXH |
| EPDRH | EEPROM & PHY High Byte Data Register | 0EH | XXH |
| WCR | Wake Up Control Register | 0FH | 00H |
| PAR | Physical Address Register | 10H-15H | Determined by EEPROM |
| MAR | Multicast Address Hash Table Register | 16H-1DH | XXH |
| GPCR | General Purpose Control Register | 1EH | 71H |
| GPR | General Purpose Register | 1FH | XXH |
| TRPAL | TX Memory Read Pointer Address Low Byte | 22H | 00H |
| TRPAH | TX Memory Read Pointer Address High Byte | 23H | 00H |
| RWPAL | RX Memory Write Pointer Address Low Byte | 24H | 00H |
| RWPAH | RX Memory Write Pointer Address High Byte | 25H | 0CH |
| VID | Vendor ID | 28H-29H | 0A46H |
| PID | Product ID | 2AH-2BH | 9051H |
| CHIPR | CHIP Revision | 2CH | 01H |
| TCR2 | Transmit Control Register 2 | 2DH | 00H |
| ATCR | Auto-Transmit Control Register | 30H | 00H |
| TCSCR | Transmit Check Sum Control Register | 31H | 00H |
| RCSCSR | Receive Check Sum Control Status Register | 32H | 00H |
| SBCR | SPI Bus Control Register | 38H | 44H |
| INTCR | INT Pin Control Register | 39H | 00H |
| EEPT | EEPROM Test Register | 3AH | 00H |
| TX_FREE | TX Free Space Status Register | 3BH | 30H |
| SD_SRC | Fiber SD Source Control Register | 3CH | 00H |
| PPCSR | Pause Packet Control Status Register | 3DH | 01H |
| EEE_IN | IEEE 802.3az Enter Counter Register | 3EH | 05H |
| EEE_OUT | IEEE 802.3az Leave Counter Register | 3FH | 0FH |
| STARPR | Strap pin Status Register | 40H | 85H |
| TCVR | Test Chip Version Register | 46H | 02H |
| ALNCR | SPI Byte Align Error Counter Register | 4AH | 00H |
| CRYPTR | Crypt Test Register | 4BH | 00H |
| RXWLTR | RX Memory Write Address Low Test Register | 4CH | 00H |
| RXWHTR | RX Memory Write Address High Test Register | 4DH | 0CH |
| TXRLTR | TX Memory Read Address Low Test Register | 4EH | 00H |
| TXRHTR | TX Memory Read Address High Test Register | 4FH | 00H |

| | | | |
|---|---|---|---|
| RLENCR | RX Packet Length Control Register | 52H | 00H |
| BCASTCR | RX Broadcast Control Register | 53H | 00H |
| INTCKCR | INT Pin Clock Output Control Register | 54H | 00H |
| MPTRCR | Memory Pointer Control Register | 55H | 00H |
| ADCMTCR | ADC Memory Test Control Register | 56H | 00H |
| MLEDCR | More LED Control Register | 57H | 00H |
| EFCR | E-fuse control Register | 58H | 00H |
| MEMSCR | Memory Control Register | 59H | 00H |
| TMESR | Transmit Memory Size Register | 5AH | 03H |
| RMESR | Receive Memory Size Register | 5BH | 0DH |
| VERR | IC Version Register | 5CH | E1H |
| MBSR | Memory BIST Status Register | 5DH | 40H |
| MBCR | Memory Boundary Control Register | 5EH | 80H |
| PSGR | PTP Status and GPIO Page Register | 60H | 00H |
| PCCR | PTP Clock Control Registers | 61H | 00H |
| PTPCR | PTP GPIO and TX/RX Control Register | 62H | 00H |
| POCCR | PTP One Step Checksum Control Register | 63H | 00H |
| PRXCR | PTP Receive Configuration 1 Register | 64H | 00H |
| POADR | PTP One Step Address Offset | 65H | 4EH |
| POCADR | PTP One Step checksum Address Offset 66H 3CH | 66H | 3CH |
| PCPR | PTP Clock Period Register | 67H | 28H |
| PSTR | PTP Timestamp Registers | 68H | 00H |
| PMNTR | PTP Monitor Register | 69H | 00H |
| PGCR | GPIO Configuration Register | 6AH | 00H |
| PGTER | GPIO Trigger/Event Configuration Register | 6BH | 00H |
| PGTPLR | GPIO Trigger Asserted Pulse Low Register | 6CH | 00H |
| PGTPHR | GPIO Trigger Asserted Pulse High Register | 6DH | 00H |
| PGTDPLR | GPIO Trigger Periodic De-asserted Pulse Low Register | 6EH | 00H |
| PGTDPHR | GPIO Trigger Periodic De-asserted Pulse High Register | 6FH | 00H |
| MRCMDX | Memory Data Pre-Fetch Read Command Without Address Increment Register | 70H | XXH |
| MRCMDX1 | Memory Read Command Without Pre-Fetch and Without Address Increment Register | 71H | XXH |
| MRCMD | Memory Data Read Command With Address Increment Register | 72H | XXH |
| SDR_DLY | SPI Data Read Delay Counter Register | 73H | 00H |
| MRRL | Memory Data Read Address Register Low Byte | 74H | 00H |
| MRRH | Memory Data Read Address Register High Byte | 75H | 00H |
| MWCMDX | Memory Data Write Command Without Address Increment Register | 76H | XXH |
| MWCMD | Memory Data Write Command With Address Increment Register | 78H | XXH |
| MWRL | Memory Data Write Address Register Low Byte | 7AH | 00H |
| MWRH | Memory Data Write Address Register High Byte | 7BH | 00H |
| TXPLL | TX Packet Length Low Byte Register | 7CH | XXH |
| TXPLH | TX Packet Length High Byte Register | 7DH | XXH |
| ISR | Interrupt Status Register | 7EH | 00H |
| IMR | Interrupt Mask Register | 7FH | 00H |

**Key to Default**

In the register description that follows, the default column takes the form:

| <Reset Value>: | | <Access Type>: | |
|---|---|---|---|
| 1 | Bit set to logic one | RO = | Read Only |
| 0 | Bit set to logic zero | RW = | Read/Write |
| X | No default value | R/C = | Read and Clear |
| P = | Power on reset default value | | |
| H = | Hardware reset default value | | |
| S = | Software reset default value | | |
| E = | Default value from EEPROM | | |
| T = | Default value from strap pin | | |
| h = | Hex, format | | |

RW/C1=Read/Write and Cleared by write 1 WO = Write Only
Reserved bits are shaded and should be written with 0. Reserved bits are undefined on read access.

### 6.1 Network Control Register (00H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P0,RW | Reserved |
| 6 | WAKEEN | P0,RW | **Enables Wakeup Function**<br>Clearing this bit will also clears all wakeup event status. This bit will not be affected after a software reset.<br>1 = Enable<br>0 = Disable |
| 5 | RESERVED | 0,RO | Reserved |
| 4 | FCOL | PS0,RW | **Force Collision Mode**<br>1 = Force Collision Mode, used for testing<br>0 = Disable |
| 3 | FDX | PS0,RO | **Duplex Mode of the Internal PHY**<br>1 = Full-Duplex<br>0 = Half-Duplex |
| 2:1 | LBK | PS00,RW | **Loopback Mode**<br>Bit: 2 1<br>0 0 Normal<br>0 1 MAC Internal loopback<br>1 0 Internal PHY 100M mode digital loopback<br>1 1 (Reserved) |
| 0 | RST | P0,RW | **Software Reset and Auto-Clear after 10us**<br>1 = Reset state<br>0 = Non-reset state |

### 6.2 Network Status Register (01H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | SPEED | X,RO | **Speed of Internal PHY**<br>This bit has no meaning when LINKST=0<br>1 = 10Mbps<br>0 = 100Mbps |
| 6 | LINKST | X,RO | **Link Status of Internal PHY**<br>1 = Link OK<br>0 = Link failed |
| 5 | WAKEST | P0, RW/C1 | **Wakeup Event Status**<br>Clears by read or write 1. This bit will not be affected after software reset.<br>1 = Wakeup event<br>0 = No wakeup event |
| 4 | RESERVED | 0,RO | Reserved |
| 3 | TX2END | PS1, RW/C1 | **TX Packet Index II Complete Status**<br>Auto-Clear at begin transmitting of TX packet index II and Auto-Set at the end of transmitting of TX packet index II.<br>1 = Transmit completion or idle of packet index II<br>0 = Packet index II transmit in progress |
| 2 | TX1END | PS1, RW/C1 | **TX Packet Index I Complete Status**<br>Auto-Clear at begin transmitting of TX packet index I and Auto-Set at the end of transmitting of TX packet index I.<br>1 = Transmit completion or idle of packet index I<br>0 = Packet index I transmit in progress |

| | | | |
|---|---|---|---|
| 1 | RXOV | PS0,RO | **RX Memory Overflow Status**<br>1 = RX memory Overflow<br>0 = Non-overflow |
| 0 | RXRDY | PS0,RO | **RX Packet Ready**<br>1 = Have packet in RX memory<br>0 = No packet in RX memory |

### 6.3 TX Control Register (02H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | TX_TS_EN | 0,RW | **Transmit TimeStamp Capture when REG_61H PTP_EN=1**<br>0: disable<br>1: enable |
| 6 | TJDIS | PS0,RW | **Transmit Jabber Timer (2048 bytes) Control**<br>1 = Disabled.<br>0 = Enable |
| 5 | EXCECM | PS0,RW | **Excessive Collision Mode Control**<br>1 = Still tries to transmit this packet<br>0 = Aborts this packet when excessive collision counts more than 15 |
| 4 | PAD_DIS2 | PS0,RW | **PAD Appends for Packet Index II**<br>1 = Disable<br>0 = Enable |
| 3 | CRC_DIS2 | PS0,RW | **CRC Appends for Packet Index II**<br>1 = Disable<br>0 = Enable |
| 2 | PAD_DIS1 | PS0,RW | **PAD Appends for Packet Index I**<br>1 = Disable<br>0 = Enable |
| 1 | CRC_DIS1 | PS0,RW | **CRC Appends for Packet Index I**<br>1 = Disable<br>0 = Enable |
| 0 | TXREQ | PS0,RW | **TX Request. Auto-Clear after Sending Completely**<br>1 = Transmit in progress<br>0 = No transmit in progress |

### 6.4 TX Status Register I (03H) for Packet Index I

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | TJTO | PS0,RO | **Transmit Jabber Time Out**<br>It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted.<br>1 = Timeout<br>0 = Non-timeout |
| 6 | LC | PS0,RO | **Loss of Carrier**<br>It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode.<br>1 = Loss of carrier<br>0 = No carrier have been loss |
| 5 | NC | PS0,RO | **No Carrier**<br>It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode.<br>1 = No carrier during transmit<br>0 = Normal carrier status during transmit |
| 4 | LC | PS0,RO | **Late Collision**<br>It is set when a collision occurs after the collision window of 64 bytes.<br>1 = Late collision<br>0 = No late collision |
| 3 | COL | PS0,RO | **Collision Packet**<br>It is set to indicate that the collision occurs during transmission.<br>1 = Have been collision<br>0 = No collision |
| 2 | EC | PS0,RO | **Excessive Collision**<br>It is set to indicate that the transmission is aborted due to 16 excessive collisions.<br>1 = 16 excessive collisions<br>0 = Less than 16 collisions |
| 1:0 | RESERVED | 0,RO | Reserved |

### 6.5 TX Status Register II (04H) for packet index II

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | TJTO | PS0,RO | **Transmit Jabber Time Out**<br>It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted.<br>1 = Timeout<br>0 = Non-timeout |
| 6 | LC | PS0,RO | **Loss of Carrier**<br>It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode.<br>1 = Loss of carrier<br>0 = No carrier have been loss |
| 5 | NC | PS0,RO | **No Carrier**<br>It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode.<br>1 = No carrier during transmit<br>0 = Normal carrier status during transmit |
| 4 | LC | PS0,RO | **Late Collision**<br>It is set when a collision occurs after the collision window of 64 bytes.<br>1 = Late collision<br>0 = No late collision |
| 3 | COL | PS0,RO | **Collision Packet**<br>It is set to indicate that the collision occurs during transmission.<br>1 = Have been collision<br>0 = No collision |
| 2 | EC | PS0,RO | **Excessive Collision**<br>It is set to indicate that the transmission is aborted due to 16 excessive collisions.<br>1 = 16 excessive collisions<br>0 = Less than 16 collisions |
| 1:0 | RESERVED | 0,RO | Reserved |

### 6.6 RX Control Register (05H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | PS0,RW | Reserved |
| 6 | WTDIS | PS0,RW | **Watchdog Timer Disable**<br>1 = When set, the Watchdog Timer (2048 bytes) is disabled<br>0 = Otherwise it is enabled |
| 5 | DIS_LONG | PS0,RW | **Discard Long Packet**<br>If Packet length is over 1522byte<br>1 = Enable<br>0 = Disable |
| 4 | DIS_CRC | PS0,RW | **Discard CRC Error Packet**<br>1 = Enable<br>0 = Disable |
| 3 | ALL | PS0,RW | **Receive All Multicast**<br>To receive packet with multicast destination address<br>1 = Enable<br>0 = Disable |
| 2 | RUNT | PS0,RW | **Receive Runt Packet**<br>To receive packet with size less than 64-bytes<br>1 = Enable<br>0 = Disable |
| 1 | PRMSC | PS0,RW | **Promiscuous Mode**<br>To receive packet without destination address checking<br>1 = Enable<br>0 = Disable |
| 0 | RXEN | PS0,RW | **RX Enable**<br>1 = Enable<br>0 = Disable |

### 6.7 RX Status Register (06H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RF | PS0,RO | **Runt Frame**<br>It is set to indicate that the size of the received frame is smaller than 64 bytes.<br>1 = Affirmative<br>0 = Negative |
| 6 | MF | PS0,RO | **Multicast Frame**<br>It is set to indicate that the received frame has a multicast address.<br>1 = Affirmative<br>0 = Negative |
| 5 | RXTS_EN | PS0,RO | **RX Time Stamp available or Late Collision Seen**<br>**If PTP_EN=1**<br>1 = RX timestamp data in RX header begin from byte 4<br>0 = no RX timestamp available<br>Else PTP_RN=0<br>It is set to indicate that a late collision is found during the frame reception.<br>1 = Affirmative<br>0 = Negative |
| 4 | RWTO | PS0,RO | **Receive Watchdog Time-Out**<br>It is set to indicate that it receives more than 2048 bytes.<br>1 = Affirmative<br>0 = Negative |
| 3 | RXTS_PARITY | PS0,RO | RX Time Stamp Odd Parity or **Physical Layer Error**<br>If PTP_EN=1<br>This is the Odd Parity value of RX Time Stamp<br>Else PTP_EN=0<br>It is set to indicate that a physical layer error is found during the frame reception.<br>1 = Affirmative<br>0 = Negative |
| 2 | RXTS_LEN | PS0,RO | **RX Time Stamp byte length or Alignment Error**<br>**If PTP_EN=1**<br>1 = 8-byte (4-byte sec + 4-byte nano-sec)<br>0 = 4-byte (2-bit sec + 4-byte nano-sec)<br>Else PTP_EN=0<br>It is set to indicate that the received frame ends with a non-byte boundary.<br>1 = Affirmative<br>0 = Negative |
| 1 | CE | PS0,RO | **CRC Error**<br>It is set to indicate that the received frame ends with a CRC error.<br>1 = Affirmative<br>0 = Negative |
| 0 | FOE | PS0,RO | **RX Memory Overflow Error**<br>It is set to indicate that a RX memory overflow error happens during the frame reception.<br>1 = Affirmative<br>0 = Negative |

### 6.8 Receive Overflow Counter Register (07H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RXFU | PS0,R/C | **Receive Overflow Counter Overflow**<br>This bit is set when the ROC has an overflow condition.<br>1 = Affirmative<br>0 = Negative |
| 6:0 | ROC | PS0,R/C | **Receive Overflow Counter**<br>This is a statistic counter to indicate the received packet count upon FIFO overflow. |

### 6.9 Back Pressure Threshold Register (08H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | BPHW | PS3, RW | **Back Pressure High Water Overflow Threshold**<br>MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value.<br>The default is 3K-byte free space. Please do not exceed SRAM size (1 unit=1K bytes). |
| 3:0 | JPT | PS7, RW | **Jam Pattern Time**<br>Default is 200us |

| bit3 | bit2 | bit1 | bit0 | time |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 10.3us |
| 0 | 0 | 0 | 1 | 20.5us |
| 0 | 0 | 1 | 0 | 30.8us |
| 0 | 0 | 1 | 1 | 51.4us |
| 0 | 1 | 0 | 0 | 102us |
| 0 | 1 | 0 | 1 | 195us |
| 0 | 1 | 1 | 0 | 288us |
| 0 | 1 | 1 | 1 | 380us |
| 1 | 0 | 0 | 0 | 483us |
| 1 | 0 | 0 | 1 | 576us |
| 1 | 0 | 1 | 0 | 678us |
| 1 | 0 | 1 | 1 | 771us |
| 1 | 1 | 0 | 0 | 867us |
| 1 | 1 | 0 | 1 | 966us |
| 1 | 1 | 1 | 0 | 1.06ms |
| 1 | 1 | 1 | 1 | 1.15ms |

### 6.10 Flow Control Threshold Register (09H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | HWOT | PS3, RW | **RX Memory High Water Overflow Threshold**<br>Send a pause packet with pause time=FFFFH when the RX memory free space is less than this value. If this value is zero, its means no fRX flow control. The default value is 3K-byte free space. Please do not exceed RX memory size (1 unit=1K bytes). |
| 3:0 | LWOT | PS8, RW | **RX Memory Low Water Overflow Threshold**<br>Send a pause packet with pause time=0000H when RX memory free space is larger than this value. This pause packet is enabled after the high water pause packet is transmitted. The default memory free space is 8K-byte. Please do not exceed RX memory size<br>(1 unit=1K bytes). |

### 6.11 RX/TX Flow Control Register (0AH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | TXP0 | PS0,RW | **Force TX Pause Packet with 0000H**<br>Set to TX pause packet with pause time field is 0000H. Auto-Clears after pause packet transmission completion. |
| 6 | TXPF | PS0,RW | **Force TX Pause Packet with FFFFH**<br>Set to TX pause packet with pause time field is FFFFH. Auto-Clears after pause packet transmission completion. |
| 5 | TXPEN | PS0,RW | **TX Pause Packet Enable**<br>Enables the pause packet for high/low water threshold control in Full-Duplex mode.<br>1 = Enable<br>0 = Disable |
| 4 | BKPA | PS0,RW | **Back Pressure Mode**<br>This mode is for Half-Duplex mode only. It generates a jam pattern when any packet comes and RX SRAM is over BPHW of MAC register 8H.<br>1 = Enable<br>0 = Disable |
| 3 | BKPM | PS0,RW | **Back Pressure Mode**<br>This mode is for Half-Duplex mode only. It generates a jam pattern when a packet's DA matches and RX SRAM is over BPHW of MAC register 8H.<br>1 = Enable<br>0 = Disable |
| 2 | RXPS | PS0,R/C | **RX Pause Packet Status, Latch and Read Clearly**<br>When there has been packet received, this bit will be latched. This bit is cleared after read.<br>1 = Has been receive pause packet<br>0 = No pause packet received |
| 1 | RXPCS | PS0,RO | **RX Pause Packet Current Status**<br>1 = Received pause packet timer down-count in progress<br>0 = Pause packet timer value is zero |
| 0 | FLCE | PS0,RW | **Flow Control Enable**<br>Set to enable the flow control mode (i.e. can disable DM9051A TX function temperately).<br>1 = Enable<br>0 = Disable |

### 6.12 EEPROM & PHY Control Register (0BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | RESERVED | 0,RO | Reserved |
| 5 | REEP | P0,RW | **Reload EEPROM**<br>Set one to reload EEPROM. Driver needs to clear it before to enable this function. |
| 4 | WEP | P0,RW | **Write EEPROM Enable**<br>Set this bit to one before the operation of write EEPROM.<br>1 = Enable<br>0 = Disable |
| 3 | EPOS | P0,RW | **EEPROM or PHY Operation Select**<br>0 = Select EEPROM<br>1 = Select PHY |
| 2 | ERPRR | P0,RW | **EEPROM Read** or **PHY Register Read Command**<br>Set one to read EEPROM or PHY register.<br>Auto-Cleared after the operation completes. |
| 1 | ERPRW | P0,RW | **EEPROM Write** or **PHY Register Write Command**<br>Set one to write EEPROM or PHY register.<br>Auto-Cleared after the operation completes. |
| 0 | ERRE | P0,RO | **EEPROM Access Status** or **PHY Access Status**<br>1 = The EEPROM or PHY access is in progress<br>0 = Completion of the EEPROM or PHY access |

### 6.13 EEPROM & PHY Address Register (0CH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | PHY_ADR | P001,RW | PHY Address bit 1 and 0, the PHY address bit [4:2] is force to 0. Force to 01 in application. |
| 5:0 | EROA | P00,RW | EEPROM Word Address or PHY Register Number. |

### 6.14 EEPROM & PHY Data Register (EE_PHY_L:0DH EE_PHY_H:0EH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | EE_PHY_L | P00,RW | **EEPROM** or **PHY Low Byte Data**<br>The low byte data read from or write to EEPROM or PHY. |
| 7:0 | EE_PHY_H | P00,RW | **EEPROM** or **PHY High Byte Data**<br>The high byte data read from or write to EEPROM or PHY. |

### 6.15 Wake Up Control Register (0FH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | RESERVED | 0,RO | Reserved |
| 5 | LINKEN | P0,RW | **Link Status Change Wake up Event**<br>To control the link status change event in WOL pin function.<br>1 = Enable<br>0 = Disable |
| 4 | SAMPLEEN | P0,RW | **Sample Frame Wake up Event**<br>To control the sample frame matched event in WOL pin function.<br>1 = Enable<br>0 = Disable |
| 3 | MAGICEN | P0,RW | **Magic Packet Wake up Event**<br>To control the Magic packet event in WOL pin function.<br>1 = Enable<br>0 = Disable |
| 2 | LINKST | P0,RO | **Link Status Change Event Occurred**<br>1 = Link change event occurred<br>0 = No link change event |
| 1 | SAMPLEST | P0,RO | **Sample Frame Event Occurred**<br>1 = Sample frame matched event occurred<br>0 = No sample frame matched |
| 0 | MAGICST | P0,RO | **Magic Packet Event Occurred**<br>1 = Magic packet received<br>0 = No magic packet received |

### 6.16 Physical Address Register (10H~15H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | PAB5 | E,RW | Physical Address Byte 5 (15H) |
| 7:0 | PAB4 | E,RW | Physical Address Byte 4 (14H) |
| 7:0 | PAB3 | E,RW | Physical Address Byte 3 (13H) |
| 7:0 | PAB2 | E,RW | Physical Address Byte 2 (12H) |
| 7:0 | PAB1 | E,RW | Physical Address Byte 1 (11H) |
| 7:0 | PAB0 | E,RW | Physical Address Byte 0 (10H) |

### 6.17 Multicast Address Hash Table Register (16H~1DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MAB7 | X,RW | Multicast Address Hash Table Byte 7 (1DH) |
| 7:0 | MAB6 | X,RW | Multicast Address Hash Table Byte 6 (1CH) |
| 7:0 | MAB5 | X,RW | Multicast Address Hash Table Byte 5 (1BH) |
| 7:0 | MAB4 | X,RW | Multicast Address Hash Table Byte 4 (1AH) |
| 7:0 | MAB3 | X,RW | Multicast Address Hash Table Byte 3 (19H) |
| 7:0 | MAB2 | X,RW | Multicast Address Hash Table Byte 2 (18H) |
| 7:0 | MAB1 | X,RW | Multicast Address Hash Table Byte 1 (17H) |
| 7:0 | MAB0 | X,RW | Multicast Address Hash Table Byte 0 (16H) |

### 6.18 General Purpose Control Register (1EH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | RESERVED | PH0,RO | Reserved |
| 3 | GPC3 | P0,RW | **General Purpose Control 3**<br>Define the input/output direction of pin GP3.<br>1 = Pin GP3 in output mode<br>0 = Pin GP3 in input mode |
| 2 | GPC2 | P0,RW | **General Purpose Control 2**<br>Define the input/output direction of pin GP2.<br>1 = Pin GP2 in output mode<br>0 = Pin GP2 in input mode |
| 1 | GPC1 | P0,RW | **General Purpose Control 1**<br>Define the input/output direction of pins GP 1.<br>1 = Pin GP1 in output mode<br>0 = Pin GP1 in input mode |
| 0 | RESERVED | P1,RO | Reserved |

### 6.19 General Purpose Register (1FH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | RESERVED | 0,RO | Reserved |
| 3 | GPIO3 | P0,RW | **General Purpose Pin Data 3**<br>When GPC3 of register 1EH is 1, the value of this bit is reflected to pin GP3.<br>When GPC3 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP3. |
| 2 | GPIO2 | P0,RW | **General Purpose Pin Data 2**<br>When GPC2 of register 1EH is 1, the value of this bit is reflected to pin GP2.<br>When GPC2 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP2. |
| 1 | GPIO1 | P0,RW | **General Purpose Pin Data 1**<br>When GPC1 of register 1EH is 1, the value of this bit is reflected to pin GP1.<br>When GPC1 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP1. |
| 0 | PHYPD | PE1,WO | **PHY Power Down Control**<br>1 = Power down PHY<br>0 = Power up PHY<br>Note: If this bit is updated from '1' to '0', the whole MAC and PHY Registers can not be accessed within 1ms. |

### 6.20 TX Memory Read Pointer Address Register (22H~23H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TRPAH | PS0,RO | TX Memory Read Pointer Address High Byte (23H) |
| 7:0 | TRPAL | PS0,RO | TX Memory Read Pointer Address Low Byte (22H) |

### 6.21 RX Memory Write Pointer Address Register (24H~25H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | RWPAH | PS,0CH,RO | RX Memory Write Pointer Address High Byte (25H) |
| 7:0 | RWPAL | PS,00H,RO | RX Memory Write Pointer Address Low Byte (24H) |

### 6.22 Vendor ID Register (28H~29H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | VIDH | PE,0AH,RO | Vendor ID High Byte (29H) |
| 7:0 | VIDL | PE,46H,RO | Vendor ID Low Byte (28H) |

### 6.23 Product ID Register (2AH~2BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | PIDH | PE,90H,RO | Product ID High Byte (2BH) |
| 7:0 | PIDL | PE,51H,RO | Product ID Low Byte (2AH) |

### 6.24 CHIP Revision (2CH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | CHIPR | P,02H,RO | CHIP Revision |

### 6.25 Transmit Control Register 2 (2DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | LED | PE0,RW | **LED Mode**<br>See the LED pin description for detailed.<br><br>1 = LED mode 1<br>0 = LED mode 0 |
| 6 | RLCP | P0,RW | **Retry Late Collision Packet**<br>Re-transmit the packet with late-collision.<br><br>1 = Enable<br>0 = Disable |
| 5 | RESERVED | P0,RW | Reserved |
| 4 | ONEPM | P0,RW | **One Packet Mode**<br>1 = Only one packet transmit command can be issued before transmit completed<br>0 = At most two packet transmit command can be issued before transmit completed |
| 3:0 | IFGS | P00,RW | **Inter-Frame Gap Setting**<br>0XXX = 96-bit<br>1000 = 64-bit<br>1001 = 72-bit<br>1010 = 80-bit<br>1011 = 88-bit<br>1100 = 96-bit<br>1101 = 104-bit<br>1110 = 112-bit<br>1111 = 120-bit |

### 6.26 Auto-Transmit Control Register (30H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | AUTO_TX | PS0,RW | **Auto-Transmit Control**<br>1 = Auto-Transmit enabled. Packet transmitted automatically when end of write TX buffer<br>0 = Auto-Transmit disabled. When transmit packet, need to set MAC register 2H bit 0 to "1" |
| 6:5 | RESERVED | P00,RO | Reserved |
| 4 | TX_MODE2 | PS0.RW | **Transmit Buffer Continued mode Control**<br>1: enable<br>0: disable |
| 3:2 | RESERVED | P00,RO | Reserved |
| 1:0 | RESERVED | PS0,RW | Reserved |

Note: When in TX_MODE2 enabled, the transmit buffer data address in dword boundary and in sequence write.
TX packet format:
Byte 0/1: TX size low/high byte
Byte 2: TX control: Bit 7= TX TimeStamp Capture enable
Bit 6= TX One-Step enable
Bit 5~0=0 reserved
Byte 3: TX Buffer control: 80H= TX buffer data available
Byte 4~TX_END_BYTE: packet payload

### 6.27 Transmit Check Sum Control Register (31H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:3 | RESERVED | 0,RO | Reserved |
| 2 | UDPCSE | PS0,RW | **UDP CheckSum Generation**<br>1 = Enable<br>0 = Disable |
| 1 | TCPCSE | PS0,RW | **TCP CheckSum Generation**<br>1 = Enable<br>0 = Disable |
| 0 | IPCSE | PS0,RW | **IPv4 CheckSum Generation**<br>1 = Enable<br>0 = Disable |

### 6.28 Receive Check Sum Status Register (32H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | UDPS | PS0,RO | **UDP CheckSum Status**<br>1 = Checksum fail, if UDP packet<br>0 = No UDP checksum error |
| 6 | TCPS | PS0,RO | **TCP CheckSum Status**<br>1 = Checksum fail, if TCP packet<br>0 = No TCP checksum error |
| 5 | IPS | PS0,RO | **IPv4 CheckSum Status**<br>1 = Checksum fail, if IP packet<br>0 = No IP checksum error |
| 4 | UDPP | PS0,RO | **UDP Packet of Current Received Packet**<br>1 = UDP packet<br>0 = Non UDP packet |
| 3 | TCPP | PS0,RO | **TCP Packet of Current Received Packet**<br>1 = TCP Packet<br>0 = Non TCP Packet |
| 2 | IPP | PS0,RO | **IPv4 Packet of Current Received Packet**<br>1 = IP Packet<br>0 = Non IP Packet |
| 1 | RCSEN | PS0,RW | **Receive CheckSum Checking Enable**<br>When set, the checksum status (bit 7~2) will be stored in bit 7:2 of packet's first byte of RX packets status header respectively.<br>1 = Enable<br>0 = Disable |
| 0 | DCSE | PS0,RW | **Discard CheckSum Error Packet**<br>When set, if IPv4/TCP/UDP checksum field is error, this packet will be discarded.<br>1 = Enable<br>0 = Disable |

### 6.29 SPI Bus Control Register (38H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P0,RW | Reserved |
| 6:5 | CURR | PE10,RW | **SPI_MISO Current Driving/Sinking Capability**<br>00 = 2mA<br>01 = 4mA<br>10 = 6mA (default)<br>11 = 8mA |
| 4:3 | RESERVED | P00,RW | Reserved |
| 2 | CSB_SPIKE | PE1,RW | **Eliminate SPI_CSB Spike**<br>1 = Eliminate about 2ns SPI_CSB spike |
| 1:0 | RESERVED | P00,RW | Reserved |

### 6.30 INT Pin Control Register (39H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:2 | RESERVED | PS0,RO | Reserved |
| 1 | INT_TYPE | PET0,RW | **INT Pin Output Type Control**<br>1 = INT Open-Collector output<br>0 = INT push-pull output |
| 0 | INT_POL | PET0,RW | **INT Pin Polarity Control**<br>1 = INT active low<br>0 = INT active high |

### 6.31 INT Pin Control Register (3BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TX_FREE | PS0,R30H | TX Free Space in 64-byte unit |

### 6.32 Fiber SD Source Control Register (3CH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:5 | RESERVED | P0,RW | Pin Monitor Mode Index<br>0XX: no monitor pins<br>1XX: see monitor pin table |
| 4 | GP1_TXC | P0,RW | **GP1 pin act as TXC for IEEE 802.3 test reference clock.**<br>0: as normal GP1 , 1: as TXC out |
| 3 | SD_POL | P0,RW | **Fiber SD Active Low Control**<br>0: active high, 1: active low |
| 2:0 | SD_SRC | P0,RW | **Fiber SD Source Index**<br>000: from Fiber RX+/- activity<br>001: from GP1<br>010: from GP2<br>011: from GP3<br>100: from LNKLED<br>101: from SPDLED<br>110: from FDXLED<br>111: reserved |

**Monitor pin table:**

| 3CH[6:4] | GP1 | GP2 | WOL | FDXLED | LNKLED | SPDLED |
|---|---|---|---|---|---|---|
| 000 | txc | rxc | txe | rxdv | crs | col |
| 001 | txc | cable_st | link | rx_lock | dsp_retry | sd |
| 010 | ptp_1sec | p_1sec_trg | link | fdx | eee_en | rxer |
| 011 | txc | rxdv | txe | rxc | ptp_1sec | p_1sec_trg |
| 100 | byte_algn | algn_err | rx_overflow | rx_empty | rx_pkt_rdy | tx_full |
| 101 | bkf_st[2] | bkf_st[1] | Bkf_st[0] | mac_st[2] | mac_st[1] | mac_st[0] |
| 110 | tx_flp | rx_flp | an_st[3] | an_st[2] | an_st[1] | an_st[0] |
| 111 | txc | rx_idle_err | link | rx_lock | txsd | lpi_en |

### 6.33 Pause Packet Control/Status Register (3DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | PAUSE_CTR | P00,RO | **Pause Packet Counter**<br>The Pause packet counter before RX SRAM flow control low threshold reached. |
| 3:0 | PAUSE_MAX | PS1,RW | **Max. Pause Packet Count**<br>The maximum count of to generate pause packet with timer field FFFFH, when the RX memory is reached to high threshold.<br>If the value of these bits are zero, the pause packet with timer field FFFFH is generated whenever the RX memory is reached to the high threshold. |

### 6.34 IEEE 802.3az Enter Counter Register (3EH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P0,RO | Reserved |
| 6:0 | ENTER | P5,RW | **Timer to Enter EEE State (unit 2us)**<br>The DM9051A will enter EEE state after TX idle timer timeout. |

### 6.35 IEEE 802.3az Leave Counter Register (3FH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | EEE_EN | PE0,RW | EEE Enable |
| 6:0 | LEAVE | P0Fh,RW | **Timer to Leave EEE State (unit 2us)**<br>The DM9051A will leave EEE state after TX leave timer timeout when transmit command issued by set MAC register 2H bit 0 or Auto-Transmit. |

### 6.36 Strap Pin Status Register (40H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | STRAP_BYTE | P1,RO | **SPI Byte Memory Boundary Strap Pin Status**<br>0: SPI in word memory boundary<br>1: SPI in byte memory boundary |
| 6 | RESERVED | P0,RO | Reserved |
| 5 | IRQ_OC | P0,RO | IRQ in Open-Collect Mode<br>0: DC high/low mode<br>1: Open-collect mode |
| 4 | IRQ_LOW | P0,RO | IRQ in Low Active Mode<br>0: High active<br>1: Low active |
| 3:2 | RESERVED | P0,RO | Reserved |
| 1 | LED_MODE | P0,RO | LED Mode<br>0: LED mode 1<br>1: LED mode 0 |
| 0 | MDIX | P0,RO | PHY MDIX mode<br>0: MDI mode<br>1: MDIX mode |

### 6.37 Test Chip Version ID Register (46H)

| Bit | Name | Default | Description |
|---|---|---|---|
| 7:5 | RESERVED | P0,RO | reserved |
| 4:2 | VER_ID | PX,RO | Test Chip Version<br>111: test chip v0<br>011: test chip v1<br>110: test chip v2<br>010: test chip v3. |
| 1:0 | RESERVED | P0,RO | reserved |

### 6.38 SPI Byte Align Error Counter Register (4AH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | ALN_ERR | P00,RO | **SPI Clock Byte Align Error Counter**<br>The counter to count the byte align error of SPI_CK at end of SPI_CSN. The maximum value is 255. Cleared by write this register with any value. |

### 6.39 Crypt Test Register (4BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | CRYPT | P00,RW | **SPI ENCRYPT/DECRYPT code**<br>Before write or read the real crypt code, write this register with 0x51 and then 0x90.. |

### 6.40 RX Memory Write Address Test Register (4CH~4DH) (test only)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | RXWLTR | PS0,RW | **RX Memory Write Addresses High Byte (4DH)** |
| 7:0 | RXWHTR | PS0,RW | **RX Memory Write Addresses Low Byte (4CH)** |

### 6.41 TX Memory Read Address Test Register (4EH~4FH) (test only)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TXRLTR | PS0,RW | **TX Memory Read Addresses High Byte (4FH)** |
| 7:0 | TXRHTR | PS0,RW | **TX Memory Read Addresses Low Byte (4EH)** |

### 6.42 RX Packet Length Control Register (52H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RXLEN | PS0,RW | **RX Packet Length Filter**<br>1 = Enable check RX packet length<br>0 = Not to check RX packet length |
| 6:5 | RESERVED | P00,RO | Reserved |
| 4:0 | MAXRXLEN | PS0,RW | **Maximum RX Packet Length Allowed (unit 64-byte)**<br>The RX packet will be discarded if the data length is more than this count.<br><br>Note: all bits 0 means no length limitation |

### 6.43 RX Broadcast Control Register (53H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | BC_EN | PS0,RW | **New RX Broadcast Packet Control Mode**<br>0X = Broadcast packet control by bit 7 of MAC register 1DH<br>10 = Not to accept broadcast packet<br>11 = Enable packet length filter of broadcast packet |
| 5 | RESERVED | P0,RO | Reserved |
| 4:0 | MAXBCLEN | PS0,RW | **Maximum RX Broadcast Packet Length Allowed** (unit 64-byte)<br>The RX packet will be discarded if the data length is more than this count.<br><br>Note: all bits 0 means no length limitation |

### 6.44 INT Pin Clock Output Control Register (54H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | INT_CTL | PS0,RW | **INT Pin in Clock Output Control**<br>1 = Enable INT pin in clock output<br>0 = INT pin output controlled by MAC register 39H |
| 6 | CK_UNIT | PS0,RW | **Clock Output Duty Cycle Width Unit**<br>1 = 1.3ms<br>0 = 40.96us |
| 5 | RESERVED | P0,RO | Reserved |
| 4:0 | DUTY_LEN | PS0,RW | **Clock Output Duty Cycle Width**<br>Note: all bits 0 means INT pin is controlled by register 39H |

### 6.45 Memory Pointer Control Register (55H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:2 | RESERVED | P00,RO | Reserved |
| 1 | RST_TX | PS0,RW | **Reset TX Memory Pointer**<br>1 = Reset TX write/read memory address, Auto-Cleared after 1us |
| 0 | RST_RX | PS0,RW | **Reset RX Memory Pointer**<br>1 = Reset RX write/read memory address, Auto-Cleared after 1us |

### 6.46 ADC Memory Test Control Register (56H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | RESERVED | P00,RO | Reserved |
| 4 | TRIG_STATUS | PS0,RO | **ADC Trig Status**<br>1 = triggered |
| 3:2 | TRIG_MODE | PS0,RW | **ADC Memory Trig Mode**<br>The following trigger mode to define the trigger condition to store ADC data to full 16K memory after ADC_START command<br>00 = always triggered<br>01 = triggered when RX idle 5B data not equal to 0x1f<br>10 = triggered when RX lock to unlocked<br>11 = triggered when RX_ER assert |
| 1 | ADC_START | PS0,RW | **ADC Memory Monitor Start**<br>1 = start to monitor, auto-clear after write<br>0 = no operation |
| 0 | ADC_EN | PS0,RW | **ADC Memory Monitor mode**<br>1 = Enable<br>0=disable |

### 6.47 More LED Control Register (57H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | LED_MOD3 | P0,RW | **New LED Mode**<br>1 = LED types in bit 2:0<br>0 = The old LED mode 0 or 1 function |
| 6:3 | RESERVED | P00,RO | Reserved |
| 2 | LED_POL | P0,RW | **The Reverse Polarity of LED Type**<br>1 = LED in high active<br>0 = LED in low active |
| 1:0 | LED_TYPE | P00,RW | **LED Type**<br>Note: see following table |

| LED_Type | LNKLED (pin 25) | SPDLED (pin 26) | FDXLED (pin 16) |
|---|---|---|---|

| | | | |
|---|---|---|---|
| 00 | Link | Traffic | Full-Duplex |
| 01 | Link & Traffic | Speed100M | Full-Duplex |
| 10 | Traffic | Speed100M | Speed10M |
| 11 | Link | Traffic100M | Traffic10M |

### 6.48 E-fuse Control Register (58H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | EF_EN | P0,RW | **E-fuse read/write function enable**<br>1: to enable read or write function from register 0BH command |
| 6:4 | RESERVED | P0,RO | Reserved |
| 3 | EF_WREN | P0,RW | **E-fuse write function enable**<br>0: disable, 1: enable |
| 2 | RESERVED | P0,RW | Reserved |
| 1:0 | RESERVED | P0,RO | Reserved |

Note 1: when write E-fuse command, the REG_1FH bit 0 must be set to “1” (i.e. PHY power-down)
Note2 : MAC ID (in REG_10H~15H) init. Flow:
1. after poer-on reset, MAC_ID have random value, except REG_10H=0x00.
2. detect external EEPROM exist or not:
3. If EEPROM present: load EEPROM byte 0~5 to MAC_ID
4. if EEPROM absent: read E-fuse
 4.1 if E-fuse byte 0 not equal to 0xff, load bytes 0~5 to MAC_ID
 4.2 Else if E-fuse byte 6 not equal to 0xff, load bytes 6~11 to MAC_ID
 4.3 Else if E-fuse byte 12 not equal to 0xff and byte 22 bits [1:0] or [3:2] or [5:4] are not equal to “01”, load bytes 12~17 to MAC_ID

### 6.49 Memory Control Register (59H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:1 | RESERVED | P00,RO | Reserved |
| 0 | MSIZE_EN | P0,RW | **TX/RX Memory Size Configurable**<br>1 = Enable to configure TX/RX memory size by MAC register 5AH<br>0 = 3K-byte for TX and 13K-byte for RX |

### 6.50 Transmit Memory Size Register (5AH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:5 | RESERVED | P00,RO | Reserved |
| 4:0 | TRAM_SIZE | P3,RW | **TX Memory Size (unit K-byte)**<br>The RX memory size is 16 – TRAM_SIZE. |

### 6.51 Memory BIST Status Register (5DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | BIST_END | P0,RO | **Memory BIST Completion**<br>1 = Completed<br>0 = In progress |
| 6 | BIST_DIS | P0,RO | **Memory BIST Control**<br>This bit is the inverse of strap pin EECS.<br><br>1 = BIST disabled<br>0 = BIST enabled |
| 5 | RESERVED | P0,RO | Reserved |
| 4 | PAT_00 | P0,RO | **BIST 00H Pattern Status**<br>1 = OK<br>0 = Fail |
| 3 | PAT_DEC | P0,RO | **BIST Decrement Pattern Status**<br>1 = OK<br>0 = Fail |
| 2 | PAT_INC | P0,RO | **BIST Increment Pattern Status**<br>1 = OK<br>0 = Fail |
| 1 | PAT_AA | P0,RO | **BIST AAH Pattern Status**<br>1 = OK<br>0 = Fail |
| 0 | PAT_55 | P0,RO | **BIST 55H Pattern Status**<br>1 = OK<br>0 = Fail |

**Note: write 0xa0 to REG_5DH will restart BIST.**

### 6.52 PTP Status Register (60H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | GP2_ST | P0,RWC 1 | **GP2 trigger/event status**<br>0: disable or trigger completed<br>1: trigger active or event ready<br>Write “1” to clear this bit |
| 6 | GP2_TYPE | P0,RO | **GP2 event type**<br>0: event 1 is falling edge<br>1: event 1 is rising edge |
| 5 | GP1_ST | P0,RWC 1 | **GP1 trigger/event status**<br>0: disable or trigger completed<br>1: trigger active or event ready<br>Write “1” to clear this bit |
| 4 | GP1_TYPE | P0,RO | **GP1 event type**<br>0: event 0 is falling edge<br>1: event 0 is rising edge |
| 3:2 | RESERVED | P0,RO | Reserved |
| 1 | GP_PAGE | P0,RW | **GPIO Registers in 6AH ~ 6FH**<br>0: for GP1<br>1: for GP2 |
| 0 | PTP_RST | P0,RW | **PTP Function**<br>0: enable<br>1: disable |

### 6.53 PTP Clock Control Register (61H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | IDX_RST | PS0,RWC | **Reset Register 68H Index**<br>Write “1” to clear register 68H index.<br>This bit is self-cleared after write |
| 6 | RATE_CTL | PS0,RW | **PTP Rate Control**<br>0: add<br>1: subtract |
| 5 | PTP_RATE | PS0,RWC | **Write PTP Rate Clock**<br>The continued value of register 68H will be added/subtract to PTP clock in 2-32ns unit at every system clock<br>This bit is self-cleared after write |
| 4 | PTP_ADD | PS0,RWC | **Add PTP Clock**<br>The continued value of register 68H will be added to PTP clock<br>This bit is self-cleared after write |
| 3 | PTP_WRITE | PS0,RWC | **Write PTP Clock**<br>The continued value of register 68H will be written to PTP clock<br>This bit is self-cleared after write |
| 2 | PTP_READ | PS0,RWC | **Read PTP Clock**<br>The PTP clock will read-out from The continued value of register 68H<br>This bit is self-cleared after write |
| 1 | PTP_DIS | PS0,RW | **PTP Clock Disable**<br>Write “1” to disable PTP clock.<br>Write bit 0 to “1” will clear this bit. |
| 0 | PTP_EN | PS0,RW | **PTP Clock Enable** |

| | | | |
|---|---|---|---|
| | | | Write “1” to enable PTP clock.<br>Write bit 1 to “1” will clear this bit. |



### 6.54 PTP GPIO and TX/RX Control Register (62H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | INT_MASK | P0,RW | **PTP Interrupt Mask**<br>0: Interrupt disabled<br>1: Interrupt enabled |
| 6 | RESERVED | P0,RO | Reserved |
| 5 | GP2_TE | P0,RWC | **GP2 Trigger Load or Event Read**<br>this bit will be cleared automatically after the loading completed<br>For trigger:<br>After set this bit, the TIMER in register 68H will be loaded into trigger timer register.<br>For event:<br>After set this bit, the event timestamp will be loaded into register 68H. |
| 4 | GP1_TE | P0,RWC | **GP1 Trigger Load or Event Read**<br>this bit will be cleared automatically after the loading completed<br>For trigger:<br>After set this bit, the TIMER in register 68H will be loaded into trigger timer register.<br>For event:<br>After set this bit, the event timestamp will be loaded into register 68H. |
| 3:1 | RESERVED | P0,RO | Reserved |
| 0 | RD_TS | P0,RWC | **Read TX Time Stamp Clock** |

| | | | |
|---|---|---|---|
| | | | The TX timestamp will read-out to register 68H<br>This bit is self-cleared after write |

### 6.55 PTP One Step Check Sum Control Register (63H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | CKSM_DIS | P0,RW | **TX One Step Check Sum disabled**<br>0: enable to update one step check sum<br>1: disable |
| 6 | RD68_DIS | P0,RW | **Read REG_68H in One SPI cycle disabled**<br>0: enable continued read in one SPI cycle<br>1: disable |
| 5:0 | RESERVED | P0,RO | Reserved |

### 6.56 PTP Receive Control 1 Register (64H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P0,RW | Reserved |
| 6:5 | RESERVED | P0,RO | Reserved |
| 4 | RXTS_EN | PS0,RW | **Capture RX Timestamp to RX memory**<br>The 8-byte RX timestamp is saved between RX header and first RX data.<br>0: disable<br>1: enable |
| 3:2 | RESERVED | P0,RO | Reserved |
| 1:0 | RXTS_FLTR | PS0,RW | **RX Timestamp Control for DA Filter**<br>00=all packets<br>01=multicast packets<br>10=DA byte 0 is 0x01<br>11=specified DA packets (see note) |

Note: specified DA packets are 01:80:C2:00:00:0E, or 01:1B:19:00:00:00, or 01:00:5E:00:01:81

### 6.57 PTP One Step Address Offset (65H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | ADR_1STEP | PS4EH, RW | **Address offset for TX One-Step**<br>When TX one-step option enable, the 8-byte TX TimeStamp will be transmitted start from packet data address of this register |

### 6.58 PTP One Step Check Sum Address Offset (66H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | ADR_1CKSM | PS3CH, RW | **Address offset for TX One-Step Check Sum**<br>When TX one-step check sum option not disabled, the 2-byte TX TimeStamp check sum will be transmitted start from packet data address of this register |

### 6.59 PTP Clock Period (67H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | CLK_WIDTH | PS28H, RW | **PTP Clock Period**<br>The PTP clock is same as system clock. |

### 6.60 PTP Timestamp Registers (68H)

The index number will be increased after write or read this register.
The all PTP Timestamp can be read in one SPI cycle.

#### PTP Timestamp Nanosecond 0 Registers (68H)- index 0

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TNS_0 | PS0,RW | Timestamp nanosecond[07:00] |

#### PTP Timestamp Nanosecond 1 Registers (68H)- index 1

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TNS_1 | PS0,RW | Timestamp nanosecond[15:08] |

#### PTP Timestamp Nanosecond 2 Registers (68H)- index 2

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TNS_2 | PS0,RW | Timestamp nanosecond[23:16] |

#### PTP Timestamp Nanosecond 3 Registers (68H)- index 3

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TNS_3 | PS0,RW | Timestamp nanosecond[31:24] |

#### PTP Timestamp Second 0 Registers (68H)- index 4

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TS_0 | PS0,RW | Timestamp second[07:00] |

### PTP Timestamp Second 1 Registers (68H)- index 5

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TS_1 | PS0,RW | Timestamp second[15:08] |

### PTP Timestamp Second 2 Registers (68H)- index 6

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TS_2 | PS0,RW | Timestamp second[23:16] |

### PTP Timestamp Second 3 Registers (68H)- index 7

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TS_3 | PS0,RW | Timestamp second[31:24] |



## 6.61 PTP Monitor Register (69H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:4 | IDX_68H | P0,RO | Index of REG_68H |
| 3:1 | RESERVED | P0,RO | Reserved |
| 0 | RD_RAT | P0,RW | **Read Clock Rate Value**<br>The PTP clock rate will read-out from the continued 5 bytes value of register 68H<br>Byte 1~4 are the clock rate value<br>Byte 5: 0=positive rate, 1=negative rate |

## 6.62 GPIO Control Register (6AH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | GP_ST | P0,RWC1 | GP2 trigger/event status<br>0: disable or trigger completed<br>1: trigger active or event ready<br>Write “1” to clear this bit |
| 6 | GP_TYPE | P0,RO | GP2 event type status<br>0: event 1 is falling edge<br>1: event 1 is rising edge |
| 2 | GP_INTEN | P0,RW | **GPIO Interrupt Control**<br>0: GPIO interrupt disable<br>1: GPIO interrupt enable |

| | | | |
|---|---|---|---|
| 1 | TRIG_EN | P0,RW | **GPIO Trigger/Event Enable Control**<br>0: trigger and event disabled<br>1: trigger or event enabled |
| 0 | GP_TYPE | P0,RW | **GPIO type**<br>0: trigger output mode<br>1: event input mode |

### 6.63 GPIO Trigger/Event Control Register (6BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P0,RO | Reserved |
| 6 | EVENT_LCK | P0,RW | **GPIO Event Timestamp Lock Disable**<br>0: lock first event, 1: can overwrite, |
| 5 | GP_R_EVT | P0,RW | **GPIO Event Rise Detect**<br>0: no detect rising edge event<br>1: detect rising edge eventv |
| 4 | GP_F_EVT | P0,RW | **GPIO Event Fall Detect**<br>0: no detect falling edge event<br>1: detect falling edge event |
| 3:2 | TRIG_TYPE | P0,RW | **Trigger Output Type**<br>00: edge output, 01: edge toggle<br>10: single pulse, 11: periodic pulse |
| 1 | TRIG_POR | P0,RW | **GPIO Trigger Polarity Control**<br>0: GPIO trigger output active low<br>1: GPIO trigger output active high |
| 0 | RESERVED | P0,RO | Reserved |

### 6.64 GPIO Trigger Asserted Pulse Low Register (6CH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | PULSE1_LO | P0,RW | Pulse Width or Periodic Pulse Asserted Period [7:0] |

### 6.65 GPIO Trigger Asserted Pulse High Register (6DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | PULSE1_U | P0,RW | **Pulse Width or Periodic Pulse Asserted Period Unit**<br>00: 120ns<br>01: 1us<br>10: 1ms<br>11: 1us |
| 5:0 | PULSE1_HI | P0,RW | Pulse Width or Periodic Pulse Asserted Period [13:8] |

### 6.66 GPIO Trigger Periodic De-asserted Pulse Low Register (6EH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | PULSE2_LO | P0,RW | Periodic Pulse Deasserted Period [7:0] |

### 6.67 GPIO Trigger Periodic De-asserted Pulse High Register (6FH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:6 | PULSE2_U | P0,RW | **Periodic Pulse De-asserted Period Unit**<br>00: 120ns<br>01: 1us<br>10: 1ms<br>11: 1us |
| 5:0 | PULSE2_HI | P0,RW ` | Periodic Pulse De-asserted Period [13:8] |

### 6.68 Memory Data Pre-Fetch Read Command without Address Increment Register (70H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MRCMDX | X,RO | **Memory Read Command**<br>Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the DM9051A starts to pre-fetch the SRAM data to internal data buffers. |

### 6.69 Memory Read Command without Data Pre-Fetch and Address Increment Register (71H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MRCMDX1 | X,RO | **Memory Read Command**<br>Read data from RX Memory. After the read of this command, the read pointer of RX memory is unchanged. And the DM9051A do not pre-fetch the memory data. |

### 6.70 Memory Data Read Command with Address Increment Register (72H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MRCMD | X,RO | **Memory Read Command**<br>Read data from RX SRAM. After the read of this command, the read pointer is increased by 1. |

### 6.71 SPI Data Read Delay Counter Register (73H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | RD_DLY | 0,WO | **Read Data Delay Counter**<br>The byte delay counter that first data is valid after command byte. |

### 6.72 Memory Data Read Address Register (74H~75H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MDRAH | PS0,RW | **Memory Data Read Addresses High Byte**<br>It will be set to 0CH, when IMR bit7 =1 (75H) |
| 7:0 | MDRAL | PS0,RW | **Memory Data Read Address Low Byte** (74H) |

### 6.73 Memory Data Write Command without Address Increment Register (76H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MWCMDX | X,WO | **Write Data to TX Memory**<br>After the write of this command, the write pointer is unchanged |

### 6.74 Memory Data Write Command with Address Increment Register (78H)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MWCMD | X,WO | **Write Data to TX SRAM**<br>After the write of this command, the write pointer is increased by 1. |

### 6.75 Memory Data Write Address Register (7AH~7BH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | MDWAH | PS0,RW | Memory Data Write Address High Byte (7BH) |
| 7:0 | MDWAL | PS0,RW | Memory Data Write Address Low Byte (7AH) |

### 6.76 TX Packet Length Register (7CH~7DH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7:0 | TXPLH | X,R/W | TX Packet Length High Byte (7DH) |
| 7:0 | TXPLL | X,R/W | TX Packet Length Low Byte (7CH) |

### 6.77 Interrupt Status Register (7EH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | RESERVED | P1,RO | Reserved |
| 6 | RESERVED | RO | Reserved |
| 5 | LNKCHG | PS0,RW/C1 | **Link Status Change**<br>1 = Affirmative<br>0 = Negative |
| 4 | RESERVED | RO | Reserved |
| 3 | ROO | PS0,RW/C1 | **Receive Overflow Counter Overflow**<br>1 = Affirmative<br>0 = Negative |
| 2 | ROS | PS0,RW/C1 | **Receive Overflow**<br>1 = Affirmative<br>0 = Negative |
| 1 | PT | PS0,RW/C1 | **Packet Transmitted**<br>1 = Affirmative<br>0 = Negative |
| 0 | PR | PS0,RW/C1 | **Packet Received**<br>1 = Affirmative<br>0 = Negative |

### 6.78 Interrupt Mask Register (7FH)

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 7 | PAR | PS0,RW | **Pointer Auto-Return Mode**<br>Enable the TX/RX memory read/write pointer to automatically return to the start address when pointers are over the TX/RX memory size. When this bit is set, the MAC register 75H will be set to 0CH automatically if RX memory size is 13K-byte.<br>1 = Enable<br>0 = Disable |
| 6 | RESERVED | RO | Reserved |
| 5 | LNKCHGI | PS0,RW | **Enable Link Status Change Interrupt**<br>1 = Enable<br>0 = Disable |
| 4 | RESERVED | RO | Reserved |
| 3 | ROOI | PS0,RW | **Enable Receive Overflow Counter Overflow Interrupt**<br>1 = Enable<br>0 = Disable |
| 2 | ROI | PS0,RW | **Enable Receive Overflow Interrupt**<br>1 = Enable<br>0 = Disable |
| 1 | PTI | PS0,RW | **Enable Packet Transmitted Interrupt**<br>1 = Enable<br>0 = Disable |
| 0 | PRI | PS0,RW | **Enable Packet Received Interrupt**<br>1 = Enable<br>0 = Disable |

# 7 EEPROM/EFuse and SPI Command Format

## 7.1.1 EEPROM Format

| Name | Word | Offset | Description |
|---|---|---|---|
| MAC Address | 0 | 0~5 | 6 Byte Ethernet Address |
| Auto Load Control | 3 | 6~7 | Bit 1:0 = 01: Update vendor ID and product ID from WORD4 and 5.<br>Bit 3:2 = 01: Accept setting of WORD6 [15,4:3]<br>Bit 5:4 = 01: Reserved, set to 00 in application<br>Bit 7:6 = 01: Accept setting of WORD7 [3:0]<br>Bit 9:8 = 01: Accept setting of WORD8[3:0]<br>Bit 11:10 = 01: Accept setting of WORD7 [7]<br>Bit 13:12 = 01: Accept setting of WORD7 [9:8]<br>Bit 15:14 = 01: Accept setting of WORD7 [15:12] |
| Vendor ID | 4 | 8~9 | 2 byte vendor ID (Default: 0A46H) |
| Product ID | 5 | 10~11 | 2 byte product ID (Default: 9051H) |
| Pin Control / Control 1 | 6 | 12~13 | When word 3 bit [3:2]=01, these bits can control the INT pins polarity.<br>Bit 2:0: Reserved; set to 0 in application<br>Bit 3: INT pin is active low when set (default: active high)<br>Bit 4: INT pin is open-collected (default: push-pull output)<br>Bit 14:5: Reserved; set to 0 in application<br>Bit 15: Enable 802.3az, to MAC register 3FH bit [7] |
| Wake-up Mode Control / Control 2 | 7 | 14~15 | Bit 0: The WOL pin is active low when set (default: active high)<br>Bit 1: The WOL pin is in pulse mode when set (default: push-pull mode)<br>Bit 2: Magic wakeup event is enabled when set. (default: disable)<br>Bit 3: Link change wakeup event is enabled when set (default disable)<br>Bit 6:4: Reserved; set to 0 in application<br>Bit 7:0 = LED mode 0, 1=LED mode 1 (default: mode 0)<br>Bit 8:1 = Internal PHY is enabled after power-on (default: disable)<br>Bit 9: Fiber Mode Control; 1= Fiber mode, 0 = TP mode<br>Bit 13:10: Reserved; set to 0 in application<br>Bit 14: Reserved; set to 1 in application<br>Bit 15: Reserved; set to 0 in application |
| Control 3 | 8 | 16~17 | Bit 0: Reserved; set to 1 in application.<br>Bit 1: Eliminate SPI_CSB high spike control<br>This bit will be load into MAC register 38H bit 2<br>Bit 3:2: SPI_MISO driving capability<br>This bit will be load into MAC register 38H bit [6:5] |

### 7.1.2 E-fuse Format

| Name | Byte | Description |
|---|---|---|
| MAC ID SET 1 | 0~5 | 6 Byte Ethernet Address Set 1 |
| MAC ID SET 2 | 6~11 | 6 Byte Ethernet Address Set 2 |
| MAC ID SET 3 | 12~17 | 6 Byte Ethernet Address Set 3<br>Valid if byte 22[5:4] and [3:2] and [1:0] are all not equal to “01” |
| Vendor ID_LO | 12 | vendor ID low byte |
| Vendor ID_HI | 13 | vendor ID high byte |
| Product ID_LO | 14 | product ID low byte |
| Product ID_HI | 15 | product ID high byte |
| SPI Pin control | 16 | When byte 22 bit [3:2]=01, these bits can be controlled.<br>Bit 4~0: Reserved, set to 0 in application<br>Bit 5: Eliminate SPI_CSB high spike control<br>This bit will be load into register 38H bit 2<br>Bit 7~6: SPI_MISO driving capability<br>This bit will be load into register 38H bit [6:5] |
| Wake-up mode control | 17 | When byte 22 bit [5:4]=01, these bits can be controlled.<br>Bit 0: The WOL pin is active low when set<br>Bit 1: The WOL pin is in pulse mode when set<br>Bit 2: Magic wakeup event is enabled when set.<br>Bit 3: Link change wakeup event is enabled when set<br>Bit 6~4: Reserved; set to 0 in application<br>Bit 7 = LED mode 0, 1=LED mode 1 |
| TRIM_RES | 18 | Trim Value of internal 50Ohm Resistor<br>Bit 7~6 = 01: Accept setting of byte 18 [5:0] as trim data PHY 50Ohm |
| CODE1 | 19 | Encryption/decryption code 1<br>Valid if not equal to 0xFF |
| CODE2 | 20 | Encryption/decryption code 2<br>Valid if not equal to 0xFF and CODE1 is not valid. |
| CODE3 | 21 | Encryption/decryption code 3<br>Valid if not equal to 0xFF and CODE1/2 are not valid. |
| Auto Load Control | 22 | When EEPROM is not exist,<br>Bit 1:0 = 01: Update vendor ID and product ID from byte 12~15.<br>Bit 3:2 = 01: Accept setting of byte 16 [7:5]<br>Bit 5:4 = 01: Accept setting of byte 17 [7,3:0]<br>Bit 7:6 = 01: Accept setting of byte 23 [4:0] |
| PHY/IRQ Control | 23 | When byte 22 bit [7:6]=01, these bits can be controlled.<br>Bit 0: 1 = Internal PHY is enabled after power-on<br>Bit 1: PHY Fiber Mode Control; 1= Fiber mode, 0: TP mode<br>Bit 2: PHY enable 802.3az, to register 3FH bit [7]<br>Bit 3: IRQ pin is active low when set<br>Bit 4: IRQ pin is open-collected |

**Note: byte 0~17, and 22~23 valid only if no EEPROM exist.**

### 7.2 SPI Command Format

| SPI | Command Phase (MOSI pin) | | Data Phase (MOSI pin) |
|---|---|---|---|
| | Byte 0 [7:0] | | Byte 1 |
| | Opcode | Register Address | Register Data |
| Register Write | 1 | A6~A0 | D7~D0 |

| SPI | Command Phase (MOSI pin) | | Data Phase (MISO pin) |
|---|---|---|---|
| | Byte 0 [7:0] | | Byte 1 |
| | Opcode | Register Address | Register Data |
| Register Read | 0 | A6~A0 | D7~D0 |
| Memory Dummy Read | 0 | 1110000 | D7~D0 |

| SPI | Command Phase (MOSI pin) | | Data Phase (MISO pin) |
|---|---|---|---|
| | Byte 0 [7:0] | | Byte 1~N |
| | Opcode | Register Address | Memory Data |
| Memory Dummy Read Without Pre-fetch | 0 | 1110001 | (D7~D0)*N (Note 1) |

Note 1: N can be 1~4

| SPI | Command Phase (MOSI pin) | | Data Phase (MOSI pin) |
|---|---|---|---|
| | Byte 0 [7:0] | | Byte 1~N |
| | Opcode | Register Address | Memory Data |
| Memory Write | 1 | 1111000 | (D7~D0)*N |

| SPI | Command Phase (MOSI pin) | | Data Phase (MISO pin) |
|---|---|---|---|
| | Byte 0 [7:0] | | Byte 1~N |
| | Opcode | Register Address | Memory Data |
| Memory Read | 0 | 1110010 | (D7~D0)*N |

| SPI | Command Phase (MOSI pin) | | Data Phase (MOSI pin) |
|---|---|---|---|
| | Byte 0 | | Byte 1~N |
| | Opcode | Register Address | Transmit Length and Packet Data |
| Auto-Transmit | 1 | 1111100 | (D7~D0)*N (see Note2,3) |

Note 2:
Byte 1: Transmit Length bit 7~0 of n-byte
Byte 2: FDH
Byte 3: Transmit Length bit 15~8 of n-byte
Byte 4: F8H
Byte 5~n+4: 5~n+4: n-byte transmit data

Note 3: This command burst is used only when register 30H bit 7 is set

| SPI | Command Phase (MOSI pin) | | Data Phase (MISO pin) |
|---|---|---|---|
| | Byte 0 | | Byte 1~N |
| | Opcode | Register Address | Chip Status Data |
| Chip Status | 0 | 1111110 | (D7~D0)*N (see NOTE4) |

NOTE 4: N can be 1 or 12
Byte 1: ISR (from register 7EH)
Byte 2: NSR (from register 01H, but bit 4 from register 02H bit 0)
Byte 3: RX memory read address 7~0
Byte 4: RX memory read address 15~8
Byte 5: RX memory write address 7~0
Byte 6: RX memory write address 15~8
Byte 7: TX memory read address 7~0
Byte 8: TX memory read address 15~8
Byte 9: TX memory write address 7~0
Byte 10: TX memory write address 15~8
Byte 11: WCR (from register 0FH)
Byte 12: GPR (from register 1FH)

| SPI | Command Phase (MOSI pin) | | Data Phase (MISO pin) |
|---|---|---|---|
| | Byte 0 | | Byte 1~N |
| | Opcode | Register Address | Time Stamp Data |
| PTP Time Stamp | 0 | 1101000 | (D7~D0)*N (see NOTE5) |

NOTE 5: N can be up to 8, if REG_63H bit 6 is 0; otherwise N is 1
Byte 1: nanosec bits 7~0
Byte 2: nanosec bits 15~8
Byte 3: nanosec bits 23~16
Byte 4: nanosec bits 29~24
Byte 5: sec bits 7 ~0
Byte 6: sec bits 15~8
Byte 7: sec bits 23~16
Byte 8: sec bits 31~24

## 8. PHY Register Description

| ADD | Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | CONTROL | Reset | Loop back | Speed select | Auto-N Enable | Power Down | Isolate | Restart Auto-N | Full Duplex | Coll. Test | Reserved | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 000_0000 | | | | | | |
| 01 | STATUS | T4 Cap. | TX FDX Cap. | TX HDX Cap. | 10 FDX Cap. | 10 HDX Cap. | Reserved | | | | Pream. Supr. | Auto-N Compl. | Remote Fault | Auto-N Cap. | Link Status | Jabber Detect | Extd Cap. |
| | | 0 | 1 | 1 | 1 | 1 | 0000 | | | | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 02 | PHYID1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03 | PHYID2 | 1 | 0 | 1 | 1 | 1 | 0 | Model No. | | | | | Version No. | | | | |
| | | | | | | | | 001010 | | | | | 0000 | | | | |
| 04 | Auto-Neg. Advertise | Next Page | FLP Rcv Ack | Remote Fault | Reserved | | FC Adv | T4 Adv | TX FDX Adv | TX HDX Adv | 10 FDX Adv | 10 HDX Adv | Advertised Protocol Selector Field | | | | |
| 05 | Link Part. Ability | LP Next Page | LP Ack | LP RF | Reserved | | LP FC | LP T4 | LP TX FDX | LP TX HDX | LP 10 FDX | LP 10 HDX | Link Partner Protocol Selector Field | | | | |
| 06 | Auto-Neg. Expansion | Reserved | | | | | | | | | | | Pardet Fault | LP Next Pg Able | Next Pg Able | New Pg Rcv | LP AutoN Cap. |
| 16 | Specified Config. | BP 4B5B | BP SCR | BP ALIGN | BP_ADP OK | Repeater | TX | FEF_EN | RMII_EN | Force 100LNK | TST_SEL0 | LEDCOL_SEL | RPDCTR-EN | Reset St. Mch | Pream. Supr. | Sleep mode | Remote LoopOut |
| 17 | Specified Conf/Stat | 100 FDX | 100 HDX | 10 FDX | 10 HDX | EEE_en | Reversed | Reversed | PHY ADDR [4:0] | | | | Auto-N. Monitor Bit [3:0] | | | | |
| 18 | 10T Conf/Stat | Rsvd | LP Enable | HBE Enable | SQUE Enable | JAB Enable | 10T Serial | Reserved | | | | | | | | | Polarity Reverse |
| 19 | PWDOR | Reserved | | | | | | | PD10DRV | PD100I | PDchip | PDcrm | PDaeq | PDdrv | PDecli | PDeclo | PD10 |
| 20 | Specified config | TSTSE1 | TSTSE2 | FORCE_TXSD | FORCE_FEF | PREAMBLEX | TX10M_PWR | NWAY_PWR | Reserved | MDIX_CNTL | AutoNeg_dlpbk | Mdix_fix Value | Mdix_down | MonSel1 | MonSel0 | Rmii_accu | PD_value |
| 21 | MDINTR | Int_sts | Reserved | Reserved | Reversed | Fdx_msk | Spd_msk | Lnk_msk | Int_msk | Reserved | Reserved | Reversed | Fdx_chg | Spd_chg | Lnk_chg | Reserved | Int_sts |
| 22 | RCVER | Receiver Error Counter | | | | | | | | | | | | | | | |
| 23 | DIS_connect | Reversed | | | | | | | | Disconnect_counter | | | | | | | |
| 24 | RSTLH | Lh_led_mode | Lh_mdintr | Lh_cabsts | Lh_isolate | Lh_rmii | Lh_seril10 | Lh_repeater | Lh_testmode | Lh_op2 | Lh_op1 | Lh_op0 | Lh_phyad4 | Lh_phyad3 | Lh_phyad2 | Lh_phyad1 | Lh_phyad0 |
| 25 | RADVR | Reserved | | | | | | | | | | | | | | | |
| 26 | RLPAR | Reserved | | | | | | | | | | | | | | | |
| 27 | DSPCR | FIL_CTL | | | reserved | | | | CABLE_LEN | | | FILTERR | | | Reserved | | |
| 28 | RGCR | Reserved | | | | | | REG_CTL | | | | | Reserved | | | | |
| 29 | PSCR | Reserved | | | LPI | preamblex | amplitude | TX_PWR | Reserved | | | | | | | | |
| 30 | MONITOR | Reserved | | | | | | | | | | | | | | | |
| 31 | PAGE | Page Number | | | | | | | | | | | | | | | |
| 1.17 | TOTCR | Reserved | | | F_TRIM | | | | Reserved | | | | | | TRIM | | |

**Key to Default**

**Key to Default**

In the register description that follows, the default column takes the form:

<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:
- RO = Read Only
- RW = Read/Write

<Attribute(s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

### 8.1 Basic Mode Control Register (BMCR) – 00H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | Reset | 0, RW/SC | **Reset**<br>1=Software reset<br>0=Normal operation<br><br>This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed. |
| 14 | Loopback | 0, RW | **Loopback**<br>Loopback control register<br>1 = Loopback enabled<br>0 = Normal operation<br><br>When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 1300ms "dead time" before any valid data appear at the MII receive outputs. |
| 13 | Speed Selection | 1, RW | **Speed select**<br>1 = 100Mbps<br>0 = 10Mbps<br><br>Link speed may be selected either by this bit or by Auto-Negotiation. When Auto-Negotiation is enabled and bit 12 is set, this bit will return Auto-Negotiation selected media type. |
| 12 | Auto-Negotiation Enable | 1, RW | **Auto-Negotiation enable**<br>1 = Auto-Negotiation is enabled, bit 8 and 13 will be in Auto-Negotiation status |
| 11 | Power Down | 0, RW | **Power Down**<br>While in the power down state, the PHY should respond to management transactions. During the transition to power down state and while in the power down state, the PHY should not generate spurious signals on the MII.<br><br>1 = Power down<br>0 = Normal operation |
| 10 | Isolate | 0,RW | **Isolate**<br>1 = Isolates the PHY from the MII with the exception of the serial management. (When this bit is asserted, the PHY does not respond to the TXD[0:3], TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RX[0:3], COL and CRS outputs. When PHY is isolated from the MII it shall respond to the management transactions)<br>0 = Normal operation |
| 9 | Restart Auto-Negotiation | 0,RW/SC | **Restart Auto-Negotiation**<br>1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. When Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until Auto-Negotiation is initiated by the PHY. The operation of the Auto-Negotiation process will not be affected by the management entity that clears this bit<br>0 = Normal operation |

| | | | |
|---|---|---|---|
| 8 | Duplex Mode | 1,RW | **Duplex Mode**<br>1 = Full-Duplex operation. Duplex selection is allowed when Auto-Negotiation is disabled (bit 12 of this register is cleared). With Auto-Negotiation enabled, this bit reflects the duplex capability selected by Auto-Negotiation<br>0 = Normal operation |
| 7 | Collision Test | 0,RW | **Collision Test**<br>1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN<br>0 = Normal operation |
| 6:0 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read |

### 8.2 Basic Mode Status Register (BMSR) – 01H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | 100BASE-T4 | 0,RO/P | **100BASE-T4 Capable**<br>1 = Able to perform in 100BASE-T4 mode<br>0 = Not able to perform in 100BASE-T4 mode |
| 14 | 100BASE-TX Full-Duplex | 1,RO/P | **100BASE-TX Full-Duplex Capable**<br>1 = Able to perform 100BASE-TX in Full-Duplex mode<br>0 = Not able to perform 100BASE-TX in Full-Duplex mode |
| 13 | 100BASE-TX Half-Duplex | 1,RO/P | **100BASE-TX Half-Duplex Capable**<br>1 = Able to perform 100BASE-TX in Half-Duplex mode<br>0 = Not able to perform 100BASE-TX in Half-Duplex mode |
| 12 | 10BASE-T Full-Duplex | 1,RO/P | **10BASE-T Full-Duplex Capable**<br>1 = Able to perform 10BASE-T in Full-Duplex mode<br>0 = Not able to perform 10BASE-TX in Full-Duplex mode |
| 11 | 10BASE-T Half-Duplex | 1,RO/P | **10BASE-T Half-Duplex Capable**<br>1 = Able to perform 10BASE-T in Half-Duplex mode<br>0 = Not able to perform 10BASE-T in Half-Duplex mode |
| 10:7 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read |
| 6 | MF Preamble Suppression | 0,RO | **MII Frame Preamble Suppression**<br>1 = PHY will accept management frames with preamble suppressed<br>0 = PHY will not accept management frames with preamble suppressed |
| 5 | Auto-Negotiation Complete | 0,RO | **Auto-Negotiation Complete**<br>1 = Auto-Negotiation process completed<br>0 = Auto-Negotiation process not completed |
| 4 | Remote Fault | 0,RO/LH | **Remote Fault**<br>1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is PHY implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05H) is set<br>0 = No remote fault condition detected |

| | | | |
|---|---|---|---|
| 3 | Auto-Negotiation Ability | 1,RO/P | **Auto Configuration Ability**<br>1 = Able to perform Auto-Negotiation<br>0 = Not able to perform Auto-Negotiation |
| 2 | Link Status | 0,RO/LL | **Link Status**<br>1 = Valid link is established (for either 10Mbps or 100Mbps operation)<br>0 = Link is not established<br>The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface. |
| 1 | Jabber Detect | 0,RO/LH | **Jabber Detect**<br>1 = Jabber condition detected<br>0 = No jabber<br>This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a PHY reset. This bit works only in 10Mbps mode. |
| 0 | Extended Capability | 1,RO/P | **Extended Capability:**<br>1 = Extended register capable<br>0 = Basic register capable only |

### 8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9051A. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15.0 | OUI_MSB | 0181h | **OUI Most Significant Bits**<br>This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2). |

### 8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:10 | OUI_LSB | 101110, RO/P | **OUI Least Significant Bits:**<br>Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively. |
| 9:4 | VNDR_MDL | 001010, RO/P | **Vendor Model Number**<br>Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9). |
| 3:0 | MDL_REV | 0000, RO/P | **Model Revision Number**<br>Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3). |

### 8.5 Auto-Negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM905(I) device as they will be transmitted to its link partner during Auto-Negotiation.

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | NP | 0,RO/P | **Next Page Indication**<br>1 = Next page available<br>0 = No next page available<br><br>The PHY has no next page, so this bit is permanently set to 0. |
| 14 | ACK | 0,RO | **Acknowledge**<br>1 = Link partner ability data reception acknowledged<br>0 = Not acknowledged<br><br>The PHY's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit. |
| 13 | RF | 0,RW | **Remote Fault**<br>1 = Local device senses a fault condition<br>0 = No fault detected |
| 12:11 | RESERVED | X,RW | **Reserved**<br>Write as 0, ignore on read |
| 10 | FCS | 0,RW | **Flow Control Support**<br>1 = Controller chip supports flow control ability<br>0 = Controller chip doesn't support flow control ability |
| 9 | T4 | 0,RO/P | **100BASE-T4 Support**<br>1 = 100BASE-T4 is supported by the local device<br>0 = 100BASE-T4 is not supported<br><br>The PHY does not support 100BASE-T4 so this bit is permanently set to 0 |
| 8 | TX_FDX | 1,RW | **100BASE-TX Full-Duplex Support**<br>1 = 100BASE-TX Full-Duplex is supported by the local device<br>0 = 100BASE-TX Full-Duplex is not supported |
| 7 | TX_HDX | 1,RW | **100BASE-TX Support**<br>1 = 100BASE-TX is supported by the local device<br>0 = 100BASE-TX is not supported |
| 6 | 10_FDX | 1,RW | **10BASE-T Full-Duplex support**<br>1 = 10BASE-T Full-Duplex is supported by the local device<br>0 = 10BASE-T Full-Duplex is not supported |
| 5 | 10_HDX | 1,RW | **10BASE-T Support**<br>1 = 10BASE-T is supported by the local device<br>0 = 10BASE-T is not supported |
| 4:0 | Selector | 00001,RW | **Protocol Selection Bits**<br>These bits contain the binary encoded protocol selector supported by this node.<br><00001> indicates that this device supports IEEE 802.3 CSMA/CD. |

### 8.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-Negotiation.

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | NP | 0,RO | **Next Page Indication**<br>1 = Link partner, next page available<br>0 = Link partner, no next page available |
| 14 | ACK | 0,RO | **Acknowledge**<br>1 = Link partner ability data reception acknowledged<br>0 = Not acknowledged<br>The PHY's Auto-Negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit. |
| 13 | RF | 0,RO | **Remote Fault**<br>1 = Remote fault indicated by link partner<br>0 = No remote fault indicated by link partner |
| 12:11 | RESERVED | X,RO | **Reserved**<br>Write as 0, ignore on read |
| 10 | FCS | 0,RW | **Flow Control Support**<br>1 = Controller chip supports flow control ability by link partner<br>0 = Controller chip doesn't support flow control ability by link partner |
| 9 | T4 | 0,RO | **100BASE-T4 Support**<br>1 = 100BASE-T4 is supported by the link partner<br>0 = 100BASE-T4 is not supported by the link partner |
| 8 | TX_FDX | 0,RO | **100BASE-TX Full-Duplex Support**<br>1 = 100BASE-TX Full-Duplex is supported by the link partner<br>0 = 100BASE-TX Full-Duplex is not supported by the link partner |
| 7 | TX_HDX | 0,RO | **100BASE-TX Support**<br>1 = 100BASE-TX Half-Duplex is supported by the link partner<br>0 = 100BASE-TX Half-Duplex is not supported by the link partner |
| 6 | 10_FDX | 0,RO | **10BASE-T Full-Duplex Support**<br>1 = 10BASE-T Full-Duplex is supported by the link partner<br>0 = 10BASE-T Full-Duplex is not supported by the link partner |
| 5 | 10_HDX | 0,RO | **10BASE-T Support**<br>1 = 10BASE-T Half-Duplex is supported by the link partner<br>0 = 10BASE-T Half-Duplex is not supported by the link partner |
| 4:0 | Selector | 00000,RO | **Protocol Selection Bits**<br>Link partner's binary encoded protocol selector. |

### 8.7 Auto-Negotiation Expansion Register (ANER) – 06H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:5 | RESERVED | X,RO | **Reserved**<br>Write as 0, ignore on read |
| 4 | PDF | 0,RO/LH | **Local Device Parallel Detection Fault**<br>1 = A fault detected via parallel detection function<br>0 = No fault detected via parallel detection function |
| 3 | LP_NP_ABLE | 0,RO | **Link Partner Next Page Able**<br>1 = Link partner, next page available<br>0 = Link partner, no next page |
| 2 | NP_ABLE | 0,RO/P | **Local Device Next Page Able**<br>1 = Next page available<br>0 = No next page |
| 1 | PAGE_RX | 0,RO/LH | **New Page Received**<br>A new link code word page received. This bit will be automatically cleared when the register (register 6H) is read by management. |
| 0 | LP_AN_ABLE | 0,RO | **Link Partner Auto-Negotiation Able**<br>A "1" in this bit indicates that the link partner supports Auto-Negotiation. |

### 8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | BP_4B5B | 0,RW | **Bypass 4B5B Encoding and 5B4B Decoding**<br>1 = 4B5B encoder and 5B4B decoder function bypassed<br>0 = Normal 4B5B and 5B4B operation |
| 14 | BP_SCR | 0,RW | **Bypass Scrambler/Descrambler Function**<br>1 = Scrambler and descrambler function bypassed<br>0 = Normal scrambler and descrambler operation |
| 13 | BP_ALIGN | 0,RW | **Bypass Symbol Alignment Function**<br>1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed<br>0 = Normal operation |
| 12 | BP_ADPOK | 0,RW | **BYPASS ADPOK**<br>Force signal detector (SD) active. This register is for debug only, not release to customer.<br>1 = Force SD is OK<br>0 = Normal operation |
| 11 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 10 | TX | 1,RW | **100BASE-TX or FX Mode Control**<br>1 = 100BASE-TX operation<br>0 = 100BASE-FX operation |
| 9 | RESERVED | 0,RO | **Reserved** |
| 8 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 7 | F_LINK_100 | 0,RW | **Force Good Link in 100Mbps**<br>1 = Force 100Mbps good link status<br>0 = Normal 100Mbps operation<br>This bit is useful for diagnostic purposes. |
| 6 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 5 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |

| | | | |
|---|---|---|---|
| 4 | RPDCTR-EN | 1,RW | **Reduced Power Down Control Enable**<br>This bit is used to enable automatic reduced power down.<br>1 = Enable automatic reduced power down<br>0 = Disable automatic reduced power down |
| 3 | SMRST | 0,RW | **Reset state machine**<br>When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed. |
| 2 | MFPSC | 1,RW | **MF Preamble Suppression Control**<br>MII frame preamble suppression control bit.<br>1 = MF preamble suppression bit on<br>0 = MF preamble suppression bit off |
| 1 | SLEEP | 0,RW | **Sleep Mode**<br>Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset. |
| 0 | RLOUT | 0, RW | Remote Loop out Control<br>When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing |

### 8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | 100FDX | 1,RO | **100M Full-Duplex Operation Mode**<br>After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode. |
| 14 | 100HDX | 1,RO | **100M Half-Duplex Operation Mode**<br>After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode. |
| 13 | 10FDX | 1,RO | **10M Full-Duplex Operation Mode**<br>After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode. |
| 12 | 10HDX | 1,RO | **10M Half-Duplex Operation Mode**<br>After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Half-Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode. |
| 11:9 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 8:4 | PHYADR[4:0] | 00001,RW | **PHY Address Bit 4:0**<br>The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY. |

<table>
<tr><td>3:0</td><td>ANMB[3:0]</td><td>0,RO</td><td>Auto-Negotiation Monitor Bits<br>These bits are for debug only. The Auto-Negotiation status will be written to these bits.<br><br>
<table>
<tr><th>b3</th><th>b2</th><th>b1</th><th>b0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>In IDLE state</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Ability match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Acknowledge match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Acknowledge match fail</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Consistency match</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Consistency match fail</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Parallel detects signal_link_ready</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Parallel detects signal_link_ready fail</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Auto-Negotiation completed successfully</td></tr>
</table>
</td></tr>
</table>

### 8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 14 | LP_EN | 1,RW | **Link Pulse Enable**<br>1 = Transmission of link pulses enabled<br>0 = Link pulses disabled, good link condition forced<br><br>This bit is valid only in 10Mbps operation. |
| 13 | HBE | 1,RW | **Heartbeat Enable**<br>1 = Heartbeat function enabled<br>0 = Heartbeat function disabled<br><br>When the PHY is configured for Full-Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full-Duplex mode). |
| 12 | SQUELCH | 1,RW | **Squelch Enable**<br>1 = Normal squelch<br>0 = Low squelch |
| 11 | JABEN | 1,RW | **Jabber Enable**<br>Enables or disables the Jabber function when the PHY is in 10BASE-T Full-Duplex or 10BASE-T transceiver loopback mode.<br><br>1 = Jabber function enabled<br>0 = Jabber function disabled |
| 10:1 | RESERVED | 0,RO | **Reserved**<br>Write as 0, ignore on read. |
| 0 | POLR | 0,RO | **Polarity Reversed**<br>When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically. |

### 8.11 Power Down Control Register (PWDOR) – 13H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:9 | RESERVED | 0,RO | Reserved<br>Read as 0, ignore on write |
| 8 | PD10DRV | 0,RW | Vendor power down control test |
| 7 | PD100DL | 0,RW | Vendor power down control test |
| 6 | PDCHIP | 0,RW | Vendor power down control test |
| 5 | PDCOM | 0,RW | Vendor power down control test |
| 4 | PDAEQ | 0,RW | Vendor power down control test |
| 3 | PDDRV | 0,RW | Vendor power down control test |
| 2 | PDEDI | 0,RW | Vendor power down control test |
| 1 | PDEDO | 0,RW | Vendor power down control test |
| 0 | PD10 | 0,RW | Vendor power down control test |

Note: When selected, the power down value is control by register 14H bit0.

### 8.12 Specified Config Register – 14H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15 | TSTSE1 | 0,RW | Vendor test select control |
| 14 | TSTSE2 | 0,RW | Vendor test select control |
| 13 | FORCE_TXSD | 0,RW | **Force Signal Detect**<br>1 = Force SD signal OK in 100M<br>0 = Normal SD signal |
| 12 | FORCE_FEF | 0,RW | Vendor test select control |
| 11 | PREAMBLEX | 1,RW | **Preamble Saving Control**<br>1 = Transmit preamble bit count is normal in 10BASE-T mode<br>0 = When bit 10 is set, the 10BASE-T transmit preamble count is reduced. When bit 11 of register 1DH is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced |
| 10 | TX10M_PWR | 1,RW | **10BASE-T Mode Transmit Power Saving Control**<br>1 = Enable transmit power saving in 10BASE-T mode<br>0 = Disable transmit power saving in 10BASE-T mode |
| 9 | NWAY_PWR | 0,RW | **Auto-Negotiation Power Saving Control**<br>1 = Disable power saving during Auto-Negotiation period<br>0 = Enable power saving during Auto-Negotiation period |
| 8 | RESERVED | 0,RW | Reserved |
| 7 | MDIX_CNTL | MDI/MDIX,RO | **The Polarity of MDI/MDIX Value**<br>1 = MDIX mode<br>0 = MDI mode |
| 6 | AutoNeg_LPBK | 0,RW | **Auto-Negotiation Loopback**<br>1 = Test internal digital Auto-Negotiation Loopback<br>0 = Normal |
| 5 | MDIX_FIX Value | 0,RW | **MDIX_CNTL Force Value**<br>When Mdix_down = 1, MDIX_CNTL value depend on the register value. |

| | | | |
|---|---|---|---|
| 4 | MDIX_Down | 0,RW | **HP Auto-MDIX Down**<br>Manual force MDI/MDIX.<br>1 = Disable HP Auto-MDIX , MDIX_CNTL value depend on Bit5<br>0 = Enable HP Auto-MDIX |
| 3 | MonSel1 | 0,RW | Vendor monitor select |
| 2 | MonSel0 | 0,RW | Vendor monitor select |
| 1 | RESERVED | 0,RW | **Reserved**<br>Force to 0, in application. |
| 0 | PD_Value | 0,RW | **Power Down Control Value**<br>Decision the value of each field register 19H.<br>1 = Power down<br>0 = Normal |

### 8.13 DSP Control Register (DSPCR) – 1BH

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:12 | FIL_CTL | 0,RW | FILTER Write Control<br>The FILTER can be written only when these three bits equal to 1111. |
| 11:10 | RESERVED | 0,RW | Reserved |
| 9:8 | FILTER | 0.RW | Equalizer Filter Control parameter |
| 7:0 | RESERVED | 0,RW | Reserved |

### 8.14 Regulator Control Register (RGCR) – 1CH

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:4 | RESERVED | 0,RW | Reserved |
| 3:2 | REG_CTL | 0,RW | **1.2V Regulator Control**<br>00: 1.2V (default)<br>01: 1.15V<br>10: 1.1V<br>11: 1.05V |
| 1:0 | RESERVED | 0,RW | Reserved |

### 8.15 Power Saving Control Register (PSCR) – 1DH

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:13 | RESERVED | 0,RO | Reserved |
| 12 | LPI | 0,RO | **Low Power Idle Status**<br>1 = In Low power idle mode<br>0 = In normal mode |
| 11 | PREAMBLEX | 0,RW | **Preamble Saving Control**<br>When both bit 10and 11 of PHY register 14H are set, the 10BASE-T transmit preamble count is reduced.<br>1 = 12-bit preamble is reduced<br>0 = 22-bit preamble is reduced |
| 10 | AMPLITUDE | 0,RW | **Transmit Amplitude Control Disabled**<br>1 = Disable Transmit amplitude reduce function<br>0 = When cable is unconnected with link partner, the TX amplitude is reduced for power saving |
| 9 | TX_PWR | 0,RW | **Transmit Power Saving Control Disabled**<br>1 = Disable transmit driving power saving function<br>0 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving |
| 8:0 | RESERVED | 0,RO | Reserved |

### 8.16 Page Number Register (PAGE) – 1FH

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15-0 | PAGE | 0,RW | Page Number |

**PHY Page 1**

### 8.17 Transmit Output Trim Control Register (TOTCR) – Page 1. 17H

| Bit | Bit Name | Default | Description |
|---|---|---|---|
| 15:13 | RESERVED | 0,RO | Reserved |
| 12 | F_TRIM | 0,RW | Trim Value Force Enable<br>When this bit is "1'", the internal 50Ohm trim value is forced by bit[5:0] ; otherwise they are latched from internal 50Ohm calibration result.<br>This bit can load from EFuse address 18 (TRIM_RES) bit 6, if TRIM_RES[7:6]=01 |
| 11:6 | RESERVED | 0,RO | Reserved |
| 5:0 | TRIM | 0,RW | Trim Value<br>These bits are to define internal 50Ohm trim value for transmit output amplitude.<br>These bits can load from EFuse address 18 (TRIM_RES) bits[5:0], if TRIM_RES[7:6]=01 |

# 9 DC Characteristics

## 9.1 Absolute Maximum Ratings (25°C) (DM9051AI support -40°C~+85°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| DVDD | Supply Voltage | -0.3 | 3.6 | V | Power pin |
| VIN | DC Input Voltage (VIN) | -0.5 | 5.5 | V | IO pin |
| VOUT | DC Output Voltage(VOUT) | -0.3 | 3.6 | V | IO pin |
| Tstg | Storage Temperature Range | -65 | +150 | ℃ | |
| TA | Ambient Temperature | 0 | +70 | ℃ | DM9051A |
| TA | Ambient Temperature | -40 | +85 | ℃ | DM9051AI |
| LT | Lead Temperature (TL,soldering,10 sec.). | — | +260 | ℃ | |

### 9.1.1 Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| DVDD | Supply Voltage | 3.135 | 3.300 | 3.465 | V | |
| PD (Power Dissipation) | 100BASE-TX | --- | 60 | --- | mA | 3.3V |
| | 100BASE-TX (802.3az) | --- | TBD | --- | mA | 3.3V |
| | 10BASE-T TX | --- | 31 | --- | mA | 3.3V |
| | Auto-Negotiation | --- | 30 | --- | mA | 3.3V |
| | Power Down Mode | --- | 3.5 | --- | mA | 3.3V |

## 9.2 DC Electrical Characteristics

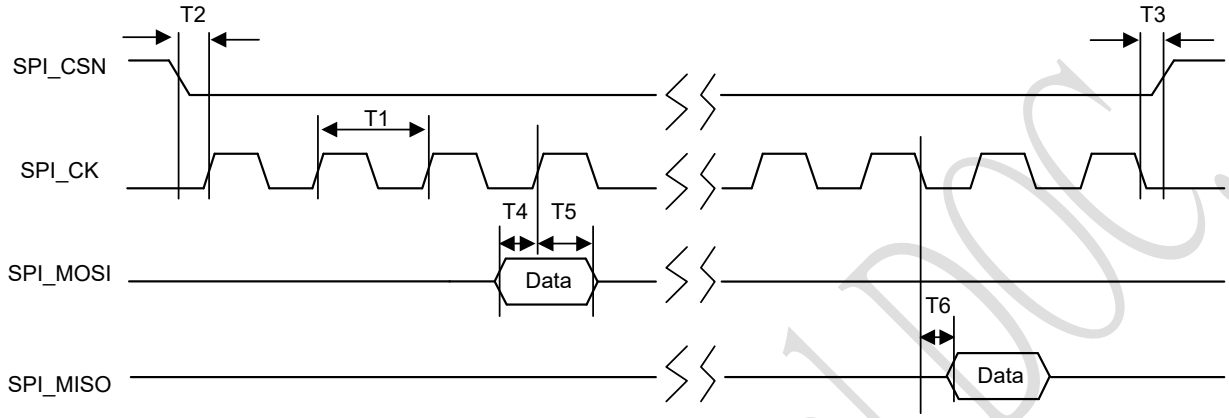
### 9.2.1 DC Electrical Characteristics (VDDIO = 3.3V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Inputs** | | | | | | |
| VIL | Input Low Voltage | - | - | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | - | - | V | |
| IIL | Input Low Leakage Current | -1 | - | - | uA | Input Voltage = 0.0V |
| IIH | Input High Leakage Current | - | - | 1 | uA | Input Voltage = 3.3V |
| **Outputs** | | | | | | |
| VOL | Output Low Voltage | - | - | 0.4 | V | IOL = 4mA |
| VOH | Output High Voltage | 2.4 | - | - | V | IOH = -4mA |

## 10. AC Electrical Characteristics & Timing Waveforms

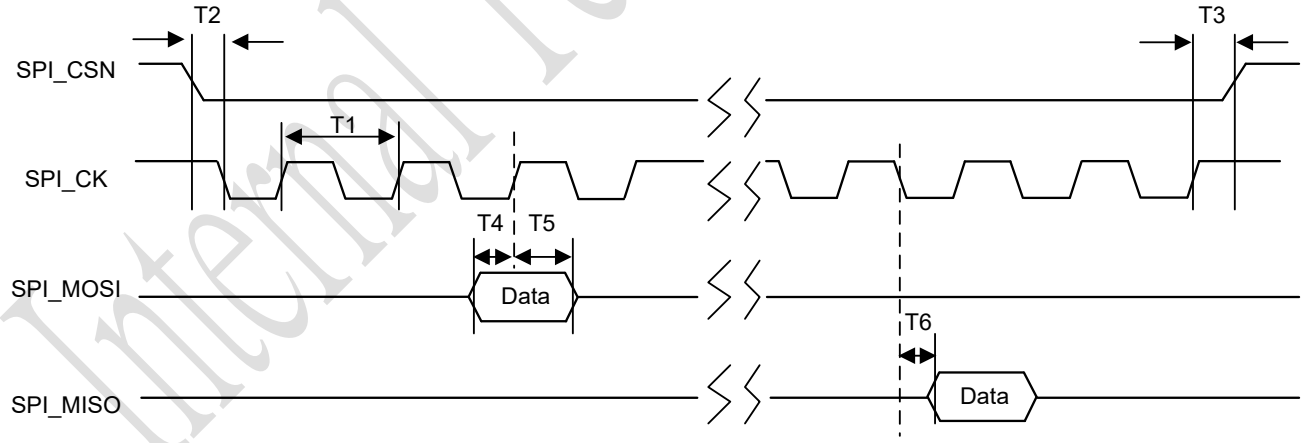
### 10.1 SPI Timing

**M0 Mode**




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| T1 | SPI_CK Frequency | - | 40 | 50 | MHz |
| T2 | SPI_CSN go low to SPI_CK go high | 10 | - | - | ns |
| T3 | SPI_CK go low to SPI_CSN go high | 10 | - | - | ns |
| T4 | SPI_MOSI setup time from SPI_CK go high | 3 | - | - | ns |
| T5 | SPI_MOSI hold time after SPI_CK go high | 3 | - | - | ns |
| T6 | SPI_MISO Output Delay after SPI_CK go low | 5 | 6 | 7 | ns |

**M3 Mode**




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| T1 | SPI_CK Frequency | - | 40 | 50 | MHz |
| T2 | SPI_CSN go low to SPI_CK go low | 0 | - | - | ns |
| T3 | SPI_CK go high to SPI_CSN go high | 0 | - | - | ns |
| T4 | SPI_MOSI setup time from SPI_CK go high | 3 | - | - | ns |
| T5 | SPI_MOSI hold time after SPI_CK go high | 3 | - | - | ns |
| T6 | SPI_MISO output delay after SPI_CK go low | 5 | 6 | 7 | ns |

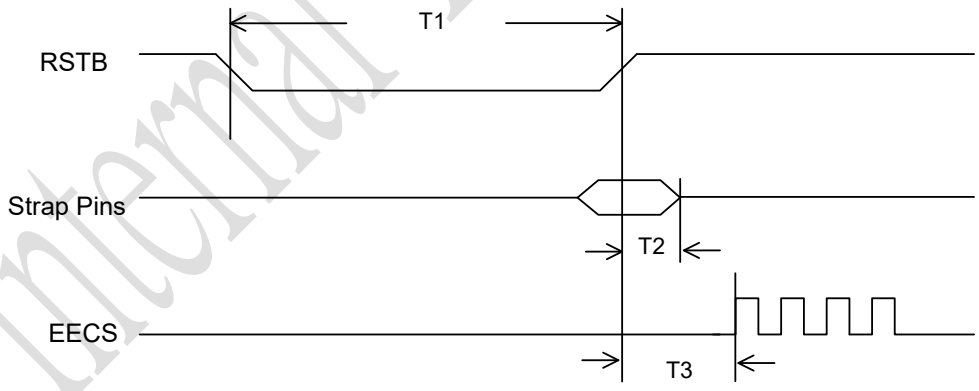
### 10.2 TP Interface

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| tTR/F | 100TX+/- Differential Rise/Fall Time | 3.0 | - | 5.0 | ns | - |
| tTM | 100TX+/- Differential Rise/Fall Time Mismatch | 0 | - | 0.5 | ns | - |
| tTDC | 100TX+/- Differential Output Duty Cycle Distortion | 0 | - | 0.5 | ns | - |
| Tt/T | 100TX+/- Differential Output Peak-to-Peak Jitter | 0 | - | 1.4 | ns | - |
| XOST | 100TX+/- Differential Voltage Overshoot | 0 | - | 5 | % | - |
| **Receiver** | | | | | | |
| VICM | RX+/RX- Common Mode Input Voltage | - | ? | - | V | 100 Ω Termination Across |
| **Transmitter** | | | | | | |
| VTD100 | 100TX+/- Differential Output Voltage | 1.9 | 2.0 | 2.1 | V | Peak to Peak |
| VTD10 | 10TX+/- Differential Output Voltage | 4.4 | 5 | 5.6 | V | Peak to Peak |

### 10.3 Oscillator/Crystal Timing

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| TCKC | OSC Clock Cycle | 39.9988 | 40 | 40.0012 | ns | 30ppm |
| TPWH | OSC Pulse Width High | 16 | 20 | 24 | ns | - |
| TPWL | OSC Pulse Width Low | 16 | 20 | 24 | ns | - |

### 10.4 Power On Reset Timing




| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| T1 | RSTB Low Period | 1 | - | - | ms | - |
| T2 | Strap Pins hold time with RSTB | 40 | - | | ns | - |
| T3 | RSTB high to EECS high | - | 9.5 | - | us | - |

### 10.5 LED (traffic ON/OFF timing) any LED as Traffic

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| T1 | LED Traffic ON Time | - | 16 | - | ms |
| T2 | LED Traffic OFF Time | 64 | - | - | ms |