Geoffrey Tomlinson, Individual Work Log

Milestone 1:

1/12/2020
Met with whole project group [3h 30m]

- We decided to make an accumulator processor due to its freedom in design and the previous experience of some of our members.
- We created two instruction types(A and I). We had a third but were able to fit its functionality into A. We choose to use a 1-bit Opcode to show which instruction type an instruction is, in addition to our 6-bit funct field.
- We also created our base set of instructions. Notably we decided to create Branch if positive and branch if negative instructions instead of implementing a less than functioin.
- Towards the end of the meeting I began drafted the relprime function.

1/13/2020
Met with whole group[30m]

- I finished the draft of the relprime and GCD functions.
- We decided what everyone should have done by the next meeting. I will have all of the semantics for the instructions done, and will type up the relprime and GCD functions in our Microsoft teams.[30m]

1/14/2020
Met with whole group[30m]

- I completed my tasks.
- We began work on translating our assembly into machine code.
- For the next meeting I will have filled out our design document with all of the information we need on it. [1h]

1/15/2020
Met with whole group []

- I had most of the content for the design document done.
- We finished editing formatting the document and turned it in.
- For the next milestone myself and Brendan will be focusing on the hardware aspect. For our next meeting we are expected to be familiar with the software.[1h]

Milestone 2:

1/16/2020
Met with whole group during class time [1 hr]

- We wrote all of our RTL for our old instructions and combined them into a multicycle RTL schematic
- Decided that we would wait for our meeting with Robert to assign any more work.

1/17/2020
Met with Robert [10m]

- Robert had us change the style of our accumulator to have no user programmable registers.
- For our next meeting everyone is supposed to bring idea for how to accomplish the task given to us by Robert.

1/19/2020
Met with whole group [3hr]

- I was only able to be there from 4pm to 7pm due to a previous commitment.
- We designed instructions for our new processor
    - We changed our instruction format to only have 1 type of instruction with an 8-bit opcode and an 8-bit immediate field
- We got most of the way done with our new RelPrime function before I had to leave.
- I did not have anything to do for next meeting, other than update myself on changes made after I left the meeting.

1/20/2020
Group met without me

- I had yet another commitment (vet appointment). Very busy week for me
- My task was to format and edit the design document for the next meeting

1/21/2020
Met with whole group [30m]

- We wrote up the RTL for all of our instructions and combined it into a multicycle RTL schematic.
- For our next meeting we are supposed to bring a list of components that we think we our processor will need.

1/22/2020
Met with whole group [1hr]

- Finalized our RTL and our design document
- We decided on to stick with multicycle for our instructions.
- We decided to wait for our next meeting with Robert to determine what we will be doing for Milestone 3.

Milestone 3

1/24/2020
Met with whole group [10m]

- We decided to meet on Sunday to create our datapath and begin work on the rest of the milestone.
- There was no work assigned to be done before Sundays meeting

1/26/2020
Met with whole group [2hr]

- We drew out the first draft of our datapath which was based off of our RTL diagram.
- We created our initial list of control bits
- We divided up the Labs. Chet and I are working on Lab 8, the interrupt lab.
    - We decided to meet on Monday after our team meeting to begin work on the lab
- Assigned work for the next meeting was minimal, just to come up with some testing methods.

1/27/2020
Met with Whole group [30m]

- Checked up on everyone's progress with the labs
- Discussed testing methods and made small changes to our datapath for aesthetics
- After the meeting Chet and I worked on the Lab [1hr]
- For next meeting my job was to create a list and description of all of our control bits

1/28/2020
Met with Whole Group [30m]

- Checked up on everyone's lab progress
- Chet and I finished our lab and did the demo for Robert
- My work for the next meeting was to add the RTL tests that were requested by Robert

1/29/2020
Met with whole group [3hr]

- We wrote out the testing and implementation methods
- Finalized our datapath
    - Changed our regwrite control bit into 2 separate bits
    - Created the BLU (branch logic unit)
    - Increased the size of accsrc
    - Changed data inputs to acc and sp
- I wrote 2x1 and 4x2 muxes for our implementation

Milestone 4

2/2/2020
Met with whole group [2hr]

- We created the first draft of our FSM diagram for our control unit.
- Revised our implementation plan after receiving advise from Robert
- I was tasked with working on the sign extender for next meeting

2/3/2020
Met with whole group [1hr]

- During this period we just worked on our tasks individually
- I finished the Sign Extender and began work on BLU

2/5/2020
Met with whole group

- I finished the BLU and made the 1bit left shifter
- We edited our FSM
    - We removed a bubble from our branch instruction and used another state in its place. We were able to do this because our hardware will wire the difference itself.

Milestone 5

2/9/2020
Met with whole group [1.5hr]

- I fixed the Extender code to use concatenation, and the tests to display a pass/fail
- I fixed the BLU tests to display a pass/fail
- Aurora and I were assigned with working on the Input and Output aspect

2/10/2020
Met with whole group [1hr]

- During this period we just kept working on what we were assigned. Similar to last week.
- We began accumulating useful symbols from other labs and planning out how we wanted the peripherals to work.

2/11/2020
Met with whole group [1hr]

- Just keep working
- We started putting the symbols together and finalized out plan for the input.
    - Use the switches to load a 4bit immediate into the acc and display the value of the acc on the LCD.

2/12/2020
Met with whole group [3hr]

- We recorded our plan for I/O in the document and finished the design for the input and output peripherals.
- We combined them to create a test module since the full processor is not ready yet. But after many trials we could not get the FPGA board to function properly
    - We plan to discuss this with Robert on Friday during our meeting

Milestone 6:

2/16/2020
Met with whole group [2hr]

- Aurora and I kept working on the IO. We created what we thought would be a working model and waited until Monday to test.
- Began work on updating the design document and started the final report

2/17/2020
Met with group [1hr]

- We tested the IO model and it did not work.
    - We made some corrections to it and our base model now worked but we still had to add the processor to the module.
    - That took pretty much the whole time
- For next meeting I would work on adding the processor and updating the design document more.

2/18/2020
Met with group [1hr]

- Worked in class, primarily on the design document and final report.
- Touched up the design for the IO but did not add the processor as we were still finishing up testing on it.

2/19/2020
Met with group [4hr]

- Finally added the processor to the IO file and everything proceeded to break.
    - When adding the processor into the schematic and loading it to the board none of the intended LEDs lit up and the rightmost switch now controls an LED on the Ethernet port.
    - We have no idea what caused this but we cannot seem to fix it.
- Since Robert is in a different lab during this period our plan is to talk to him on Thursday and Friday to see if we can get this bug sorted out.
- I worked a little more on the final report as well.