Chet Zhang, WORK LOG

MILESTONE 2 WORK:

Sunday, Jan 19, 2020

Met with team [3.5 hrs]

- Since we had to reconsider everything, we basically redid all of the design document. We came up with an idea of how to implement an assembly without having registers as any operands. Then I wrote the assembly codes for relPrime and GCD with Geoffrey. [1 hr]

Monday, Jan 20, 2020

Met with team [30 mins]

- Having the version of old design document as the template, we quickly replaced places that is necessary. I had the assembly codes typed up and checked it to make sure it can function correctly. [1 hr]

Tuesday, Jan 21, 2020

Met with team [30 mins]

- According to the new design, we came up with the new RTL. Excel table was created. Also, we completed what should be done in the new milestone 1. [30 mins]

Wednesday, Jan 22, 2020

Met with team [30 mins]

- I met with the team and finished RTL and have it checked and visually formatted, so it can fit perfectly into the design document. [30 mins]

MILESTONE 3 WORK:

Sunday, Jan 26, 2020

- We wrote a data-path for our accumulator according to the RTL we have. Also to make sure our RTL can work properly we double checked RTL. [1.5 hrs]

Monday, Jan 27, 2020

- Fixed and added detailed description of how to manage return address, arguments and return values in programming convention part. [1 hr]

Tuesday, Jan 28, 2020

Met with team [30 mins]

- I drew the data-path and added to design document. [1 hr]

Wednesday, Jan 29, 2020

Met with team [30 mins]

- We fixed the data-path and some of the calling convention. Not for this milestone though, I finished implementing register that takes in writeReg, data, address and outputs data in Xilinx with some tests. Detailed tests will be uploaded in the design document in next milestone.[3 hrs]

MILESTONE 4 WORK:

Sunday, Feb 2, 2020

- We completed State diagram and made detailed integration plan. Brendan was assigned to do the first integration, I and Aurora was assigned to do the second integration plan. [1.5 hrs]

Tuesday, Feb 4, 2020

- I updated State diagram and the description of the first part of the integration plan, which contains Memory, Control, several registers and multiplexers.

Wednesday, Feb 5, 2020

- Aurora and I completed ALU and gave exhaustive tests to pretty much every instruction. Small changes were made to the datapath, then the design document was updated correspondingly. [2 hrs]

MILESTONE 5 WORK:

Saturday, Feb 16, 2020

- I finished 2nd part of the integration plan with aurora based on her ALU16. We ran several tests over it and it worked fine. [3 hr]

Monday, Feb 10, 2020

- Brendan and I started connecting the first and second parts of the integration plan. All outputs and inputs were connected but some tests pointed out that something has gone wrong within our schematic file. [2 hrs]

Wednesday, Feb 12, 2020

- We performed more tests on our processor and fixed schematic files, previous Verilog files, and testbenches accordingly. For testing purposes, we made several extra outputs pointing out. Now every type of instruction was tested on our architecture except branches and jumps. We are going to test them this weekend. All written test file names and their locations are listed in the table that I added at the end of the design document. [4 hrs]

MILESTONE 6 WORK:

Sunday, Feb 16, 2020

- I tested jumps and branches with Brendan. After we knew our implementation could run every instruction we ran a sum tests which also passed. [2 hr]

Monday, Feb 17, 2020

- Work time. Dealt with design document and more tests were applied. [1 hrs]

Wednesday, Feb 19, 2020

- This is the first time we tried to run relprime. After debugging relprime worked but it took 1 ms to get result of (13B0)hex. We don't know if that is long or not. Further possible optimizations might be done, but getting our implementation programmed on FPGA board is our first priority now. [4 hrs]