Aurora Ouyang, WORK LOG

MILESTONE 1 WORK:

Sunday, January 12, 2020

Met with team [3.5 hours]

We decided to build an accumulator based processor. Based on the 16-bit requirement, we created instructions and two instruction types (A-type and I-type). Besides these, we also discussed how the Euclid's algorithm can be translated into assembly and machine code, discussed what the funct code would be like, and camp up some thoughts with jumping to ACC or register 15.

Monday, January 13, 2020

Met with team [0.5 hour]

We discussed how we should implement the Euclid's algorithm based on our own assembly code and decided how the jump would work.

We assigned work for milestone 1. My tasks are:

1. Organize the design document with the data we have
2. Work on the missing parts except for the machine code part, which include:
    a. Project description
    b. Register description
    c. Special purpose register

Tuesday, January 14, 2020

Met with team [0.5 hour]

We discussed how the opcode and funct work.

Wednesday, January 15, 2020

Met with team [0.5 hour]

We finished formatting the design document and turned it in.

We assigned work for milestone 2. My task is:

1. Get familiar to our design and the software
2. Working on the RTL

MILESTONE 2 WORK:

Thursday, January 16, 2020

Met with team [1 hour]

We discussed how the RTL looks like together.

Friday, January 17, 2020

Met with Dr. Robert [0.2 hour]

We discussed our design. Dr. Robert gave us some advice for our design like remove the register bits and make the memory less.

Sunday, January 19, 2020

Met with team [3.5 hour]

We discussed how the instruction type and the instructions of the new version looks like. We created one instruction type named A-type, and assigned work to each team member.

We assigned work for this new version. My tasks are:

1. Organize the design document with the data we have
2. Work on the list of instructions, finish the description and the sematic

Monday, January 20, 2020

Met with team [0.5 hour]

We decided the registers, pseudo-instructions. We discussed our rel-prime and gcd codes.

Wednesday, January 22, 2020

Met with team [1 hour]

We kept working on the RTL and the hardware component.

MILESTONE 3 WORK:

Friday, January 24, 2020

Met with team [1 hour]

We kept working on the RTL and the hardware component.

Sunday, January 26, 2020

Met with team [3 hour]

We discussed the datapath and divided our work.

We assigned work for milestone 3, my tasks are:

1. Lab 6
2. Working on our own ALU

Monday, January 27, 2020

Met with team [0.5 hour]

We specified how our datapath looks like. I finished the 1-bit ALU.

Wednesday, January 28, 2020

Met with team [4 hour]

We finished our milestone 3 and talked about the lab process. I met errors in my 4-bit ALU and tried to redo it.

MILESTONE 4 WORK:

Friday, January 30, 2020

Met with instructor [0.5 hour]

We discussed about our milestone 3.

Sunday, February 1, 2020

Met with team [2 hour]

We assigned tasks for each team member, my tasks are:

1. Finish the ALU Verilog for our team.
2. Help with teammate about the Finite State Diagram.
3. Work on partial of the integration tests with Chet.

Wednesday, February 5, 2020

Met with team [1.5 hour]

We finished our milestone 4.

MILESTONE 5 WORK:

Thursday, February 6, 2020

Met with instructor [0.5 hour]

We discussed about our milestone 4 and listed something to do in future milestones.

Sunday, February 9, 2020

Met with team [2 hour]

We assigned tasks for each team member, my tasks are:

1. Work on the input and output thing with Geoffrey.

Monday, February 10, 2020

Met with team [1 hour]

We keep doing what we are assigned for this week.

Tuesday, February 11, 2020

Met with team [1 hour]

We keep doing what we are assigned for this week.

Wednesday, February 12, 2020

Met with team [4 hour]

We organized our milestone 3 and what we have been done. I and Jeff was doing the I&O part, but we met an error that nothing worked when we plugin the board.

MILESTONE 6 WORK:

Friday, February 14, 2020

Met with instructor [0.5 hour]

We discussed about our milestone 5 and listed something to do in future milestones.

Sunday, February 16, 2020

Met with team [2 hour]

We assigned tasks for each team member, my tasks are:

1. Work on the I/O with Jeff
2. Work on the final report

Tuesday, February 18, 2020

Met with team [0.2 hour]

We keep doing what we are assigned for this week.

Wednesday, February 19, 2020

Met with team [4 hour]

We organized our milestone 6 work and decided how we are going to do for the final presentation. We debugged for the integration3 and tested it on the board. It works well for the test but met error when we connected to the board.