POLITECNICO DI TORINO

Computer architecture

exam 2022.07.05

	TOMMASO CERRUTI 282754
Iniziato	martedì, 5 luglio 2022, 14:29
Terminato	martedì, 5 luglio 2022, 15:17
Tempo impiegato	48 min.
Valutazione	Non ancora valutato

Domanda 1

Risposta non data

Non valutata

In case you do not want your solution to be corrected, please write it explicitly here. Thx

In case you did experience any technical problems please let us know and how you di tackle them by writing here a few lines. Thank you.

Also, if and only if you have not been able to upload pictures and/or to use the space for the open questions 7-9, please use this space to provide your answers.

ONLY FOR STUDENTS HAVING THE EXAM IN REMOTE MODE: PLEASE STRICTLY FOLLOW THE GUIDANCE PROVIDED IN THE NEXT "QUESTION BOX". IF YOU DO NOT, YOUR EXAM WILL BE VOIDED.

Students attending the exam in person DO NOT have to comply with the instructions in the next "question box".

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You'll find:

- 4 closed questions, 3 of them with single choice and one with multiple choices. For all calls, the single choice questions the points are as follows: correct = +2, wrong = -1, not given = 0; for the multiple choice question, there will be 2 positive points, shared among all correct answers and from 3 to 3.2 negative points to be equally shared among all negative answers
- 4 open questions (up to 4 points each)
- one "comments section" (i.e., this one) to be used as a "spare/communication space";

for questions 7, 8 and 9 (the first 3 following the closed question, i.e. the first 3 open), you have to:

1. write your textual response by using the keyboard; DO NOT write your verbal response to the paper which is used for the drawings.
2. use a piece of paper for the drawings that you wish/need to attach to the text.
3. the drawings should be uploaded by taking a picture of your paper by using your webcam.

To take the picture please click on the small camera icon which is found on the right of the tools menu right above the answer window.

4. please take a good picture as what I cannot read will not be evaluated; this includes being clear in preparing the drawing and not to hiding it with your fingers when taking the picture.
5. you can delete a picture by simply pressing "canc"/"del" key(s). In case of multiple pictures of the same drawing (DON'T TAKE MULTIPLE PICTURES OF THE SAME DRAWING!) only the most recent will be considered.
6. In case you have not been able to take a picture in the boxes of questions 7-9, please upload here your picture(s)

Domanda 2

Risposta non data

Non valutata

IF ATTENDING IN REMOTE MODE ONLY (STUDENTS ATTENDING IN PERSON ARE REQUESTED TO SKIP THIS "QUESTION")

- **YOU HAVE TO TAKE (ANOTHER) PICTURE OF YOUR POLITO ID AND UPLOAD IT HERE.**
- **THERE WILL BE NO ROLL CALL AND THE EXAM WILL BE SUPERVISED BY PROCTORING SOFTWARE**
- **THERE WILL BE NO INTERACTION WITH THE PROFESSORS DURING THE EXAM**

Domanda 3

Risposta corretta

Punteggio ottenuto 2,00 su 2,00

Even parity bit...

- (a) None of the other answers
- (b) Can detect only an even number of errors
- (c) Can detect only an odd number of errors ✓
- (d) Can help to prevent multiple soft errors, no matter how many they are

Risposta corretta.

La risposta corretta è: Can detect only an odd number of errors

Domanda 4

Risposta errata

Punteggio ottenuto -0,50 su 2,00

We have a 4**-way-set-associative** cache memory with 65536 = 2^{16} lines (i.e. = entries) globally (i.e., *globally the 65636 lines are split across the four sets*). Each line is hosting 8 data. How many bits are stored as TAG if the address bus is on 32 bits?

- (a) None of the other answers ✗
- (b) 15
- (c) 29
- (d) 13

Risposta errata.

La risposta corretta è: 15

Domanda 5

Risposta corretta

Punteggio ottenuto 2,00 su 2,00

A D-flip flop…

- (a) Is a combinational device
- (b) Can be used in the design of shift registers ✓
- (c) None of the other answers
- (d) Can be used in the design of multiplexers

Risposta corretta.

La risposta corretta è: Can be used in the design of shift registers

Domanda 6

Risposta corretta

Punteggio ottenuto 2,00 su 2,00

For this multiple choice question, there will be **2 positive points**, equally shared among all correct answers and from 3 up to 3.2 negative points equally shared among all wrong answers

... **Please mark all statements that are correct (at least one is correct).**

Scegli una o più alternative:

- [x] (a) Daisy chaining has fixed priority and all the devices cascaded to a non working device become non reachable ✓
- [ ] (b) The parity bit is a code for detecting and correcting errors
- [ ] (c) Static memories are usually slower than dynamic memories
- [ ] (d) Interrupt controllers cannot be cascaded (i.e., connected in cascade)
- [ ] (e) RAID 1 (mirroring) is a very cheap architectural solution
- [ ] (f) None of the other statements is correct

Risposta corretta.

La risposta corretta è: Daisy chaining has fixed priority and all the devices cascaded to a non working device become non reachable

Domanda 7

Completo

Punteggio max.: 4,00

For this question you have to:

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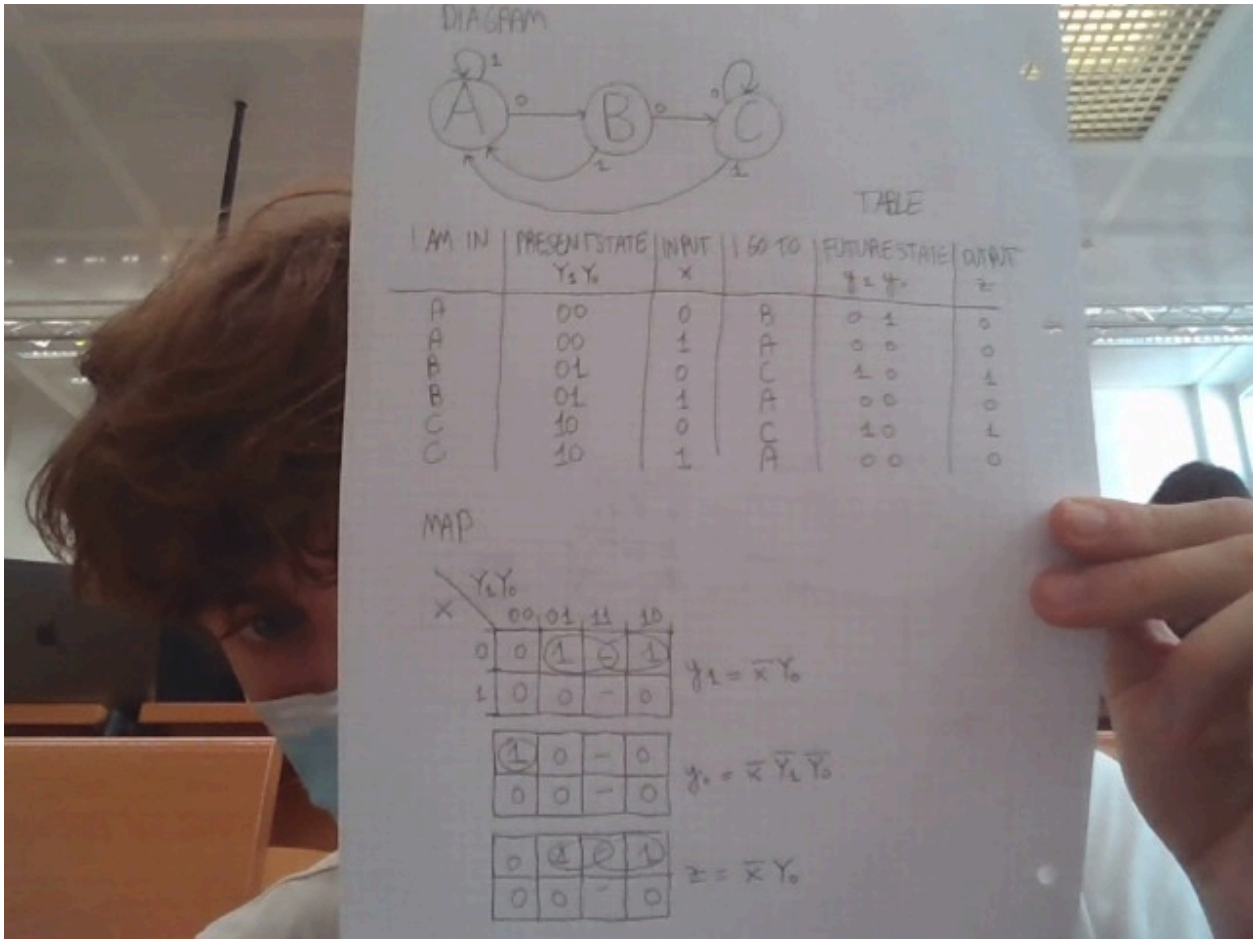
- Please provide the picture of the state machine of a sequencer recognizing the serial input "00", which after a sequence has been recognized, immediately starts a new recognition with possible overlap (if any) with the previous.
- Please also provide the maps and equations of the final circuit implementing the sequencer. The picture of the **final circuit is NOT requested**.
- **Please name the states A=00, B=01, C=10** and so on (if there are other states beyond C).



Domanda 8

Completo

Punteggio max.: 4,00

For this question you have to:

1. write your textual response by using the keyboard; DO NOT write your verbal response to the paper which is used for the drawings.
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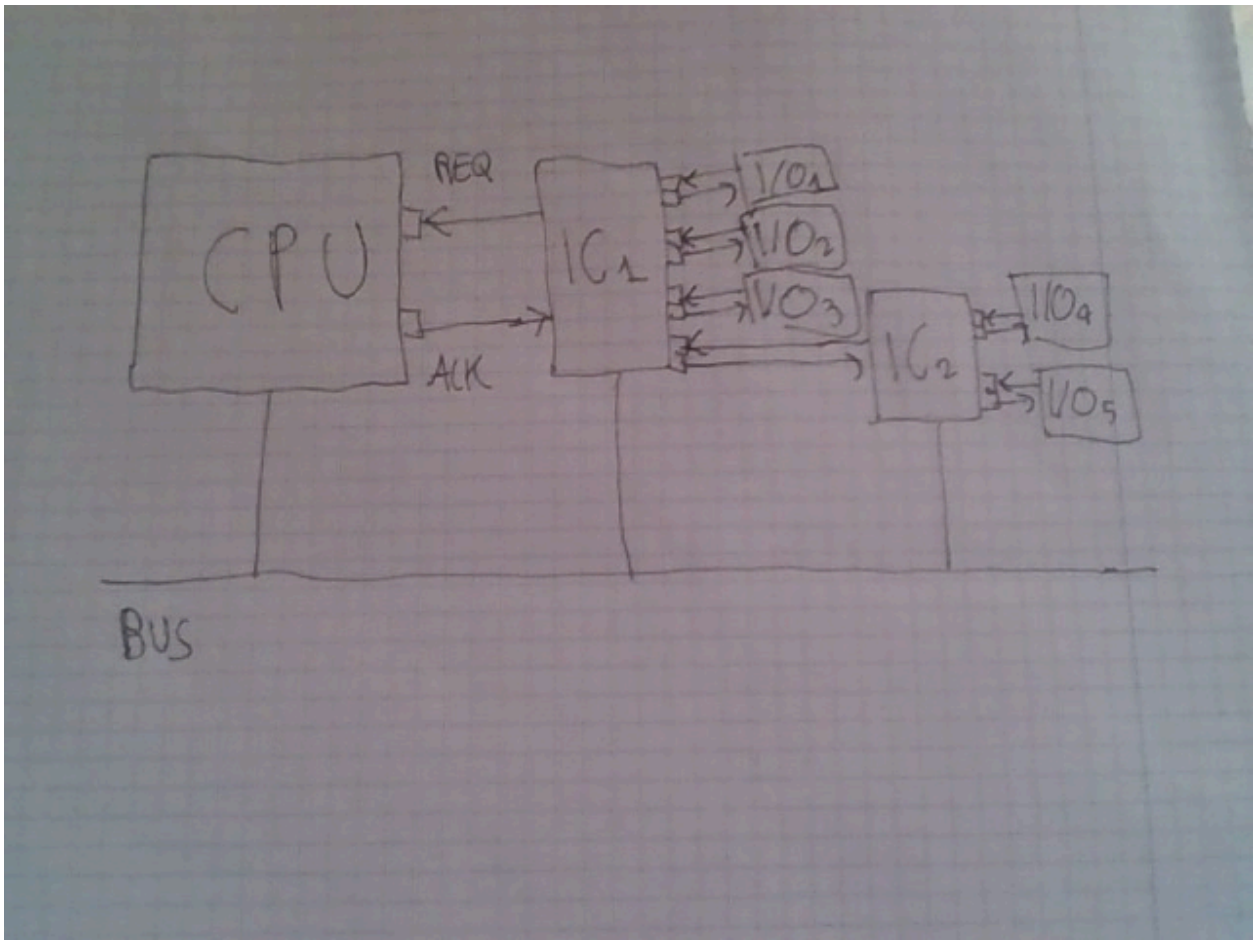
Please provide the picture of the organization (architecture) of an **Interrupt Controller based I/O device management system** where each interrupt controller unit can manage up to 4 devices and the number of I/O devices is 5. Please also briefly describe clearly and schematically what is an interrupt service routine, where it is found and what it does (in general).



The Interrupt Controller is an internal device that manages the communication between the CPU and peripherals, since they cannot communicate on their own as they need permission from the CPU. An interrupt service routine is the routine with which peripherals connected with interrupt controllers are able to communicate with the CPU, and it goes as follows. The peripheral that needs attention sends a request REQ signal to its respective Interrupt Controller (example: in the picture I/O2 sends it to IC1), which sends back the acknowledgment ACK signal back to the peripheral and stops when it is found. Then the interrupt controller also sends a REQ signal to the CPU which answers with an ACK signal that cascades throught the interrupt controllers until the one requesting attention is found. Once found, the peripheral can finally communicate with the CPU via the bus that is connected to its respective controller.

Domanda 9

Completo

Punteggio max.: 4,00

For this question you have to:

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Please provide convincing explanations on what is the **final value stored in AX** (the contents of the other registers is of no interest) after having completed the execution of the following portion of assembly code. Assume that at the beginning **AX stores a** and **BX stores b** and that both a and b are in two's complement and their modules are smaller than 1000.

(Helpful note: do not be tricked and say that AX and BX will remain the same as they were at the beginning of the operation! BX will NOT be overwritten by the "POP" instructions! If this note is not clear to you, please discard it. No further explanation will be provided)

PUSH AX

PUSH BX

ADD AX, BX

ADD BX, AX

POP AX

SHL AX,1

SUB BX, AX

POP AX

PUSH AX; putting a on TOS (top of the stack), without affecting AX, <ax>=a

PUSH BX; putting b on TOS, above a, without affecting BX, <bx>=b

ADD AX, BX; adding the content of BX to AX, and store it there in AX, so <ax>=a+b

ADD BX, AX; adding the content of AX to BX, and store it there in BX, so <bx>=b+(a+b)=a+2b

POP AX; retrieving the element on TOS (in this case b) and store it to AX, so <ax>=b

SHL AX,1; shifting left the digits of AX, since in binary it is like multiplying by 2^1, so <ax>=2b

SUB BX, AX; subtracting the content of AX to BX, and store it there in BX, so <bx>=(a+2b)-(2b)=a

POP AX; retrieving the element on TOS and store it to AX, so <ax>=a

Final value: <ax>=a

Domanda 10

Completo

Punteggio max.: 4,00

Please write down the microinstructions to implement the instruction ADD [R1], R1, adding the content of R1 to the memory cell pointed by R1 and rewriting the result to the same memory cell.

Please add a short but significant explanation to each single microinstruction.

R1out, MARin; storing the address stored in R1 to MAR

READ, R1out, Yin; read from memory and in parallel store the value of R1 to Y

MDRout, ALUadd; add the two numbers in the ALU

Zout, MDRin; store the value of the result to MDR

WRITE; write the result to memory