COMP4300

Lab Exercise One,   Spring 2022

Objective

This lab is aimed at getting you familiar with using the ModelSim simulator. The circuits you will be simulating should be familiar to you from ELEC2200.

Instructions

Write a VHDL program consisting of a single entity whose architecture is a single process that implements a one-bit full adder . That is, a circuit which behaves as specified in the following truth table. You should implement your architecture as a single process, like the AND gate implemented in class.

- ```
  inputs                        |outputs
  ```
- ```
  ---------------------------+---------------
  ```
- `carry_in        a_in        b_in |  result carry_out`
- `0               0           0    |    0      0`
- `0               0           1    |    1      0`
- `0               1           0    |    1      0`
- `0               1           1    |    0      1`
- `1               0           0    |    1      0`
- `1               0           1    |    0      1`
- `1               1           0    |    0      1`
- `1               1           1    |    1      1`

Use exactly the names given above for the signals. All your signals should be of type `bit` (NOT integer). Use a propagation delay of 10ns.

Deliverables

Please turn in the following things for this lab:

  - o   The file with your VHDL code.
  - o   A screen shot of your exhaustive simulation.
  - o   A screen shot of a successful compilation of your code.