ECE 273: Introduction to Digital Logic

Project 2

By

<Tommy Tran, Jacob Connolly, Paul Tran >

Lab Instructor: Dr. Kaufman

September 16, 2021
Fall 2021

Honor Code:

I have neither given nor received unauthorized assistance on this graded report.

X_____Type student name(s) here: Tommy Tran, Jacob Connolly, Paul Tran

Department of Electrical and Computer Engineering
College of Engineering and Computer Science
The University of Michigan-Dearborn

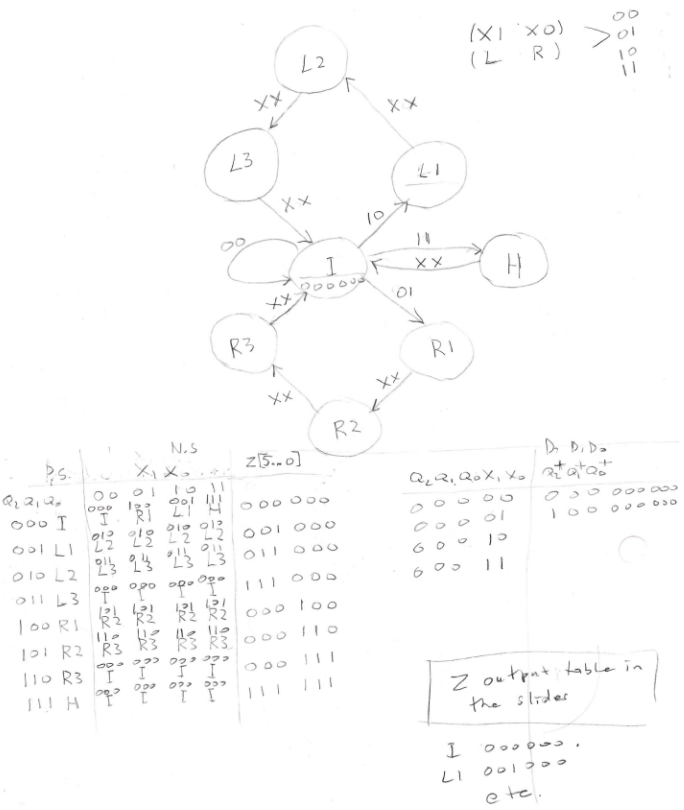
Statement of the Problem

The purpose of this lab is to create a sequential taillight controller. These types of taillight controllers can be found in cars such as the Ford Mustangs. Students will develop a state machine in order to differentiate idle, left, and right signals. They will implement the synchronous state machine into Quartus Lite. It will then b tested using an FPGA board and waveforms.

Description of Solution/Design

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
D[2]-Z[0]	5	9	10, 1...	22, 1...	0, 0, ...	Unmini...	Not mapped

Term	Q[2]	Q[1]	Q[0]	X[0]	X[1]	=>	D[2]	D[1]	D[0]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]
0	0	0	0	0	0		0	0	0	0	0	0	0	0	0
1	0	0	0	0	1		0	0	1	0	0	0	0	0	0
2	0	0	0	1	0		1	0	0	0	0	0	0	0	0
3	0	0	0	1	1		1	1	1	0	0	0	0	0	0
4	0	0	1	0	0		0	1	0	0	0	1	0	0	0
5	0	0	1	0	1		0	1	0	0	0	1	0	0	0
6	0	0	1	1	0		0	1	0	0	0	1	0	0	0
7	0	0	1	1	1		0	1	0	0	0	1	0	0	0
8	0	1	0	0	0		0	1	1	0	1	1	0	0	0
9	0	1	0	0	1		0	1	1	0	1	1	0	0	0
10	0	1	0	1	0		0	1	1	0	1	1	0	0	0
11	0	1	0	1	1		0	1	1	0	1	1	0	0	0
12	0	1	1	0	0		0	0	0	1	1	1	0	0	0
13	0	1	1	0	1		0	0	0	1	1	1	0	0	0
14	0	1	1	1	0		0	0	0	1	1	1	0	0	0
15	0	1	1	1	1		0	0	0	1	1	1	0	0	0
16	1	0	0	0	0		1	0	1	0	0	0	1	0	0
17	1	0	0	0	1		1	0	1	0	0	0	1	0	0
18	1	0	0	1	0		1	0	1	0	0	0	1	0	0
19	1	0	0	1	1		1	0	1	0	0	0	1	0	0
20	1	0	1	0	0		1	1	0	0	0	0	1	1	0
21	1	0	1	0	1		1	1	0	0	0	0	1	1	0
22	1	0	1	1	0		1	1	0	0	0	0	1	1	0
23	1	0	1	1	1		1	1	0	0	0	0	1	1	0
24	1	1	0	0	0		0	0	0	0	0	0	1	1	1
25	1	1	0	0	1		0	0	0	0	0	0	1	1	1
26	1	1	0	1	0		0	0	0	0	0	0	1	1	1
27	1	1	0	1	1		0	0	0	0	0	0	1	1	1
28	1	1	1	0	0		0	0	0	1	1	1	1	1	1
29	1	1	1	0	1		0	0	0	1	1	1	1	1	1
30	1	1	1	1	0		0	0	0	1	1	1	1	1	1
31	1	1	1	1	1		0	0	0	1	1	1	1	1	1



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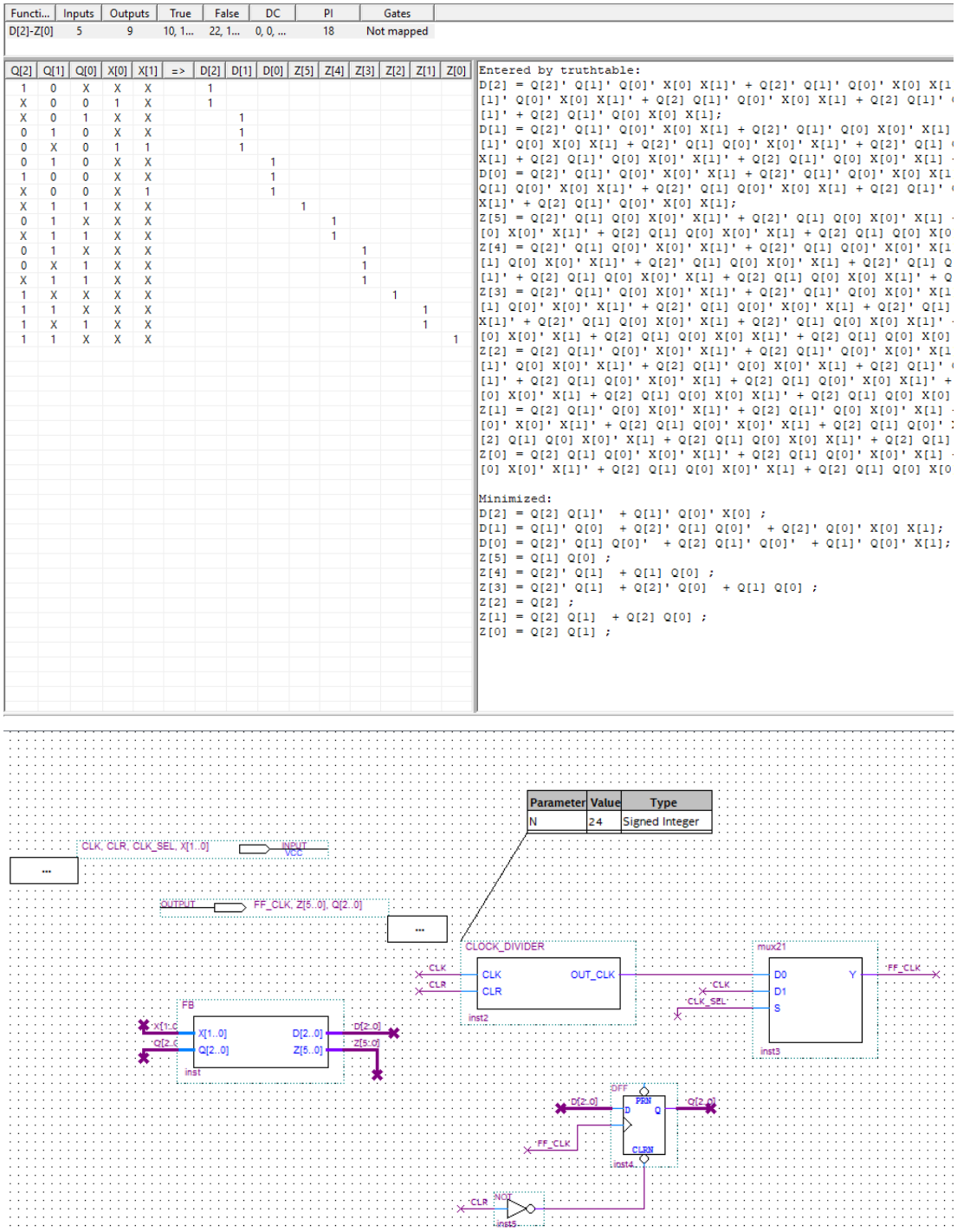

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
D[2]-Z[0]	5	9	10, 1...	22, 1...	0, 0, ...	18	Not mapped

Q[2]	Q[1]	Q[0]	X[0]	X[1]	=>	D[2]	D[1]	D[0]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]
1	0	X	X	X		1								
X	0	0	1	X		1								
X	0	1	X	X			1							
0	1	0	X	X			1							
0	X	0	1	1			1							
0	1	0	X	X				1						
1	0	0	X	X				1						
X	0	0	X	1				1						
X	1	1	X	X					1					
0	1	X	X	X						1				
X	1	1	X	X						1				
0	1	X	X	X							1			
0	X	1	X	X							1			
X	1	1	X	X							1			
1	X	X	X	X								1		
1	1	X	X	X									1	
1	X	1	X	X									1	
1	1	X	X	X										1

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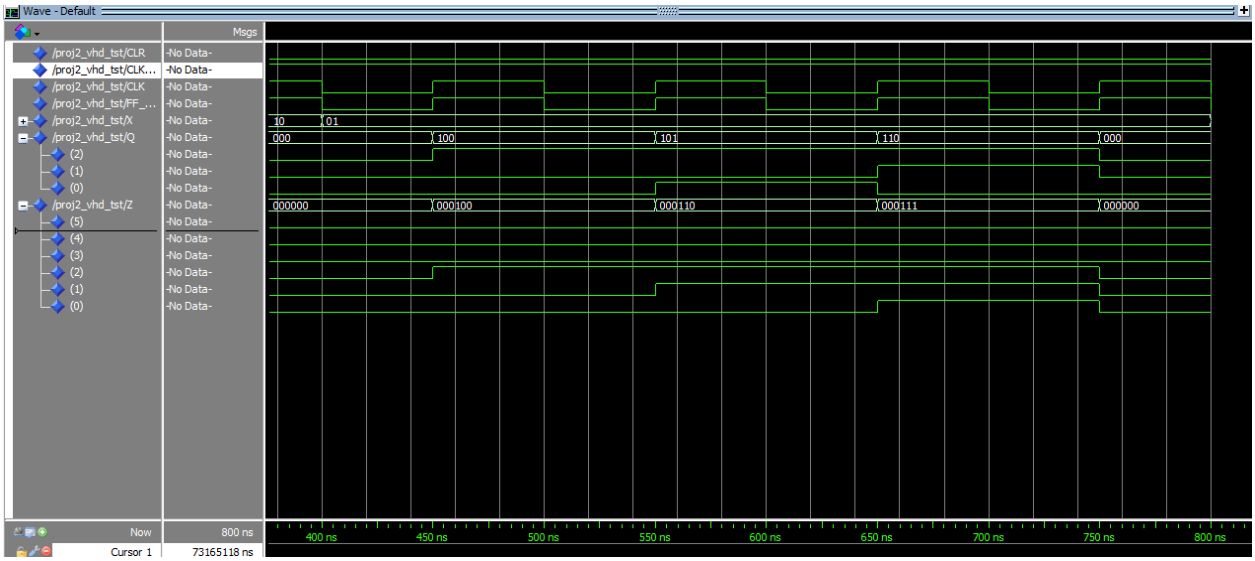
Entered by truthtable:
D[2] = Q[2]' Q[1]' Q[0]' X[0] X[1]' + Q[2]' Q[1]' Q[0]' X[0] X[1
[1]' Q[0]' X[0] X[1]' + Q[2] Q[1]' Q[0]' X[0] X[1] + Q[2] Q[1]' (
[1]' + Q[2] Q[1]' Q[0] X[0] X[1];
D[1] = Q[2]' Q[1]' Q[0]' X[0] X[1] + Q[2]' Q[1]' Q[0] X[0]' X[1]
[1]' Q[0] X[0] X[1] + Q[2]' Q[1] Q[0]' X[0]' X[1]' + Q[2]' Q[1] (
X[1] + Q[2] Q[1]' Q[0] X[0]' X[1]' + Q[2] Q[1]' Q[0] X[0]' X[1]
D[0] = Q[2]' Q[1]' Q[0]' X[0]' X[1] + Q[2]' Q[1]' Q[0]' X[0] X[1
Q[1] Q[0]' X[0] X[1]' + Q[2]' Q[1] Q[0]' X[0] X[1] + Q[2] Q[1]' (
X[1]' + Q[2] Q[1]' Q[0]' X[0] X[1];
Z[5] = Q[2]' Q[1] Q[0] X[0]' X[1]' + Q[2]' Q[1] Q[0] X[0]' X[1]
[0] X[0]' X[1]' + Q[2] Q[1] Q[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0
Z[4] = Q[2]' Q[1] Q[0]' X[0]' X[1]' + Q[2]' Q[1] Q[0]' X[0]' X[1
[1] Q[0] X[0]' X[1]' + Q[2]' Q[1] Q[0] X[0]' X[1] + Q[2]' Q[1] Q
[1]' + Q[2] Q[1] Q[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0] X[1]' + Q
Z[3] = Q[2]' Q[1]' Q[0] X[0]' X[1]' + Q[2]' Q[1]' Q[0] X[0]' X[1
[1] Q[0]' X[0]' X[1]' + Q[2]' Q[1] Q[0]' X[0]' X[1] + Q[2]' Q[1]
X[1]' + Q[2]' Q[1] Q[0] X[0]' X[1] + Q[2]' Q[1] Q[0] X[0] X[1]'
[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0] X[1]' + Q[2] Q[1] Q[0] X[0]
Z[2] = Q[2] Q[1]' Q[0]' X[0]' X[1]' + Q[2] Q[1]' Q[0]' X[0]' X[1
[1]' Q[0] X[0]' X[1]' + Q[2] Q[1]' Q[0] X[0]' X[1] + Q[2] Q[1]' (
[1]' + Q[2] Q[1] Q[0]' X[0]' X[1] + Q[2] Q[1] Q[0]' X[0] X[1]' +
[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0] X[1]' + Q[2] Q[1] Q[0] X[0]
Z[1] = Q[2] Q[1]' Q[0] X[0]' X[1]' + Q[2] Q[1]' Q[0] X[0]' X[1]
[0]' X[0]' X[1]' + Q[2] Q[1] Q[0]' X[0]' X[1] + Q[2] Q[1] Q[0]'
[2] Q[1] Q[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0] X[1]' + Q[2] Q[1]
Z[0] = Q[2] Q[1] Q[0]' X[0]' X[1]' + Q[2] Q[1] Q[0]' X[0]' X[1]
[0] X[0]' X[1]' + Q[2] Q[1] Q[0] X[0]' X[1] + Q[2] Q[1] Q[0] X[0

Minimized:
D[2] = Q[2] Q[1]'  + Q[1]' Q[0]' X[0] ;
D[1] = Q[1]' Q[0]  + Q[2]' Q[1] Q[0]'  + Q[2]' Q[0]' X[0] X[1];
D[0] = Q[2]' Q[1] Q[0]'  + Q[2] Q[1]' Q[0]'  + Q[1]' Q[0]' X[1];
Z[5] = Q[1] Q[0] ;
Z[4] = Q[2]' Q[1]  + Q[1] Q[0] ;
Z[3] = Q[2]' Q[1]  + Q[2]' Q[0]  + Q[1] Q[0] ;
Z[2] = Q[2] ;
Z[1] = Q[2] Q[1]  + Q[2] Q[0] ;
Z[0] = Q[2] Q[1] ;
```


The schematic makes use of feedback, clock divider, 2x1 multiplex, and a D-flipflop. The Input variables include the CLK, CLR, CLK_SEL, and X[1..0]. The

output is the FF_CLK, Z[5..0], and Q[2..0]. The state table is developed in order of idle, left, and right, for implementation of the feedback input. At the bottom right of the Logic Friday table is the minimized equation for each specific light. The minimized equation is used to create the feedback input in Quartus Lite.

Results and Testing



The waveform shows which digits will “light” up to synchronous with each other. You can see during certain parts of the waveform when the light will indicate right, left, or idle.

Conclusion

In conclusion, we can use Quartus Lite to implement a synchronous state machine. We can develop a synchronous state machine to create a sequential taillight controller. We can test our schematic to see the results on a waveform. We can finally implement our code on an FPGA board.