SCHA63T-K03 Data Sheet

SCHA63T-K03: 6-DOF XYZ-Axis Gyroscope and xyz-Axis Accelerometer with digital SPI interface

Features

- ±300°/s angular rate measurement range
- ± 6 g acceleration measurement range
- −40°C…+110°C operating temperature range
- 3.0V…3.6V supply voltage
- 2 SPI digital interfaces
- Extensive self-diagnostics features
- Size 19.71 mm x 12.15 mm x 4.6 mm (l × w × h), 32 pins
- RoHS compliant robust SOIC plastic package suitable for lead free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology
- Can be used in Safety Critical Applications

Applications

SCHA63T-K03 is targeted at applications demanding high performance with tough environmental requirements. Typical applications include:

- Inertial Measurement Units (IMUs)
- Navigation and positioning
- Machine control and guidance
- Dynamic inclination
- Robotic control and UAVs

Restriction

- https://www.murata.com/en-global/support/militaryrestriction

Overview

The SCHA63T-K03 is a combined high performance 3-axis angular rate and 3-axis accelerometer. It consists of X-, Y- and Z-axis angular rate sensors and integrated 3-axis accelerometer based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done with two mixed signal ASICs that provides angular rate via flexible SPI digital interface. Sensor elements and ASIC are packaged to premolded SOIC 32 plastic housing that guarantees reliable operation over product's lifetime.

The SCHA63T-K03 is designed, manufactured and tested for high stability, reliability and quality requirements. Component has extremely stable output over temperature, humidity and vibration. Component has several advanced self-diagnostic features and is suitable for SMD mounting and is compatible with RoHS and ELV directives.

TABLE OF CONTENTS

1 Introduction

This document contains essential technical information about SCHA63T-K03 sensor including specifications, SPI interface descriptions, user accessible register details, electrical properties and application information. This document should be used as a reference when designing in SCHA63T-K03 component.

2 Specifications

2.1 Abbreviations

ASIC	Application Specific Integrated Circuit
CCM	Channel calibration and monitoring
Cpk	Process Capability Index
CSB	Chip Select
CST	Continuous Self Test
DPS	Degrees per second
DUE	ASIC for ZY-axis rate
FFB	Force Feedback (Gyro operating principle)
FS	Full scale
HPC	High Performance Combo
MOSI	Master Out Slave In
MISO	Master In Slave Out
MCU	Microcontroller
RT	Room Temperature
SCK	Serial Clock
SPI	Serial Peripheral Interface
UNO	ASIC for X-axis rate and XYZ-axis accelerometer
F_prim	Gyro primary frequency
Rx	Rate X axis
Ry	Rate Y axis
Rz	Rate Z axis
Ax	Accelerometer X axis
Ay	Accelerometer Y axis
Az	Accelerometer Z axis

2.2 General Specifications

General specifications for SCHA63T-K03 component are presented in Table 1. All analog voltages are related to the potential at GNDA and all digital voltages are related to the potential at GNDD.

Table 1. General specifications.

Parameter	Condition	SC/CC	Min	Typ	Max	Unit
Supply voltage: V3p3A			3.0	3.3	3.6	V
Supply voltage: V3p3D			3.0	3.3	3.6	V
Supply current: V3p3A DUE				8.5		mA
Supply current: V3p3D DUE				9.5		mA
Supply current: V3p3A+D DUE				18		mA
Supply current: V3p3A UNO				6.25		mA
Supply current: V3p3D UNO				6.25		mA
Supply current: V3p3A+D UNO				12.5		mA
Total current, I_TOTAL UNO+DUE	I_V3p3A + I_V3p3D Temperature range -40 ... +110 °C	CC		30.5		mA
Total current reset UNO+DUE	Total average current during reset				4	mA
Output update rate	Gyro, Accelerometer and Temperature sensor			F_prim /2		Hz
TMODE	Wait time to set the operation mode after the supply in the specification. Wait time needed after power on or after reset. (Wait time starts when supply is inside spec limits.) SPI is not functional during this time.		25			ms
TSPIR	SPI communication is not allowed for 2ms after SPI Hardreset.		2			ms

2.3 Performance Specifications for Gyroscope

Table 2. Gyro performance specifications (VDD = 3.3 V and at room temperature unless otherwise specified). Below values are from device Product and Process Validation (PV) phase unless otherwise specified.

Parameter	Condition	Axis	Min	Typ	Max	Unit
Measurement range	Minimum saturation flag	XYZ	± 300			°/s
Offset [A)]	Offset after calibration, 3σ N > 234	XYZ	-0.8	0	0.8	°/s
Offset temperature dependency [B)]	-40°C ≤ T ≤ +110°C, 3σ N = 234	XY	-0.65		0.65	°/s
		Z	-0.085		0.085	°/s
Offset change over lifetime [C)]	1000 hours of high temperature operating life (HTOL) at 125°C, VDD=3.6V N = 234	XY	-0.22		0.22	°/s
		Z	-0.06		0.06	°/s
Sensitivity [D)]	Sensitivity after calibration at ±300°/s, 3σ N > 90	XYZ	79	80	81	LSB/°/s
Sensitivity temperature dependency [E)]	-40°C ≤ T ≤ +110°C, 3σ N = 234	XY	-0.2		0.6	%
		Z	0		0.2	%
Sensitivity change over lifetime [F)]	1000 hours of high temperature operating life (HTOL) at 125°C, VDD=3.6V N = 234	XY	-0.75		0.75	%
		Z	-0.21		0.21	%
Linearity error [G)]	End point fit to ±300 °/s N = 12	XYZ		0.15	0.25	°/s
Noise density	3σ, N = 12	XYZ		0.0015	0.0019	°/s/$\sqrt{Hz}$
Angle Random Walk	3σ, N = 12	XYZ		0.09	0.11	°/$\sqrt{h}$
Bias Instability [H) I) J)]	At RT, Allan Variance minimum divided by 0.664, 3σ, N = 12	XYZ		1.64	2.57	°/h
Orthogonality error	Axis to axis after external cross axis compensation, 3σ, N = 234	XYZ	-0.25		0.25	%
Amplitude response −3 dB frequency	13 Hz Filter, 3σ, N = 15	XYZ	12.1	13.6	14.3	Hz
	20 Hz Filter, 3σ, N = 15		18.5	20.2	21.5	Hz
	46 Hz Filter, 3σ, N = 15		42.1	46.1	48.9	Hz
	300 Hz Filter, 3σ, N = 15		280	305.8	325.6	Hz
Power on start-up time [k)]	13 Hz filter (after SPI power on command), MAX	XYZ			620	ms
	20 Hz filter (after SPI power on command), MAX				620	ms
	46 Hz filter (after SPI power on command), MAX				500	ms
	300 Hz filter (after SPI power on command), MAX				500	ms
F_prim	Nominal operation frequency of the sensor element. All ASIC internal clocks are derived from a multiple of this frequency	XY	15.8	16.8	17.8	kHz
		Z	18.3	19.3	20.3	kHz
Output update rate		XYZ		F_prim/2		
G sensitivity(1g x,y,z axis static)	For DC gravity input, 3σ, N = 48	XYZ			0.006	(°/s)/g

A) Initial offset at Murata Production measurement after calibration

B) Offset temperature dependency is determined by the larger absolute value of [(maximum offset over temperature) – (offset at 25°C)] or [(minimum offset over temperature) – (offset at 25°C)]

C) Estimated from offset change during 1000 hours of high temperature operating live (HTOL) test at 125°C and maximum supply voltages

D) Sensitivity is defined as

$$Sensitivity = \frac{AR_{meas}(\Omega_{max}) - AR_{meas}(\Omega_{min})}{\Omega_{max} - \Omega_{min}}$$

Where
Ω_{max}=applied angular rate at maximum operating range
Ω_{min}=applied angular rate at minimum operating range
$AR_{meas}(\Omega_{n})$=measured angular rate at Ω_{n} [LSB]

E) Sensitivity temperature dependency is determined by the larger absolute value of
[(maximum sensitivity value over temperature) - (sensitivity at 25°C)] /sensitivity at 25°C*100% or
[(minimum sensitivity value over temperature) - (sensitivity at 25°C)] /sensitivity at 25°C*100%

F) Estimated from sensitivity change during 1000 hours of high temperature operating life (HTOL) test at 125°C and maximum supply voltages

G) Linearity is the maximum deviation from the straight line defined by the measured values at the operating range end points.

H) Allan Variance Minimum divided by 0.664

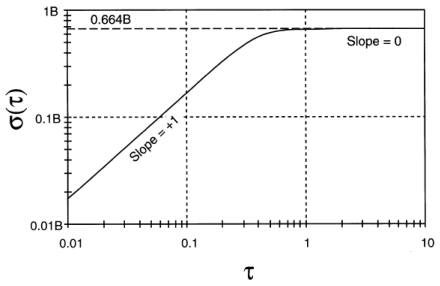


Figure C.2—σ(τ) Plot for bias instability (for f_0 = 1)

I) Optimization for SPI duty cycle or sample rate is required to achieve typical Allan variance in table

J) Device powered four hours before data collection starts to permit fully settling from power up.

K) Max values are determined from product platform validations

Note :

- Specification is valid after 24hours from reflow.
- Each system design including SCHA63T-K03 must be evaluated by the customer in advance to guarantee proper functionality during operation.
- Min and Max values are from validation mean ±3 sigma variation limits from test population at the minimum. Min and Max values are not guaranteed. Nominal values are mean values from validation test population.

2.4 Performance Specifications for Accelerometer

Table 3. Accelerometer performance specifications (VDD = 3.3 V and room temperature unless otherwise specified). Below values are from device Product and Process Validation (PV) phase unless otherwise specified.

Parameter	Condition	Axis	Min	Typ	Max	Unit
Measurement range	Minimum saturation flag	XYZ	6			g
Offset [A)]	Offset after calibration, 3σ N = 234	XYZ	-13.5		13.5	mg
Offset temperature dependency [B)]	-40°C ≤ T ≤ +110°C, 3σ N = 234	XYZ	-7.3		7.3	mg
Offset change over lifetime [C)]	1000 hours of high temperature operating life (HTOL) at 125°C, VDD=3.6V N = 234	XYZ	-22		22	mg
Sensitivity [D)]	Sensitivity after calibration at ±1g, 3σ N = 234	XYZ	4899	4905	4911	LSB/g
Sensitivity temperature dependency [E)]	-40°C ≤ T ≤ +110°C, 3σ N = 234	XYZ	-0.15		0.15	%
Sensitivity change over lifetime [F)]	1000 hours of high temperature operating life (HTOL) at 125°C, VDD=3.6V N = 234	XYZ	-0.06		0.06	%
Linearity error [G)]	End point fit to ±6g 3σ, N = 30	XYZ	1.9	6.3	17.2	mg
	End point fit to ±1g 3σ, N = 30	XYZ			1	mg
Noise density	3σ, N = 12	XYZ		59.5	66.0	µg/$\sqrt{Hz}$
Velocity random walk	3σ, N = 12	XYZ		35.0	38.8	mm/s /$\sqrt{h}$
Bias instability	At RT, Allan Variance minimum divided by 0.664, 3σ, N = 12	XYZ		12.2	18.3	µg
Orthogonality error	Axis to axis after external cross axis compensation, 3σ, N = 234	XYZ	-0.14		0.14	%
Amplitude response −3 dB frequency	13 Hz Filter, 3σ, N = 15	XYZ	13.2	13.7	14.2	Hz
	20 Hz Filter, 3σ, N = 15	XYZ	19.7	20.3	20.8	Hz
	46 Hz Filter, 3σ, N = 15	XYZ	45.0	46.3	47.5	Hz
	300 Hz Filter, 3σ, N = 15	XYZ	247.4	264.2	286.7	Hz
Power on start-up time [H)]	13 Hz filter (after SPI power on command) , MAX	XYZ			450	ms
	20 Hz filter (after SPI power on command) , MAX				450	ms
	46 Hz filter (after SPI power on command) , MAX				320	ms
	300 Hz filter (after SPI power on command) , MAX				320	ms
Output update rate	Tied to X-gyro F_prim/2	XYZ	7.9	8.4	8.9	kHz

A) Initial offset at Murata Production measurement after calibration

B) Offset temperature dependency is determined by the larger absolute value of [(maximum offset over temperature) – (offset at 25°C)] or [(minimum offset over temperature) – (offset at 25°C)]

C) Estimated from offset change during 1000 hours of high temperature operating life (HTOL) test at 125°C

D) Sensitivity is defined as

$$Sensitivity = \frac{ACC_{meas}(a_{+1g}) - ACC_{meas}(a_{-1g})}{a_{+1g} - a_{-1g}}$$

Where
a_{+1g}=applied acceleration at +1g
a_{-1g}=applied acceleration at -1g
$ACC_{meas}(a_n)$=measured acceleration at a_n [LSB]

E) Sensitivity temperature dependency is determined by the larger absolute value of
[(maximum sensitivity value over temperature) - (sensitivity at 25°C)] /sensitivity at 25°C*100% or
[(minimum sensitivity value over temperature) - (sensitivity at 25°C)] /sensitivity at 25°C*100%

F) Estimated from Sensitivity change during 1000 hours of high temperature operating life (HTOL) test at 125°C

G) Linearity is the maximum deviation from the straight line defined by the measured values at the specified range end points.

H) Max values are determined from product platform validations

Note :

- Specification is valid after 24hours from reflow.
- Each system design including SCHA63T-K03 must be evaluated by the customer in advance to guarantee proper functionality during operation.
- Min and Max values are validation ±3 sigma variation limits from test population at the minimum. Min and Max values are not guaranteed. Nominal values are mean values from validation test population.

2.5 Performance Specification for Temperature Sensor

Table 4. Temperature sensor performance specifications.

Parameter	Condition	Min.	Typ	Max.	Unit
Temperature signal range		-50		+150	°C
Temperature signal sensitivity	Temperature sensor output in 2's complement format		30		LSB/°C

Temperature is converted to °C with following equation:

Temperature [°C] = 25 + (TEMP / 30),

where TEMP is temperature sensor output register content in decimal format.

2.6 Cross-Axis Compensation

SCHA63T-K03 ASIC stores the cross-axis compensation and offset fine tuning terms both for the rate and accelerometer and cross-axis compensation can be done in the external microprocessor according to the following equations.

Equation 1: Rate Cross-Axis Compensation

$$\vec{\Omega_{real}} = \begin{pmatrix} c_{xx} & c_{xy} & c_{xz} \\ c_{yx} & c_{yy} & c_{yz} \\ c_{zx} & c_{zy} & c_{zz} \end{pmatrix} * (\vec{\Omega_{meas}} - \vec{\Omega_{offs}})$$

where

c_{ii} = is the corresponding rate cross-axis compensation term (in non-volatile memory, see Table 5: Cross-Axis Compensation Register Map)

Equation 2: Compensated rate vector

$$\vec{\Omega_{real}} = \begin{pmatrix} \Omega_{rx} \\ \Omega_{ry} \\ \Omega_{rz} \end{pmatrix}$$

Equation 3: Measured rate vector (from the component)

$$\vec{\Omega_{meas}} = \begin{pmatrix} \Omega_{mx} \\ \Omega_{my} \\ \Omega_{mz} \end{pmatrix}$$

Equation 4: Rate offset compensation vector (Not stored in the memory). Rate offset zeroing in system level e.g. after PCB assembly is recommended.

$$\vec{\Omega_{offs}} = \begin{pmatrix} \Omega_{ox} \\ \Omega_{oy} \\ \Omega_{oz} \end{pmatrix}$$

For the accelerometers following equations apply:

Equation 5: Accelerometer Cross-Axis Compensation

$$\vec{a_{real}} = \begin{pmatrix} b_{xx} & b_{xy} & b_{xz} \\ b_{yx} & b_{yy} & b_{yz} \\ b_{zx} & b_{zy} & b_{zz} \end{pmatrix} * (\vec{a_{meas}} - \vec{a_{offs}})$$

where

b_{ii} = is the corresponding accelerometer cross-axis compensation term (see Table 5: Cross-Axis Compensation Register Map)

Equation 6: Compensated accelerometer vector

$$\vec{a_{real}} = \begin{pmatrix} a_{rx} \\ a_{ry} \\ a_{rz} \end{pmatrix}$$

Equation 7: Measured accelerometer vector (from the component)

$$\vec{a_{meas}} = \begin{pmatrix} a_{mx} \\ a_{my} \\ a_{mz} \end{pmatrix}$$

Equation 8: Acceleration offset compensation vector (Not stored in the memory). Acceleration offset zeroing in system level e.g. after PCB assembly is recommended.

$$\vec{a_{offs}} = \begin{pmatrix} a_{ox} \\ a_{oy} \\ a_{oz} \end{pmatrix}$$

Note: Sensing element axes are independent from each other by the mechanical design. The cross-axis compensation doesn't affect to axis independency as long as no axes are saturated.

Table 5: Cross-Axis Compensation Register Map

Parameter	Bank (DUE ASIC)	Address (hex)	Register	Range (2's complement)	Floating number
c_{xx}	05h	0Bh	ACC_DC1[7:0]	- 128 .. 127 LSB	1+value/4096
c_{xy}	05h	0Bh	ACC_DC1[15:8]	- 128 .. 127 LSB	value/4096
c_{xz}	05h	13h	ACC_DC9[7:0]	- 128 .. 127 LSB	value/4096
c_{yx}	05h	13h	ACC_DC9[15:8]	- 128 .. 127 LSB	value/4096
c_{yy}	05h	14h	ACC_DC10[7:0]	- 128 .. 127 LSB	1+value/4096
c_{yz}	05h	14h	ACC_DC10[15:8]	- 128 .. 127 LSB	value/4096
c_{zx}	05h	15h	ACC_DC11[7:0]	- 128 .. 127 LSB	value/4096
c_{zy}	05h	15h	ACC_DC11[15:8]	- 128 .. 127 LSB	value/4096
c_{zz}	05h	16h	ACC_DC12[7:0]	- 128 .. 127 LSB	1+value/4096
b_{xx}	05h	16h	ACC_DC12[15:8]	- 128 .. 127 LSB	1+value/4096
b_{xy}	05h	17h	ACC_DC13[7:0]	- 128 .. 127 LSB	value/4096
b_{xz}	05h	17h	ACC_DC13[15:8]	- 128 .. 127 LSB	value/4096
b_{yx}	05h	18h	ACC_DC14[7:0]	- 128 .. 127 LSB	value/4096
b_{yy}	05h	18h	ACC_DC14[15:8]	- 128 .. 127 LSB	1+value/4096
b_{yz}	05h	1Bh	ACC_MD1[7:0]	- 128 .. 127 LSB	value/4096
b_{zx}	05h	1Bh	ACC_MD1[15:8]	- 128 .. 127 LSB	value/4096
b_{zy}	05h	1Ch	ACC_MD2[7:0]	- 128 .. 127 LSB	value/4096
b_{zz}	05h	1Ch	ACC_MD2[15:8]	- 128 .. 127 LSB	1+value/4096

2.6.1 Test Mode For Reading Cross-Axis Terms

Procedure
1) Activate test mode (open lock) after Step 3 (or 4 or 5 or 6) of start-up sequence in Figure 7

- Write/Read Register 19h (Mode)
  - Write Mode='RRRRRRRR RR010RRR'b
  - Read Mode
  - Write Mode='RRRRRRRR RR001RRR'b
  - Read Mode
  - Write Mode='RRRRRRRR RR100RRR'b
  - Read Mode
  - Dummy read, for example read Mode to get Mode read response
- Verify test mode
  - Check the read data bits Mode[2:0]='111'b

2) Change bank to 5
- Write data 5'h to address 1F'h

3) Read cross-axis terms
- Read registers according to Table 5

4) Save cross-axis terms to MCU
5) Power-off or SPI reset command via register 18h or reset by EXTRESN pin to exit test mode
6) Return to Step 1 of start-up sequence in Figure 7

*Write operation to an unspecified register after test mode access may permanently damage the component.

2.7 Absolute Maximum Ratings

Within the maximum ratings (Table 6. Absolute maximum ratings.), no damage to the component shall occur. Parametric values may deviate from specification, yet no functional deviation shall occur. All analog voltages are related to the potential at GNDA, all digital voltages are related to GNDD.

Table 6. Absolute maximum ratings.

Parameter	Remark	Min.	Typ	Max.	Unit
VDD	Supply voltage	-0.3		4.3	V
AIN/AOUT	Maximum voltage at analog input and output pins	-0.3		VDD+0.3 (4.3)	V
DIN/DOUT	Maximum voltage at digital input and output pins	-0.3		VDD+0.3 (4.3)	V
Topr	Operating temperature range	-40		110	°C
Tstg	Storage temperature range	-40		150	°C
ESD_HBM	ESD according Human Body Model (HBM), Q100-002	±2000			V
ESD_MM	ESD according Machine Model (MM), Q100-003	±200			V
ESD_CDM	ESD according Charged Device Model (CDM), Q100-011	±500 ±750 (corner pins)			V
US	Ultrasonic agitation (cleaning, welding, etc)	Prohibited			

2.8 Pin Description

The pinout for SCHA63T-K03 is presented in Figure 1, while the pin descriptions can be found in Table 7.

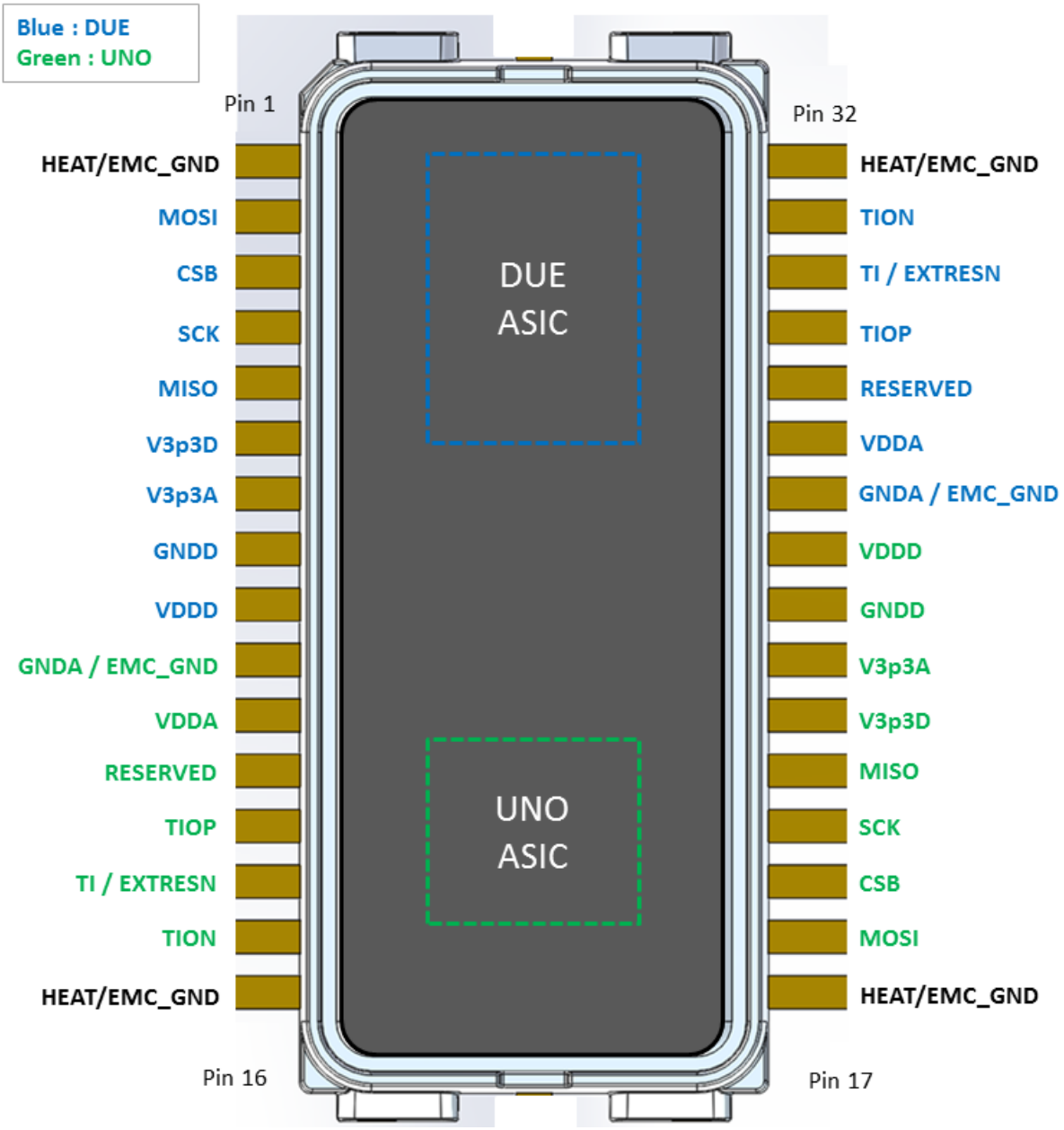


Figure 1. Pinout for SCHA63T-K03.

Table 7. SCHA63T-K03 pin descriptions.

Pin#	Name	ASIC	Type	Description
1	HEAT/EMC_GND	-	GND	Heatsink interface to GNDA
2	MOSI	DUE	DIN	Data In of SPI Interface
3	CSB	DUE	DIN	Chip Selected of SPI Interface
4	SCK	DUE	DIN	Clock Signal of SPI Interface
5	MISO	DUE	DOUT	Data Out of SPI Interface
6	V3p3D	DUE	SUPPLY	Digital Supply voltage
7	V3p3A	DUE	SUPPLY	Analog Supply voltage
8	GNDD	DUE	GND	Digital Supply return (ground), connect externally to GNDA.
9	VDDD	DUE	AOUT	Regulated supply for digital core. Use external capacitor which is connected according to the diagram in Figure 15.
10	GNDA / EMC_GND	UNO	GND	Analog Supply return (ground), connect externally to GNDD
11	VDDA	UNO	AOUT	Regulated supply for analog core. Use external capacitor which is connected according to the diagram in Figure 15.
12	RESERVED	UNO	-	Factory use only, connect to GND
13	TIOP	UNO	-	Factory use only, connect to GND.
14	TI/EXTRESN	UNO	DIN	Optional external Reset, 3.3V logic compatible Schmitt-trigger input with internal pull-up, LOW-HIGH transition causes system restart. Minimum low time 100us.
15	TION	UNO	-	Factory use only, connect to GND.
16	HEAT/EMC_GND	-	GND	Heatsink interface to GNDA
17	HEAT/EMC_GND	-	GND	Heatsink interface to GNDA
18	MOSI	UNO	DIN	Data In of SPI Interface
19	CSB	UNO	DIN	Chip Selected of SPI Interface
20	SCK	UNO	DIN	Clock Signal of SPI Interface
21	MISO	UNO	DOUT	Data Out of SPI Interface
22	V3p3D	UNO	SUPPLY	Digital Supply voltage
23	V3p3A	UNO	SUPPLY	Analog Supply voltage
24	GNDD	UNO	GND	Digital Supply return (ground), connect externally to GNDA.
25	VDDD	UNO	AOUT	Regulated supply for digital core. Use external capacitor which is connected according to the diagram in Figure 15.
26	GNDA / EMC_GND	DUE	GND	Analog Supply return (ground), connect externally to GNDD
27	VDDA	DUE	AOUT	Regulated supply for analog core. Use external capacitor which is connected according to the diagram in Figure 15.
28	RESERVED	DUE	-	Factory use only, connect to GND
29	TIOP	DUE	-	Factory use only, connect to GND.
30	TI/EXTRESN	DUE	DIN	Optional external Reset, 3.3V logic compatible Schmitt-trigger input with internal pull-up, LOW-HIGH transition causes system restart. Minimum low time 100us.
31	TION	DUE	-	Factory use only, connect to GND.
32	HEAT/EMC_GND	-	GND	EMC protection and ground

2.9 Typical performace characteristics

2.9.1 Gyro typical characteristics

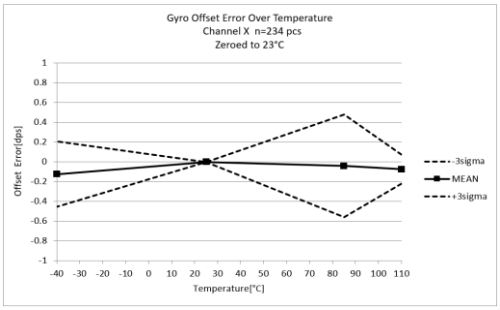


Chart 1 Gyro Offset Error over temperature X-axis

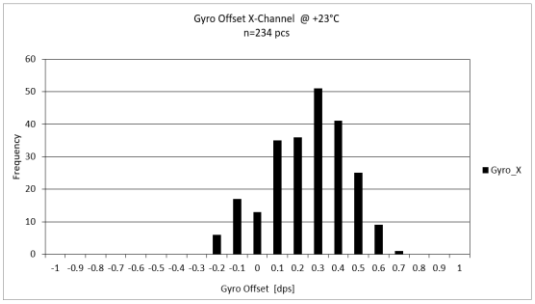


Chart 2 Gyro Offset Error @ +23°C X-axis

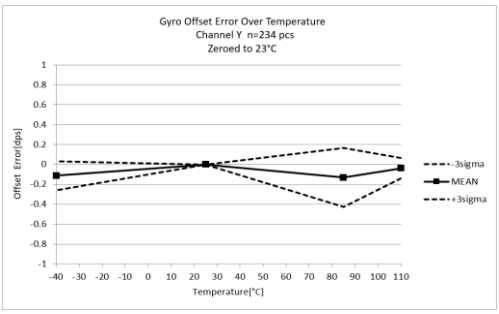


Chart 3 Gyro Offset Error over temperature Y-axis

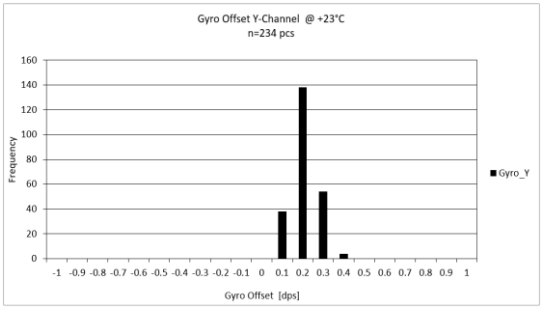


Chart 4 Gyro Offset Error @ +23°C Y-axis

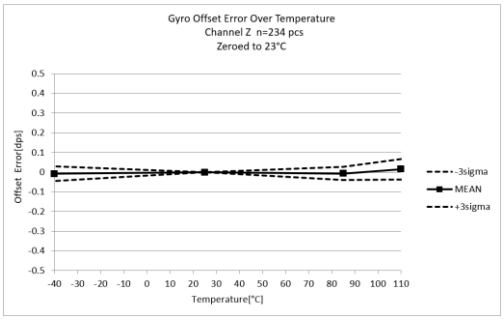


Chart 5 Gyro Offset Error over temperature Z-axis

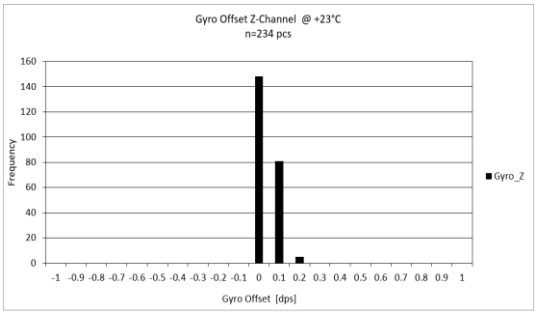


Chart 6 Gyro Offset Error @ +23°C Z-axis

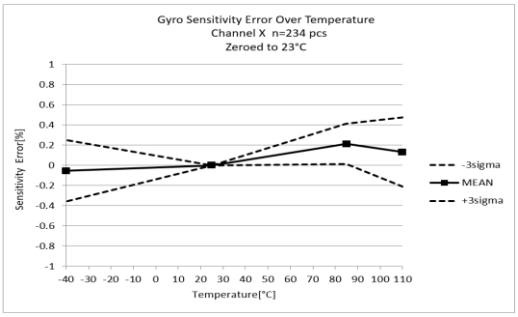


Chart 7 Gyro Sensitivity Error over temperature X-axis

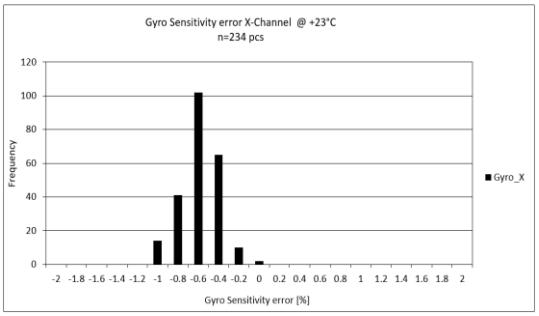


Chart 8 Gyro Sensitivity Error @ +23°C X-axis

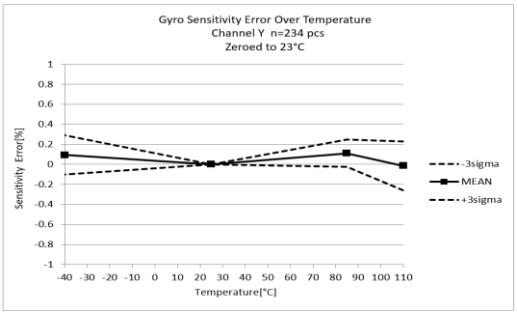


Chart 9 Gyro Sensitivity Error over temperature Y-axis

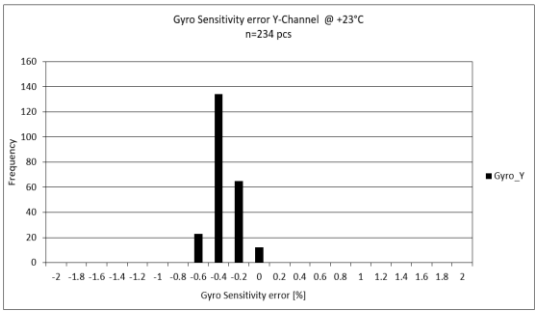


Chart 10 Gyro Sensitivity Error @ +23°C Y-axis

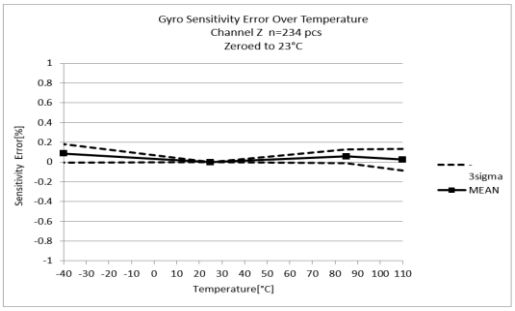


Chart 11 Gyro Sensitivity Error over temperature Z-axis

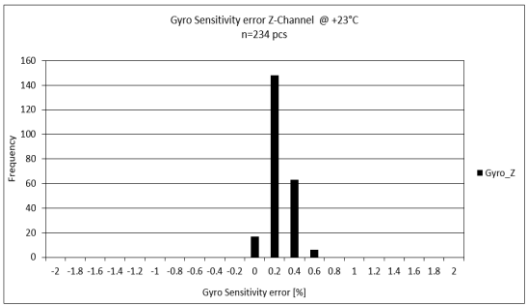


Chart 12 Gyro Sensitivity Error @ +23°C Z-axis

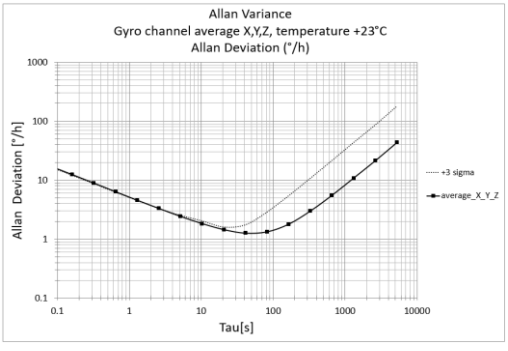


Chart 13 Gyro Allan Deviation X-,Y, and Z-axis

2.9.2 Acceleration typical characteristics

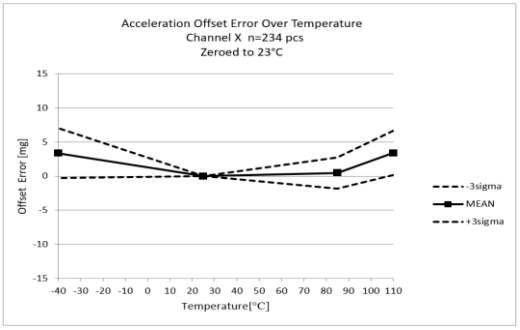


Chart 14 Accelerometer offset error over temperature X-axis

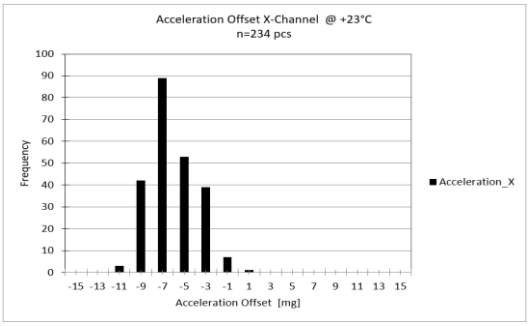


Chart 15 Accelerometer Offset Error @ +23°C X-axis

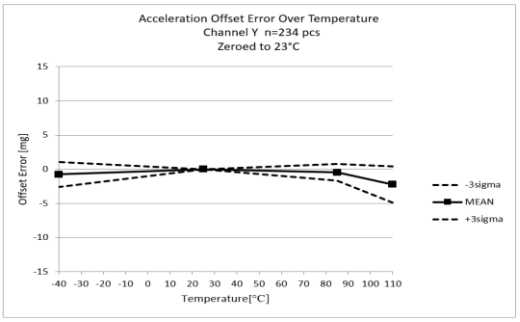


Chart 16 Accelerometer offset error over temperature Y-axis

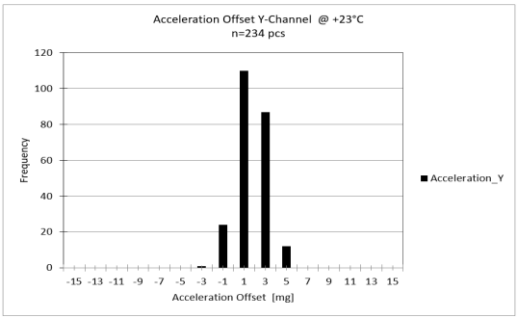


Chart 17 Accelerometer Offset Error @ +23°C Y-axis

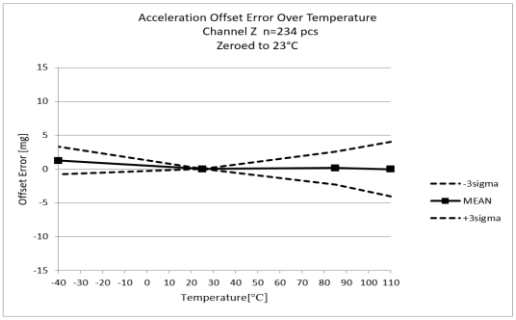


Chart 18 Accelerometer offset error over temperature Z-axis

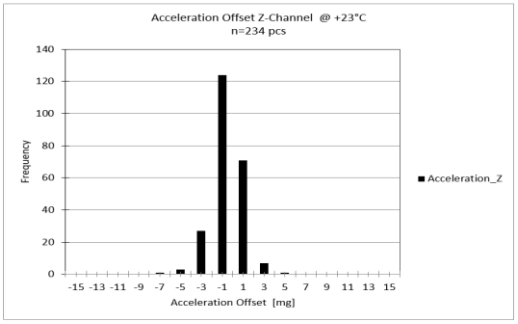


Chart 19 Accelerometer Offset Error @ +23°C Z-axis

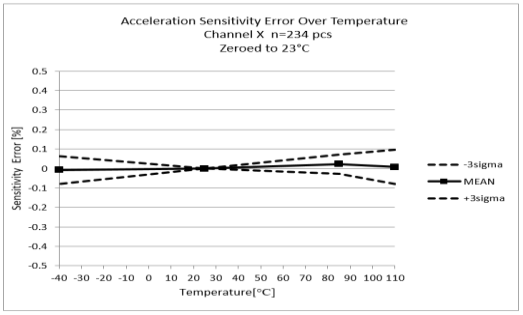


Chart 20 Accelerometer Sensitivity Error over temperature X-axis

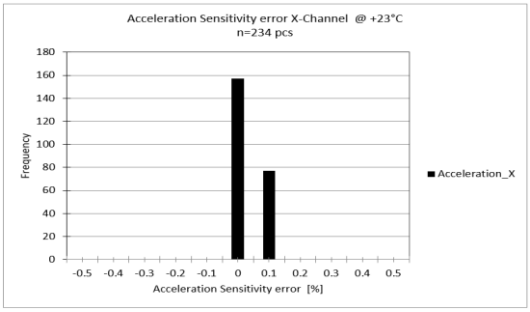


Chart 21 Accelerometer Sensitivity Error @ +23°C X-axis

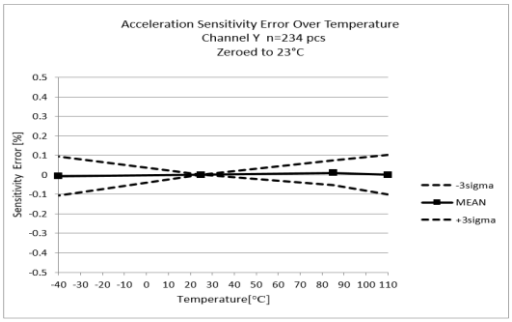


Chart 22 Accelerometer Sensitivity Error over temperature Y-axis

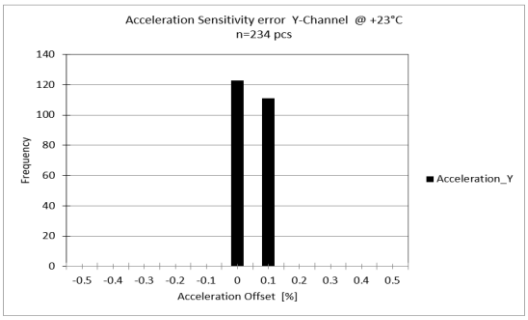


Chart 23 Accelerometer Sensitivity Error @ 23°C Y-axis

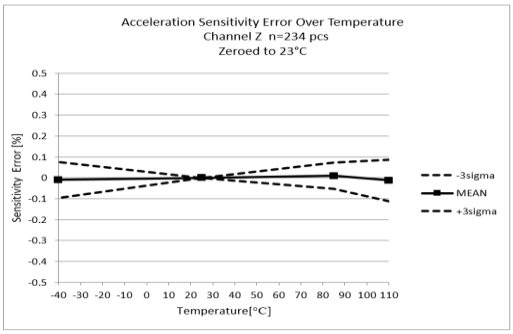


Chart 24 Accelerometer Sensitivity Error over temperature Z-axis

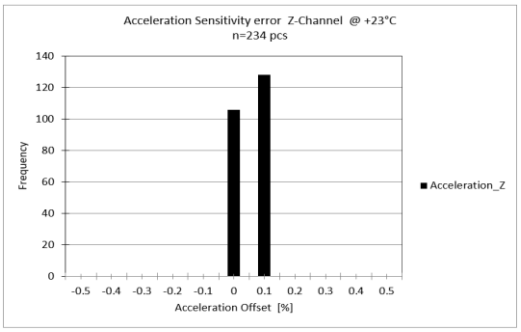


Chart 25 Accelerometer Sensitivity Error @ 23°C Z-axis

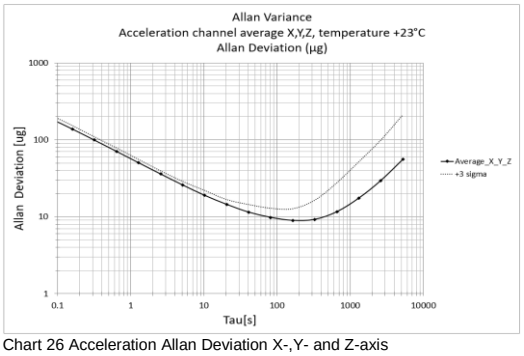


Chart 26 Acceleration Allan Deviation X-,Y- and Z-axis

2.10 Digital I/O Specification

Table 8 describes the DC characteristics of SCHA63T-K03 sensor SPI I/O pins. Supply voltage is 3.3 V unless otherwise specified. Current flowing into the circuit has a positive value.

Table 8. SPI DC characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
Serial Clock SCLK					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull down)	24		36	uA
Cin	Input capacitance			6	pF
Chip select CSB (Pull Up), low active					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull Up), Vin = 0V	24		36	uA
Cin	Input capacitance			6	pF
Vin_open	Open circuit output voltage	2			V
Serial data input MOSI (Pull Down)					
VinHigh	Input high voltage	2		V3p3D+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Input current source (Pull Up), Vin = DVDD	24		36	uA
Cin	Input capacitance			6	pF
Vin_open	Open circuit output voltage			0.3	V
Serial data output MISO (Tri state)					
VoutHigh_-1mA	Output high voltage, Iout = -1mA	V3p3D-0.5			V
VinHigh_1mA	Output low voltage, Iout = +1mA			0.5	V
Iout_Hz	High impedance output current, 0V < VMISO < V3p3D	-1		1	uA
Cld_miso	Capacitive load. The slope of the MISO output signal can be controlled to meet EMI requirements under specified load conditions.			200	pF

Table 9. EXTRESN pin characteristics

Symbol	Description	Min.	Nom.	Max.	Unit
Digital pin EXTRESN					
VinHigh	Input high voltage	2		V3p3A+0.3	V
VinLow	Input low voltage	-0.3		0.8	V
Vhy	Input hysteresis	0.2			V
Isource	Start-up indication phase inactive Start-up indication phase active	60 30		160 80	µA µA

2.11 SPI AC Characteristics

The AC characteristics of SCHA63T-K03 are defined in Figure 2 and Table 10.

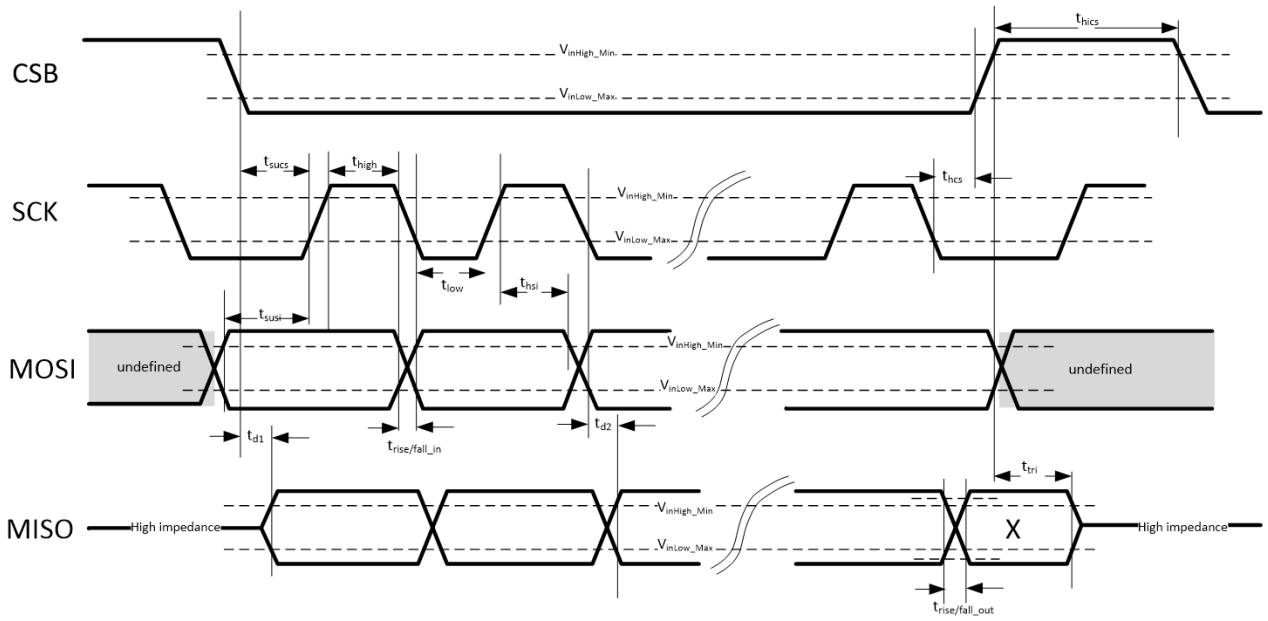


Figure 2. Timing diagram of SPI communication.

Table 10. SPI AC electrical characteristics.

Symbol	Description	Min.	Nom.	Max.	Unit
fSPI	Master (MCU): SPI SCLK frequency	0.1	-	10	MHz
tSPI	Master (MCU): SPI SCLK period	-	1/ fSPI	-	-
thigh	Master (MCU): High time: duration of logical high level at SCLK (from VinHigh_min to VinHigh_min)	35	tSPI/2	-	ns
tlow	Master (MCU): Low time: duration of logical low level at SCLK (from VinLow_max to VinLow_max)	35	tSPI/2	-	ns
tsucs	Master (MCU): Setup time CSB: time between the falling edge of CSB and the rising edge of SCLK (from VinLow_max to VinLow_max)	40	tSPI/2	-	ns
tsusi	Master (MCU): Setup time at MOSI: setup time of MOSI before the rising edge of SCLK (from VinLow_max to VinLow_max or from VinHigh_min to VinLow_max)	10	-	-	ns
thsi	Master(MCU): Hold time at MOSI: hold time of MOSI after rising edge of SCLK (from VinHigh_min to VinLow_max or to VinHigh_min)	20	-	-	ns
thcs	Master (MCU): Hold time of CSB: time between the falling edge of SCLK and the rising edge of CSB (from VinLow_max to VinLow_max)	30	tSPI/2	-	ns
thics	Master (MCU): Minimum high time of CSB between two consecutive transfers (from VinHigh_min to VinHigh_min)	30	tSPI/2		ns
trise/fall_in	Master (MCU): Rise/fall time of SCK/MOSI signals (from VinLow_max to VinHigh_min or from VinHigh_min to VinLow_max)	-	-	0.15x tSPI	ns
td1	Slave(=SCHA63T-K03 ASIC): Delay time: time delay from the falling edge of CSB to data valid at MISO (from VinLow_max to VInLow_max or to VInHigh_min)	-	-	30	ns

td2	Slave(=SCHA63T-K03 ASIC): Delay time: time delay from falling edge of SCLK to data valid at MISO (from VinLow_max to VInLow_max or to VInHigh_min)	0	-	30	ns
ttri	Slave(=SCHA63T-K03 ASIC): Tri-state delay time: time between the rising edge of CSB to MISO in Tri-state (from VinHigh_min to X)	-	-	25	ns
trise/fall_out	Slave(=SCHA63T-K03 ASIC): Rise/fall time of MISO signal (VOut_10% to VOut_90% and from VOut_90% to VOut_10%) User selectable MISO slew rate control in Mode register (19h)	4	10	16	ns

2.12 Measurement Axis and Directions

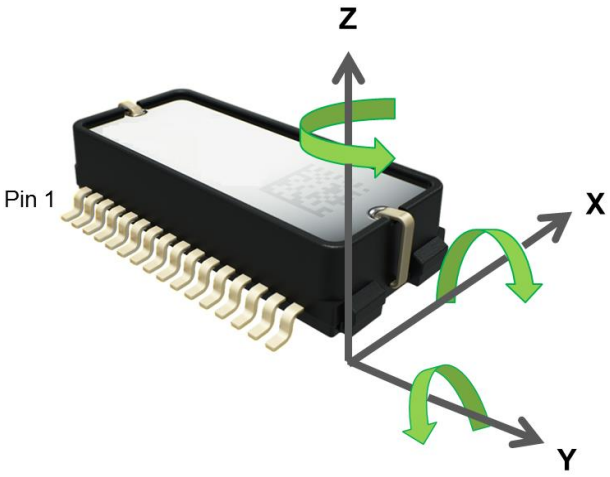
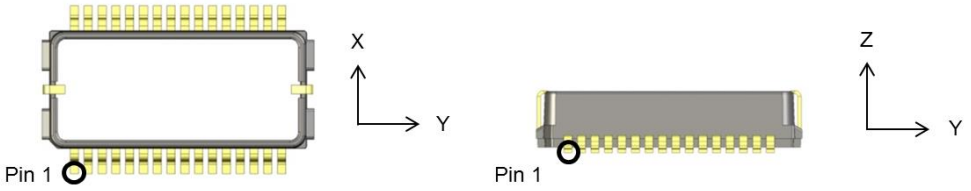


Figure 3. SCHA63T-K03 measurement directions.

Table 11 SCHA63T-K03 accelerometer measurement directions and outputs

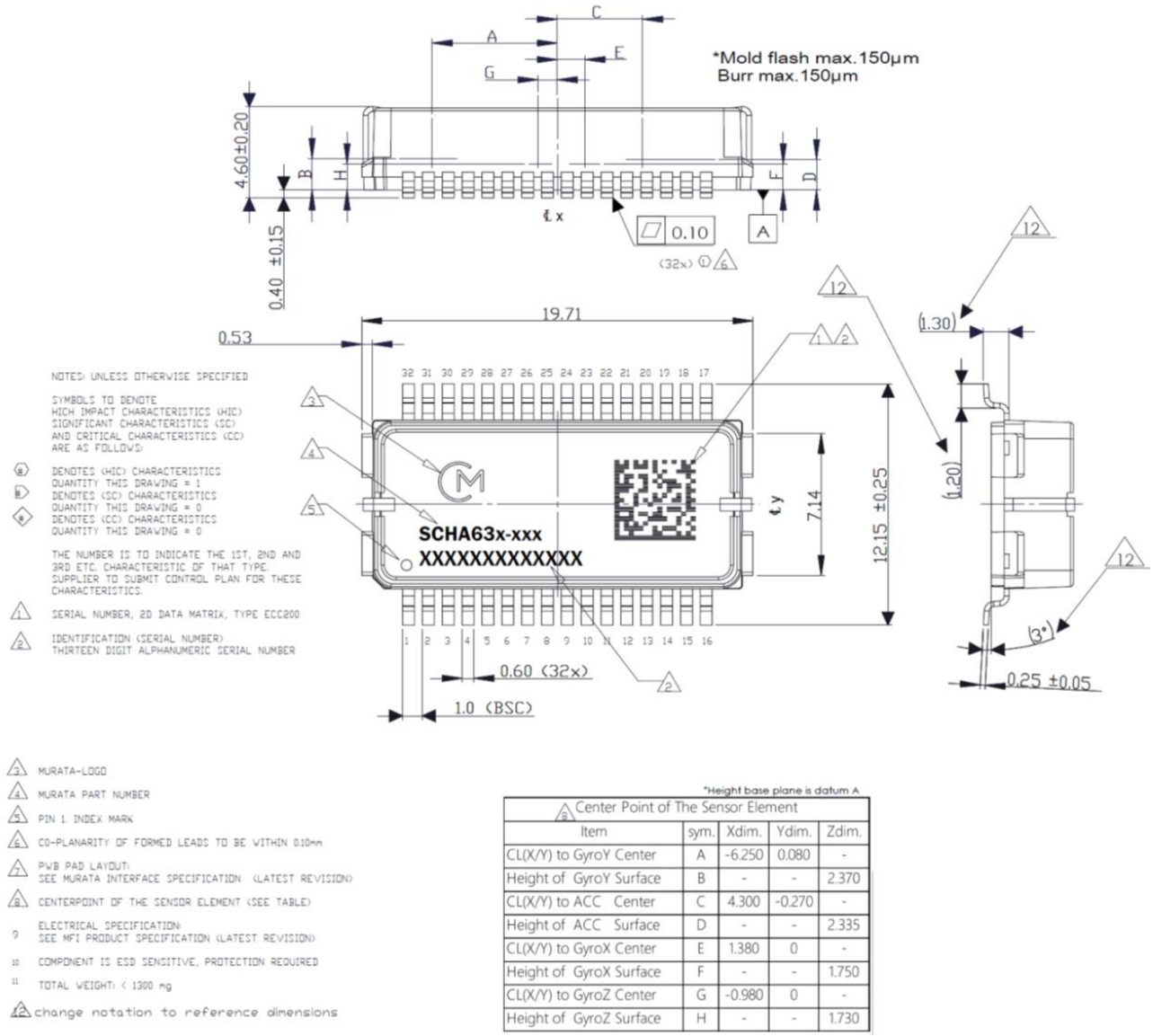


1g	1g	1g
X: 0g Y: 0g Z: 1g	0LSB 0LSB 4905LSB	X: -1g Y: 0g Z: 0g	-4905LSB 0LSB 0LSB	X: 0g Y: 0g Z: -1g	0LSB 0LSB -4905LSB
1g	1g	1g
X: 0g Y: 1g Z: 0g	0LSB 4905LSB 0LSB	X: 1g Y: 0g Z: 0g	4905LSB 0LSB 0LSB	X: 0g Y: -1g Z: 0g	0LSB -4905LSB 0LSB

2.13 Package Characteristics

2.13.1 Package Outline Drawing

The SCHA63T-K03 package outline and dimensions are presented in The outline of the SCHA63T-K03 package (SOIC-32) in mm. and Table 12. Limits for linear measures (ISO2768-f) unless tolerance is not specified in Figure 4 The outline of the SCHA63T-K03 package (SOIC-32) in mm.



*Height base plane is datum A

Center Point of The Sensor Element

Item	sym.	Xdim.	Ydim.	Zdim.
CL(X/Y) to GyroY Center	A	-6.250	0.080	-
Height of GyroY Surface	B	-	-	2.370
CL(X/Y) to ACC Center	C	4.300	-0.270	-
Height of ACC Surface	D	-	-	2.335
CL(X/Y) to GyroX Center	E	1.380	0	-
Height of GyroX Surface	F	-	-	1.750
CL(X/Y) to GyroZ Center	G	-0.980	0	-
Height of GyroZ Surface	H	-	-	1.730

Figure 4 The outline of the SCHA63T-K03 package (SOIC-32) in mm.

Table 12. Limits for linear measures (ISO2768-f) unless tolerance is not specified in Figure 4 The outline of the SCHA63T-K03 package (SOIC-32) in mm.

Tolerance class	Limits in mm for nominal size in mm			
	0.5 to 3	Above 3 to 6	Above 6 to 30	Above 30 to 120
f (fine)	±0.05	±0.05	±0.1	±0.15

It is not applicable for number shown in table of center point of the sensor element in figure 4, which is only for reference.

2.14 PCB Footprint

SCHA63T-K03 footprint dimensions are presented in Figure 5. Recommended PWB pad layout for SCHA63T-K03.

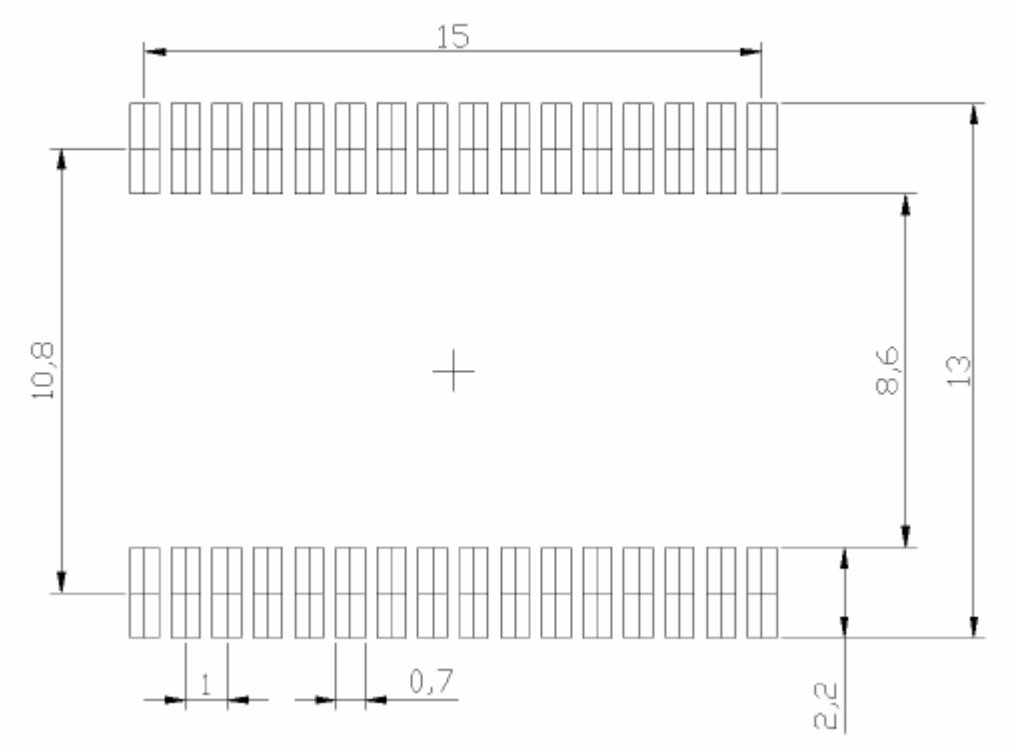


Figure 5. Recommended PWB pad layout for SCHA63T-K03.

3 General Product Description

3.1 Component block diagram

The SCHA63T-K03 sensor consists of independent acceleration and angular rate sensing elements, and two Application-Specific Integrated Circuits (ASIC) used to sense and control those elements. Figure 6 contains an upper level block diagram of the component for one rate channel. The ASIC provides two SPI interface used to control and read the accelerometer and the gyroscopes. Figure 6 shows UNO (1 axis gyro + 3 axis accelerometer) diagram. DUE has additional gyro block.

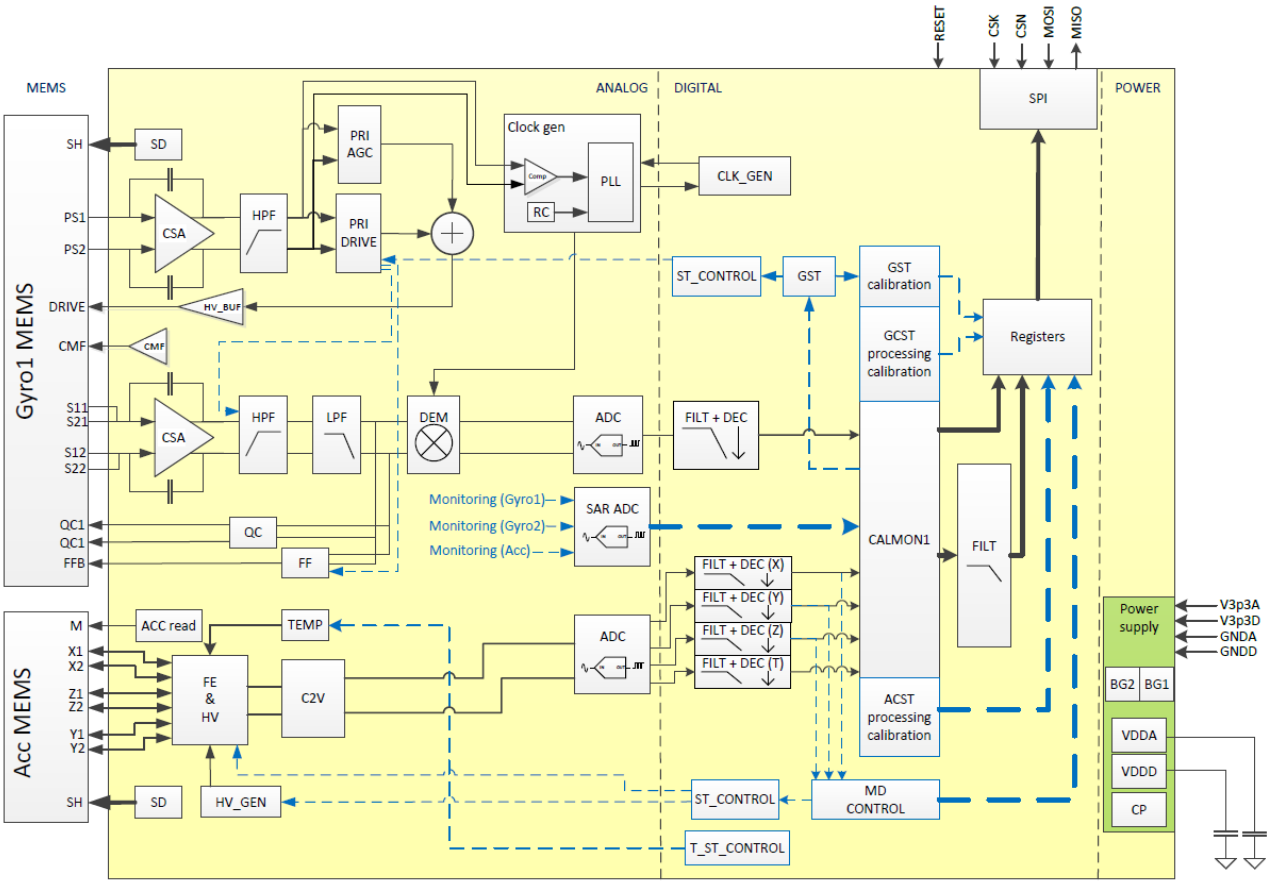


Figure 6. SCHA63T-K03 component block diagram.

The angular rate and acceleration sensing elements are manufactured using Murata proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

3.2 Acceleration sensing element

The acceleration sensing element consists of three acceleration sensitive masses. Acceleration causes capacitance change that is converted into a voltage change in the signal conditioning ASIC.

3.3 Angular rate sensing element

3 separated angular rate MEMS elements are used for SCHA63T-K03.
The angular rate sensing element consists of moving masses that are intentionally exited to in-plane drive motion. Rotation in sensitive direction causes out-of-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

3.4 Factory Calibration

SCHA63T-K03 sensors are factory calibrated. No separate calibration is required in the application. Parameters that are trimmed during production include offset and sensitivity for gyroscope and offset for accelerometer. Fail safe monitoring signals are also calibrated. Offset and sensitivity are calibrated with 2nd order polynomial at -40°C, +25°C and +110°C. Calibration parameters are stored to non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

4 Component Operation, Reset and Power Up

4.1 Component Operation

The SCHA63T-K03 component has internal power-on reset circuit. It releases the internal reset-signal once the power supplies are within the specified range and reads configuration and calibration data from the non-volatile memory to volatile registers. After the memory read, the sensor goes to power-down mode and external SPI command is needed to switch to run mode. An internal startup sequence is performed, when operation mode is activated. (Note: 2 times of write SPI command to set operation mode is required to start DUE internal startup sequence for Rate Y.)Start-up time is dependent of low pass filter setting. After the power on or reset, sensor shall be able to provide valid acceleration and angular rate data after specified Power on Start-up time.

SCHA63T-K03 sensor uses lowest available low pass filter setting by default. In case the some other low pass filter is desired the filter can be selected by SPI command.
SCHA63T-K03 component has extensive internal fail-safe diagnostics to detect over range and possible internal failures. The diagnostic status can be monitored via SPI RS - and status register bits.

4.2 Internal Failsafe Diagnostics

During the startup sequence the sensor performs a series of internal tests that will set various error flags in the sensor status registers and to clear them it is necessary to read summary status register after the startup sequence is complete.

Once startup sequence is completed and End of Initialization bit (EOI bit) has been written to one, the SPI frame Return Status bits (RS bits) indicate sensor operation status. Normal operation is indicated with RS bit content of 01b.

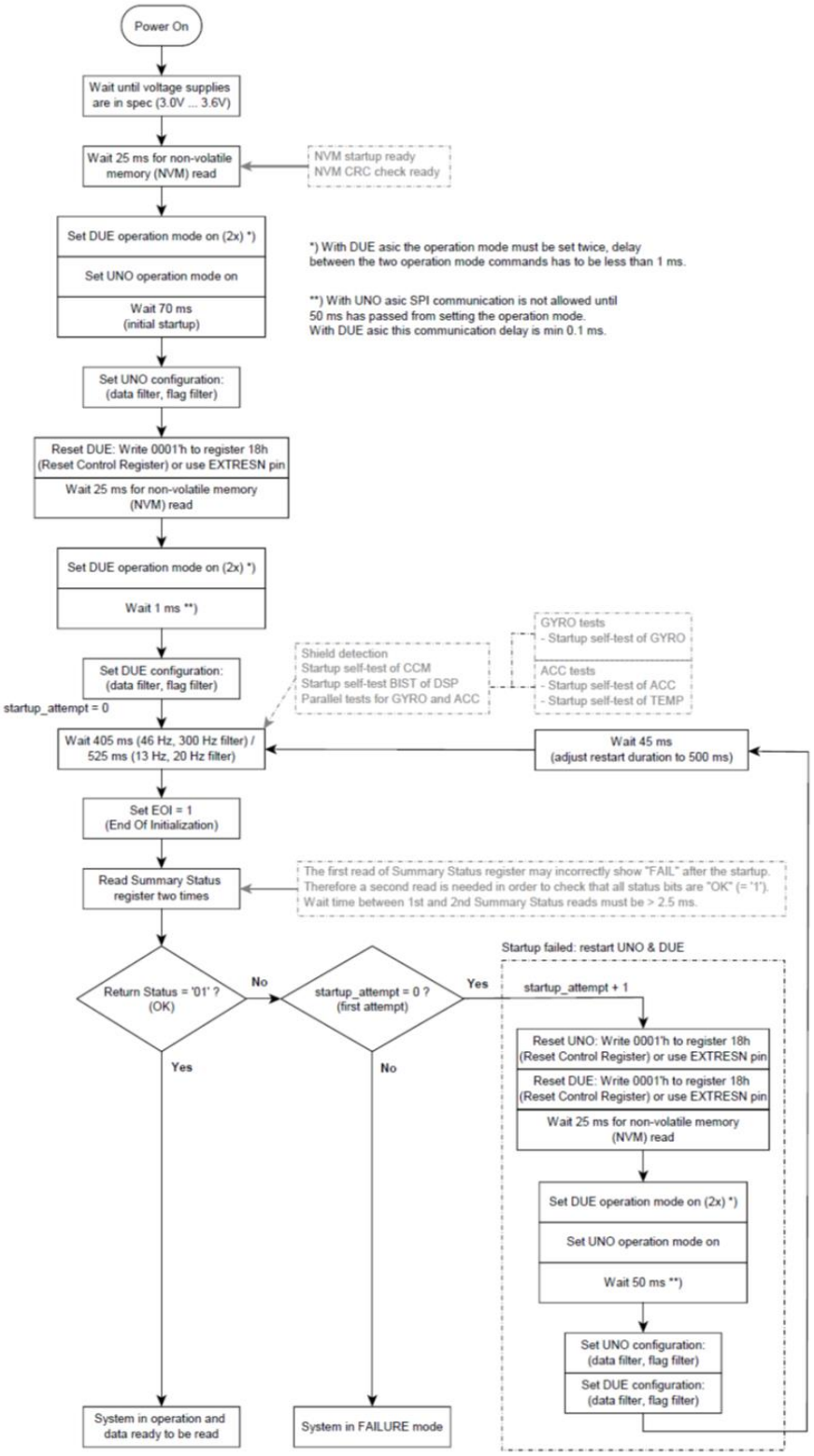


Figure 7 Power up sequence.

5 Component Interfacing

5.1 SPI Interface

5.1.1 General

The SCHA63T-K03 has two common physical SPI interfaces for the accelerometer and the angular rate sensors. SPI communication transfers data between the SPI master and registers of the SCHA63T-K03 ASIC. The SCHA63T-K03 always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used.
The same serial clock (SCK) is recommended for both ASICs(DUE and UNO) in case of parallel SPI communication by two individual SPI interfaces.

Table 13: Sensor outputs and SPI/register mapping

Parameter	SPI Interface	Register (hex)
Rate X	UNO	01h
Rate Y	DUE	03h
Rate Z	DUE	01h
Accel X	UNO	04h
Accel Y	UNO	05h
Accel Z	UNO	06h

SPI interface pins:

CSB	Chip Select (active low)	MCU → ASIC
SCK	Serial Clock	MCU → ASIC
MOSI	Master Out Slave In	MCU → ASIC
MISO	Master In Slave Out	ASIC → MCU

5.1.2 Protocol

SPI communication uses off-frame protocol so each transfer has two phases.

The first phase contains the SPI command (Request) and the data (Response) of the previous command. The second phase contains the next Request and the Response to the Request of the first phase, see Figure 8.

Data word length is 32 bits, the data is transferred MSB first. The first response after reset is undefined and shall be discarded.

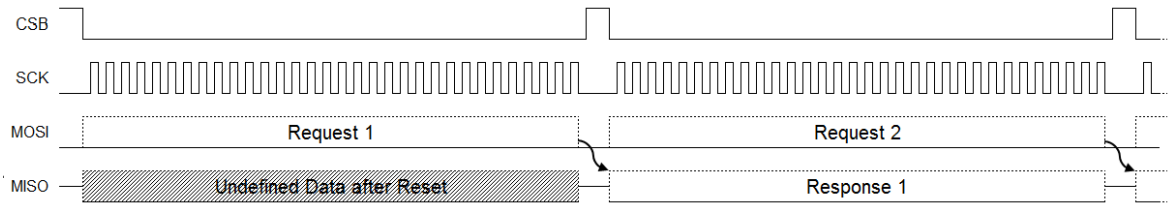


Figure 8. SPI protocol example.

The interleaved Request - Response cycle then continues as shown in Figure 9.

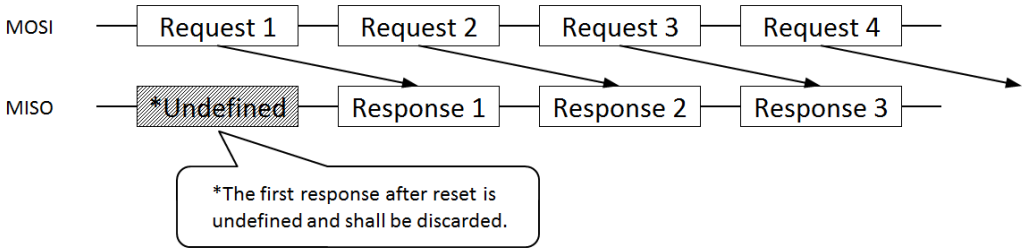


Figure 9. Request – Response frame relationship.

The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK's falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), see Figure 10.

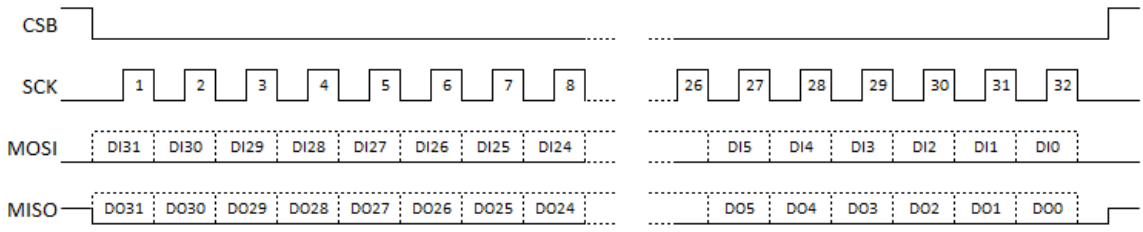


Figure 10. SPI Frame Format.

5.1.3 General Instruction format

The SPI frame is divided into four parts (See Figure 11 and Table 14):

1. Operation Code (OP)
2. Return status (RS, in MISO)
3. Data (DI, DO)
4. Checksum (CRC)

Unused bits shall be set to 0, this is important for the checksum calculation.

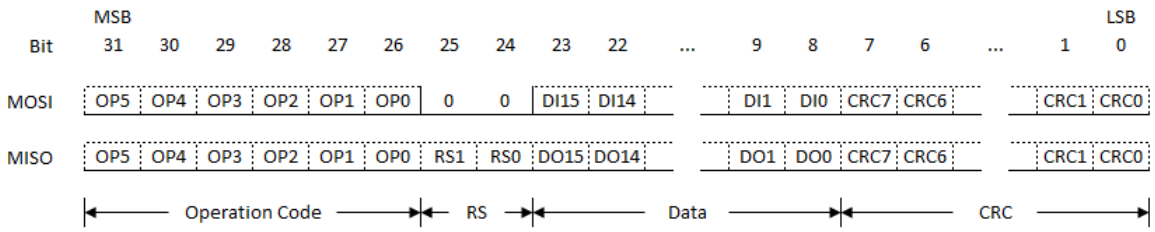


Figure 11. SPI instruction format.

Table 14. SPI bit definitions.

Bits	Name	MOSI	MISO
OP[5:0]	Operation code	Requested operation: • OP5: Write =1 / Read = 0 • OP[4:0] = Register address	Performed operation: • OP5: Write = 1 / Read = 0 • OP[4:0] = Register address
RS[1:0]	Return status	n.a.	Sensor status
D[15:0]	Data	Data to be written	Return data
CR[7:0]	Checksum	Checksum of MOSI bits [31:8]	Checksum of MISO bits [31:8]

5.1.4 Operations

Table 15. Operations and their equivalent SPI frames

Operation	ASIC	Register	SPI Frame Binary (OP, RS, Data, CRC)	SPI Frame Hex
Set Operation mode	DUE/UNO	MODE (19h)	111001 00 0000000000000000 01100111	E4000067h
Select 13Hz filter for RATE	DUE/UNO	G_FILT_DYN (16h)	110110 00 0000000000000000 01000101	D8000045h
Select 46Hz filter for RATE	DUE/UNO	G_FILT_DYN (16h)	110110 00 0001001000010010 10011110	D812129Eh
Select 13Hz filter for ACC	UNO	A_FILT_DYN (1Ah)	111010 00 0000000000000000 01101101	E800006Dh
Select 46Hz filter for RATE	UNO	A_FILT_DYN (1Ah)	111010 00 0000001000100010 01001000	E8022248h
Set EOI bit	DUE/UNO	ResCTRL (18h)	111000 00 0000000000000010 01011011	E000025Bh
Reset via SPI	DUE/UNO	ResCTRL (18h)	111000 00 0000000000000001 01111100	E000017Ch
Read RATE_X	UNO	RATE_X (01h)	000001 00 0000000000000000 11110111	040000F7h
Read RATE_Y	DUE	RATE_Y (03h)	000011 00 0000000000000000 11111011	0C0000FBh
Read RATE_Z	DUE	RATE_Z (01h)	000001 00 0000000000000000 11110111	040000F7h
Read ACC_X	UNO	ACCX (04h)	000100 00 0000000000000000 11101001	100000E9h
Read ACC_Y	UNO	ACCY (05h)	000101 00 0000000000000000 11101111	140000EFh
Read ACC_Z	UNO	ACCZ (06h)	000110 00 0000000000000000 11100101	180000E5h
Read TEMP	DUE/UNO	TEMP (07h)	000111 00 0000000000000000 11100011	1C0000E3h
Read Summary Status	DUE/UNO	S_Sum (0Eh)	001110 00 0000000000000000 11010101	380000D5h
Read Rate Status 1	DUE/UNO	R_S1 (10h)	010000 00 0000000000000000 10010001	40000091h
Read Rate Status 2	DUE	R_S2 (11h)	010001 00 0000000000000000 10010111	44000097h
Read Accelerometer Status 1	UNO	A_S1 (12h)	010010 00 0000000000000000 10011101	4800009Dh
Read Common Status 1	DUE/UNO	C_S1 (14h)	010100 00 0000000000000000 10001001	50000089h
Read Common Status 2	DUE/UNO	C_S2 (15h)	010101 00 0000000000000000 10001111	5400008Fh

5.1.5 Return Status

SPI frame Return Status bits (RS bits) indicate the functional status of the sensor, see Return Status definitions in Table 16 and in Figure 12.

Table 16. Return Status definitions.

RS[1]	RS[0]	Description
0	0	Initialization running
0	1	Normal operation of selected channel
1	0	Selftest of selected channel ongoing or not started
1	1	Reserved or not existing register addressed, error of selected channel or common failure

The priority of the return status states is from high to low: 10 → 00 → 11 → 01.

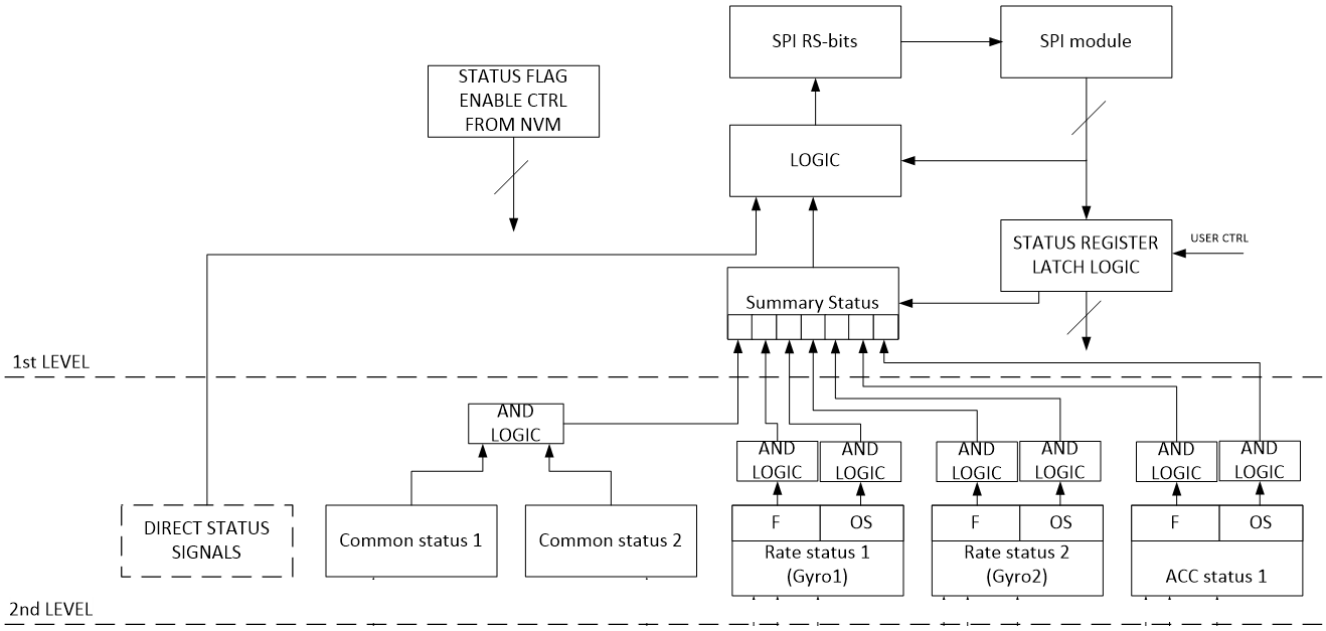


Figure 12. Return Status (RS) bits (in the 1st level) will be generated via logic from various sources in the 2nd level. The Rate status 2 (Gyro2) is a reserved option.

5.1.6 Checksum (CRC)

For SPI transmission error detection a Cyclic Redundancy Check (CRC) is implemented, for details see Table 17.

Table 17. SPI CRC definition.

Parameter	Value
Name	CRC-8
Width	8 bit
Poly	1Dh (generator polynom: X8+X4+X3+X2+1)
Init	FFh (initialization value)
XOR out	FFh (inversion of CRC result)

The CRC value used in system level software has to be initialized with FFh to ensure a CRC failure in case of stuck-at-0 and stuck-at-1 error on the SPI bus. C-programming language example for CRC calculation is presented in Figure 13. It can be used as is in an appropriate programming context.

```
// Calculate CRC for 24 MSB's of the 32 bit dword
// (8 LSB's are the CRC field and are not included in CRC calculation)
uint8_t CalculateCRC(uint32_t Data)
{
  uint8_t BitIndex;
  uint8_t BitValue;
  uint8_t CRC;

  CRC = 0xFF;
  for (BitIndex = 31; BitIndex > 7; BitIndex--)
  {
    BitValue = (uint8_t)((Data >> BitIndex) & 0x01);
    CRC = CRC8(BitValue, CRC);
  }
  CRC = (uint8_t)~CRC;
  return CRC;
}

static uint8_t CRC8(uint8_t BitValue, uint8_t CRC)
{
  uint8_t Temp;

  Temp = (uint8_t)(CRC & 0x80);
  if (BitValue == 0x01)
  {
    Temp ^= 0x80;
  }
  CRC <<= 1;
  if (Temp > 0)
  {
    CRC ^= 0x1D;
  }
  return CRC;
}
```

Figure 13. C-programming language example for CRC calculation.

CRC calculation example:
Read RATE register (01h) -> SPI[31:8] = 040000h -> CRC [7:0] -> F7h.
Further examples can be found in Table 15.

6 Register Definition

Table 18. Address space overview.

Reg (hex)	R/W (Due)	Register Name (Due)	R/W (Uno)	Register Name (Uno)
00h	N/A	Reserved	N/A	Reserved
01h	R	RATE_Z (Rz)	R	RATE_X (Rx)
02h	N/A	Reserved	N/A	Reserved
03h	R	RATE_Y (Ry)	N/A	Reserved
04h	N/A	Reserved	R	ACC_X (Ax)
05h	N/A	Reserved	R	ACC_Y (Ay)
06h	N/A	Reserved	R	ACC_Z (Az)
07h	R	TEMP	R	TEMP
08h	R	Reserved	N/A	Reserved
09h	R	Reserved	N/A	Reserved
0Ah	R	Reserved	N/A	Reserved
0Bh	R	RATE_Z2 (Rz2)	R	RATE_X2 (Rx2)
0Ch	N/A	Reserved	N/A	Reserved
0Dh	R	RATE_Y2 (Ry2)	N/A	Reserved
0Eh	R	S_Sum	R	S_Sum
0Fh	R/W	SCtrl	R/W	SCtrl
10h	R	R_S1	R	R_S1
11h	R	R_S2	R	R_S2
12h	R	A_S1	R	A_S1
13h	N/A	Reserved	N/A	Reserved
14h	R	C_S1	R	C_S1
15h	R	C_S2	R	C_S2
16h	R/W	G_FILT_DYN	R/W	G_FILT_DYN
17h	N/A	SYS_TEST	R/W	SYS_TEST
18h	R/W	ResCTRL	R/W	ResCTRL
19h	R/W	Mode	R/W	Mode
1Ah	N/A	Reserved	R/W	A_FILT_DYN
1Bh	R	C_ID	R	C_ID
1Ch	R	T_ID2	R	T_ID2
1Dh	R	T_ID0	R	T_ID0
1Eh	R	T_ID1	R	T_ID1
1Fh	R/W	SelBnk	R/W	SelBnk

R/W operation to Reserved registers sets RS bits to ‘11’. However, R/W to Factory Use Only registers does not normally set RS bits to ‘11’. User should not access to Factory Use Only Registers.

6.1 Sensor Data Block

Table 19. Sensor data block.

ASIC	Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
UNO	01h	[15:0]	RATE X	16	R	Rate output in 2's complement format
DUE	03h	[15:0]	RATE Y	16	R	Rate output in 2's complement format
DUE	01h	[15:0]	RATE Z	16	R	Rate output in 2's complement format
UNO	04h	[15:0]	ACC_X	16	R	X-axis 6g acceleration output in 2's complement format
UNO	05h	[15:0]	ACC_Y	16	R	Y-axis 6g acceleration output in 2's complement format
UNO	06h	[15:0]	ACC_Z	16	R	Z-axis 6g acceleration output in 2's complement format
DUE/UNO	07h	[15:0]	TEMP	16	R	Temperature sensor output in 2's complement format.

SPI read frames with CRC content for these registers are shown in Table 15.

6.1.1 Example of Angular Rate Data Conversion

For example, if RATE X register (01h) read results: RATE X = **05FFE08B**h, the register content is converted to angular rate as follows:

- 05h = 000001 01b
  - 000011b = operation code = Read RATE X
  - 01b = return status (RS bits) = no error
- FFE0h = 1111 1111 1110 0000b = RATE X register content
  - FFE0h in 2's complement format = -32d
  - Angular rate = -32LSB / sensitivity = -32LSB / (160LSB/(°/s)) = -0.2°/s
- 08h = CRC of 0DFFE0h

In case of 300dps version, resolution is 80LSB/(°/s)

6.1.2 Example of Acceleration Data Conversion

For example, if ACC_Z register read results: ACC_Z = **1900DC0E**h, the register content is converted to acceleration rate as follows:

- 19h = 000110 01b
  - 000110b = operation code = Read ACC_Z
  - 01b = return status (RS bits) = no error
- 00DCh = bin 0000 0000 1101 1100b = ACC_Z register content
  - 00DCh in 2's complement format = 220d
  - Acceleration = 220LSB / sensitivity = 220LSB / (4905LSB/g) = 0.049g
- 0Eh = CRC of 1900DCh

6.1.3 Example of Temperature Data Conversion

For example, if TEMP register read results: TEMP = **1DFE6F4E**h, the register content is converted to temperature as follows:

- 1Dh = bin 000111 01b
  - bin 000111b = operation code = Read TEMP
  - 01 = return status (RS bits) = no error
- FE6Fh = bin 1111 1110 0110 1111 = TEMP register content
  - FE6Fh in 2's complement format = -401d
  - Temperature = 25 + (TEMP / 30) = 25 + [-401/30] = +11.6°C
  - See section 2.5 for temperature conversion equation
- 4Eh = CRC of 1DFE6Fh

6.2 Sensor Status Block and Control

Table 20. Sensor status block and control.

Addr OP[4:0]	Bits	Register Name	No. of Bits	Read/ Write	Description
0Eh	[15:0]	S_Sum	16	R	Summary Status
0Fh	[15:0]	SCtrl	16	R/W	Safe control
10h	[15:0]	R_S1	16	R	Rate Status 1
11h	[15:0]	R_S2	16	R	Rate Status 2
12h	[15:0]	A_S1	16	R	Accelerometer Status 1
14h	[15:0]	C_S1	16	R	Common Status 1
15h	[15:0]	C_S2	16	R	Common Status 2
16h	[15:0]	G_FILT_DYN	16	R/W	Filter and dynamic control for RATE
18h	[15:0]	ResCtrl	16	R/W	Reset Control and EOI set
19h	[15:0]	Mode	16	R/W	Mode Register
1Ah	[15:0]	A_FILT_DYN	16	R/W	Filter and dynamic control for ACC

Note:
R/W for the register means, that the content of the register can be read, and that it is also possible to over write the content of the register in normal mode operation if EOI is 0. If EOI=1 only the reset bit b0 of ResCtrl register and SYS_TEST register can be written. The following signal blocks will then operate with the value written to the register. After a write cycle to the register, the register will keep its value until another write cycle or reset occurs.

SPI read and write frames with CRC content for these registers are shown in Table 15.

6.2.1 Summary Status Register (0Eh)

Table 21. Summary Status register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	S_OK_C	S_OK_Ry_F	S_OK_Ry_OS	S_OK_Rz_F	S_OK_Rz_OS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STUP_OK_Rz	STUP_OK_Ry
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	S_OK_C	Reserved	Reserved	S_OK_Rx_F	S_OK_Rx_OS	S_OK_Ax_F	S_OK_Ax_OS	Reserved	S_OK_Ay_F	S_OK_Ay_OS	Reserved	S_OK_Az_F	S_OK_Az_OS	Reserved	STUP_OK_Rx	Reserved

Summary Status register indicates saturation or failure in component. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 22. Summary Status register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	S_OK_C	-	S_OK_C	Status summary flag for common blocks
D14	-	S_OK_Ry_F	-	Reserved	Status summary flag for Ry (expect *OS)
D13	-	S_OK_Ry_OS	-	Reserved	Status summary of saturation flags for Ry
D12	-	S_OK_Rz_F	-	S_OK_Rx_F	Status summary flag for Rz/Rx (expect *OS)
D11	-	S_OK_Rz_OS	-	S_OK_Rx_OS	Status summary of saturation flags for Rz/Rx
D10	-	Reserved	-	S_OK_Ax_F	Status summary flag for Ax (expect *OS)
D9	-	Reserved	-	S_OK_Ax_OS	Status summary of saturation flags for Ax
D8	-	Reserved	-	Reserved	Reserved
D7	-	Reserved	-	S_OK_Ay_F	Status summary flag for Ay (expect *OS)
D6	-	Reserved	-	S_OK_Ay_OS	Status summary of saturation flags for Ay
D5	-	Reserved	-	Reserved	Reserved
D4	-	Reserved	-	S_OK_Az_F	Status summary flag for Az (expect *OS)
D3	-	Reserved	-	S_OK_Az_OS	Status summary of saturation flags for Az
D2	-	Reserved	-	Reserved	Reserved
D1	-	STUP_OK_Rz	-	STUP_OK_Rx	Status summary flag of startup functions for Rz/Rx
D0	-	STUP_OK_Ry	-	Reserved	Status summary flag of startup functions for Ry

6.2.2 Safe Control Register (0Fh)

Table 23. Safe Control register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	RATEsat[3:0]				Reserved				Stat_rmode	St_req_ccm	St_req_temp	St_req_Ry	St_req_Rz	Reserved	St_req_sys	Sat_mode
UNO	Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	RATEsat[3:0]				ACCsat[3:0]				Stat_rmode	St_req_ccm	St_req_temp	Reserved	St_req_Rx	St_req_ACC	St_req_sys	Sat_mode

Table 24. Safe Control register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	Yes	RATEsat[3:0]	Yes	RATEsat[3:0]	Saturation flag filtering of rate signals. User can set the counter value, which is used to filter short output saturation periods before post filter. Same control is used for all rate outputs. Time is between RATEsat x LSB and (RATEsat+1) x LSB. One counter LSB=32 x F_pri_period
D14	Yes		Yes		
D13	Yes		Yes		
D12	Yes		Yes		
D11	Yes	Reserved	Yes	ACCsat[3:0]	Saturation flag filtering of acceleration signals. User can set the counter value, which is used to filter short output saturation periods before post filter. Same control is used for all acceleration outputs. Time is between ACCsat x LSB and (ACCsat+1) x LSB. One counter LSB=32 x F_pri_period
D10	Yes		Yes		
D9	Yes		Yes		
D8	Yes		Yes		
D7	Yes	Stat_rmode	Yes	Stat_rmode	Status read mode 0 - Reading of Summary Status register "S_Sum" will clear all Bank0 status registers to 1 after delay of 36 x F_prim_period 1 - Reading of Summary Status register "S_Sum" will clear all Bank0 status registers to 1 without delay Note1: After reading of “S_Sum”, the delay of ≥ 2.5ms is required before “Stat_rmode” can be written 1 Note2: Reading other status register than S_Sum will clear the read status register to 1 without delay regardless of Stat_rmode value. Note3: 36 x F_prim_period is 2.02-2.28ms for UNO and 1.77-1.97ms for DUE in SCHA63T-K03.
D6	Yes	St_req_ccm	Yes	St_req_ccm	Request CCM self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.

D5	Yes	St_req_temp	Yes	St_req_temp	Request Temperature start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
D4	Yes	St_req_Ry	Yes	Reserved	Request Ry start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
D3	Yes	St_req_Rz	Yes	St_req_Rx	Request Rz/Rx start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
D2	Yes	Reserved	Yes	St_req_ACC	Request ACC channels start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
D1	Yes	St_req_sys	Yes	St_req_sys	Request system start-up self-test by writing this bit to '1'. Bit is set automatically to '0' when test is over.
D0	Yes	Sat_mode	Yes	Sat_mode	Saturation flag mode selection, common for all output data saturation flags: 0 - (default) Error flag is set when saturation occurs and it has to be acknowledged (SPI read) by user before setting saturation status to OK state. 1 - Error flag is set when saturation occurs and it is automatically removed when saturation does not occur anymore.

6.2.3 Rate Status 1 Register (10h)

Table 25. Rate Status 1 register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	OVS_ANAz_OK	OVS_DIGz_OK	CST_Rz_OK	GST_Rz_OK	PLL_OSC_FRz_OK	MON_VCMF_Rz_OK	MON_PRIz_FE_OK	MON_SECz_FE_OK	MON_DRV_Rz_OK	MON_AGC_Rz_OK	MON_QC_Rz_OK	MON_LPF_Rz_OK	Reserved	MEMS_INT_Rz_OK	Rz_PP_CRC_OK	Rz_PRI_OK
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	OVS_ANAx_OK	OVS_DIGx_OK	CST_Rx_OK	GST_Rx_OK	PLL_OSC_FRx_OK	MON_VCMF_Rx_OK	MON_PRIx_FE_OK	MON_SECx_FE_OK	MON_DRV_Rx_OK	MON_AGC_Rx_OK	MON_QC_Rx_OK	MON_LPF_Rx_OK	Reserved	MEMS_INT_Rx_OK	Rx_PP_CRC_OK	Rx_PRI_OK

Table 26. Rate Status 1 register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	OVS_ANAz_OK	-	OVS_ANAx_OK	Overflow Saturation status of Rz/Rx analog part (1 = OK)
D14	-	OVS_DIGz_OK	-	OVS_DIGx_OK	Overflow Saturation status of Rz/Rx digital part (1 = OK)
D13	-	CST_Rz_OK	-	CST_Rx_OK	Rz/Rx Continuous self-test ok (1 = OK)
D12	-	GST_Rz_OK	-	GST_Rx_OK	Rz/Rx Start-up self-test ok (1 = OK)
D11	-	PLL_OSC_FRz_OK	-	PLL_OSC_FRx_OK	Rz/Rx PLL frequency comparison to RC oscillator (1 = OK)
D10	-	MON_VCMF_Rz_OK	-	MON_VCMF_Rx_OK	CCM Monitoring: Rz/Rx VCMF ok (1 = OK)
D9	-	MON_PRIz_FE_OK	-	MON_PRIx_FE_OK	Rz/Rx primary front end ok (1 = OK)
D8	-	MON_SECz_FE_OK	-	MON_SECx_FE_OK	Rz/Rx secondary front end ok (1 = OK)
D7	-	MON_DRV_Rz_OK	-	MON_DRV_Rx_OK	CCM Monitoring: Rz/Rx drive path ok (1 = OK)
D6	-	MON_AGC_Rz_OK	-	MON_AGC_Rx_OK	CCM Monitoring: Rz/Rx AGC ok (1 = OK)
D5	-	MON_QC_Rz_OK	-	MON_QC_Rx_OK	CCM Monitoring: Rz/Rx quadrature compensation path ok (1 = OK)
D4	-	MON_LPF_Rz_OK	-	MON_LPF_Rx_OK	CCM Monitoring: Rz/Rx force-feedback path ok (1 = OK)
D3	-	Reserved	-	Reserved	Reserved
D2	-	MEMS_INT_Rz_OK	-	MEMS_INT_Rx_OK	Rz/Rx MEMS interface ok (1 = OK)
D1	-	Rz_PP_CRC_OK	-	Rx_PP_CRC_OK	Rz/Rx filter coefficient CRC status (1 = OK)
D0	-	Rz_PRI_OK	-	Rx_PRI_OK	Rz/Rx primary channel ok (1 = OK)

6.2.4 Rate Status 2 Register (11h)

Table 27. Rate Status 2 register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	OVS_ANAy_OK	OVS_DIGy_OK	CST_Ry_OK	GST_Ry_OK	PLL_OSC_FRy_OK	MON_VCMF_Ry_OK	MON_PRIy_FE_OK	MON_SECy_FE_OK	MON_DRV_Ry_OK	MON_AGC_Ry_OK	MON_QC_Ry_OK	MON_LPF_Ry_OK	Reserved	MEMS_INT_Ry_OK	DSP2_OK	Ry_PRI_OK
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 28. Rate Status 2 register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	OVS_ANAy_OK	-	Reserved	Overflow Saturation status of Ry analog part (1 = OK)
D14	-	OVS_DIGy_OK	-	Reserved	Overflow Saturation status of Ry digital part (1 = OK)
D13	-	CST_Ry_OK	-	Reserved	Ry Continuous self-test ok (1 = OK)
D12	-	GST_Ry_OK	-	Reserved	Ry Start-up self-test ok (1 = OK)
D11	-	PLL_OSC_FRy_OK	-	Reserved	Ry PLL frequency comparison to RC oscillator (1 = OK)
D10	-	MON_VCMF_Ry_OK	-	Reserved	CCM Monitoring: Ry VCMF ok (1 = OK)
D9	-	MON_PRIy_FE_OK	-	Reserved	Ry primary front end ok (1 = OK)
D8	-	MON_SECy_FE_OK	-	Reserved	Ry secondary front end ok (1 = OK)
D7	-	MON_DRV_Ry_OK	-	Reserved	CCM Monitoring: Ry drive path ok (1 = OK)
D6	-	MON_AGC_Ry_OK	-	Reserved	CCM Monitoring: Ry AGC ok (1 = OK)
D5	-	MON_QC_Ry_OK	-	Reserved	CCM Monitoring: Ry quadrature compensation path ok (1 = OK)
D4	-	MON_LPF_Ry_OK	-	Reserved	CCM Monitoring: Ry force-feedback path ok (1 = OK)
D3	-	Reserved	-	Reserved	Reserved
D2	-	MEMS_INT_Ry_OK	-	Reserved	Ry MEMS interface ok (1 = OK)
D1	-	DSP2_OK	-	Reserved	DSP 2 ok (1 = OK)
D0	-	Ry_PRI_OK	-	Reserved	Ry primary channel ok (1 = OK)

6.2.5 Accelerometer Status 1 Register (12h)

Table 29. Accelerometer Status 1 register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	OVS_ANA_Ax_OK	OVS_ANA_Ay_OK	OVS_ANA_Az_OK	OVS_DIG_Ax_OK	OVS_DIG_Ay_OK	OVS_DIG_Az_OK	Reserved	Reserved	Reserved	CST_Ax_OK	CST_Ay_OK	CST_Az_OK	ACC_PP_CRC_OK	STU_MD_STAT_OK	STAT_SD_ACC_OK	Reserved

Table 30. Accelerometer Status register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	Reserved	-	OVS_ANA_Ax_OK	Overflow Saturation status of Ax analog part (1 = OK)
D14	-	Reserved	-	OVS_ANA_Ay_OK	Overflow Saturation status of Ay analog part (1 = OK)
D13	-	Reserved	-	OVS_ANA_Az_OK	Overflow Saturation status of Az analog part (1 = OK)
D12	-	Reserved	-	OVS_DIG_Ax_OK	Overflow Saturation status of Ax digital part (1 = OK)
D11	-	Reserved	-	OVS_DIG_Ay_OK	Overflow Saturation status of Ay digital part (1 = OK)
D10	-	Reserved	-	OVS_DIG_Az_OK	Overflow Saturation status of AZ digital part (1 = OK)
D9	-	Reserved	-	Reserved	Reserved
D8	-	Reserved	-	Reserved	Reserved
D7	-	Reserved	-	Reserved	Reserved
D6	-	Reserved	-	CST_Ax_OK	Status of continuous self-test of Ax (1=OK)
D5	-	Reserved	-	CST_Ay_OK	Status of continuous self-test of Ay (1=OK)
D4	-	Reserved	-	CST_Az_OK	Status of continuous self-test of Az (1=OK)
D3	-	Reserved	-	ACC_PP_CRC_OK	ACC filter coefficient CRC status (1=OK)
D2	-	Reserved	-	STU_MD_STAT_OK	Status of ACC start-up mass deflection self-test (1=OK)
D1	-	Reserved	-	STAT_SD_ACC_OK	Status of ACC shield detection self-test (1=OK)
D0	-	Reserved	-	Reserved	Reserved

6.2.6 Common Status 1 Register (14h)

Table 31. Common Status 1 register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	EOI_state	STDIS_C	STDIS_Ry	STDIS_Rz	Reserved	BIST_DSP2_DONE	MCLK2_stat	Reserved	Reserved	Reserved	Nmode_OK	NVM_START_OK	HV_OK	CRC_SPI_OK	CRC_REG_OK	CRC_NVM_OK
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	EOI_state	STDIS_C	Reserved	STDIS_Rx	STDIS_A	BIST_DSP2_DONE	Reserved	Reserved	Reserved	Reserved	Nmode_OK	NVM_START_OK	HV_OK	CRC_SPI_OK	CRC_REG_OK	CRC_NVM_OK

Table 32. Common Status 1 register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	EOI_state	-	EOI_state	End of Initialization: Start-up sequence completed ok (1 = OK)
D14	-	STDIS_C	-	STDIS_C	All common start-up self-tests inactive/active (1 = inactive / 0 = active)
D13	-	STDIS_Ry	-	Reserved	Status of all Ry start-up self-tests: currently inactive/active (1 = inactive / 0 = active)
D12	-	STDIS_Rz	-	STDIS_Rx	Status of all Rz/Rx start-up self-tests: currently inactive/active (1 = inactive / 0 = active)
D11	-	Reserved	-	STDIS_A	All ACC start-up self-tests disabled/enabled (1 = disabled / 0 = enabled)
D10	-	BIST_DSP2_DONE	-	BIST_DSP2_DONE	Bist test of DSP2 done, valid only for DUE. Constant 1 in UNO.
D9	-	MCLK2_stat	-	Reserved	Comparison of PLL signals from gyro 1 and gyro 2.
D8	-	Reserved	-	Reserved	Reserved
D7	-	Reserved	-	Reserved	Reserved
D6	-	Reserved	-	Reserved	Reserved
D5	-	Nmode_OK	-	Nmode_OK	Normal mode OK (1 = normal mode; 0 = any test mode activated)
D4	-	NVM_START_OK	-	NVM_START_OK	NVM module OK (1 = OK)
D3	-	HV_OK	-	HV_OK	HV generator OK (1 = OK)
D2	-	CRC_SPI_OK	-	CRC_SPI_OK	SPI CRC comparison OK (1 = OK)
D1	-	CRC_REG_OK	-	CRC_REG_OK	Register map CRC OK (1 = OK)
D0	-	CRC_NVM_OK	-	CRC_NVM_OK	NVM CRC OK (1 = OK)

6.2.7 Common Status 2 Register (15h)

Table 33. Common Status 2 register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	MON_TEMP_OK	MON_FAIL_P_OK	MON_V3p3D_OK	MON_V3p3A_OK	MON_DVBG_OK	MON_FAIL_N_OK	MON_VDDD_OK	TEMP_ANA_OK	CCM_CAL_OK	Reserved	Reserved	Reserved	TEMP_CALC_OK	DSP1_CLOCK_OK	DSP1_OK	ST_STAT_TEMP
UNO	Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Name	MON_TEMP_OK	MON_FAIL_P_OK	MON_V3p3D_OK	MON_V3p3A_OK	MON_DVBG_OK	MON_FAIL_N_OK	MON_VDDD_OK	TEMP_ANA_OK	CCM_CAL_OK	Reserved	Reserved	Reserved	TEMP_CALC_OK	DSP1_CLOCK_OK	DSP1_OK	ST_STAT_TEMP

Table 34. Common Status 2 register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	MON_TEMP_OK	-	MON_TEMP_OK	CCM Monitoring: Temperature sensor OK (1 = OK)
D14	-	MON_FAIL_P_OK	-	MON_FAIL_P_OK	CCM Monitoring: FAIL_P OK (1 = OK)
D13	-	MON_V3p3D_OK	-	MON_V3p3D_OK	CCM Monitoring: V3p3D voltage supply OK (1 = OK)
D12	-	MON_V3p3A_OK	-	MON_V3p3A_OK	CCM Monitoring: V3p3A voltage supply OK (1 = OK)
D11	-	MON_DVBG_OK	-	MON_DVBG_OK	CCM Monitoring: DVBG OK (1 = OK)
D10	-	MON_FAIL_N_OK	-	MON_FAIL_N_OK	CCM Monitoring: FAIL_N OK (1 = OK)
D9	-	MON_VDDD_OK	-	MON_VDDD_OK	CCM Monitoring: VDDD OK (1 = OK)
D8	-	TEMP_ANA_OK	-	TEMP_ANA_OK	Temperature analog data path ok (1 = OK)
D7	-	CCM_CAL_OK	-	CCM_CAL_OK	CCM internal monitoring OK (1 = OK)
D6	-	Reserved	-	Reserved	
D5	-	Reserved	-	Reserved	
D4	-	Reserved	-	Reserved	
D3	-	TEMP_CALC_OK	-	TEMP_CALC_OK	Ok status of temperature calculations (1=OK)
D2	-	DSP1_CLOCK_OK	-	DSP1_CLOCK_OK	DSP1 clock OK (1 = OK)
D1	-	DSP1_OK	-	DSP1_OK	DSP1 OK (1 = OK)
D0	-	ST_STAT_TEMP	-	ST_STAT_TEMP	Status of Temperature start-up self-test (1=OK)

6.2.8 Gyro filter control (16h)

Table 35. Gyro filter and dynamic control register

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved	Rz2_DYN	Rz2_FILT[2]	Rz2_FILT[1]	Rz2_FILT[0]	Rz_FILT[2]	Rz_FILT[1]	Rz_FILT[0]	Reserved	Ry2_DYN	Ry2_FILT[2]	Ry2_FILT[1]	Ry2_FILT[0]	Ry_FILT[2]	Ry_FILT[1]	Ry_FILT[0]
UNO	Write	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved	Rx2_DYN	Rx2_FILT[2]	Rx2_FILT[1]	Rx2_FILT[0]	Rx_FILT[2]	Rx_FILT[1]	Rx_FILT[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 36. Gyro filter and dynamic control register description for Uno.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	Reserved	-	Reserved	
D14	Yes	Rz2_DYN	Yes	Rx2_DYN	Rz2/Rx2 output dynamic range selection 0 - nominal dynamic range (default dynamic range is 204.8dps in 125dps version and 409.6dps in 300dps version) 1 - nominal dynamic range divided by 2 (dynamic range is half than above) It's shift option after post filter (only digital gain). LSB step is half and quantization noise is half.
D13	Yes	Rz2_FILT[2]	Yes	Rx2_FILT[2]	Rz2/Rx2 filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended) 1xx - 300Hz 3rd order filter
D12	Yes	Rz2_FILT[1]	Yes	Rx2_FILT[1]	
D11	Yes	Rz2_FILT[0]	Yes	Rx2_FILT[0]	
D10	Yes	Rz_FILT[2]	Yes	Rx_FILT[2]	Rz/Rx filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended) 1xx - 300Hz 3rd order filter
D9	Yes	Rz_FILT[1]	Yes	Rx_FILT[1]	
D8	Yes	Rz_FILT[0]	Yes	Rx_FILT[0]	
D7	-	Reserved	-	Reserved	

D6	Yes	Ry2_DYN	Yes	Reserved	Ry2 output dynamic range selection 0 - nominal dynamic range (default dynamic range is 204.8dps in 125dps version and 409.6dps in 300dps version) 1 - nominal dynamic range divided by 2 (dynamic range is half than above) It's shift option after post filter (only digital gain). LSB step is half and quantization noise is half.
D5	Yes	Ry2_FILT[2]	Yes	Reserved	Ry2 filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended) 1xx - 300Hz 3rd order filter
D4	Yes	Ry2_FILT[1]	Yes	Reserved	
D3	Yes	Ry2_FILT[0]	Yes	Reserved	
D2	Yes	Ry_FILT[2]	Yes	Reserved	Ry filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter (not recommended) 1xx - 300Hz 3rd order filter
D1	Yes	Ry_FILT[1]	Yes	Reserved	
D0	Yes	Ry_FILT[0]	Yes	Reserved	

6.2.9 SYS_TEST Register (17h)

16bit read/write register which can be used to check the accessibility of the device or if multiple devices are connected to the SPI bus, to check if the SC signals are working properly. 17h register is not locked by EOI bit.

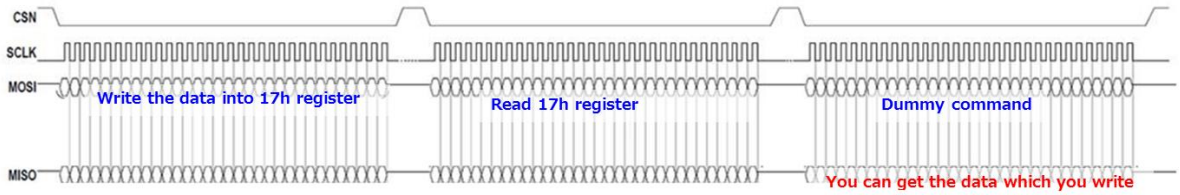


Figure 14 Test register operation

6.2.10 Reset Control Register (18h)

Table 37. Reset Control register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	-	-	-	-	-	-	-	-	-	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved										TDEL_CTRL[1]	TDEL_CTRL[0]	Reserved	Reserved	EOI	HardReset
UNO	Write	-	-	-	-	-	-	-	-	-	-	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved										TDEL_CTRL[1]	TDEL_CTRL[0]	Reserved	Reserved	EOI	HardReset

Table 38. Reset control register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	Reserved	-	Reserved	
D14	-		-		
D13	-		-		
D12	-		-		
D11	-		-		
D10	-		-		

D9	-		-		
D8	-		-		
D7	-		-		
D6	-		-		
D5	Yes	TDEL_CTRL[1]	Yes	TDEL_CTRL[1]	S_Sum TDEL (if Stat_rmode=0 in 0F'h register): 00 [1.7...2.4ms] 01 [0.7...1.0ms] 10 [0.3...0.5ms] 11 [0.089...0.123ms] Note: TDEL is started by read of S_Sum. If detailed status registers are read after S_Sum read, they need to be read during TDEL time, otherwise the failure information is lost.
D4	Yes	TDEL_CTRL[0]	Yes	TDEL_CTRL[0]	
D3	Yes	Reserved	Yes	Reserved	Write zero.
D2	Yes	Reserved	Yes	Reserved	
D1	Yes	EOI	Yes	EOI	**End of Initialization**, lock all R/W registers (expect Hardreset bit in this register) and SYS_TEST register(17h), reset needed to set EOI=0 This bit can be set/written to '1' only if all start-up self-tests have been completed. 1 - Normal operation 0 - Initiliazation state, SPI RS cannot be 01 (normal operation)
D0	Yes	HardReset	Yes	HardReset	Writing this bit to '1' **resets** the ASIC, and the bit will be set automatically to zero

6.2.11 Mode Register (19h)

Table 39. Mode register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved	Reserved	OP_MODE	Dis_Ry	Dis_Rz	Reserved	Dis_ACCT	Dis_CST_Ry	Dis_CST_Rz	Miso_SR	Unlock_ASM[2:0]			Stat_ASM[2:0]		
UNO	Write	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Dis_CST_ACC	Reserved	OP_MODE	Reserved	Dis_Rx	Dis_ACC	Dis_ACCT	Reserved	Dis_CST_Rx	Miso_SR	Unlock_ASM[2:0]			Stat_ASM[2:0]		

Table 40. Mode register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	Yes	Reserved	Yes	Dis_CST_ACC	Disable CST of ACC channel (1 = disable, not useful with EOI function) * In case of disable, offset and sensitivity shift in Az are visible
D14	Yes	Reserved	Yes	Reserved	
D13	Yes	OP_MODE	Yes	OP_MODE	Operation modes: 1 - Low power mode (Default after reset) 0 - Normal operation mode
D12	Yes	Dis_Ry	Yes	Reserved	Disable Z-Gyro (1 = disable, not useful with EOI function)
D11	Yes	Dis_Rz	Yes	Dis_Rx	Disable X-Gyro (1 = disable, not useful with EOI function)
D10	Yes	Reserved	Yes	Dis_ACC	Disable accelerometer (1 = disable, not useful with EOI function)
D9	Yes	Dis_ACCT	Yes	Dis_ACCT	Disable accelerometer and temp sensor (1 = disable, not useful with EOI function)
D8	Yes	Dis_CST_Ry	Yes	Reserved	Disable CST of Ry
D7	Yes	Dis_CST_Rz	Yes	Dis_CST_Rx	Disable CST of Rz/Rx
D6	Yes	Miso_SR	Yes	Miso_SR	MISO slew rate control 0 - CMISO 10...85pF, default 1 - CMISO 70...200pF
D5	Yes	Unlock_ASM[2:0]	Yes	Unlock_ASM[2:0]	Unlock the ASIC State Machine: needed write codes to open test mode: Unlock_ASM[2:0] = 010; Unlock_ASM[2:0] = 001; Unlock_ASM[2:0] = 100;
D4	Yes		Yes		

D3	Yes		Yes		Once this sequence has been written the ASIC enters into the test mode.
D2	Yes	Stat_ASM[2:0]	Yes	Stat_ASM[2:0]	Status of ASIC State Machine (read of bits is needed always after writing new Unlock_ASM code): 000=> no or invalid activation code received 010=> activation code 010 accepted 011=> activation code 001 accepted 111=> activation code 100 accepted All test registers are now writeable. Only way to lock the test registers again is to do the Power On Reset.
D1	Yes		Yes		
D0	Yes		Yes		

6.2.12 ACC filter control (1Ah)

Table 41 ACC filter and dynamic control register.

ASIC	Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DUE	Write	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
UNO	Write	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Name	Reserved	Reserved	Reserved	Reserved	Ax_DYN	Ax_FILT[2]	Ax_FILT[1]	Ax_FILT[0]	Ay_DYN	Ay_FILT[2]	Ay_FILT[1]	Ay_FILT[0]	Az_DYN	Az_FILT[2]	Az_FILT[1]	Az_FILT[0]

Table 42 ACC filter and dynamic control register bit description.

ASIC	DUE		UNO		Description
Bit	Write	Name	Write	Name	
D15	-	Reserved	-	Reserved	
D14	Yes	Reserved	Yes	Reserved	
D13	Yes	Reserved	Yes	Reserved	
D12	Yes	Reserved	Yes	Reserved	
D11	Yes	Reserved	Yes	Ax_DYN	Ax output dynamic range selection 0 - nominal dynamic range (default dynamic range 6.7g, default measurement range 6g) 1 - nominal dynamic range divided by 4 (dynamic range is 1/4 than above) It's shift option after post filter (only digital gain). LSB step is 1/4 and quantization noise is 1/4.
D10	Yes	Reserved	Yes	Ax_FILT[2]	Ax filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
D9	Yes	Reserved	Yes	Ax_FILT[1]	
D8	Yes	Reserved	Yes	Ax_FILT[0]	
D7	Yes	Reserved	Yes	Ay_DYN	Ay output dynamic range selection 0 - nominal dynamic range (default dynamic range 6.7g, default measurement range 6g) 1 - nominal dynamic range divided by 4 (dynamic range is 1/4 than above) It's shift option after post filter (only digital gain). LSB step is 1/4 and quantization noise is 1/4.
D6	Yes	Reserved	Yes	Ay_FILT[2]	Ay filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter
D5	Yes	Reserved	Yes	Ay_FILT[1]	

D4	Yes	Reserved	Yes	Ay_FILT[0]	011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
D3	Yes	Reserved	Yes	Az_DYN	Az output dynamic range selection 0 - nominal dynamic range (default dynamic range 6.7g, default measurement range 6g) 1 - nominal dynamic range divided by 4 (dynamic range is 1/4 than above) It's shift option after post filter (only digital gain). LSB step is 1/4 and quantization noise is 1/4.
D2	Yes	Reserved	Yes	Az_FILT[2]	Az filter selection 000 - 13Hz 3rd order filter 001 - 20Hz 3rd order filter 010 - 46Hz 3rd order filter 011 - 200Hz 3rd order filter 1xx - 300Hz 3rd order filter
D1	Yes	Reserved	Yes	Az_FILT[1]	
D0	Yes	Reserved	Yes	Az_FILT[0]	

6.2.13 Component ID Register (1Bh)

Table 43 Component ID 1 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
CID[15]	CID[14]	CID[13]	CID[12]	CID[11]	CID[10]	CID[9]	CID[8]	CID[7]	CID[6]	CID[5]	CID[4]	CID[3]	CID[2]	CID[1]	CID[0]	Read

6.2.14 Traceability 2 Register (1Ch)

Table 44 Traceability 2 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
Reserved	Reserved	Reserved	Reserved	TID2[3]	TID2[2]	TID2[1]	TID2[0]	ASIC_type[1]	ASIC_type[0]	ASIC_ver[2]	ASIC_ver[1]	ASIC_ver[0]	Reserved	Reserved	Reserved	Read

ASIC_type[1:0]

- 01 - UNO ASIC
- 10 - DUE ASIC

ASIC_ver[2:0]

- 001 - ASIC ver1
- 010 - ASIC ver2

6.2.15 Traceability 0 Register (1Dh)

Table 45 Traceability 0 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
TID0[15]	TID0[14]	TID0[13]	TID0[12]	TID0[11]	TID0[10]	TID0[9]	TID0[8]	TID0[7]	TID0[6]	TID0[5]	TID0[4]	TID0[3]	TID0[2]	TID0[1]	TID0[0]	Read

6.2.16 Traceability 1 Register (1Eh)

Table 46 Traceability 1 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bit
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Write
TID1[15]	TID1[14]	TID1[13]	TID1[12]	TID1[11]	TID1[10]	TID1[9]	TID1[8]	TID1[7]	TID1[6]	TID1[5]	TID1[4]	TID1[3]	TID1[2]	TID1[1]	TID1[0]	Read

The SMD component shall be traceable by a unique electronically readable serial number.
Serial number string format : **DDDYYFHHHHH00**

DDD : Production day as decimal value (1..366)
YY : Production year as decimal value (18..99)
F : Hexadecimal running number, or F can be used for FAB coding
HHHH : Hexadecimal running number
H00 : Fixed code for SCHA63T-K03 product family

Serial number is stored in NVM registers 1Ch, 1Eh, 1Dh.

H00 is a fixed ending and not therefore not stored to NVM

1Ch [11:8] (ID_1) -> F (4bit hex to string, 0...F)
Example : 0000
therefore 0

1Dh [15:0] (ID_0) -> HHHH (16bit hex to string, 0000...FFFF)
Example : 0001 0100 1001 0111
0001 = 1
0100 = 4
1001 = 9
0111 = 7
therefore1497

1Eh [15:0] (ID_2) -> DDDYY (16 unsigned integer to decimal string, 0....65535)
Example : 1000 1010 0101 1001
therefore 35417

Serial number result is 3541701497H00

7 Application information

7.1 Application Circuitry and External Component Characteristics

See Figure 15 and Table 47 for specification of the external components.

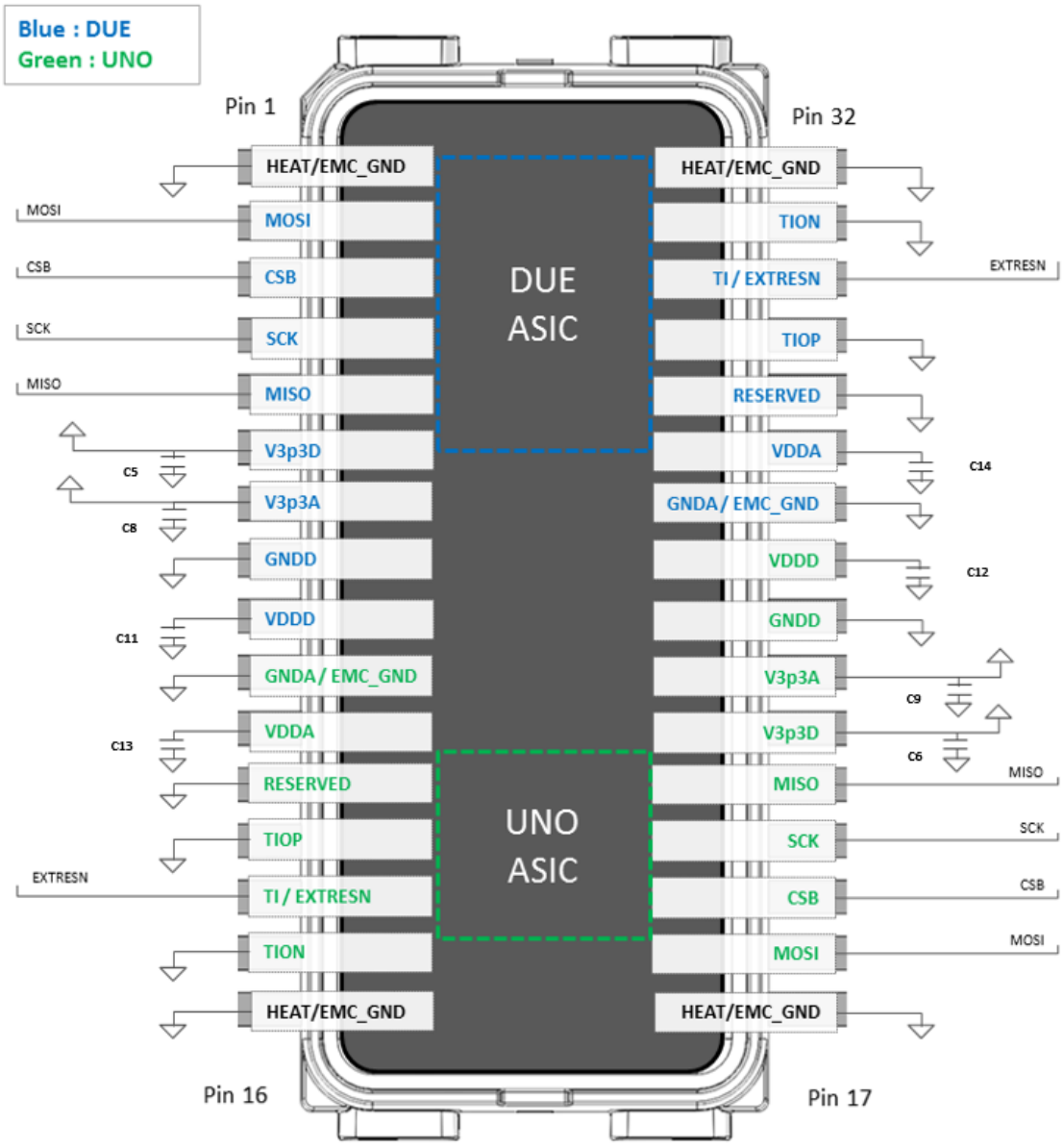


Figure 15. Application schematic.

Table 47. External component description for SCHA63T-K03.

Symbol	Description	Min.	Nom.	Max.	Unit
C5 C6	Decoupling capacitor between V3p3D and GNDD (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF
C8 C9	Decoupling capacitor between V3p3A and GNDA (ESR <100mOhm @ 1 MHz)	70	100	130	nF
C11 C12	Decoupling capacitor between VDDD and GNDD (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF
C13 C14	Decoupling capacitor between VDDA and GNDA (ESR <100mOhm @ 1 MHz)	0.7	1	1.3	uF

7.2 General Application PCB layout

See below figure and notification for example e.g. 1 SPI connection save PCB space or 2 SPI connection provide system redundancy.

- Connect SMD decoupling capacitors right next to the component on top layer
- Locate a solid ground plate under component. Each ground pin should be connected to the ground directly.
- Only signal lines of this component (SCHA6xx series), can be routed under the component on top layer if signals are read out with recommended. sampling rate. See more details in chapter 10 SPI crosstalk optimization
- Individual analog and digital power supply lines with individual decoupling capacitors are recommended. In case of one power lines, connect star shaped separation at the point between regulated power supply and decoupling capacitors to power line. Note! layout example below is not star shaped.
- Keep all routing as low resistance as possible.

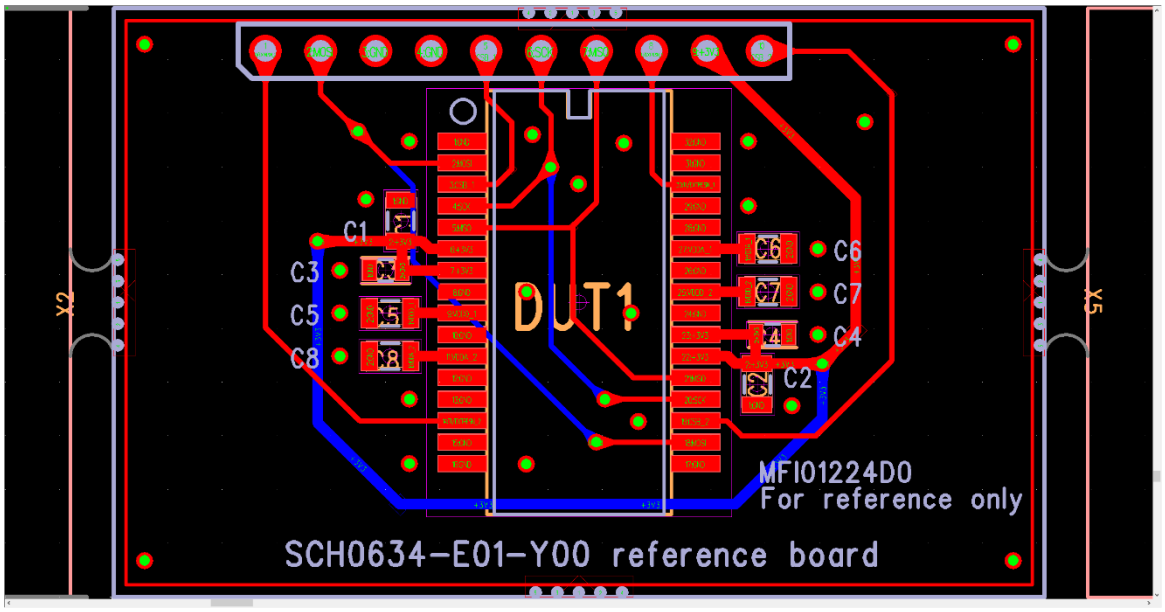


Figure 16 general application PCB layout example (1 SPI interface)

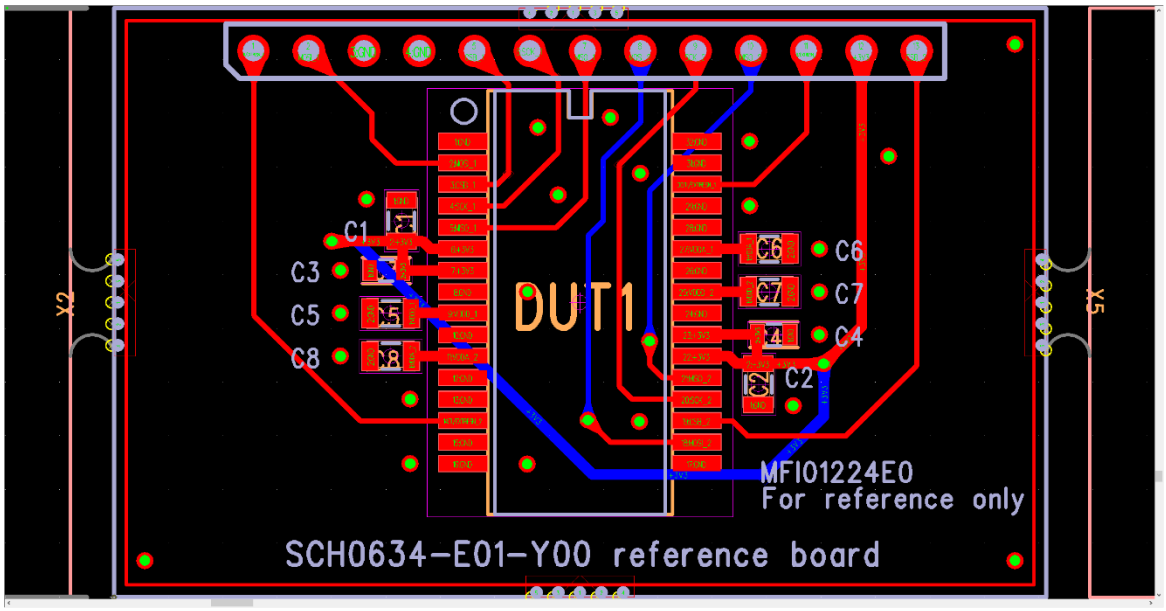


Figure 17 general application PCB layout example (2 SPI interface)

8 Assembly Instructions

The coating material and coating process used should be validated. For additional assembly related details please refer to “Technical Note 96” for assembly instructions: Assembly instructions for SCHA63T-K03 ENG.pdf

9 Known Bugs

ASIC	Version	Bug	Workaround

10 Electrical and mechanical robustness

10.1 SPI Crosstalk Optimization

Table 48: Recommended sampling frequency

Frequency (kHz)	Tolerance (Hz)
2.58	+/-26
3.01	+/-30
3.61	+/-36
4.51	+/-45
6.02	+/-60

The digital SPI communication may interfere with the angular rate signal due to the electrical coupling inside the component. The coupling is depending on the used SPI parameters like the external sample rate for used reading the sensor signals and the duty cycle (1 in SPI communication. The Figure 18: SPI Crosstalk Effect shows the RMS noise (y-axis) when sweeping the SPI data rate (x-axis). The primary frequency of the tested MEMS was 19.558 kHz and the critical sample rate are shown in Table 49: SPI Crosstalk vs Harmonics.

Table 49: SPI Crosstalk vs Harmonics

Harmonic	Frequency (Hz)
F_PRIM	19558
F_PRIM div 2	9779
F_PRIM div 3	6519
F_PRIM div 4	4889
F_PRIM div 5	3912
F_PRIM div 6	3260
F_PRIM div 7	2794
F_PRIM div 8	2445
F_PRIM div 9	2173
F_PRIM div 10	1956

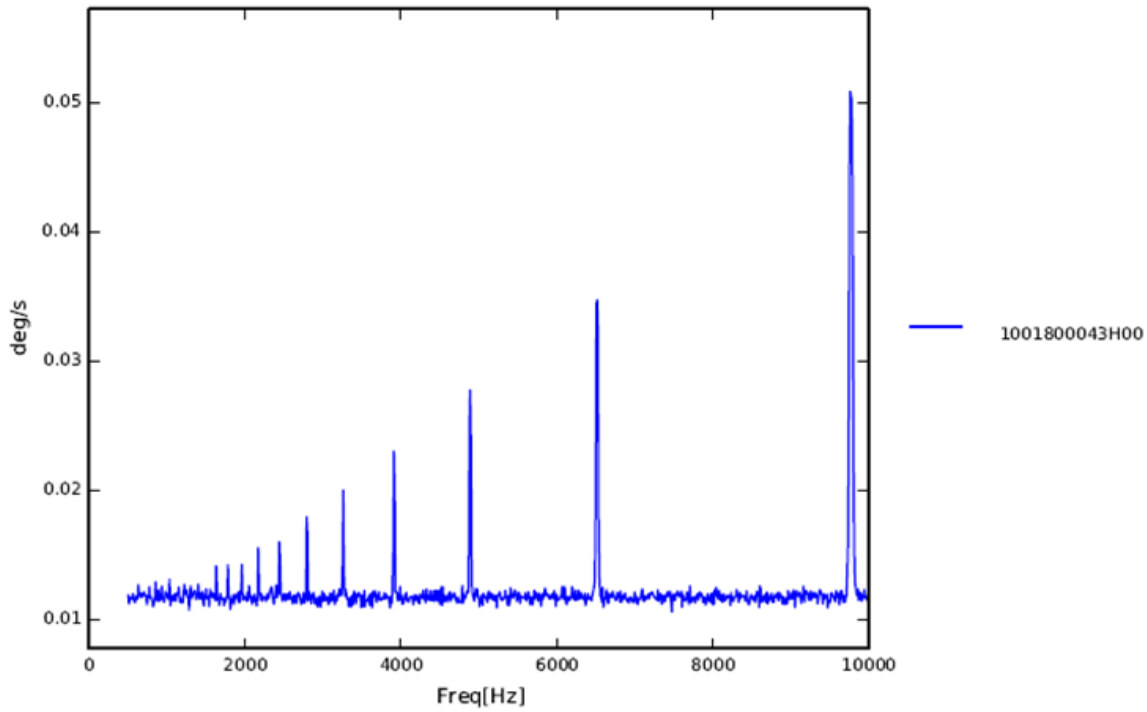


Figure 18: SPI Crosstalk Effect

Typically the sample rates are varying from some hundred Hz to several kHz depending on the application requirements. The harmonic tones of SPI sample frequency can hit to the MEMS primary frequency and cannot be filtered from the real input signal if the tones are in the measurement bandwidth.

The critical frequency ranges for MEMS Gyros in SCHA63T-K03 are

MEMS	F_PRIM_min (kHz)	F_PRIM_typ (kHz)	F_PRIM_max (kHz)
Z-gyro	18.3	19.3	20.3
X and Y -gyro	15.8	16.8	17.8

In order to reduce the SPI effect the sample rates and/or duty cycles should be chosen based on the Table 50: Optimized SPI parameters for reducing SPI crosstalk. For example, by choosing the sample rate 3.01 kHz it means that the 5th, 6th and 7th harmonics are not hitting the primary frequency range of the used MEMS elements. In addition, by choosing the duty cycle of 16.7 % for fs=3.01 kHz the contribution of the 6th harmonic can be minimized.

The variation of the sample frequency should be < 1 % not to overlap with primary frequency range, for example (1+1%)*3.01=18.2 kHz < 18.3 kHz (minimum RATE_Z F_PRIM)

Table 50: Optimized SPI parameters for reducing SPI crosstalk.

	Harmonic							
fs (kHz)	2	3	4	5	6	7	8	
	50.0	33.3	25.0	20.0	16.7	14.3	12.5	Duty Cycle (%)
9.03	18.05							
6.02	12.03	18.05	24.07					
4.51		13.54	18.05	22.56				
3.61			14.44	18.05	21.66			
3.01				15.04	18.05	21.06		
2.58					15.47	18.05	20.63	

Notes:
1) Duty cycle means CSB low time vs whole sampling duration

Duty Cycle = CSB active time (low) / sampling period

10.2 Mechanical robustness

Component is sensitive to acoustic disturbance especially in range of F_prim because of MEMS resonance. Customer need to evaluate these effect in system operation. See also assemble instruction.