GaAs FET Device and Circuit Simulation in SPICE

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Abstract—**We have developed a GaAs FET model suitable for SPICE circuit simulations. The dc equations are accurate to about 1 percent of the maximum drain current. A simple but accurate interpolation formula for drain current as a function of gate-to-source voltage connects the square-law behavior just above pinchoff and the square-root law for larger values of the drain current.**

The ac equations, with charge-storage elements, describe the variation of the gate-to-source and gate-to-drain capacitances as the drain-to-source voltage approaches zero and when this voltage becomes negative. Under normal operating conditions the gate-to-source capacitance is much larger than the gate-to-drain capacitance. At zero drain-to-source voltage both capacitances are about equal. For negative drain-to-source voltages the original source acts like a drain and vice versa. Consequently the normally large gate-to-source capacitance becomes small and acts like a gate-to-drain capacitance. In order to model these effects it is necessary to realize that, contrary to conventional SPICE usage, there are no separate gate-to-source and gate-to-drain charges, but that there is only one gate charge which is a function of gate-to-source and gate-to-drain voltages. The present treatment of these capacitances permits simulations in which the drain-to-source voltage reverses polarity, as occurs in pass-gate circuits.

I. Introduction

IN ANY INTEGRATED circuit design one usually starts with a computer simulation of the circuit to be built. If the circuit consists of not more than a few hundred devices then the well-known program SPICE, originally developed at the University of California, Berkeley, is often used. While SPICE can model transistors at different levels of complexity and usually gives answers with great reliability, it was written originally for silicon devices only. In principle, the physics of Si junction FET's is very similar to GaAs FET's. Some of the differences are that in GaAs one usually deals with a Schottky-barrier junction instead of a p–n junction, and also in GaAs the conducting channel is confined on one side by a space-charge region and on the other side by a semi-insulating region. In Si the channel is usually, but not always, constricted from both sides by space-charge regions formed around the gate p–n junctions. Thus one might expect that both types of devices could be modeled by the same equations. This unfortunately cannot be done. The physical reason for this dissimilarity lies in the fact that in GaAs the electron velocity saturates near the rather low electric field of 3×10^3 V/cm whereas Si obeys ohmic behavior over a range approximately ten times larger. Thus in GaAs the saturation of drain current with increasing drain-to-source voltage is caused by carrier-velocity saturation, whereas in silicon it is channel pinchoff that causes the drain current to saturate.

The equations derived at this laboratory in [1] and [2] are rather accurate and generally more accurate than those used in the SPICE program. However, the resulting expressions are very complex and would execute too slowly in a practically useful SPICE implementation. The challenge then presented to us consisted of finding simple expressions that execute quickly but at the same time are accurate enough to give reliable circuit simulations.

II. The DC Equations

Recently a publication appeared [3] in which the dc equations exclusive of parasitic resistances are approximated by

$$I_d = \beta(V_{gs} - V_T)^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}). \quad (1)$$

In this equation, I_d is the drain current, β is a parameter, V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source voltage, V_T is the threshold voltage, λ is a parameter related to drain conductance, and α determines the voltage at which the drain current characteristics saturate. Note that the drain current saturates at the same drain-to-source voltage irrespective of the gate-to-source voltage. This is different from conventional JFET or MOSFET models and occurs because the critical field E_{sat} in the channel is reached at approximately the same voltage $V_{ds} = E_{\text{sat}} \times L$, where L is the channel length. When comparing [1] against experiment, we found that the expression is a good representation of the current for a given V_{gs}. However, the behavior of I_d as a function of V_{gs} is only poorly represented, especially if the pinchoff voltage of the transistor is large. Our earlier work had shown that, except for V_{gs} near the pinchoff voltage, the saturated drain current I_{ds} is proportional to the height of the undepleted channel region near the source end. This is because the reduction in channel height between the channel entrance and the point where the carrier velocity saturates is usually a negligible fraction of the height at the entrance. Thus the current may be approximately calculated by assuming that all carriers at the channel opening are moving at their saturated velocity. For constant channel doping, the saturated drain current I_{ds} should then vary approximately as

$$I_{ds} = Z v_{\text{sat}} \sqrt{2\epsilon q N_d} \left(\sqrt{(-V_T + V_B)} - \sqrt{(-V_{gs} + V_B)}\right) \quad (2)$$

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where Z is the channel width, v_{sat} is the saturated electron velocity, ϵ is the dielectric constant, q is the electron charge, N_d is the donor density, V_T is the threshold or pinchoff voltage, and V_B is the built-in potential of the gate junctions. Note that V_{gs} and V_T are normally negative. The first term in (2) is proportional to the height of the space-charge region at the threshold voltage, and thus is proportional to the thickness of the doped region under the gate. The second term in (2) is proportional to the height of the space-charge region when the gate-to-source voltage V_{gs} is applied. Thus (2) is indeed proportional to the height of the undepleted channel.

The full (2) is obtained by assuming that all carriers in the channel opening move at their saturated velocity. The approximation for the current in (2) breaks down when the voltage drop from the entrance of the channel to the point of velocity saturation of the carriers is comparable to the voltage difference $V_{gs}-V_T$. Under these conditions the assumption of constant channel height breaks down. We may get an idea of the magnitude of this critical voltage by considering an example. Let us assume that we are dealing with an FET with a 1-μm channel length. Obviously the length under the channel where the carriers move at their unsaturated velocity has to be less than the total gate length. The electric field strength along the same portion of the channel has to be less than E_{sat} because the carriers are moving at less than saturated velocity. Thus an upper limit of the voltage drop along the channel, before the carriers become saturated, is $E_{sat}\,L$, where L is the total channel length. For the known value of E_{sat} of about 3×10^3 V/cm, the above critical voltage drop becomes 0.3 V or less. Hence, we thus expect that the above approximation in (2) is not valid when $|V_{gs} - V_T| \lesssim 0.3$ V. In the limit of gate voltages near the pinchoff point, the equations of [1] and [2] lead to a quadratic law

$$I_{ds} \sim \beta(V_{gs} - V_T)^2. \tag{3}$$

This situation is similar to what is found in the conventional JFET model. The derivation of (3) from the expressions in [1] and [2] is not shown here. Unfortunately, (3) is valid only near $V_{gs} - V_T = 0$. Elsewhere the behavior is better described by (2). To illustrate the theoretical expectations of [1] and [2], we have programmed the relevant equations on a computer and show in Fig. 1(a) and (b) I_{ds} versus V_{gs} for transistors with pinchoff voltages of -0.5 and -2.5 V, respectively. As may be seen, the curves start quadratically but soon change and follow more of a square-root-like behavior as exhibited by (2).

To smoothly connect a law like (3) for small $V_{gs} - V_T$ to an expression like (2) for larger $V_{gs} - V_T$, we chose the empirical expression

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)}. \tag{4}$$

For small values of $V_{gs} - V_T$, the expression is indeed quadratic while for larger values, I_{ds} becomes almost linear in $V_{gs} - V_T$. The denominator in (4) is new and it has not been used, to our knowledge, by the modeling community. Note that the expressions derived in [1] and [2] apply to a truly abrupt interface between the active layer and the undoped buffer. In Fig. 1(a) and (b) we show by a solid line a fit based on (4). The b values found are 2.6 and 1.5 V^{-1}, respectively. The situation becomes more complicated when one considers that in all practical devices there is a gradual transition in doping from the channel into the buffer caused by diffusion and/or implant-produced doping tails. Because of this diffuse channel edge, the depletion region quickly expands as the pinchoff point is approached. The transconductance at any one point is approximately inversely proportional to the distance between the gate and the channel edge. Real doping profiles then produce curves of I_{ds} versus V_{gs} which rise more gradually than calculated in [1] and [2]. Interestingly, we find that the empirical expression (4) still describes actual transistor characteristics exceptionally well, but with changed parameters β and b. The more gradual doping profiles appear to give a lower value of b. To illustrate this point, we show in Fig. 1(c) and (d) measured characteristics for both implanted devices and transistors made on epitaxial material. We find that (4) is accurate and the error is usually less than 1-percent of the maximum current. In Fig. 1(c) we depict a device made in MBE material, and (4) is seen to be a good approximation over most of the range. Fitting the expression (4) to experiment requires a value of $b = 0.45$ V^{-1}. Furthermore Fig. 1(c) shows $(I_d)^{1/2}$ rather than I_d to better illustrate the behavior at low drain currents. We also show the above discussed approximations based on (2) with the square-root law, and (3) using the square law. It is evident that the new model fits the data much better than either of the other two approximations alone. Transistors produced by our standard digital process are shown in Fig. 1(d). They use an implanted channel in conjunction with a recessing gate etch, and thus have a more gradual profile. Their b-value is about 0.3 (see Fig. 1(d)). The values quoted for b refer to a bare transistor without parasitic source and drain resistors. In extracting the characteristics of a bare transistor from measured ones, there is always some uncertainty about the values of the parasitic resistors, and the values of b reflect these uncertainties. Interestingly, (4) is rather forgiving, permitting good fits to transistor curves even when the parasitic resistors are not extracted. The values of β and b are, however, different in these cases.

The value of b of the bare transistor is a measure of the doping profile extending into the insulating substrate and thus depends on the fabrication process. Neglecting b cannot be tolerated in most circuit simulations.

We also found that the tanh function in (1) consumes considerable computer time. We further approximated the tanh function below saturation by a simple polynomial P of the form

$$P = 1 - \left(1 - \frac{\alpha V_{ds}}{n}\right)^n, \quad \text{with} \quad n = 2 \text{ or } 3. \tag{5}$$

In the saturated region ($V_{ds} > n/\alpha$), the tanh function is

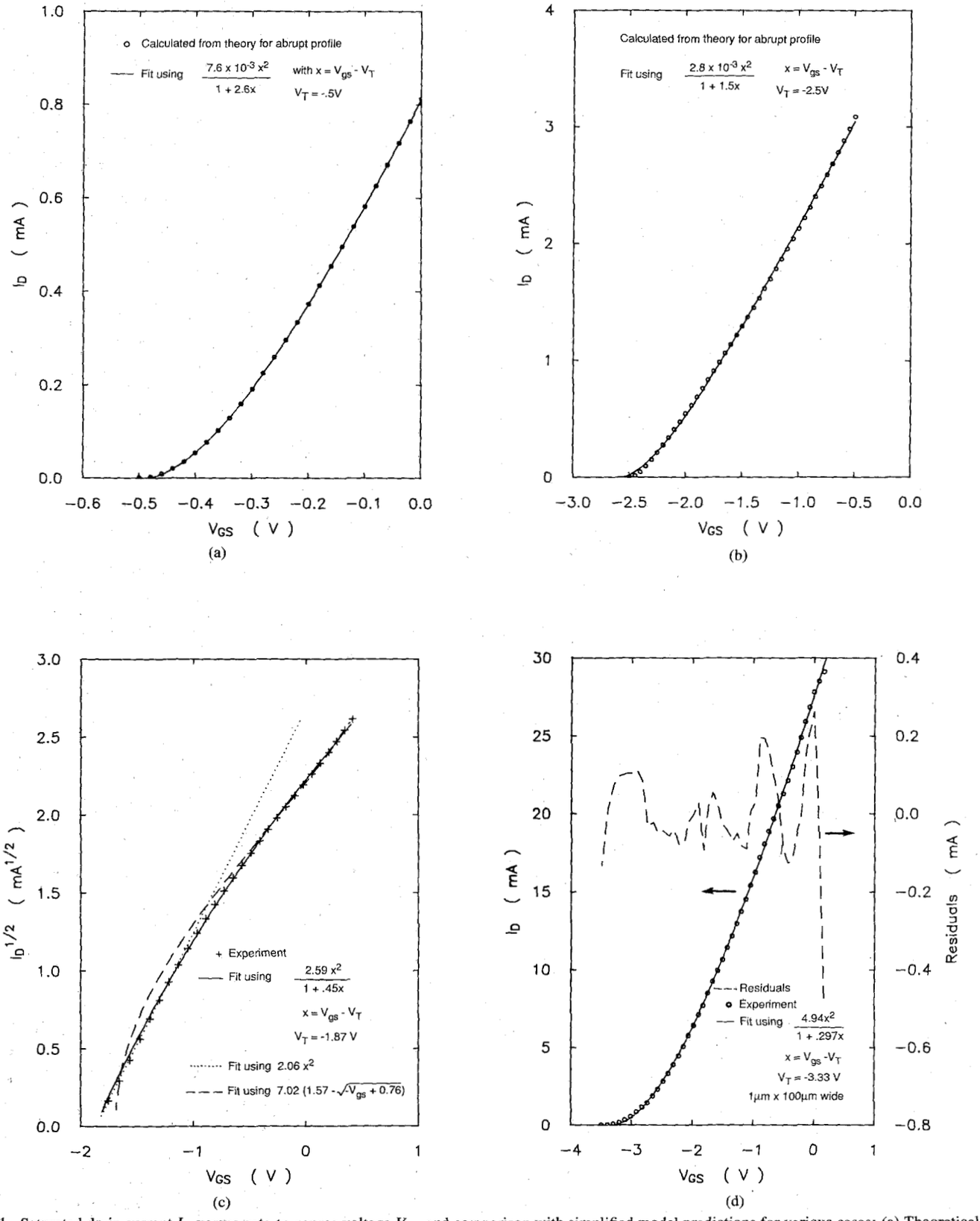

Fig. 1. Saturated drain current I_{ds} versus gate-to-source voltage V_{gs}, and comparison with simplified model predictions for various cases: (a) Theoretical characteristics for an abrupt profile with a pinchoff voltage of -0.5 V and a 1×20 μm gate. There are no parasitic source and drain resistors. (b) Same but with pinchoff voltage of -2.5 V. (c) Experimentally measured characteristics for a transistor with a 1×20 μm gate and a rather abrupt doping profile fabricated on MBE-grown epitaxial material. The plot also shows in addition the comparison with two other approximate models as explained in the text. We plot here $(I_d)^{1/2}$ instead of I_d to show more clearly the model comparisons in the low current region. The experimental curves represent a "bare" transistor without parasitic source and drain resistors. (d) Measured characteristics for an FET made by ion-implantation followed by a gate recessing etch. Gate dimensions are 1×100 μm. The curves have been corrected for source and drain resistors.

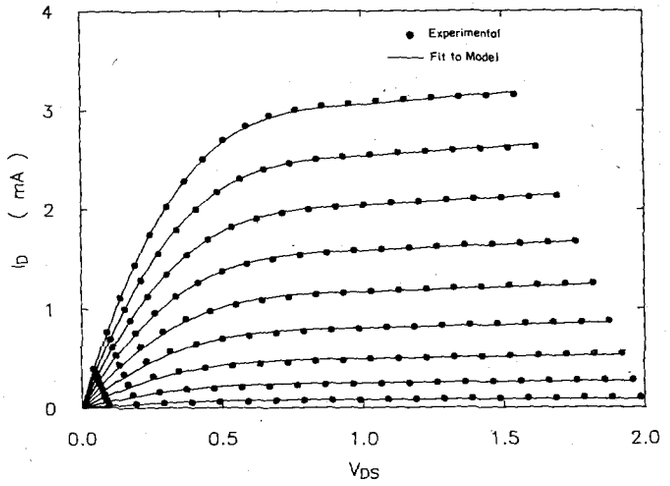

Fig. 2. Drain current I_d versus drain voltage V_{ds} for an experimental FET, and the approximation representing the polynomial model with $n \approx 3$.

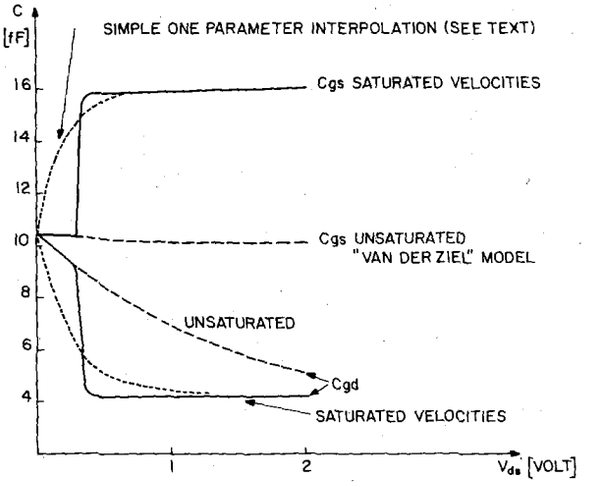

Fig. 3. Gate-to-source and gate-to-drain capacitances for a 1×20 μm gate on GaAs with 1×10^{17} donors/cm^3. The figure shows the unsaturated model of van der Ziel (long dashes), the saturated velocity model (solid lines), and a simple one-parameter interpolation (short dashes) as discussed in the text.

replaced by unity. This is similar to what is done in the conventional SPICE program.

The slope at $V_{ds} = 0$ of the polynomial is α and is equal to that of the $\tanh(\alpha V_{ds})$ function. While the tanh function and the two-section approximations with $n = 2$ or 3 all give good fits to experimentally measured curves, we found consistently that the polynomial with $n = 3$ gives the best fit. Note that for $n = 3$ the two-section function has first and second derivatives which are continuous for all $V_{ds} > 0$. In making comparisons with experiments, as in Fig. 2, the experimental curves are corrected for voltage drops across the parasitic resistors between source and gate as well as gate and drain. No allowance has been made for the fact that these resistors change as the gate-to-source voltage is varied, owing to the constriction of the current flow to and from the variable height channel.

In summary, we have modified the code in SPICE to include a GaAs model with the following dc equations:

$$I_d = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} \left\{1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right\} (1 + \lambda V_{ds}),$$

$$\text{for} \quad 0 < V_{ds} < \frac{3}{\alpha} \tag{6a}$$

$$I_d = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} (1 + \lambda V_{ds}),$$

$$\text{for} \quad V_{ds} \geq \frac{3}{\alpha}. \tag{6b}$$

III. Source and Drain Capacitance

Source and drain capacitance models have been considered in the literature [2], [6]–[9]. Current GaAs device simulations use a diode-like capacitance between source and gate, where the space-charge region thickness and thus the capacitance is determined by the gate-to-source voltage. A similar diode model is often used to describe the normally much smaller gate-to-drain capacitance. These approximations have serious shortcomings. Consider, for example, the case of zero source-to-drain voltage. From the symmetry of the physics of the FET one concludes that the gate-to-source and gate-to-drain capacitances should be equal, yet the above model says that they may be very different. Even worse inaccuracies are encountered when the transistor is reverse-biased, i.e., when the drain really acts like a source, and the source acts like a drain. Now the model says that the large capacitance is still between the original source and gate while in reality the big capacitance is now between the original drain and gate. Thus, large errors can be introduced into simulations when low source-to-drain voltages or reverse-biased transistors are encountered, as in transmission gate circuits.

While the above objections apply to both Si and GaAs devices, the behavior for GaAs is further complicated by the early onset of carrier-velocity saturation. Let us briefly review some of the underlying theory. Van der Ziel [6] calculated capacitances for FET's without including effects of velocity saturation. In Fig. 3 we show the unsaturated velocity values of C_{gs} and C_{gd} as a function of V_{ds} for $V_{gs} = 0$ V. The channel is assumed to have a doping of 1×10^{17} donors/cm^3 and the gate has dimensions of 1×20 μm with $V_B = 0.8$ V. It is seen that C_{gs} is approximately constant as a function of V_{ds}. While we have not shown the capacitance curves for V_{gs} not equal to zero, they follow approximately the diode capacitance model as a function of V_{gs}. This is presumably the basis for the diode-like behavior programmed into Si JFET devices. The gate-drain capacitance C_{gd} starts at the same value as C_{gs} for $V_{ds} = 0$. It then falls continuously with increasing V_{ds} and goes to zero when the drain side of the channel becomes pinched off.

When velocity saturation is taken into account, the situation changes drastically. In [2], the total junction capacitance between the gate and the rest of the device is

derived. These results can be readily extended to calculate C_{gs} and C_{gd} separately by taking the partial derivatives of the total gate charge with respect to gate–source and gate–drain potentials. For the convenience of the reader, we summarize these capacitance expressions in the Appendix, including those previously unpublished. Evaluating the resulting saturated velocity expressions gives a gate-to-source capacitance that rises rather abruptly from the van der Ziel model at the onset of saturation and quickly approaches a nearly constant value as a function of V_{ds}. Similarly the gate-to-drain capacitance drops abruptly to a low value and then stays approximately constant. In reality one may expect that the transition to the saturated velocity capacitance model is not quite as abrupt because the onset of velocity saturation of the carrier is also more gradual. There are almost no published data on C_{gs} and C_{gd} for GaAs FET's. However, the few data available indicate qualitative agreement with these models.

An additional problem is encountered in the SPICE code. The integration routines require from the device model separate closed-form expressions for the source-to-gate charge and gate-to-drain charge. These charges are used in the program to calculate displacement currents due to finite voltage steps. For these displacement currents, the absolute values of the charges are immaterial but their changes are of importance. Since in the real device there are no separate gate–drain or gate–source charges but only one gate charge, which is a function of V_{gs} and V_{gd}, we choose to set the initial values of each of these charges in the code, during a simulation, to half of the total gate charge Q_g. Each charge is then incremented when the voltage levels change. In the case of the gate-to-source charge Q_{gs} we take

$$\Delta Q_{gs} = Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) - Q_g(V_{gs}, V_{gd}). \tag{7a}$$

This formula may be generalized if simultaneously both voltages V_{gs} and V_{gd} change by ΔV_{gs} and ΔV_{gd} by averaging (7a) over the two values of V_{gd}.

$$\begin{aligned}\Delta Q_{gs} = \tfrac{1}{2}\,(&Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) \\ &- Q_g(V_{gs}, V_{gd} + \Delta V_{gd}) \\ &+ Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) \\ &- Q_g(V_{gs}, V_{gd})).\end{aligned} \tag{7b}$$

This definition for the gate–source charge is somewhat artificial, but the displacement currents calculated from the above expressions should be rather accurate. An analogous equation can be written down for ΔQ_{gd}

$$\begin{aligned}\Delta Q_{gd} = \tfrac{1}{2}\,(&Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) \\ &- Q_g(V_{gs} + \Delta V_{gs}, V_{gd}) \\ &+ Q_g(V_{gs}, V_{gd} + \Delta V_{gd}) \\ &- Q_g(V_{gs}, V_{gd})).\end{aligned} \tag{7c}$$

Equations (7b) and (7c) are still approximations, albeit very good ones. However, note that the total gate-charge changes are calculated exactly. This may be seen by calculating, with the help of (7b) and (7c), the total change ΔQ_g in the gate charge due to a simultaneous voltage change in both V_{gs} and V_{gd}

$$\begin{aligned}\Delta Q_g &= \Delta Q_{gs} + \Delta Q_{gd} \\ &= Q_g(V_{gs} + \Delta V_{gs}, V_{gd} + \Delta V_{gd}) - Q_g(V_{gs}, V_{gd})\end{aligned} \tag{8}$$

which is obviously an exact result.

A major challenge is to find a simple expression for the gate charge Q_g. Measurements as well as calculations based on [2] confirm that the gate–source capacitance C_{gs} is approximated by a simple diode-capacitance model, in the normal bias range $V_{ds} >> 0$. The gate-to-drain capacitance C_{gd} in this voltage range is small as compared to C_{gs} ($C_{gd} \simeq 0.1 - 0.3\ C_{gs}$), and furthermore, C_{gd} is approximately constant and nearly independent of V_{gs} or V_{gd}.

We may thus choose a gate charge (for constant doping under the gate) and for a normally (forward) biased transistor

$$Q_g = 2\ C_{gs0} V_B \left(1 - \sqrt{1 - \frac{V_{gs}}{V_B}}\right) + C_{gd0} V_{gd} \tag{9a}$$

for $V_{ds} >> 0$, or alternatively, $-V_{gd} >> -V_{gs}$. (The use of $-V_{gs}$ and $-V_{gd}$ instead of V_{gs} and V_{gd} allows for the fact that both voltages are usually negative, and it is usually easier to think in terms of positive quantities.)

In (9a), C_{gs0} is the gate-to-source capacitance for zero source-to-gate bias, V_B is the built-in junction potential and C_{gd0} is the gate-to-drain capacitance. The charge has been normalized to be zero when $V_{gs} = 0$ and $V_{gd} = 0$. Note that V_{gs} is negative in the normal bias range. The first part of (9a) follows directly from Poisson's equation and is identical to the form used in SPICE.

For a reverse-biased transistor ($V_{ds} << 0$), different equations are needed, since the nominal source now really acts like a drain and the nominal drain like a source. The corresponding charge expression, obtained by interchanging V_{gd} and V_{gs}, is

$$Q_g = 2C_{gs0} V_B \left(1 - \sqrt{1 - \frac{V_{gd}}{V_B}}\right) + C_{gd0} V_{gs} \tag{9b}$$

for $V_{ds} << 0$ or alternatively $-V_{gd} << -V_{gs}$.

The transition from (9a) to (9b) can be envisioned to occur at $V_{ds} = 0$, or $V_{gd} = V_{gs}$. At $V_{ds} = 0$, Q_g is continuous, as may be seen by inspection. The derivatives of Q_g with respect to the voltages, however, are discontinuous. In particular, we find for $V_{ds} > 0$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{gs}}{V_B}}}$$

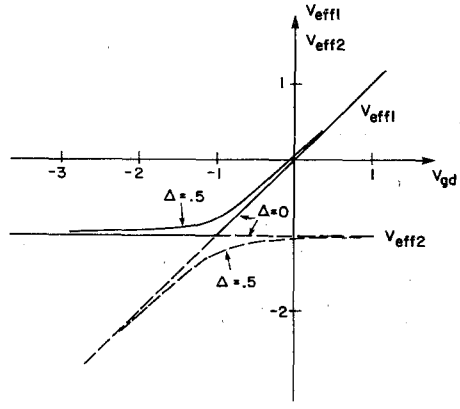

Fig. 4. V_{eff1} and V_{eff2} for $V_{gs} = -1$ V as a function of V_{gd} from -4 to $+2$ V for $\Delta = 0$ and 0.5.

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = C_{gd0} \tag{10}$$

and for $V_{ds} < 0$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = C_{gd0}$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{gd}}{V_B}}}.$$

Equation (10) approximates the desired behavior but is still deficient in that the abrupt transitions or steps in the values of C_{gs} and C_{gd} at $V_{ds} = 0$ are nonphysical and also would cause convergence difficulties in the numerical analysis.

Let us next address the achievement of a gradual transition of the capacitance values near $V_{ds} = 0$. Note that (9a) and (9b) can be written in the form

$$Q = 2C_{gs0}V_B\left(1 + \sqrt{1 - \frac{V_{eff1}}{V_B}}\right) + C_{gd0}V_{eff2}. \tag{11}$$

Here $(-V_{eff1})$ is meant to stand for the smaller of the two values of $(-V_{gd})$ or $(-V_{gs})$ and $(-V_{eff2})$ for the larger of the two. Mathematically, we can select these values by using the functions

$$V_{eff1} = \tfrac{1}{2}\{V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}\} \tag{12a}$$

$$V_{eff2} = \tfrac{1}{2}\{V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}\} \tag{12b}$$

with $\Delta = 0$. The inclusion of a nonzero Δ produces a smooth transition of width Δ in the value of V_{eff1} and V_{eff2} as a function of V_{gs} or V_{gd}. To illustrate (12), we plot in Fig. 4 V_{eff1} and V_{eff2} for $V_{gs} = -1$ V as a function of V_{gd} from -4 to 2 V for $\Delta = 0$ and 0.5.

The use of V_{eff1} and V_{eff2} in (12) also yields a smooth interpolation of C_{gs} and C_{gd} through the former point of discontinuity at $V_{ds} = 0$. Differentiating (11) gives

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{eff1}}{V_B}}}\frac{1}{2}\left\{1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} \tag{13a}$$

$$C_{gd} = \frac{C_{gs0}}{\sqrt{1 - \dfrac{V_{eff1}}{V_B}}}\frac{1}{2}\left\{1 - \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1 + \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \Delta^2}}\right\}. \tag{13b}$$

As already stated, the charge Q_g should not change if the values of V_{gs} and V_{gd} are interchanged, to reflect the symmetry of the transistor. Equations (11) and (12) satisfy this condition.

The transition width Δ has the dimensions of a voltage and is an adjustable parameter. Its magnitude is related to the voltage at which velocity saturation is reached. Studies based on Fig. 3 and the analysis of [1] and [2] show the establishment of a velocity-saturated zone under the gate for voltages V_{ds} just above the onset of velocity saturation. The length of the velocity-saturated zone depends only weakly on V_{ds}. Both the capacitances C_{gs} and C_{gd} as well as the drain current stabilize near the same voltage point (see Fig. 3). Further increases in drain voltage only weakly affect their values. From (2) and (6), $V_{ds} = 1/\alpha$ describes the onset of drain-current saturation. In accordance with the above reasoning we shall use in the following $\Delta = 1/\alpha$. This interpolation is shown by the dashed line in Fig. 3. Compare it to calculations based on the model of [2]. There is obviously room for more elaborate approximations to reproduce the fine structure of the capacitance at small voltages.

We have plotted, in Fig. 5, C_{gs} from (13a), for V_{ds} between 4 and -4 V and $V_{gs} = 0$, -1, -2, and -3 V, to illustrate the behavior of the gate-to-source capacitance in our model. For positive V_{ds} (normal operating mode) the gate-to-source capacitance shows the capacitance behavior of a diode with voltage V_{gs}. In the reverse-biased direction ($V_{ds} < 0$), the gate-to-source capacitance approaches C_{gd0}. The transition region width from high to low capacitance has a value of about $1/\alpha$, as chosen above.

The plot for negative V_{ds} is somewhat confusing. Along any one curve V_{gs} is a parameter and held constant. However, for negative V_{ds}, V_{gd} and not V_{gs} becomes the important gate voltage, because of the discussed role reversal of source and drain. V_{gs} is kept constant along one curve and V_{gd} varies with V_{ds}. Thus for negative drain-to-source voltages the "effective drain" may be thought of being tied through a battery to the gate. Furthermore, for large negative V_{ds}, V_{gd} (the "effective V_{gs}") becomes positive. Each of the plotted capacitance curves is carried to

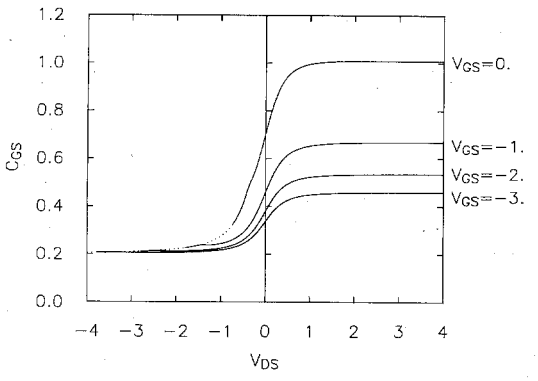

Fig. 5. Gate-to-source capacitance for V_{ds} between +4 and −4 V and $V_{gs} = 0, -1, -2$, and −3 V. Note for negative drain-to-source voltages, the capacitance approaches the small gate-to-drain capacitance.

the point where V_{gd} becomes +0.5 V. This brings us to another important point, namely the well-known singularity in the junction capacitance when the depletion region thickness collapses to zero.

Positive junction voltages with values of V_B or larger give rise, in the present approximation, to nonphysical infinite or complex capacitances. In order to avoid imaginary numbers or dividing by zero in (7)–(13), when V_{eff1} becomes positive and equal to or larger than V_B, we limit the values of V_{eff1} to a maximum value of $V_{\max}$. In the following we have chosen $V_{\max}$ to be 0.5 V. This procedure limits the value of the junction capacitance; the particular choice of $V_{\max}$ determines its maximum value. For voltages beyond $V_{\max}$, we take the capacitance to remain constant. This is similar to a more elaborate approach used by Poon and Gummel [8]. There exist no good models that would indicate what the capacitance should be for voltages beyond $V_{\max}$ and near V_B. As pointed out in [8], this detailed behavior is probably not important because the large forward currents of the junction, in this voltage region, are larger than the displacement currents. If this region were to be modeled more accurately, a distinction between Schottky-barrier and p–n junction gates would have to be made: The Schottky-barrier junction would not exhibit the large diffusion capacitance associated with minority-carrier injection.

As stated above, the gate-to-source capacitance would go to infinity for $V_{\text{eff1}} = V_B$. We now keep the capacitance constant, when $V_{\text{eff1}} > V_{\max}$, by using the following function for Q_g:

$$Q_g = C_{gs0}\left\{2V_B\left(1-\sqrt{1-\frac{V_{\max}}{V_B}}\right)+\frac{V_{\text{eff1}}-V_{\max}}{\sqrt{1-\frac{V_{\max}}{V_B}}}\right\} + C_{gd0}V_{\text{eff2}}, \text{ for } V_{\text{eff1}} \geqq V_{\max}. \quad (14)$$

IV. Capacitance Beyond The Pinchoff Point

When FET is pinched off, the gate-to-source junction capacitance falls to a small value, usually determined by the sidewall capacitance of the space-charge region. Simply setting the capacitance C_{gs} equal to zero would cause a discontinuity and result in convergence problems in the simulations. We thus once more use the smooth interpolation that we employed in (12) and (13). Accordingly, we introduce a V_{new} that is to be essentially equal to V_{eff1} before pinchoff and to V_T beyond pinchoff. In other words, V_{new} is to select the smaller of the two values of $-V_T$ and $-V_{\text{eff1}}$. Applying the procedure of (12) once more gives

$$V_{\text{new}} = \tfrac{1}{2}(V_{\text{eff1}} + V_T + \sqrt{(V_{\text{eff1}} - V_T)^2 + \delta^2}) \quad (15)$$

where δ represents the voltage range over which the transition between these two values is accomplished, as above. In our simulations, we arbitrarily use $\delta = 0.2$ volts. Introducing the function of (15), in place of V_{eff1}, into (11), one may again calculate, through partial differentiation, the values of C_{gs} and C_{gd}.

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1-\frac{V_{\text{new}}}{V_B}}}\frac{1}{2}\left\{1+\frac{V_{\text{eff1}}-V_T}{\sqrt{(V_{\text{eff1}}-V_T)^2+\delta^2}}\right\} \times \frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \quad (16)$$

$$C_{gd} = \frac{C_{gs0}}{\sqrt{1-\frac{V_{\text{new}}}{V_B}}}\frac{1}{2}\left\{1+\frac{V_{\text{eff1}}-V_T}{\sqrt{(V_{\text{eff1}}-V_T)^2+\delta^2}}\right\} \times \frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} + C_{gd0}\frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\}. \quad (17)$$

Similarly V_{eff1} in (14) should also be replaced by V_{new}.

In Fig. 6 we illustrate the behavior of C_{gs} from (16) as a function of V_{gs} and for various source-to-drain voltages. For $V_{ds} >> 0$ (normal biasing conditions,) C_{gs} follows a diode-like capacitance model as a function of V_{gs}. However, when V_{gs} approaches the pinchoff voltage V_T, C_{gs} falls rapidly to zero within a voltage range δ. For V_{ds} negative, C_{gs} is really a gate-to-drain capacitance because the reverse bias interchanges the roles of source and drain. The capacitance in this range becomes small and independent of V_{gs}. Because of the smooth transition from posi-

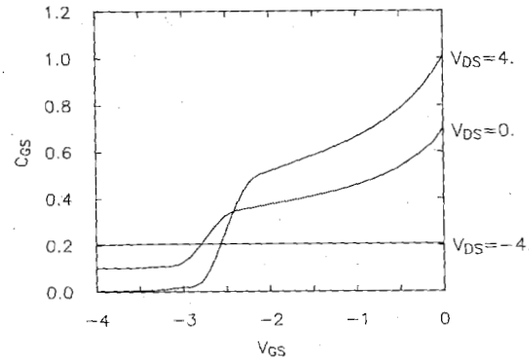

Fig. 6. This figure illustrates how, in the presented model, the gate-to-source capacitance behaves as V_{gs} goes through the pinchoff point V_T (here equal to −2.5 V).

tive to negative drain-to-source voltages, the situation for $V_{ds} = 0$ is intermediate between the two cases outlined above.

Code changes based on the above equations have been introduced into the SPICE code. Satisfactory circuit simulations without convergence problems have been obtained.

The above models may be further refined as more experience is obtained from their use and as deficiencies or inaccuracies become apparent.

Appendix

We shall summarize expressions for the gate–source and gate–drain capacitances C_{gs} and C_{gd}. For completeness we shall first repeat the expressions of van der Ziel [6] which are valid when the carrier velocity is unsaturated. The nomenclature is essentially that of [2]. With the voltage sign conventions corresponding to an n-type FET with a Schottky-barrier (or p-type) gate, we introduce the following reduced potentials and definitions:

$$W_{oo} = -V_T + V_B = \frac{qN}{2\epsilon} a^2 \tag{A1}$$

$$W_s = -V_{gs} + V_B \tag{A2}$$

$$s = \sqrt{\frac{W_s}{W_{oo}}} \tag{A3}$$

$$d = \sqrt{\frac{-V_{gs} + V_B + V_d}{W_{oo}}} \tag{A4}$$

$$p = \sqrt{\frac{-V_{gs} + V_B + V_p}{W_{oo}}}. \tag{A5}$$

In the above, W_{oo} is a positive quantity corresponding to the total voltage (including built-in voltage) needed to pinchoff the undepleted channel of thickness a, with doping density N. Furthermore, q is the electronic charge and ϵ is the dielectric constant of GaAs. W_s is again usually positive and represents the total voltage difference, including built-in voltage between the gate and the source end of the channel. The quantity s is defined in (A3). By replacing W_s in it by the total voltage between the gate and the drain end of the channel, the quantity d is obtained; by using instead of W_s the total voltage between the gate and the channel at the point of velocity saturation, the quantity p is obtained. The parameter p is only needed when the carrier velocities become saturated. It has to be calculated for each s value, utilizing [2]. Typically one uses the equation for V_{ds}, which is a function of s and p. It results in a transcendental equation for p as a function of s and V_{ds}. The gate-to-source voltage specifies s as seen in (A3), p is then determined for each given V_{ds}.

In the "van der Ziel" or unsaturated velocity regimes [6]

$$C_{gs} = \epsilon Z \frac{2L}{a} \frac{[\frac{2}{3}(d^3 - s^3) - \frac{1}{2}(d^4 - s^4)]\,(1 - s) - f_1(s, d)(s - s^2)}{f_1(s, d)^2} \tag{A6}$$

$$C_{gd} = \epsilon Z \frac{2L}{a} \frac{[-\frac{2}{3}(d^3 - s^3) + \frac{1}{2}(d^4 - s^4)]\,(1 - d) - f_1(s, d)(d - d^2)}{f_1(s, d)^2}. \tag{A7}$$

In (A6) and (A7) and in the following unsymmetric transistors with one gate are assumed: L is the gate length and Z is the gate width. $f_1(s, d)$ is defined as

$$f_1(s, d) = d^2 - s^2 - \tfrac{2}{3}(d^3 - s^3). \tag{A8}$$

Equations (A6) and (A7) are plotted by long dashed lines in Fig. 3.

In the saturated velocity region we start from the total gate charge Q_g in [2, eq. (107b)]. By taking a partial derivative of Q_g with respect to V_{gd}, holding V_{gs} constant, one finds

$$C_{gd} = \epsilon Z(f_3 + f_4). \tag{A9}$$

Here, f_3 and f_4 are defined by

$$f_3 = -\frac{2W_{oo}}{f_1^2(s, p)} \left[f_1(s, p)\, f_2'(s, p) \frac{L_1}{a} + f_1(s, p) f_2(s, p) \frac{L_1'}{a} - f_1'(s, p) f_2(s, p) \frac{L_1}{a} \right] \tag{A10}$$

$$f_4 = -2W_{oo} \left[-\left(\frac{p}{a} + \frac{\xi}{2L} \sinh\left(\frac{\pi L_2}{2a} \right) \right) L_1' + \frac{L_2}{a} p' \right]. \tag{A11}$$

The primes in (A10) and (A11) indicate derivatives with respect to source-to-drain voltage. f_1 is defined as in (A8), except by replacing d with p. f_2 is given by

$$f_2(s, p) = \tfrac{2}{3}(p^3 - s^3) - \tfrac{1}{2}(p^4 - s^4). \tag{A12}$$

L_1 and L_2 are the lengths of the channel where the carrier velocity is unsaturated and saturated, respectively. Of course, $L_1 + L_2 = L$. Expressions for L_1 and L_2 as a function of s and p may be found in [2]. After some algebraic manipulation one finds

$$f_1'(s, p) = 2p(1 - p)p' \tag{A13}$$

$$f_2'(s, p) = pf_1'(s, p) \tag{A14}$$

$$p' = \frac{f_1 - \left(\frac{L_1}{L}\xi\right)^2 \frac{1}{f_r} \cosh\left(\frac{\pi L_2}{2a}\right)}{W_{oo}\, 2p\left[(1 - p)\frac{L_1}{L}\xi \cosh\left(\frac{\pi L_2}{2a}\right) - f_1\right]} \tag{A15}$$

$$\xi = \frac{E_s L}{W_{oo}} \tag{A16}$$

$$f_r = \frac{1}{1 - p}\left[\left(2p(1 - p) + \xi\frac{L_1}{L}\right)\cosh\left(\frac{\pi L_2}{2a}\right) - 2p(1 - p)\right] \tag{A17}$$

$$L_1' = \frac{2pL_1\left(1 - p - \xi\frac{L_1}{L}\frac{1}{f_r}\right)}{W_{oo}2p\left[(1 - p)\frac{L_1}{L}\xi\cosh\left(\frac{\pi L_2}{2a}\right) - f_1\right]}. \tag{A18}$$

The quantity C_{gs} can be obtained from the total gate capacitance C_{gg} (derived in [2, eq. (109)]), according to

$$C_{gs} = C_{gg} - C_{gd}. \tag{A19}$$

In the present notation we find

$$C_{gg} = \epsilon Z\left[\frac{2}{f_1(s, p)}\frac{L_1}{a}\left(f_g\frac{2p^2(1 - p)^2 + f_2}{1 - p} - s(1 - s)\right) + 2\frac{L_2}{a}f_g + (1 + 2pf_g)\left(2\frac{L}{a}\frac{1}{\xi}\frac{p}{\cosh\left(\frac{\pi L_2}{2a}\right)} + \tanh\left(\frac{\pi L_2}{2a}\right)\right)\right] \tag{A20}$$

where f_g is now defined as

$$f_g = \frac{(1 - s)\cosh\left(\frac{\pi L_2}{2a}\right) - (1 - p)}{\left[2p(1 - p) + \xi\frac{L_1}{L}\right]\cosh\left(\frac{\pi L_2}{2a}\right) - 2p(1 - p)}. \tag{A21}$$

In Fig. 3, C_{gs} and C_{gd} from (A9)–(A21) are shown as solid lines.

The formulas in (A9) and (A20) do not contain the fringing field corrections which become important for gate lengths of 1 μm and less. Following [2], C_{gg} in (A20) should be increased by adding $\epsilon Z(\pi/2)$, allowing for field fringing from the gate toward both the source and the drain. Similarly, the expression of (A9) should be augmented by $\epsilon Z(\pi/4)$ to correct for field fringing towards the drain.

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