**Rochester Institute of Technology**

**Department of Computer Engineering**

**EECC 630/730 VLSI Design**

**Lab 03. Mirror Adder**

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Lab Section: L1

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# Abstract

In this lab activity a 1-bit mirror adder will be constructed using the Design Architect-IC software. This circuit will be simulated in a similar fashion as last lab exercise, using the EZWave Simulation tool. The simulations performed will be both functional and timing simulations. This exercise stresses the ability to understand how to size PMOS and NMOS transistors in order to properly ensure equal resistance.

# Design Methodology and Theory

The circuit schematic for the mirror adder accurately ensures that the effective resistances match the effective resistance of a standard inverter in this system. The sizing of the transistors is determined by the worst possible path through the circuit. The worst path in the circuit shown in Figure 1.0 is three transistors in series resulting in the widths of the NMOS as 12 lamda and the PMOS widths as 24 lamda. This sizing should result in equivalent effective resistance, which was tested in the simulations of the circuit.

# Results and Data Analysis

After proper completion of the circuit and sizing of the transistors the circuit could then be simulated. Different test cases were simulated with varying conditions for Vdd, temperature and capacitance. The waveforms resulting from these test cases can be seen below in graphs 1.0 to 1.3. Also the associated rise and fall times can be seen, as well as the HI-LO, and LO-HI delay. These results are aggregated in Tables 1.0 and 1.1. In Table 1.2 the maximum input and throughput frequencies for the different conditions. By examining these tables you can perceive the percentage decrease between the nominal and worst case conditions for the output signals. Even though the test condition changes were small they greatly affected the performance of the outputs, in particular the signal for S.

Sum

|  | Vdd | Temp | Load | Rise  Time | Fall  Time | Tp, HL | Tp, LH |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Worst  Case | 1.62 | 125 | 0 | 153.12 Ps | 98.223Ps | 10.387 Ns | 13.332 Ns |
| 1.62 | 125 | 120 | 2.0573 Ns | 1.0903 Ns | 14.406 Ns | 10.995 Ns |
| Nominal  Case | 1.8 | 70 | 0 | 83.784 Ps | 93.667 Ps | 10.724 Ns | 10.768 Ns |
| 1.8 | 70 | 120 | 1.4626 Ns | 890.45 Ps | 11.432 Ns | 11.271 Ns |

Table 1.0

Carry out

|  | Vdd | Temp | Load | Rise  Time | Fall  Time | Tp, HL | Tp, LH |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Worst  Case | 1.62 | 125 | 0 | 153.12 Ps | 98.223 Ps | 2.0348 Ns | 355.03 Ps |
| 1.62 | 125 | 120 | 924.36 Ps | 2.6173 Ns | 2.9582 Ns | 1.0903 Ns |
| Nominal  Case | 1.8 | 70 | 0 | 411.26 Ps | 287.25 Ps | 526.26 Ps | 472.46 Ps |
| 1.8 | 70 | 120 | 791.29 Ns | 768.89 Ps | 867.74 Ps | 979.53 Ps |

Table 1.1

Overall Sum Results

|  | Vdd | Temp | Load | Finput, max | Fthroughput, max |
| --- | --- | --- | --- | --- | --- |
| Worst  Case | 1.62 | 125 | 0 | 3978626816.74 | 74949107.6822 |
| 1.62 | 125 | 120 | 317601473.671 | 90831421.7861 |
| Nominal  Case | 1.8 | 70 | 0 | 5635358493.33 | 92775360.0519 |
| 1.8 | 70 | 120 | 424980344.659 | 44047042.2411 |

Table 1.2

Overall Cout Results

|  | Vdd | Temp | Load | Finput, max | Fthroughput, max |
| --- | --- | --- | --- | --- | --- |
| Worst  Case | 1.62 | 125 | 0 | 3978626816.74 | 418439805.342 |
| 1.62 | 125 | 120 | 282353472.665 | 247005063.604 |
| Nominal  Case | 1.8 | 70 | 0 | 1431618731.30 | 1001281640.50 |
| 1.8 | 70 | 120 | 1262532.38569 | 541339381.899 |

Table 1.3

# Conclusions

This lab was able to successfully enforce the transistor size in order to have equal resistance throughout the circuit. It also successfully used ELDO to perform simulations and analyze how varying parameters of the circuit affects the performance of various devices. An advanced circuit design was able to be constructed in order to be used for future exercises where a 1-bit adder may be needed.

# Appendices

Worst Case with Load = 0fF Figure 1.1

1-Bit Full Adder Schematic Figure 1.2