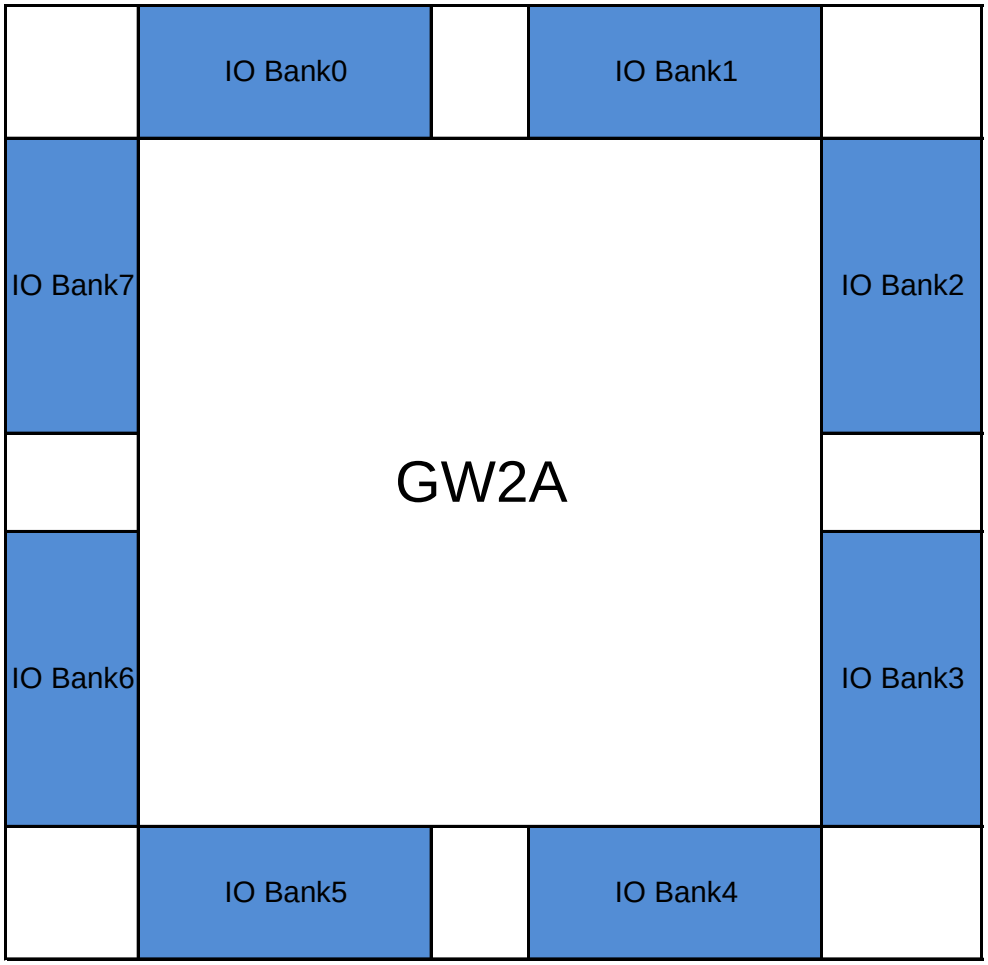
Version History

Date	Version	Description
08/04/2016	1.0E	Initial version published.
12/10/2019	1.1E	The info. of package PG256E added.
03/09/2020	1.2E	The multiplexing relationship of VCCPLLL, VCCPLLR, and VCC in package PG256C, UG324, and PG256E added. GW2A-18C devices added.
04/03/2020	1.3E	The location of pin R15 and T9 in package UG324 modified. The location of pin E7 and E8 in package UG324 modified.
07/16/2021	1.4E	The location of pin L11 in package PG256E modified. The location of pin P14, N10, R8, N7, R4 in package PG256S modified. Package UG484, PG256CF added.
11/15/2021	1.5E	Pin definitions updated. Package PG256SF added.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	O	MI in MSPI mode
MO	I	MO in MSPI mode

Pin Name	I/O	Description
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	High, the operation is efficient in SSPI mode or CPU mode; Low, the operation is inefficient in SSPI mode or CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE1	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
MODE0	I, internal weak pull-up	Selection signal port in GowinCONFIG mode If this pin is not bonded, it's internally grounded.
Other Pins		
EXTR	NA	External 10K 1% resistor to ground
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
VCCPLLL0/1	NA	Left PLL0/1 voltage supply pin, LQFP is separately packaged.
VCCPLLR0/1	NA	Right PLL0/1 voltage supply pin, LQFP is separately packaged.
VCCPLLL	NA	Package PBGA: Left PLL0/1 voltage supply pin
VCCPLLR	NA	Package PBGA: Right PLL0/1 voltage supply pin

Note!
[1] Ready and Done can not be driven to low before and during configuration.
[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.



Note!

[1] Each Bank has independent reference voltage (VREF);

[2] You can select to use IOB internal VREF (equals to 0.5 X VCCO);

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
EXTR[2]	Ground		N/A				47(Tie to VSS by 10K Resisitor)	75(Tie to VSS by 10K Resisitor)	75(Tie to VSS by 10K Resisitor)		L7(Tie to VSS by 10K Resisitor)				N17(Tie to VSS by 10K Resisitor)				
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	44		E2	P4	N3	D2			V8	N3	P4
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	45		E3	T4	P3	D1			U8	P3	T4
IOB13A	I/O	DQ5	5		True_of_IOB13B	NONE					B3				AB1		W6		
IOB13B	I/O	DQ5	5		Comp_of_IOB13A	NONE					A2				AB2		V7		
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	46		C1		R3	F4	Y6	P12	AA8	R3	
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	47		D2		T3	F3	AA6	P11	AB8	T3	
IOB15A	I/O	DQ5	5		True_of_IOB15B	NONE											T10		
IOB15B	I/O	DQ5	5		Comp_of_IOB15A	NONE											U10		
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE				N12	E1	L8	R4	E3	W7		AA6	R4	L8
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE				P12	F2	L7	T4	E1	W8		AB6	T4	L7
IOB17A	I/O	DQ5	5		True_of_IOB17B	NONE		48	48						AB3	T8	V9		
IOB17B	I/O	DQ5	5		Comp_of_IOB17A	NONE		49	49						AB4	T7	W8		
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31				F4	N5	N5	H6	Y7		AA7	N5	N5
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32				G6	P5	N6	H5	Y8		AB7	N6	P5
IOB19A	I/O	DQ5	5		True_of_IOB19B	NONE					F3				V10	P8	Y8		
IOB19B	I/O	DQ5	5		Comp_of_IOB19A	NONE					F1				V11	P7	W9		
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50	50	N10	G5	R5	M6	F2	W9		Y9	M6	R5
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51	51	P10	G4	T5	P6	F1	Y9		Y10	P6	T5
IOB21A	I/O	DQS5	5		True_of_IOB21B	NONE					G2		M7	J7	AB5	M9	AA9	M7	
IOB21B	I/O	DQS5	5		Comp_of_IOB21A	NONE					G3		K8	J6	AB6	M8	AB9	K8	
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52	52		F5	P6	R5	G3	AA7	T5	V10	R5	P6
IOB22B	I/O	DQ5	5		Comp_of_IOB22A	TRUE		54	54		H6	T6	T5	G1	AB7	T6	W10	T5	T6
IOB23A	I/O	DQ5	5		True_of_IOB23B	NONE							R7		t		T11	R7	
IOB23B	I/O	DQ5	5		Comp_of_IOB23A	NONE							T7		AB8		U11	T7	
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33			L8	G1	R7	R6	L7	W10		AA11	R6	R7
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34			M8	H2	T7	T6	K6	W11		AB11	T6	T7
IOB25A	I/O	DQ5	5		True_of_IOB25B	NONE							L7		AA11	P5	V11	L7	
IOB25B	I/O	DQ5	5		Comp_of_IOB25A	NONE									AB11	P6	Y11		
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE					H4		L8	H4	Y10		AA10	L8	
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE					J6		M8	H3	Y11		AB10	M8	
IOB27A/GCLKT_5	I/O	DQ5	5	GCLKT_5	True_of_IOB27B	NONE				N8	J1	P7	N8	L5	AB9		U12	N8	P7
IOB27B/GCLKC_5	I/O	DQ5	5	GCLKC_5	Comp_of_IOB27A	NONE				P8	J3	M7	P8	K5	AB10		V12	P8	M7
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE					A4			C2	U6	P9	AA2		
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE					C5			C1	U7	P10	AB2		
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	56	N7	L2	P8	R9	L2	AB12	K15	AB12	R9	P8
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	57	P7	M1	T8	T9	L1	AA12	L15	AA12	T9	T8
IOB31A	I/O	DQ6	4		True_of_IOB31B	NONE									Y12		Y12		
IOB31B	I/O	DQ6	4		Comp_of_IOB31A	NONE									Y13		T12		
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE					H3		K9	H2	W12		V13	K9	
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE					H1		L9	H1	W13		U13	L9	
IOB33A	I/O	DQ6	4		True_of_IOB33B	NONE		58	58					K4	AB13	P16	AB13		
IOB33B	I/O	DQ6	4		Comp_of_IOB33A	NONE		59	59					K3	AB14	P15	AA13		
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	60	N6	J2	M9	M9	J3	AB15		Y13	M9	M9
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	61	P6	K1	N8	N9	J1	AA15		W13	N9	N8
IOB35A	I/O	DQ6	4		True_of_IOB35B	NONE					H5				V12	N14	U14		

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOB35B	I/O	DQ6	4		Comp_of_IOB35A	NONE					J4				V13	M14	V14		
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE					K3	R9	R10	K2	AB16		T13	R10	R9
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE					K2	T9	T10	K1	AA16		T14	T10	T9
IOB37A	I/O	DQS6	4		True_of_IOB37B	NONE				N5	J5			L4	Y14	N16	AB14		
IOB37B	I/O	DQS6	4		Comp_of_IOB37A	NONE				P5	K6			L3	Y15	N15	AA14		
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	62	L4	L1	L10	R11	P2	V14	L16	Y14	R11	L10
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	63	M4	L3	M10	T11	P1	V15	M16	W14	T11	M10
IOB39A	I/O	DQ6	4		True_of_IOB39B	NONE					K4				AB17		AB15		
IOB39B	I/O	DQ6	4		Comp_of_IOB39A	NONE					L5				AB18		AA15		
IOB3A	I/O	DQ4	5		True_of_IOB3B	NONE					D6				W5		V6		
IOB3B	I/O	DQ4	5		Comp_of_IOB3A	NONE					E7				W6		U6		
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	64	N4	K5	N9	R12	M3	AA17		Y15	R12	N9
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	65	P4	L4	P9	T12	M1	Y17		W15	T12	P9
IOB41A	I/O	DQ6	4		True_of_IOB41B	NONE					N2				W14		AB16		
IOB41B	I/O	DQ6	4		Comp_of_IOB41A	NONE					P1				W15		AA16		
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	66		M3		L10	N2			V15	L10	
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE	42	67	67		N1		K10	N1			U15	K10	
IOB43A	I/O	DQ6	4		True_of_IOB43B	NONE	41			N3	M2				AB19	J16	AB17		
IOB43B	I/O	DQ6	4		Comp_of_IOB43A	NONE				P3	N3				AB20	K16	AA17		
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE					R1			T2	Y16		Y17		
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE					P2			T1	W16		V16		
IOB45A	I/O	DQ6	4		True_of_IOB45B	NONE					P4		P9				Y18	P9	
IOB45B	I/O	DQ6	4		Comp_of_IOB45A	NONE					T4		P11				W17	P11	
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	68		R3		R13	U2	Y19		AB18	R13	
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	69	M12	T2		T13	U1	Y18		AA18	T13	
IOB49A	I/O	DQ7	4		True_of_IOB49B	NONE										R14	AB19		
IOB49B	I/O	DQ7	4		Comp_of_IOB49A	NONE										P14	AA19		
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE					A3	M4		F6	V6		AA3		M4
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE					B4	M3		F5	V7		AB3		M3
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE					P5		M10	L6	V16		T9	M10	
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE					R5	P11	N11	M5	U16		U9	N11	P11
IOB51A	I/O	DQ7	4		True_of_IOB51B	NONE									W17		T15		
IOB51B	I/O	DQ7	4		Comp_of_IOB51A	NONE									W18		U16		
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE					R4	N12	T14	P4		R16	AB20	T14	N12
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE					T3	P12	T15	P3		R15	AA20	T15	P12
IOB53A	I/O	DQ7	4		True_of_IOB53B	NONE		70	70				R14		AA20	T15	Y19	R14	
IOB53B	I/O	DQ7	4		Comp_of_IOB53A	NONE		71	71						Y20	T14	W18		
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE					R6	M12	P14	N4	V17		AB21	P14	M12
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE					T5	M11	L11	N3	V18		AA21	L11	M11
IOB55A	I/O	DQ7	4		True_of_IOB55B	NONE						L11	M11		W19		V17	M11	L11
IOB55B	I/O	DQ7	4		Comp_of_IOB55A	NONE		72	72				N12		V19		T16	N12	
IOB5A	I/O	DQ4	5		True_of_IOB5B	NONE		38	38							T9	Y4		
IOB5B	I/O	DQ4	5		Comp_of_IOB5A	NONE		39	39							T10	W5		
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE	25	40	40					E4	Y4		U7		
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	41					D3	Y5		T8		
IOB7A	I/O	DQ4	5		True_of_IOB7B	NONE		42	42		A5				V8		AA4		
IOB7B	I/O	DQ4	5		Comp_of_IOB7A	NONE		43	43		B6				V9		AB4		
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27				B1	M6	R8	H7		T12	AA5	R8	M6
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28				C2	N6	T8	G6		T11	AB5	T8	N6

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOB9A	I/O	DQS4	5		True_of_IOB9B	NONE					D3		T2		Y3		Y5	T2	
IOB9B	I/O	DQS4	5		Comp_of_IOB9A	NONE					D1				AA3		Y6		
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE					F10	B2		B14	C2	F3	E1		B2
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE						A2		A14	C1	G3	F1		A2
IOL12A	I/O	DQ1	7		True_of_IOL12B	NONE									D1	F2	G3		
IOL12B	I/O	DQ1	7		Comp_of_IOL12A	NONE									E1	F1	G4		
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE					B11	G6		C13			H4		G6
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE					A12	G5		A13			H3		G5
IOL14A	I/O	DQ1	7		True_of_IOL14B	NONE								D12	F2	G4	G2		
IOL14B	I/O	DQ1	7		Comp_of_IOL14A	NONE								C12	G2	H4	G1		
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE				C1	A11	C1		B12	F1		H2		C1
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE				B1	C11	B1		A12	G1		H1		B1
IOL16A	I/O	DQ1	7		True_of_IOL16B	NONE									H4	G2	J7		
IOL16B	I/O	DQ1	7		Comp_of_IOL16A	NONE									J4	H2	J6		
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE					D10	D1		B11	H3		H5		D1
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE					E10	D3		A11	J3		J5		D3
IOL18A	I/O	DQ1	7		True_of_IOL18B	NONE						C3			H2		J4		C3
IOL18B	I/O	DQ1	7		Comp_of_IOL18A	NONE						C2			H1		J3		C2
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE				D4		K5	F2	G9	J1		J2	F2	K5
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE				D3		K6	F1	F9	K1		J1	F1	K6
IOL21A	I/O	DQ1	7		True_of_IOL21B	NONE									K5		K7		
IOL21B	I/O	DQ1	7		Comp_of_IOL21A	NONE									L5		K6		
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9	9	E2	D11	E2	G2	G11	L2	H3	L7	G2	E2
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10	10	E1		E1	G1	F10	L1	J3	K5	G1	E1
IOL23A	I/O	DQ1	7		True_of_IOL23B	NONE									K3		K4		
IOL23B	I/O	DQ1	7		Comp_of_IOL23A	NONE									L3		K3		
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE				F4		L4		C10	K4		K2		L4
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE				F3		L5		A10	L4		K1		L5
IOL25A	I/O	DQ1	7		True_of_IOL25B	NONE								F11	M2		L6		
IOL25B	I/O	DQ1	7		Comp_of_IOL25A	NONE								E11	M1		L5		
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE				F2		H4		D11	P1		L1		H4
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE				F1		H3		C11	N1		M2		H3
IOL27A/GCLKT_7	I/O	DQ1	7	GCLKT_7	True_of_IOL27B	NONE		11	11	H2	A9	J6	E1	B9	R1	G1	L3	E1	J6
IOL27B/GCLKC_7	I/O	DQ1	7	GCLKC_7	Comp_of_IOL27A	NONE		12	12	H1	C9	H5	J3	A9	T1	H1	L4	J3	H5
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25	25	G2	C8	K3	M2	D9	M4	K1	M1	M2	K3
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26	26	G1	A8	J4	M1	C9	M3	L1	N1	M1	J4
IOL2A	I/O	DQ0	7		True_of_IOL2B	TRUE		3	3		B14	B3	D1	B16	E5	D1	G7	D1	B3
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4		A15	A3	C2	A16	F5	E1	F6	C2	A3
IOL30A	I/O	DQ2	6		True_of_IOL30B	NONE									U1	J1	N2		
IOL30B	I/O	DQ2	6		Comp_of_IOL30A	NONE									U2	K2	P1		
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE				J2	F9	F2	J2	B8	N4		M6	J2	F2
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE				J1	E11	F1	J1	A8	N3		M5	J1	F1
IOL32A	I/O	DQ2	6		True_of_IOL32B	NONE		23	23						M5	L2	N3		
IOL32B	I/O	DQ2	6		Comp_of_IOL32A	NONE		24	24						N5	M2	N4		
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27	27	J4	B9	G3	K6	D8	T2	M1	P2	K6	G3
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28	28	J3	A10	G1	L6	C8	R2	N1	R1	L6	G1
IOL34A	I/O	DQ2	6		True_of_IOL34B	NONE									V1		P3		
IOL34B	I/O	DQ2	6		Comp_of_IOL34A	NONE									W1		M7		
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE				K2	F8		K2	B6	P3	M3	P4	K2	

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE				K1	D9		K1	A6	R3	N3	N5	K1	
IOL36A	I/O	DQS2	6		True_of_IOL36B	NONE		29	29			H2	L2	E8	P4	L4	N6	L2	H2
IOL36B	I/O	DQS2	6		Comp_of_IOL36A	NONE		30	30			H1	L1	E7	R4	L5	N7	L1	H1
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE					D8	J3	N2	C7	Y1		R2	N2	J3
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE					E9	J1	N1	A7	Y2		T1	N1	J1
IOL39A	I/O	DQ2	6		True_of_IOL39B	NONE									T3	P1	P5		
IOL39B	I/O	DQ2	6		Comp_of_IOL39A	NONE									U3	R1	P6		
IOL3A	I/O	DQ0	7		True_of_IOL3B	NONE									B3	E4	D4		
IOL3B	I/O	DQ0	7		Comp_of_IOL3A	NONE									B2	F4	D3		
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE					B7		K5	G8			T2	K5	
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE					C7		L4	F8			U1	L4	
IOL41A	I/O	DQ2	6		True_of_IOL41B	NONE										P2	R3		
IOL41B	I/O	DQ2	6		Comp_of_IOL41A	NONE										P3	R4		
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	32				P2	F7			R5	P2	
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	33				P1	E6			P7	P1	
IOL43A	I/O	DQ2	6		True_of_IOL43B	NONE											R6		
IOL43B	I/O	DQ2	6		Comp_of_IOL43A	NONE													
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE								C5	V3		T3		
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE								A5	W3		T4		
IOL45A/LPLL2_T_in	I/O	DQ2	6	LPLL2_T_in	True_of_IOL45B	NONE	13	34	34	L2	F7	K2	L3	B4	AA1		R7	L3	K2
IOL45B/LPLL2_C_in	I/O	DQ2	6	LPLL2_C_in	Comp_of_IOL45A	NONE				L1	E8	K1	J6	A4	AA2		T5	J6	K1
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15			M2	C4	R2	R1	B3	P5		U2	R1	R2
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16			M1	B5	R1		A3	R5		V1		R1
IOL48A	I/O	DQ3	6		True_of_IOL48B	NONE						M2		D6	T4	T2	W1		M2
IOL48B	I/O	DQ3	6		Comp_of_IOL48A	NONE						M1		C6	U4	T3	W2		M1
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17					L3					Y1		L3
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18					L1					AA1		L1
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE						F6	F3		G6	E3	E4	F3	F6
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE						F5	F4		G5		F5	F4	F5
IOL50A	I/O	DQS3	6		True_of_IOL50B	NONE						N3			V4		U3		N3
IOL50B	I/O	DQS3	6		Comp_of_IOL50A	NONE						N1			W4		U4		N1
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19					P2		B2		R2	W3		P2
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20					P1		A2		R3	Y2		P1
IOL52A	I/O	DQ3	6		True_of_IOL52B	NONE											V4		
IOL52B	I/O	DQ3	6		Comp_of_IOL52A	NONE											U5		
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE					E6	M5		D4	V5		Y3		M5
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE					D7	N4		C4	U5		W4		N4
IOL54A	I/O	DQ3	6		True_of_IOL54B	NONE									T5		V5		
IOL54B	I/O	DQ3	6		Comp_of_IOL54A	NONE									T6		T7		
IOL5A	I/O	DQ0	7		True_of_IOL5B	NONE									D3	D3	G6		
IOL5B	I/O	DQ0	7		Comp_of_IOL5A	NONE									C3	D2	H7		
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE						E4	B1	D14	E4		C1	B1	E4
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE						E3		C14	E3		D2		E3
IOL7A/LPLL1_T_in	I/O	DQ0	7	LPLL1_T_in	True_of_IOL7B	NONE	4	6	6	D2	C12	F4	F5	C15	F4	K3	G5	F5	F4
IOL7B/LPLL1_C_in	I/O	DQ0	7	LPLL1_C_in	Comp_of_IOL7A	NONE		7	7	D1	B12	F3	G5	A15	G4	L3	H6	G5	F3
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE					B13		D4	F13	F3	J4	D1	D4	
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE					A14		E5	E13	G3	K4	E2	E5	
IOL9A	I/O	DQ0	7		True_of_IOL9B	NONE								F12	H5		E3		
IOL9B	I/O	DQ0	7		Comp_of_IOL9A	NONE								E12	J5				

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE					R12	F13	D15	U11	G19			D15	F13
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE					P13	F14	D16	V11	G20		G20	D16	F14
IOR12A	I/O	DQ10	2		True_of_IOR12B	NONE									F20		G19		
IOR12B	I/O	DQ10	2		Comp_of_IOR12A	NONE									F21		G18		
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE				C12		C15	F13	R11			H22	F13	C15
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE				C13		C16	F14	T11			H21	F14	C16
IOR14A	I/O	DQ10	2		True_of_IOR14B	NONE									C22		G17		
IOR14B	I/O	DQ10	2		Comp_of_IOR14A	NONE									D22		H20		
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE						E15			H20		H19		E15
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE						E16			H21		H18		E16
IOR16A	I/O	DQ10	2		True_of_IOR16B	NONE									J19		H17		
IOR16B	I/O	DQ10	2		Comp_of_IOR16A	NONE									J20		H16		
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE				E13	R11	F15		T12	F22		J18		F15
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE				E14	T12	F16		V12	E22		J19		F16
IOR18A	I/O	DQ10	2		True_of_IOR18B	NONE									G21		J21		
IOR18B	I/O	DQ10	2		Comp_of_IOR18A	NONE									G22		J22		
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	102		R13	G14		N10	H22		J16		G14
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	101		T14	G16		P11	J22		J17		G16
IOR21A	I/O	DQ10	2		True_of_IOR21B	NONE								M11	K22	H16	J20		
IOR21B	I/O	DQ10	2		Comp_of_IOR21A	NONE								N11	L22	J15	K20		
IOR22A	I/O	DQS10	2		True_of_IOR22B	TRUE		100	100	F11	M10	H15	B16	M10	K19		K19	B16	H15
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	99	F12	N11	H16		N9	L19		K18		H16
IOR23A	I/O	DQ10	2		True_of_IOR23B	NONE						H13			K20		L17		H13
IOR23B	I/O	DQ10	2		Comp_of_IOR23A	NONE						H14			L20		L16		H14
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE				G13	T11	G12	F15	R10	L21	J13	K17	F15	G12
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE				G14	P11	H11	F16	T10	M21	J14	K16	F16	H11
IOR25A/TDO	I/O	DQ10	2	TDO	True_of_IOR25B	NONE	8	18	18	C14	C6	E14	J4	D16	M22	C2	L19	J4	E14
IOR25B/TMS	I/O	DQ10	2	TMS	Comp_of_IOR25A	NONE	5	13	13	B14	B8	A15	J5	B18	N22	B2	K22	J5	A15
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	14	B13	A7	C14	H3	A17	N20	B1	L20	H3	C14
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	16	A13	A6	C12	H4	D15	M20	C1	L21	H4	C12
IOR27A/GCLKT_2	I/O	DQ10	2	GCLKT_2	True_of_IOR27B	NONE		98	98	F13	N10	J11	E15	U10	M19	K13	L22	E15	J11
IOR27B/GCLKC_2	I/O	DQ10	2	GCLKC_2	Comp_of_IOR27A	NONE		97	97	F14	M11	J12	E16	V10	N19	L13	M17	E16	J12
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE	63			H13	T7	J13	M15	R8	P22		M22	M15	J13
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE				H14	R8	K14	M16	T8	R22		M21	M16	K14
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE						E13		U16	F18		C22		E13
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE						E12		V16	F19		G16		E12
IOR30A/MODE0	I/O	DQ9	3	MODE0	True_of_IOR30B	NONE	88	144	144	N9	M16	T11	H13	T15[1]	T22		M20	H13	T11
IOR30B/MODE1	I/O	DQ9	3	MODE1	Comp_of_IOR30A	NONE	87	142	142	P13	B16	N11	H12	T15[1]	U22		N22	H12	
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE		143	143		C15		G12	N12	U21		M19	G12	N11
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE	9	20	20	N1	B10	T2	H5	V2	T21	C15	P21	H5	T2
IOR32A/READY	I/O	DQ9	3	READY	True_of_IOR32B	NONE		22	22	N2	A13	R3	G16	U3	L18	D14	M16	G16	R3
IOR32B/DONE	I/O	DQ9	3	DONE	Comp_of_IOR32A	NONE		21	21	N14	C13	P13	H14	V17	M18	E12	N16	H14	P13
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	96	N11	P10	P10	H2	R13	P19	H13	N17		
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61	95	95	P11	R10	T10	C1	T13	P20	H14	N18		
IOR34A/MCS_N/D5	I/O	DQ9	3	MCS_N/D5	True_of_IOR34B	NONE	60	94	94	P2	M9	T3	D2	V3	N18	D16	N20		
IOR34B/MCLK/D4	I/O	DQ9	3	MCLK/D4	Comp_of_IOR34A	NONE	59	93	93	N13	L10	R11	H1	R15	P18	E15	N19		
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N/D3	True_of_IOR35B	TRUE	57	92	92	P9	R9	K12	G15	T9	R20	F14	R22		
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	90	L12	T10	K11		V9	R21		R21	D2	

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOR36A/SO/D1	I/O	DQS9	3	SO/D1	True_of_IOR36B	NONE	56	88	88	H11	M8	N14	K11	M8	V22	E13	P22	G15	
IOR36B/SSPI_CS_N/D0	I/O	DQS9	3	SSPI_CS_N/D0	Comp_of_IOR36A	NONE	55	87	87	H12	N9	N16		N8	W22	F13	P20	K11	
IOR38A/DIN/CLKHOLD_N	I/O	DQ9	3	DIN/CLKHOLD_N	True_of_IOR38B	TRUE	54	86	86	J13	T9	J14		U8	T20	G14	T22	H2	P10
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	85	J14	P9	J16		V8	U20	G13	T21	C1	T10
IOR39A/SCLK	I/O	DQ9	3	SCLK	True_of_IOR39B	NONE	52	15	15		C10			P12	T19	D13	P19	H1	R11
IOR39B	I/O	DQ9	3		Comp_of_IOR39A	NONE								P13	R19		P18		K12
IOR3A	I/O	DQ11	2		True_of_IOR3B	NONE									E19		F17		
IOR3B	I/O	DQ11	2		Comp_of_IOR3A	NONE									E20		C21		
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE				J11	N8	K15		U7		B16	P17		T3
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE				J12	L9	K16		V7			P16		K11
IOR41A	I/O	DQ9	3		True_of_IOR41B	NONE								N7		A12	U22		N14
IOR41B	I/O	DQ9	3		Comp_of_IOR41A	NONE								P8		A13	U21		N16
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84	84	K13	P8	M15	K12	T6			V22	K12	M15
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83	83	K14	T8	M16	L12	V6			W22	L12	M16
IOR43A	I/O	DQ9	3		True_of_IOR43B	NONE										C12	R20		J14
IOR43B	I/O	DQ9	3		Comp_of_IOR43A	NONE										C13	R19		J16
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE				L13	M6	L14	M12	R7	Y22		R18	M12	K15
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE				L14	L8	L16	N13	T7	AA22			N13	K16
IOR45A/RPLL2_T_in	I/O	DQ9	3	RPLL2_T_in	True_of_IOR45B	NONE	51	82	82	M13		M13	J15	U5	R18	E14	R16	J15	L14
IOR45B/RPLL2_C_in	I/O	DQ9	3	RPLL2_C_in	Comp_of_IOR45A	NONE				M14		M14	J16	V5	T18		R17	J16	L16
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE					M7	R15	J12	R3	Y21	C16	T19	J12	M13
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE					N7	R16	J14	T3	AA21		T18	J14	M14
IOR48A	I/O	DQ8	3		True_of_IOR48B	NONE							J13	N6	W20	E16	Y22	J13	R15
IOR48B	I/O	DQ8	3		Comp_of_IOR48A	NONE							J11	P7	V20	G15	W21	J11	R16
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80	80		R7		L15			F16	T17	L15	
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79	79		P7		L16			F15	U20	L16	
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE						B15		U15	G17		D22		B15
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE						B16		V15	G18		D21		B16
IOR50A	I/O	DQS8	3		True_of_IOR50B	NONE		78	78			R14	K15	R5	AB22	G16	AA22	K15	R14
IOR50B	I/O	DQS8	3		Comp_of_IOR50A	NONE		76	76			T15	K16	T5	AB21		Y21	K16	T15
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE					N6	T14	N15	N5		B15	U19	N15	T14
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE						T13	N16	P6		C14	U18	N16	T13
IOR52A	I/O	DQ8	3		True_of_IOR52B	NONE						L12	L13			A14	U17	L13	L12
IOR52B	I/O	DQ8	3		Comp_of_IOR52A	NONE						L13	L14			A15	V19	L14	L13
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE					P6	R12	R16	T4	T17		V18	R16	R12
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE					T6	T12	P16	V4	U17		W20	P16	T12
IOR54A	I/O	DQ8	3		True_of_IOR54B	NONE						P15	P15		U19	B13	W19	P15	P15
IOR54B	I/O	DQ8	3		Comp_of_IOR54A	NONE						P16	N14		U18	B14	Y20	N14	P16
IOR5A	I/O	DQ11	2		True_of_IOR5B	NONE									H19		D19		
IOR5B	I/O	DQ11	2		Comp_of_IOR5A	NONE									H18		D20		
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE						F12	C15		D19		E22	C15	F12
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE						G11	C16		D20		E21	C16	G11
IOR7A/RPLL1_T_in	I/O	DQ11	2	RPLL1_T_in	True_of_IOR7B	NONE		106	106	D13	T15	D14	G11	T14	B20	K14	F22	G11	D14
IOR7B/RPLL1_C_in	I/O	DQ11	2	RPLL1_C_in	Comp_of_IOR7A	NONE		105	105	D14	R14	D16		V14	C20	L14	G22		D16
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE					P12			U13	B21		E19		
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE					T13			V13	C21		E20		
IOR9A	I/O	DQ11	2		True_of_IOR9B	NONE									J18		F18		

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOR9B	I/O	DQ11	2		Comp_of_IOR9A	NONE									K18		F19		
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	134		F12	B6		H12			B5		B6
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	133		G13	A6		G13			A6		A6
IOT13A	I/O	DQ14	0		True_of_IOT13B	NONE					G15				D7		D6		
IOT13B	I/O	DQ14	0		Comp_of_IOT13A	NONE					G14				D8		E7		
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	132		G11	F7		E16	A2		B6		F7
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	131		H12	E6	A5	E18	A3		A7	A5	E6
IOT15A	I/O	DQ14	0		True_of_IOT15B	NONE											C6		
IOT15B	I/O	DQ14	0		Comp_of_IOT15A	NONE											D7		
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE				B2	G16	C7	E6	K12	C7		C8	E6	C7
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE				A2	H15	A7	E7	K13	C8		D8	E7	A7
IOT17A	I/O	DQ14	0		True_of_IOT17B	NONE	82	130	130						A4		E8		
IOT17B	I/O	DQ14	0		Comp_of_IOT17A	NONE	81	129	129						A5		E9		
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE				B3	H13	D6	B4	F17	B6		B8	B4	D6
IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE				A3	J12	C6	A4	F18	A6		A8	A4	C6
IOT19A	I/O	DQ14	0		True_of_IOT19B	NONE		128	128						E8		C9		
IOT19B	I/O	DQ14	0		Comp_of_IOT19A	NONE									E9		D9		
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE					H14		B5	H13	D9		F9	B5	
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE					H16		A2	H14	D10		G9	A2	
IOT21A	I/O	DQS14	0		True_of_IOT21B	NONE				B4			B6	H15	B7	D7	B9	B6	
IOT21B	I/O	DQS14	0		Comp_of_IOT21A	NONE				A4			A6	H16	A7	D8	A9	A6	
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE		125	125	B5	J16	B8		G16	C9		F10		B8
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE				A5	J14	A8		G18	C10		E10		A8
IOT23A	I/O	DQ14	0		True_of_IOT23B	NONE		126	126				B7		B8	A8	D10	B7	
IOT23B	I/O	DQ14	0		Comp_of_IOT23A	NONE		124	124				A7		A8	A9	C10	A7	
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE				B6	J15	C9	F8	J13	A9	B7	B10	F8	C9
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE				A6	K16	A9	E8	K14	A10	A7	A10	E8	A9
IOT25A	I/O	DQ14	0		True_of_IOT25B	NONE							C8		E10	B6	G11	C8	
IOT25B	I/O	DQ14	0		Comp_of_IOT25A	NONE									E11	A6	F11		
IOT26A	I/O	DQ14	0		True_of_IOT26B	TRUE							B8	L12	A11	C6	B11	B8	
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE							A8	L13	A12	C7	A11	A8	
IOT27A/GCLKT_0	I/O	DQ14	0	GCLKT_0	True_of_IOT27B	NONE	80	123	123	B7	H11	B10	C6	K15	B11	E8	E11	C6	B10
IOT27B/GCLKC_0	I/O	DQ14	0	GCLKC_0	Comp_of_IOT27A	NONE	79	122	122	A7	J13	A10	D8	K16	B12	E9	D11	D8	A10
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE					L15	C4		F15	D5		B1		C4
IOT2B	I/O	DQ15	0		Comp_of_IOT2A	TRUE		141	141			A4		F16	D6		A2		A4
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	121	D8	K14	E7	D9	L15	D11	D9	B12	D9	E7
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	120	C8	K15	E8	C9	L16	D12	C9	A12	C9	E8
IOT31A	I/O	DQ13	1		True_of_IOT31B	NONE								H17	C11		D12		
IOT31B	I/O	DQ13	1		Comp_of_IOT31A	NONE								H18	C12		E12		
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE				B8	J11	E10	B10	J16	E12		G12	B10	E10
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE				A8	L12	C10	A10	J18	E13		F12	A10	C10
IOT33A	I/O	DQ13	1		True_of_IOT33B	NONE									A13		C13		
IOT33B	I/O	DQ13	1		Comp_of_IOT33A	NONE									A14		D13		
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75			B9	L16		B11	L17	A15		E13	B11	
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74			A9	L14		A11	L18	B15		F13	A11	
IOT35A	I/O	DQ13	1		True_of_IOT35B	NONE								K17	C13		C14		
IOT35B	I/O	DQ13	1		Comp_of_IOT35A	NONE								K18	D13		D14		
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE					K13		B12	M16	C14		A14	B12	
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE					K12		A12	M18	C15		B14	A12	

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOT37A	I/O	DQS13	1		True_of_IOT37B	NONE				B10				N15	A16	C10	E14		
IOT37B	I/O	DQS13	1		Comp_of_IOT37A	NONE				A10				N16	B16	B10	E15		
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	119	B11	K11		E10	N17	A17	C11	A15	E10	
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	118	A11	L13		E11	N18	B17	B11	B15	E11	
IOT39A	I/O	DQ13	1		True_of_IOT39B	NONE									D14		A16		
IOT39B	I/O	DQ13	1		Comp_of_IOT39A	NONE									D15		B17		
IOT3A	I/O	DQ15	0		True_of_IOT3B	NONE									E6	A4	E6		
IOT3B	I/O	DQ15	0		Comp_of_IOT3A	NONE									E7	A5	F7		
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	117	B12	M14	D8	B14	P17	A18		C15	B14	D8
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	116	A12	M15	C8	A14	P18	A19		D15	A14	C8
IOT41A	I/O	DQ13	1		True_of_IOT41B	NONE									C16	A10	C17		
IOT41B	I/O	DQ13	1		Comp_of_IOT41A	NONE									C17	A11	D16		
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	115	D11		C11	B13	U17			A13	B13	C11
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	114	C11		A11	A13	U18			B13	A13	A11
IOT43A	I/O	DQ13	1		True_of_IOT43B	NONE									A20	D10	E16		
IOT43B	I/O	DQ13	1		Comp_of_IOT43A	NONE									A21	E11	D17		
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71				D14	F9	D12	T17	C18		A17	D12	F9
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70				E15	D9	D11	T18	C19		B18	D11	D9
IOT45A	I/O	DQ13	1		True_of_IOT45B	NONE							D14			C8	A19	D14	
IOT45B	I/O	DQ13	1		Comp_of_IOT45A	NONE							C14			B9	B20	C14	
IOT48A	I/O	DQS12	1		True_of_IOT48B	TRUE		113	113		N15	B12	B9	M14	D16		A18	B9	B12
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	112		P16	A12	A9	N14	E16		B19	A9	A12
IOT49A	I/O	DQ12	1		True_of_IOT49B	NONE											C18		
IOT49B	I/O	DQ12	1		Comp_of_IOT49A	NONE											D18		
IOT4A	I/O	DQ15	0		True_of_IOT4B	TRUE	86	140	140		D16	B5	D3	C17	D4	A2	C3	D3	B5
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139	139		E14	A5	C3	C18	C4	A3	C4	C3	A5
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE	69	111	111			C13	E9		E14		G14	E9	C13
IOT50B	I/O	DQ12	1		Comp_of_IOT50A	TRUE		110	110			A13			E15		F14		A13
IOT51A	I/O	DQ12	1		True_of_IOT51B	NONE									D17		F15		
IOT51B	I/O	DQ12	1		Comp_of_IOT51A	NONE									D18		G15		
IOT52A	I/O	DQ12	1		True_of_IOT52B	TRUE					N16	F10	A15	L14			A20	A15	F10
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE					N14	E11	F11	M13			B21	F11	E11
IOT53A	I/O	DQ12	1		True_of_IOT53B	NONE									F16		C19		
IOT53B	I/O	DQ12	1		Comp_of_IOT53A	NONE									F17		C20		
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE					P15	B14	F9	P15	A22	D11	A21	F9	B14
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE					R16	A14	F10	P16	B22	D12	B22	F10	A14
IOT55A	I/O	DQ12	1		True_of_IOT55B	NONE						D11			E17		F16		D11
IOT55B/JTAGSEL_N	I/O	DQ12	1	JTAGSEL_N	Comp_of_IOT55A	NONE						D12	C11	R16	E18		E17	C11	D12
IOT5A	I/O	DQ15	0		True_of_IOT5B	NONE					C16					C3	B2		
IOT5B	I/O	DQ15	0		Comp_of_IOT5A	NONE					D15					B3	A3		
IOT6A	I/O	DQ15	0		True_of_IOT6B	TRUE	84	138	138		E16		D6	F14	F6	D4	B4	D6	
IOT6B	I/O	DQ15	0		Comp_of_IOT6A	TRUE	83	137	137		F15		D5	G14	F7	C4	A5	D5	
IOT7A	I/O	DQ15	0		True_of_IOT7B	NONE		136	136						C5	C5	F8		
IOT7B	I/O	DQ15	0		Comp_of_IOT7A	NONE		135	135						C6	B5	G8		
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE					F13		F7	D17		E6	B3	F7	
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE					G12		F6	D18		D6	A4	F6	
IOT9A	I/O	DQS15	0		True_of_IOT9B	NONE					F14	D5	B3		B1	D5	D5	B3	D5
IOT9B	I/O	DQS15	0		Comp_of_IOT9A	NONE					F16	C5	A3		A1	E5	C5	A3	C5
NC	N/A		N/A									P14	L5			G6		F12	P14

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
NC	N/A		N/A										F12			G11		L5	
NC	N/A		N/A													K11			
NC	N/A		N/A													K6			
VCC	Power		N/A				1										K13		G7
VCC	Power		N/A				22										N13		G9
VCC	Power		N/A				45										K12		H8
VCC	Power		N/A				66										L12		J9
VCC	Power		N/A								A1	G7			G7		M12		K10
VCC	Power		N/A								A16	G9			G8		N12		K8
VCC	Power		N/A								G7				G9		K11		
VCC	Power		N/A								K10	J9			G12		L11		
VCC	Power		N/A								T1	K10			G13		M11		
VCC	Power		N/A								T16	K8			G14		N11		
VCC	Power		N/A									H8			G10		K10		
VCC	Power		N/A												G16		N10		
VCC	Power		N/A												G11				
VCC	Power		N/A												G15				
VCC	Power		N/A												H16				
VCC	Power		N/A												H7				
VCC	Power		N/A												J16				
VCC	Power		N/A												J7				
VCC	Power		N/A												L16				
VCC	Power		N/A												L7				
VCC	Power		N/A												M16				
VCC	Power		N/A												M7				
VCC	Power		N/A												P16				
VCC	Power		N/A												P7				
VCC	Power		N/A												R16				
VCC	Power		N/A												R7				
VCC	Power		N/A												T10				
VCC	Power		N/A												T11				
VCC	Power		N/A												T12				
VCC	Power		N/A												T13				
VCC	Power		N/A												T14				
VCC	Power		N/A												T15				
VCC	Power		N/A												T16				
VCC	Power		N/A												T7				
VCC	Power		N/A												T8				
VCC	Power		N/A												T9				
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							E10									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							E5									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							E6									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							E9									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							F10									

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							F5									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							F6									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							F9									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							J5									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							J6									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							J9									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							K10									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							K5									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							K6									
VCC/VCCPLLL0/VCCPLLL1/VCCPLLR0/VCCPLLR1	Power		N/A							K9									
VCC/VCCPLLL1	Power		N/A					1	1										
VCC/VCCPLLL1	Power		N/A					36	36										
VCC/VCCPLLL1	Power		N/A					73	73										
VCC/VCCPLLL1	Power		N/A					108	108										
VCC/VCCPLLL/VCCPLLR	Power		N/A										G6	G7		J10		G6	
VCC/VCCPLLL/VCCPLLR	Power		N/A										G7	H11		K7		G7	
VCC/VCCPLLL/VCCPLLR	Power		N/A										G8	H9		F5		G8	
VCC/VCCPLLL/VCCPLLR	Power		N/A										H6	J10		K9		G9	
VCC/VCCPLLL/VCCPLLR	Power		N/A										H11	J8		G8		G10	
VCC/VCCPLLL/VCCPLLR	Power		N/A										K7	K11		H7		H6	
VCC/VCCPLLL/VCCPLLR	Power		N/A										G9	K9		G10		H11	
VCC/VCCPLLL/VCCPLLR	Power		N/A										D13	L10		M10		K7	
VCC/VCCPLLL/VCCPLLR	Power		N/A										G10	L8		L9		N4	
VCC/VCCPLLL/VCCPLLR	Power		N/A										N4	M12		L8		D13	
VCC/VCCPLLL/VCCPLLR	Power		N/A											M7		M7			
VCCO0	Power		N/A				78							J14		E7	C7	C4	D7
VCCO0	Power		N/A					127	127					E17		F7	H9	C7	B4
VCCO0	Power		N/A							C10	H10	B4	C4	G15	B10		G10	A1	B9
VCCO0	Power		N/A							C4		B9	C7		F11		H11		
VCCO0	Power		N/A								E13	D7	A1		B5				
VCCO1	Power		N/A				67	109	109					R17		F9	C12	C10	D10
VCCO1	Power		N/A							C5	J10	D10	A16	J17	B14	E10	H12	C13	B13
VCCO1	Power		N/A							C9	M13		C10	M15	B19		G13	A16	
VCCO1	Power		N/A									B13	C13		F12		H14		
VCCO1	Power		N/A														C16		
VCCO2	Power		N/A							D12	N12	D15	E14		E21			E14	D15
VCCO2	Power		N/A							E12		G13	G14	P9	K21	H11		G14	G13
VCCO2	Power		N/A							G11		J15		R12	L17	G12			J15
VCCO2	Power		N/A											U14					

Note!
[1] IOR30A shares pin T15 with IOR30B in package UG324.
[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VCCO3	Power		N/A				58	91	91					R6		N7	M15	K14	K13
VCCO3	Power		N/A					77	77					U4		F12	N15	M14	N15
VCCO3	Power		N/A							G12	K8	K13	K14	U9	M17	N8	P15		R13
VCCO3	Power		N/A							K11	N5	N15	M14		P21		M18		
VCCO3	Power		N/A							K12		R13			W21		V20		
VCCO4	Power		N/A				44					N10		J5		J11	R14	P10	N10
VCCO4	Power		N/A					55	55			R8		M4		M13	W16	P13	R8
VCCO4	Power		N/A							M10	J7		P13	R2	AA18		R13	T16	
VCCO4	Power		N/A							M5			T16		U12		R12		
VCCO4	Power		N/A								M4		P10		AA13				
VCCO5	Power		N/A				23	37	37			N7		E2		N9	W11	P4	N7
VCCO5	Power		N/A							M6	E4	R4	P4	G4	U11	N10	R11	P7	R4
VCCO5	Power		N/A							M9	H7		P7	J2	AA4	N11	R10	T1	
VCCO5	Power		N/A										T1		AA9	N5	R9		
VCCO5	Power		N/A													N12	W7		
VCCO5	Power		N/A													N6			
VCCO6	Power		N/A							E3		N2	M3	B5	N2	J6		K3	K4
VCCO6	Power		N/A							E4		J2		D7	V2	M4		M3	N2
VCCO6	Power		N/A							G3	D5	K4	K3	B10	M6				J2
VCCO7	Power		N/A				3	5	5					B15		H6			G4
VCCO7	Power		N/A					19	19					D13		G5			D2
VCCO7	Power		N/A							H3	G9	G4		E10	D2				
VCCO7	Power		N/A							K3	D12				J2				
VCCO7	Power		N/A							K4		D2			L6				
VCCO6/VCCO7	Power		N/A														M3		
VCCO6/VCCO7	Power		N/A														N8		
VCCO6/VCCO7	Power		N/A														J8		
VCCO6/VCCO7	Power		N/A														P8		
VCCO6/VCCO7	Power		N/A														V3		
VCCO6/VCCO7	Power		N/A														L8		
VCCO6/VCCO7	Power		N/A														M8		
VCCO6/VCCO7	Power		N/A														K8		
VCCO6/VCCO7	Power		N/A														F3		
VCCPLLL	Power		N/A								G10	J7			N7				J7
VCCPLLL	Power		N/A												K7				
VCCPLLL0	Power		N/A					8	8								F4		
VCCPLLL1	Power		N/A				14										T6		
VCCPLLR	Power		N/A								K7	H10			N16				H10
VCCPLLR	Power		N/A												K16				
VCCPLLR0	Power		N/A					104	104								G21		
VCCPLLR1	Power		N/A				50	81	81								T20		
VCCX	Power		N/A							D7		L9		B1	U14	F8			E5
VCCX	Power		N/A							E7	K9	E5		B17	F14	H12			F11
VCCX	Power		N/A							G10	G8	F11		E14	F9	L10			F8
VCCX	Power		N/A							G9		F8		E5	J6	H5			G10
VCCX	Power		N/A							H5		G10		E9	J17	K5			H6
VCCX	Power		N/A							H6		H6		G10	P6	K12			J10
VCCX	Power		N/A							K7		J10		J12	P17				L6
VCCX	Power		N/A							L7		L6		K7	U9				L9

Note!
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[2] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VCCX	Power		N/A											M9					
VCCX	Power		N/A											P10					
VCCX	Power		N/A											P14					
VCCX	Power		N/A											P5					
VCCX/VCCO2																	F20		
VCCX/VCCO2																	K15		
VCCX/VCCO2																	L15		
VCCX/VCCO2																	J15		
VCCX/VCCO2/VCCO6	Power		N/A				12	31	31										
VCCX/VCCO2/VCCO6	Power		N/A				64	103	103										
VCCX/VCCO7	Power		N/A										E3					E3	
VCCX/VCCO7	Power		N/A										G3					G3	
VSS	Ground		N/A				2	2	2							R13	A1	H7	A1
VSS	Ground		N/A				21	35	35							A1		H8	A16
VSS	Ground		N/A				24									N2		H9	B11
VSS	Ground		N/A				43									J2		H10	B7
VSS	Ground		N/A				46	74	74									J7	D13
VSS	Ground		N/A				65	107	107					A1		M5		J8	D4
VSS	Ground		N/A				68							A18		T4		J9	E9
VSS	Ground		N/A					17	17					B13				J10	G15
VSS	Ground		N/A					53	53					B7		B4		B2	G2
VSS	Ground		N/A					89	89					C16		H9		B15	G8
VSS	Ground		N/A							A1	B2	A1	H7	C3	B4	T1		C5	H12
VSS	Ground		N/A							A14	B15	A16	H8	D10	AA5	N13	A22	C12	H7
VSS	Ground		N/A							C2	C3	B11	H9	D5	AA10	R4	AB22	D7	H9
VSS	Ground		N/A							C3	C14	B7	H10	E15	AA14	M12	F21	D10	J5
VSS	Ground		N/A							C6	D4	D13	J7	G12	AA19	A16	K21	E4	J8
VSS	Ground		N/A							C7	D13	D4	J8	G17	B9	E2	N21	E13	K7
VSS	Ground		N/A							D10	E5	E9	J9	G2	B13	H8	V21	G4	K9
VSS	Ground		N/A							D5	E12	G15	J10	G5	B18	R11	E18	G13	L15
VSS	Ground		N/A							D6	F6	G2	B2	H10	D21	P4	L18	K4	L2
VSS	Ground		N/A							D9	F11	G8	B15	H8	E2	D15	B16	K13	M8
VSS	Ground		N/A							E11	H8	H12	C5	J11	H8	K10	Y16	M4	N13
VSS	Ground		N/A							E8	H9	H7	C12	J15	H9	T13	H15	M13	P3
VSS	Ground		N/A							F7	J8	H9	D7	J4	H10	R9	R15	N7	R10
VSS	Ground		N/A							F8	J9	J5	D10	J9	H11	R12	J14	N10	R6
VSS	Ground		N/A							G4				K10	L10	R10	K14	P5	T1
VSS	Ground		N/A							G5	L6	J8	E4	K8	H12	L6	L14	P12	T16
VSS	Ground		N/A							G6	L11	K7	E13	L11	H13	J12	M14	R2	
VSS	Ground		N/A							G7	M5	K9	G4	L9	H14	L12	N14	R15	
VSS	Ground		N/A							G8	M12	L15	G13	M17	H15	H15	P14	E2	
VSS	Ground		N/A							H10	N4	L2	K4	M2	J8	F6	H13	H16	
VSS	Ground		N/A							H4	N13	M8	K13	M6	J9	R8	J13	H15	
VSS	Ground		N/A							H7	P3	N13	M4	N13	J10	P13	L13	M5	
VSS	Ground		N/A							H8	P14	P3	M13	R1	J11	J9	M13	E12	
VSS	Ground		N/A							H9	R2	R10	N7	R14	J12	G7	P13		
VSS	Ground		N/A							J10	R15	R6	N10	R18	J13	R5	J12		
VSS	Ground		N/A							J7		T1	P5	R4	J14	J8	P12		
VSS	Ground		N/A							J8		T16	P12	R9	J15	F10	W12		

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VSS	Ground		N/A							K8			R2	T16	J21	N4	C11		
VSS	Ground		N/A							L10			R15	U12	K2	J5	J11		
VSS	Ground		N/A							L11			E2	U6	K8	M15	P11		
VSS	Ground		N/A							L3			H16	V1	K9	T16	H10		
VSS	Ground		N/A							L5			H15	V18	K10		J10		
VSS	Ground		N/A							L6					K11	G9	L10		
VSS	Ground		N/A							L9			M5		K12	B8	M10		
VSS	Ground		N/A							M11			E12		K13	M6	P10		
VSS	Ground		N/A							M3					K14	R6	J9		
VSS	Ground		N/A							M7					K15	K8	K9		
VSS	Ground		N/A							P1					L8	J7	L9		
VSS	Ground		N/A							P14					L9	L7	M9		
VSS	Ground		N/A												F10	H10	N9		
VSS	Ground		N/A												F13	B12	P9		
VSS	Ground		N/A												F15	M11	H8		
VSS	Ground		N/A												F8	F11	R8		
VSS	Ground		N/A												H17	R7	B7		
VSS	Ground		N/A												H6	L11	Y7		
VSS	Ground		N/A												K17		E5		
VSS	Ground		N/A												K6		M4		
VSS	Ground		N/A												L11		C2		
VSS	Ground		N/A												L12		F2		
VSS	Ground		N/A												L13		L2		
VSS	Ground		N/A												L14		V2		
VSS	Ground		N/A												L15				
VSS	Ground		N/A												M10		AB1		
VSS	Ground		N/A												M11				
VSS	Ground		N/A												M12				
VSS	Ground		N/A												M13				
VSS	Ground		N/A												M14				
VSS	Ground		N/A												M15				
VSS	Ground		N/A												M8				
VSS	Ground		N/A												M9				
VSS	Ground		N/A												N10				
VSS	Ground		N/A												N11				
VSS	Ground		N/A												N12				
VSS	Ground		N/A												N13				
VSS	Ground		N/A												N14				
VSS	Ground		N/A												N15				
VSS	Ground		N/A												N21				
VSS	Ground		N/A												N6				
VSS	Ground		N/A												N8				
VSS	Ground		N/A												N9				
VSS	Ground		N/A												P10				
VSS	Ground		N/A												P11				
VSS	Ground		N/A												P12				
VSS	Ground		N/A												P13				
VSS	Ground		N/A												P14				
VSS	Ground		N/A												P15				

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
VSS	Ground		N/A												P2				
VSS	Ground		N/A												P8				
VSS	Ground		N/A												P9				
VSS	Ground		N/A												R10				
VSS	Ground		N/A												R11				
VSS	Ground		N/A												R12				
VSS	Ground		N/A												R13				
VSS	Ground		N/A												R14				
VSS	Ground		N/A												R15				
VSS	Ground		N/A												R17				
VSS	Ground		N/A												R6				
VSS	Ground		N/A												R8				
VSS	Ground		N/A												R9				
VSS	Ground		N/A												U10				
VSS	Ground		N/A												U13				
VSS	Ground		N/A												U15				
VSS	Ground		N/A												U8				
VSS	Ground		N/A												V21				
VSS	Ground		N/A												W2				

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
BANK7 True LVDS Pair																			
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE						B2		B14	C2	F3	E1		B2
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE						A2		A14	C1	G3	F1		A2
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE					B11	G6		C13			H4		G6
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE					A12	G5		A13			H3		G5
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE				C1	A11	C1		B12	F1		H2		C1
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE				B1	C11	B1		A12	G1		H1		B1
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE					D10	D1		B11	H3		H5		D1
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE					E10	D3		A11	J3		J5		D3
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE				D4		K5	F2	G9	J1		J2	F2	K5
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE				D3		K6	F1	F9	K1		J1	F1	K6
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9	9	E2		E2	G2	G11	L2	H3	L7	G2	E2
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10	10	E1		E1	G1	F10	L1	J3	K5	G1	E1
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE				F4		L4		C10	K4		K2		L4
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE				F3		L5		A10	L4		K1		L5
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE				F2		H4		D11	P1		L1		H4
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE				F1		H3		C11	N1		M2		H3
IOL2A	I/O	DQ0	7		True_of_IOL2B	TRUE		3	3		B14	B3	D1	B16	E5	D1	G7	D1	B3
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4		A15	A3	C2	A16	F5	E1	F6	C2	A3
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE						F6	F3		G6		E4	F3	F6
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE						F5	F4		G5		F5	F4	F5
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE						E4		D14	E4		C1		E4
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE						E3		C14	E3		D2		E3
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE					B13		D4	F13	F3	J4	D1	D4	
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE					A14		E5	E13	G3	K4	E2	E5	
BANK6 True LVDS Pair																			
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25	25	G2	C8	K3	M2	D9	M4	K1	M1	M2	K3
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26	26	G1	A8	J4	M1	C9	M3	L1	N1	M1	J4
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE				J2	F9	F2	J2	B8	N4		M6	J2	F2
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE				J1	E11	F1	J1	A8	N3		M5	J1	F1
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27	27	J4	B9	G3	K6	D8	T2	M1	P2	K6	G3
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28	28	J3	A10	G1	L6	C8	R2	N1	R1	L6	G1
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE				K2	F8		K2	B6	P3	M3	P4	K2	
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE				K1	D9		K1	A6	R3	N3	N5	K1	
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE					D8	J3	N2	C7	Y1		R2	N2	J3
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE					E9	J1	N1	A7	Y2		T1	N1	J1
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE					B7		K5	G8			T2	K5	
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE					C7		L4	F8			U1	L4	
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	32				P2	F7			R5	P2	
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	33				P1	E6			P7	P1	
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE								C5	V3		T3		
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE								A5	W3		T4		
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15			M2	C4	R2		B3	P5		U2		R2
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16			M1	B5	R1		A3	R5		V1		R1
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17					L3					Y1		L3
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18					L1					AA1		L1
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19					P2		B2		R2	W3		P2
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20					P1		A2		R3	Y2		P1

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE					E6	M5		D4	V5		Y3		M5
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE					D7	N4		C4	U5		W4		N4
BANK5 True LVDS Pair																			
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	44		E2	P4	N3	D2			V8	N3	P4
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	45		E3	T4	P3	D1			U8	P3	T4
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	46		C1		R3	F4	Y6	P12	AA8	R3	
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	47		D2		T3	F3	AA6	P11	AB8	T3	
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE				N12	E1	L8	R4	E3	W7		AA6	R4	L8
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE				P12	F2	L7	T4	E1	W8		AB6	T4	L7
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31				F4	N5	N5	H6	Y7		AA7	N5	N5
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32				G6	P5	N6	H5	Y8		AB7	N6	P5
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50	50	N10	G5	R5	M6	F2	W9		Y9	M6	R5
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51	51	P10	G4	T5	P6	F1	Y9		Y10	P6	T5
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52	52		F5	P6	R5	G3	AA7	T5	V10	R5	P6
IOB22B	I/O	DQ5	5		Comp_of_IOB22A	TRUE		54	54		H6	T6	T5	G1	AB7	T6	W10	T5	T6
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33			L8	G1	R7	R6	L7	W10		AA11	R6	R7
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34			M8	H2	T7	T6	K6	W11		AB11	T6	T7
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE					H4		L8	H4	Y10		AA10	L8	
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE					J6		M8	H3	Y11		AB10	M8	
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE					A4			C2	U6	P9	AA2		
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE					C5			C1	U7	P10	AB2		
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE					A3	M4		F6	V6		AA3		M4
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE					B4	M3		F5	V7		AB3		M3
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE	25	40	40					E4	Y4		U7		
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	41					D3	Y5		T8		
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27				B1	M6	R8	H7		T12	AA5	R8	M6
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28				C2	N6	T8	G6		T11	AB5	T8	N6
BANK4 True LVDS Pair																			
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	56	N7	L2	P8	R9	L2	AB12	K15	AB12	R9	P8
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	57	P7	M1	T8	T9	L1	AA12	L15	AA12	T9	T8
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE					H3		K9	H2	W12		V13	K9	
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE					H1		L9	H1	W13		U13	L9	
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	60	N6	J2	M9	M9	J3	AB15		Y13	M9	M9
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	61	P6	K1	N8	N9	J1	AA15		W13	N9	N8
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE					K3	R9	R10	K2	AB16		T13	R10	R9
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE					K2	T9	T10	K1	AA16		T14	T10	T9
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	62	L4	L1	L10	R11	P2	V14	L16	Y14	R11	L10
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	63	M4	L3	M10	T11	P1	V15	M16	W14	T11	M10
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	64	N4	K5	N9	R12	M3	AA17		Y15	R12	N9
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	65	P4	L4	P9	T12	M1	Y17		W15	T12	P9
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	66		M3		L10	N2			V15	L10	
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE		67	67		N1		K10	N1			U15	K10	
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE					R1			T2	Y16		Y17		
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE					P2			T1	W16		V16		
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	68		R3		R13	U2	Y19		AB18	R13	
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	69		T2		T13	U1	Y18		AA18	T13	
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE					P5		M10	L6	V16		T9	M10	
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE					R5		N11	M5	U16		U9	N11	

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE					R4	N12	T14	P4		R16	AB20	T14	N12
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE					T3	P12	T15	P3		R15	AA20	T15	P12
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE					R6	M12	P14	N4	V17		AB21	P14	M12
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE					T5	M11	L11	N3	V18		AA21	L11	M11
BANK3 True LVDS Pair																			
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE				H13	T7	J13	M15	R8	P22		M22	M15	J13
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE				H14	R8	K14	M16	T8	R22		M21	M16	K14
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE		143	143		C15		G12	N12	U21		M19	G12	N11
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE	9	20	20	N1	B10		H5	V2	T21		P21	H5	T2
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	96	N11	P10	P10	H2	R13	P19	H13	N17		
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61	95	95	P11	R10	T10	C1	T13	P20	H14	N18		
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N/D3	True_of_IOR35B	TRUE	57	92	92	P9	R9	K12		R15	R20		R22		
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	90	L12	T10	K11		V9	R21		R21		
IOR38A/DIN/CLKHOLD_N	I/O	DQ9	3	DIN/CLKHOLD_N	True_of_IOR38B	TRUE	54	86	86	J13	T9	J14		U8	T20	G14	T22	H2	P10
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	85	J14	P9	J16		V8	U20	G13	T21	C1	T10
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE				J11	N8	K15		U7			P17		T3
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE				J12	L9	K16		V7			P16		K11
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84	84	K13	P8	M15	K12	T6			V22	K12	M15
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83	83	K14	T8	M16	L12	V6			W22	L12	M16
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE				L13	M6	L14	M12	R7	Y22			M12	K15
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE				L14	L8	L16	N13	T7	AA22			N13	K16
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE					M7	R15	J12	R3	Y21		T19	J12	M13
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE					N7	R16	J14	T3	AA21		T18	J14	M14
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80	80		R7		L15			F16	T17	L15	
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79	79		P7		L16			F15	U20	L16	
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE						T14	N15	N5		B15	U19	N15	T14
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE						T13	N16	P6		C14	U18	N16	T13
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE					P6	R12	R16	T4	T17		V18	R16	R12
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE					T6	T12	P16	V4	U17		W20	P16	T12
BANK2 True LVDS Pair																			
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE					R12	F13	D15	U11	G19			D15	F13
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE					P13	F14	D16	V11	G20			D16	F14
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE				C12		C15	F13	R11			H22	F13	C15
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE				C13		C16	F14	T11			H21	F14	C16
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE						E15			H20		H19		E15
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE						E16			H21		H18		E16
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE				E13	R11	F15		T12	F22		J18		F15
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE				E14	T12	F16		V12	E22		J19		F16
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	102		R13	G14		N10	H22		J16		G14
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	101		T14	G16		P11	J22		J17		G16
IOR22A	I/O	DQS10	2		True_of_IOR22B	TRUE		100	100	F11	M10	H15		M10	K19		K19		H15
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	99	F12	N11	H16		N9	L19		K18		H16
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE				G13	T11	G12	F15	R10	L21	J13	K17	F15	G12
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE				G14	P11	H11	F16	T10	M21	J14	K16	F16	H11
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	14	B13	A7	C14	H3	A17	N20	B1	L20	H3	C14

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	16	A13	A6	C12	H4	D15	M20	C1	L21	H4	C12
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE						E13		U16	F18		C22		E13
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE						E12		V16	F19		G16		E12
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE						B15		U15	G17		D22		B15
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE						B16		V15	G18		D21		B16
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE						F12	C15		D19		E22	C15	F12
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE						G11	C16		D20		E21	C16	G11
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE					P12			U13	B21		E19		
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE					T13			V13	C21		E20		
BANK1 True LVDS Pair																			
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	121	D8	K14	E7	D9	L15	D11	D9	B12	D9	E7
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	120	C8	K15	E8	C9	L16	D12	C9	A12	C9	E8
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE				B8	J11	E10	B10	J16	E12		G12	B10	E10
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE				A8	L12	C10	A10	J18	E13		F12	A10	C10
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75			B9	L16		B11	L17	A15		E13	B11	
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74			A9	L14		A11	L18	B15		F13	A11	
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE					K13		B12	M16	C14		A14	B12	
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE					K12		A12	M18	C15		B14	A12	
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	119	B11	K11		E10	N17	A17	C11	A15	E10	
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	118	A11	L13		E11	N18	B17	B11	B15	E11	
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	117	B12	M14	D8	B14	P17	A18		C15	B14	D8
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	116	A12	M15	C8	A14	P18	A19		D15	A14	C8
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	115	D11		C11	B13	U17			A13	B13	C11
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	114	C11		A11	A13	U18			B13	A13	A11
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71				D14	F9	D12	T17	C18		A17	D12	F9
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70				E15	D9	D11	T18	C19		B18	D11	D9
IOT48A	I/O	DQS12	1		True_of_IOT48B	TRUE		113	113		N15	B12	B9	M14	D16		A18	B9	B12
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	112		P16	A12	A9	N14	E16		B19	A9	A12
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE		111	111			C13			E14		G14		C13
IOT50B	I/O	DQ12	1		Comp_of_IOT50A	TRUE		110	110			A13			E15		F14		A13
IOT52A	I/O	DQ12	1		True_of_IOT52B	TRUE					N16	F10	A15	L14			A20	A15	F10
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE					N14	E11	F11	M13			B21	F11	E11
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE					P15	B14	F9	P15	A22	D11	A21	F9	B14
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE					R16	A14	F10	P16	B22	D12	B22	F10	A14
BANK0 True LVDS Pair																			
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	134		F12	B6		H12			B5		B6
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	133		G13	A6		G13			A6		A6
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	132		G11	F7		E16	A2		B6		F7
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	131		H12	E6		E18	A3		A7		E6
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE				B2	G16	C7	E6	K12	C7		C8	E6	C7
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE				A2	H15	A7	E7	K13	C8		D8	E7	A7
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE				B3	H13	D6	B4	F17	B6		B8	B4	D6
IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE				A3	J12	C6	A4	F18	A6		A8	A4	C6
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE					H14		B5	H13	D9		F9	B5	
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE					H16		A2	H14	D10		G9	A2	
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE				B5	J16	B8		G16	C9		F10		B8
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE				A5	J14	A8		G18	C10		E10		A8
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE				B6	J15	C9	F8	J13	A9	B7	B10	F8	C9

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88	LQ144	EQ144	MG196	PG256	PG256S	PG256C	UG324	PG484	PG256E	UG484	PG256CF	PG256SF
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE				A6	K16	A9	E8	K14	A10	A7	A10	E8	A9
IOT26A	I/O	DQ14	0		True_of_IOT26B	TRUE							B8	L12	A11	C6	B11	B8	
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE							A8	L13	A12	C7	A11	A8	
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE						C4		F15	D5		B1		C4
IOT2B	I/O	DQ15	0		Comp_of_IOT2A	TRUE						A4		F16	D6		A2		A4
IOT4A	I/O	DQ15	0		True_of_IOT4B	TRUE	86	140	140		D16	B5	D3	C17	D4	A2	C3	D3	B5
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139	139		E14	A5	C3	C18	C4	A3	C4	C3	A5
IOT6A	I/O	DQ15	0		True_of_IOT6B	TRUE	84	138	138		E16		D6	F14	F6	D4	B4	D6	
IOT6B	I/O	DQ15	0		Comp_of_IOT6A	TRUE	83	137	137		F15		D5	G14	F7	C4	A5	D5	
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE					F13		F7	D17		E6	B3	F7	
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE					G12		F6	D18		D6	A4	F6	

Note!
[1] It is recommended to set Bank VCCO of True LVDS to 2.5V.
[2] It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions of Package QN88 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL1	Left PLL 1 supply voltage	0.95V	1.05V
VCCPLLR1	Right PLL 1 supply voltage	0.95V	1.05V
VCCX/VCCO2/VCCO6	I/O Bank voltage, VCCX/VCCO2/VCCO6 are internally short-circuited.	2.7V	3.465V
VCCO0, VCCO1, VCCO3, VCCO4, VCCO5, VCCO7	I/O Bank voltage	1.14V	3.465V
Recommended Operating Conditions of Package LQ144/EQ144 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC/VCCPLLL1	VCCPLLL1 and VCC are internally short-circuited.	0.95V	1.05V
VCCPLLL0	Left PLL 0 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCX/VCCO2/VCCO6	I/O Bank voltage, VCCX/VCCO2/VCCO6 are internally short-circuited.	2.7V	3.465V
VCCO0, VCCO1, VCCO3, VCCO4, VCCO5, VCCO7	I/O Bank voltage	1.14V	3.465V
Recommended Operating Conditions of Package MG196 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC/VCCPLLL0/VCCPLLL1	Core voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V
Recommended Operating Conditions of Package PG256/PG484 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V

Note!
[1] It is recommended to set Bank VCCO of True LVDS to 2.5V.
[2] It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions of Package PG256S in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO4/VCCO5	VCCO4/VCCO5 are internally connected, supply voltage should be the	1.14V	3.465V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V

Recommended Operating Conditions of Package PG256C in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6	I/O Bank voltage	1.14V	3.465V
VCCX/VCCO7	VCCX/VCCO7 are internally connected.	2.7V	3.465V

Recommended Operating Conditions of Package UG324 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V

Note!
[1] It is recommended to set Bank VCCO of True LVDS to 2.5V.
[2] It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions of Package PG256E in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V

Recommended Operating Conditions of Package UG484 in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO3, VCCO4, VCCO5	I/O Bank voltage	1.14V	3.465V
VCCO6/VCCO7	I/O Bank voltage, VCCO6 and VCCO7 are internally short-circuited.	1.14V	3.465V
VCCX/VCCO2	Auxiliary voltage and VCCO2 are internally connected.	2.7V	3.465V

Recommended Operating Conditions of Package PG256CF in GW2A-18			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6	I/O Bank voltage	1.14V	3.465V
VCCX/VCCO7	VCCX/VCCO7 are internally connected.	2.7V	3.465V

Note!
[1] It is recommended to set Bank VCCO of True LVDS to 2.5V.
[2] It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions of Package PG256SF in GW2A-18

Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL supply voltage	0.95V	1.05V
VCCPLLR	Right PLL supply voltage	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7	I/O Bank voltage	1.14V	3.465V
VCCX	Auxiliary voltage	2.7V	3.465V