CS311: Computer Organization

Fall 2018

Classroom E11 Terman Hall

Course Web Page

Instructor Prof. Soontae Kim (김순태)

Email **kims@kaist.ac.kr**

Web: http://ecl.kaist.ac.kr

Office N1 Building room 903

Telephone 350-3554

Office Hour TBA

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Objective of the Course

We will study the internals of modern computer systems and how to design them. We will first look at instruction set design issues. Then, we will design the datapath and memory system. Parallel processors are also studied. After taking this course, you should be able to understand the organization and design issues of modern computer systems and to explain them to other non-major people.

Prerequisites

Logic design or System programming (mandatory), experience with high-level language(C/C++) programming, basic math

Textbook

Patterson and Hennessy, Computer Organization and Design The hardware/Software Interface, 5th Ed., Elsevier Korea LLC (Asian edition).

Grading Policy (tentative)

Homework assignments	20%
Project	20%
Midterm exam	25%
Final exam	30%
Attendance	5% (-1 for missing a class)

Cheating is **not allowed** in all exams and homework assignments. **You will be given zero points for cheating. Do not look at the solutions you obtained on the Internet for homework assignments. Do not make noise and move around not to annoy me and other students. If you do so, I may ask you to leave the classroom.**

Course Schedule (subject to change)

Week	Date	Topic	Reading (textbook)	Assignments
1		Class introduction		
		Computer abstractions and technology	Chapter1	
2		Instruction set architecture(ISA)	Chapter 2.1 ~2.3	
		No Class		Holiday
3		No Class		Holiday
		MIPS ISA	Chapter 2.4 ~2.7	
4		MIPS ISA II	Chapter 2.8 ~2.10	
		MIPS assembly programming	Section 2.11 ~ 2.13	Hw#1
5		Review - combinational logic	Appendix B	
		Integer arithmetic	Section 3.1 ~ 3.4	
6		Floating-point arithmetic	Section 3.5	
		Review - sequential logic	Appendix C	
7		Building a datapath	Section 4.1 ~ 4.3	Hw#2
		Datapath – simple implementation	Section 4.4	
8		Midterm exam	Chapter 1 ~ 4.4, Appendix B	
9		Pipelining – overview	Section 4.5	
		Pipelining – datapath & control	Section 4.6	
10		Pipelining – data hazards	Section 4.7	
		Pipelining – control hazards	Section 4.8	
11		Pipelining – exceptions	Section 4.9	
		Instruction-level parallelism	Section 4.10	Hw#3
12		Memory hierarchy – basics	Section 5.1, 5.2	
		Memory hierarchy – cache performance	Section 5.3	
13		No Class		Undergraduate Exam
		Memory hierarchy – cache performance II	Section 5.4	
14		Memory hierarchy – virtual memory	Section 5.5~5.7	
		Memory hierarchy – common framework	Section 5.8~5.10	
15		Memory hierarchy – real stuffs	Section 5.13	Hw#4
		Parallel processing, SIMD, multithreading	Section 6.1 ~ 6.4	
16		Final exam	Chapter 4.5~6.4	