Computer organization, Spring 2018

Lab 6 : Pipeline CPU II

Due : 2018/06/23 (SAT) 23:59:59

1. Goal

In Lab6, you need to modify the CPU designed in Lab5 and implement an advanced version pipelined CPU which can handle hazard.

2. Demands

A. Please use ModelSim or Xilinx as your HDL simulator.

B. One person forms a group. Please attach your name and student ID as comments in the top of the file. (Ex. Lab6_Student ID.zip) The type of compressed file must be "zip". (Other form of file will get -10%.)
The assignment you upload on E3 must have the form of **"Lab6_student ID.zip".**

C. Testbench .v is supplied.

3. Data/Control Hazard description

a. Code:
Data hazard:

ADD, ADDI, SUB, AND, OR, NOR, LUI, SLT, SLL, LW and SW.

- Need to implement **Hazard Detection** and **Forwarding**

(i.e. Forwarding.v and HazardDetectionUnit.v)

- Need to **stall** pipelined CPU if it detects **load-use.**
- Need to **forward** data if instructions have data dependency.

(Bonus) Control hazard:

BEQ, BNE, JUMP

- **Modify Hazard Detection Unit**. Once a branch instruction is taken or a jump instructions performed, you should flush the IF/ID, ID/EX, and EX/MEM pipeline registers, and then fetch the correct instruction from the new PC value

b. Testbench :

Please use **CO_P6_test_1.txt** to test **data hazard, CO_P6_test_2.txt** to test **control hazard**.

CO_P6_test_1.txt

```
addi   $1, $0, 5
addi   $2, $0, 2
addi   $3, $0, 11
addi   $4, $0, 6
sw     $1, 4($0)
addi   $7, $1, 10
lw     $5, 4($0)
and    $8, $5, $3
```

Result:
r1=5; r2=2; r3=11; r4=6; r5=5; r7=15;r8=1; r29=128;

data_mem[1]=5;

others are 0.

CO_P6_test_2.txt

```
        addi   $1, $0, 2
        addi   $2, $0, 2
        addi   $3, $0, 2
        addi   $4, $0, 4
        addi   $5, $0, -1
        beq    $1, $2, L1
        slt    $9  $2, $4
        sw     $1, 4($0)
        or     $10  $1, $4
L1:     addi   $6, $0, 2
        addi   $1, $1, 3
        addi   $2, $2, 3
        and    $7, $3, $4
        sub    $8, $5, $3
```

Result:

r1=5; r2=5; r3=2; r4=4; r5=-1; r6=2; r7=0; r8=-3; r29=128;

data_mem[1]=0

others are 0.

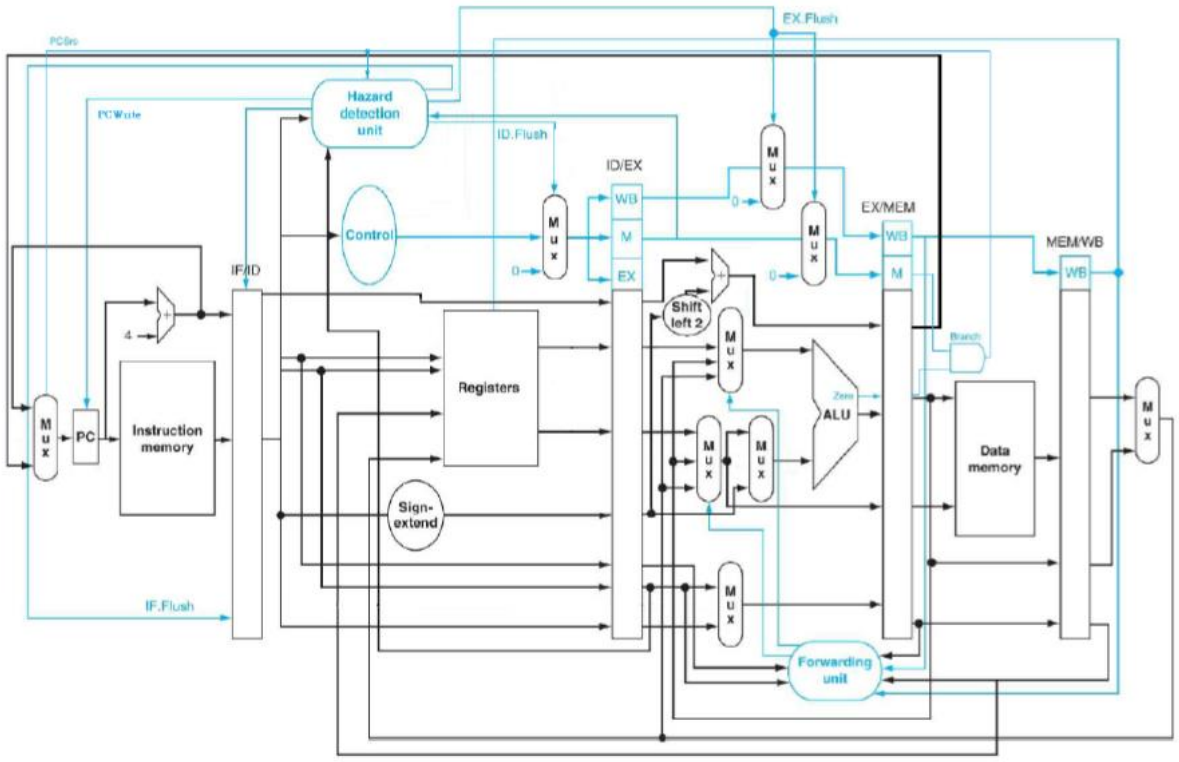
c. Report:

The context must include and the report is at most 3 pages.

:

1. HDL simulator you used
2. Finished part
3. Architecture diagrams
4. Hardware module analysis
5. Problems you met and solutions
6. Summary

4. Architecture



5. Grade

Total score: 100+20 bonus pts. COPY WILL GET A 0 POINT!

a. Data hazard: 80 pts
b. (bonus) Control hazard: 20 pts
c. Report: 20 pts

d. incorrect file form: -10pts

6. Hand in your assignment

Please upload the assignment to the E3.
Put all of *.v source files and report into same compressed file.

(Use your student ID to be the name of your compressed file and must have the form of "Lab6_student ID.zip")

7. Q&A

If you have any question, just send email to TA (coco335715@gmail.com).