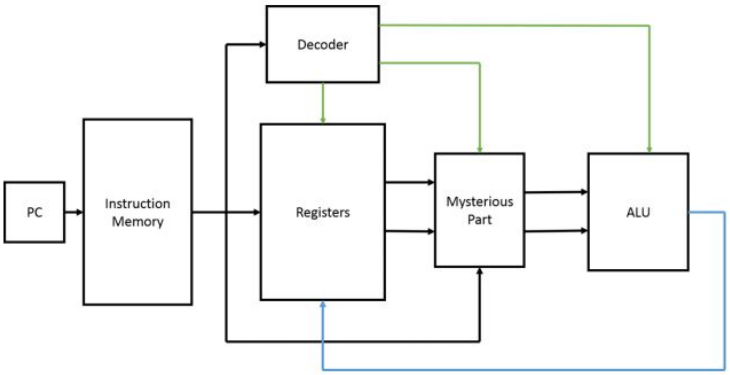
DLAB FINNAL PROJECT REPORT

童柏勛, 0413359

***Abstract*—use verilog to simulate a simple CPU**

I. INTRODUCTION

In this final project,we have to design a simple CPU. It can read machine code from instruction register, including put four registers integer doing some operations and logical operator. It can also get value from register ,compute result in ALU,and store the result back in register.



II. EVENT DIAGRAM

send 20 bits instruction
from pc_instruction

⇩

first 4 bits put in decoder
following 16 bits put in register
also put 8 bits in mysterious

⇩

before decoder analyze
put op_code in
mysterious,register,ALU

⇩

base on decoder messager
choose what the CPU
should do and return the
value to original register

III. INTRODUCE MODULE

A. Pc_instruction

This module's output control which intstruction should output. In each clk will send one 20 bit instruction.

B. Register

There are totally four register in this design. We choose one register when we want to output answer then storing answer in this register.

C. Decoder

This module is the control unit. It receives op_code from instruction and decode op_code to control everything in this design. The op_code is the forward four bits in instruction.

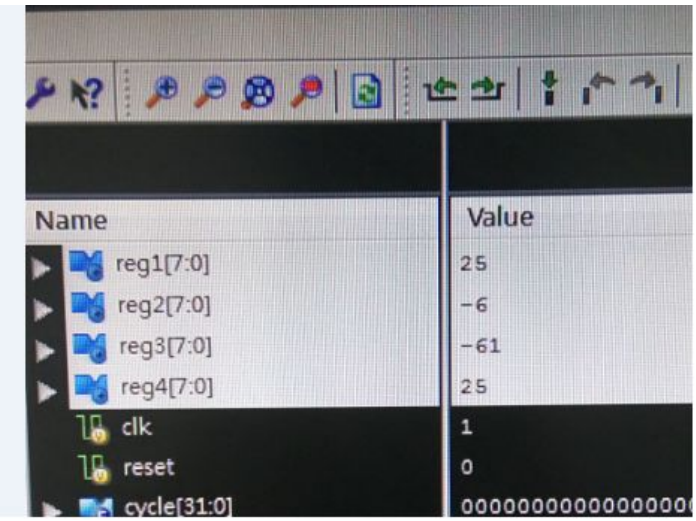
D. Mysterious

This module design whether we use input integer or not.

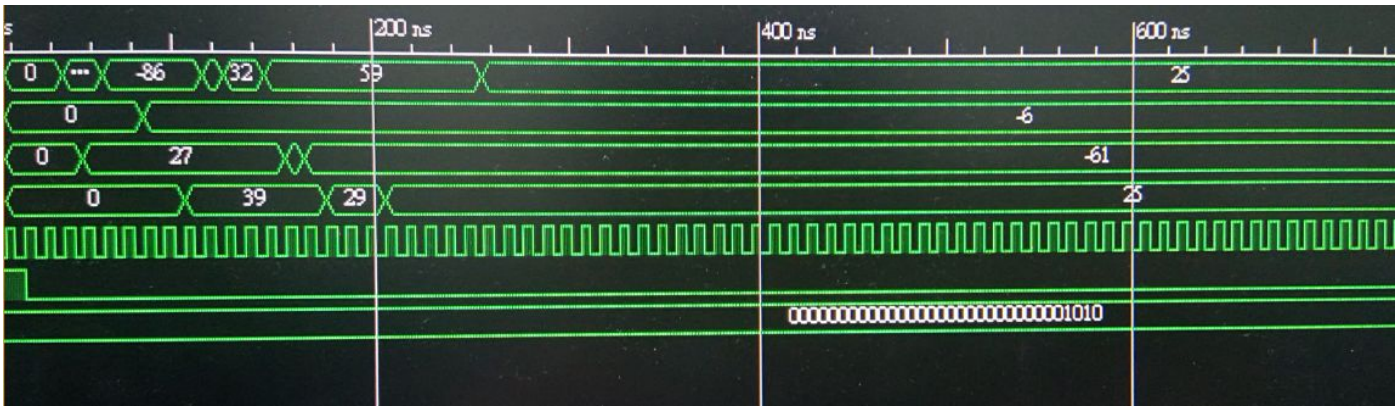
E. ALU

According to the decoder's messages, chosing what the module shiuld do. After caculating , ALU returns answer back.

IV. Result



VI. TIMING DIAGRAM



CONCLUSION

We can design a simple CPU ,using above modules and methods.This CPU can read commands,choose the data_memory location,caculate the result,and also choose the correct memory’s location to store the consequence.