LAB 9 LAKER

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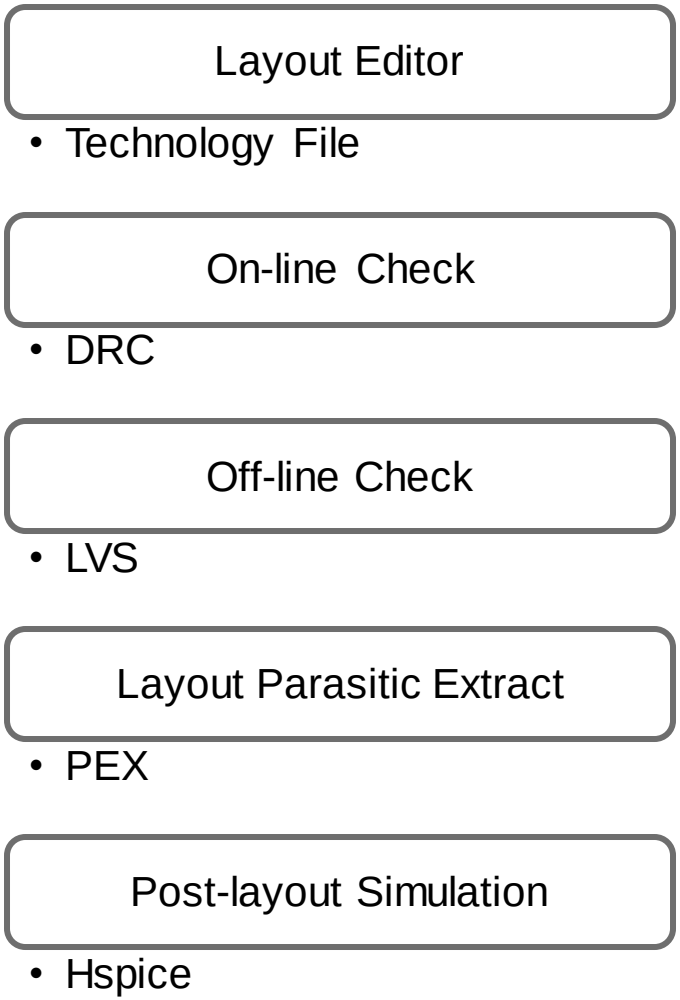
TEL : 06-2757575 ext. 62400 ext. 2860

DESIGN FLOW


Circuit Design
Pre-Simulation
Layout Design
Post Layout verification
Tape out

INTRODUCTION

- **Full-custom Design Flow**
  - 電路編輯軟體
    - Text editor, schematic editor(icfb)
  - 電路模擬軟體
    - Hspice
  - 佈局編輯軟體
    - Cadence Virtuoso, Laker
  - 佈局驗證軟體
    - Calibre

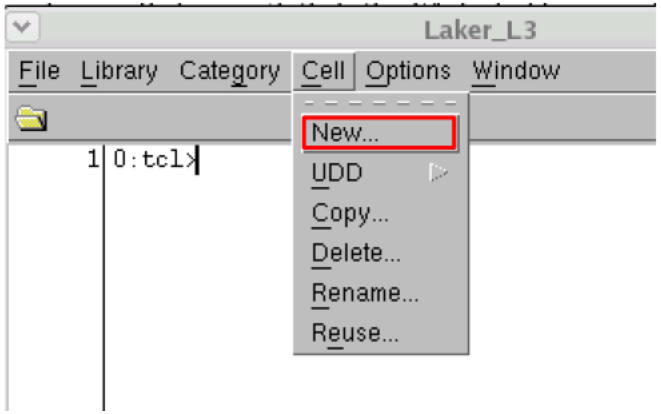


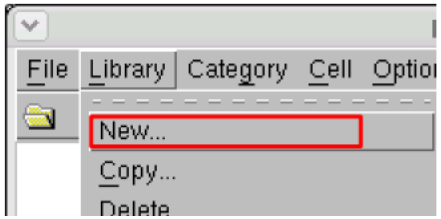
LAKER

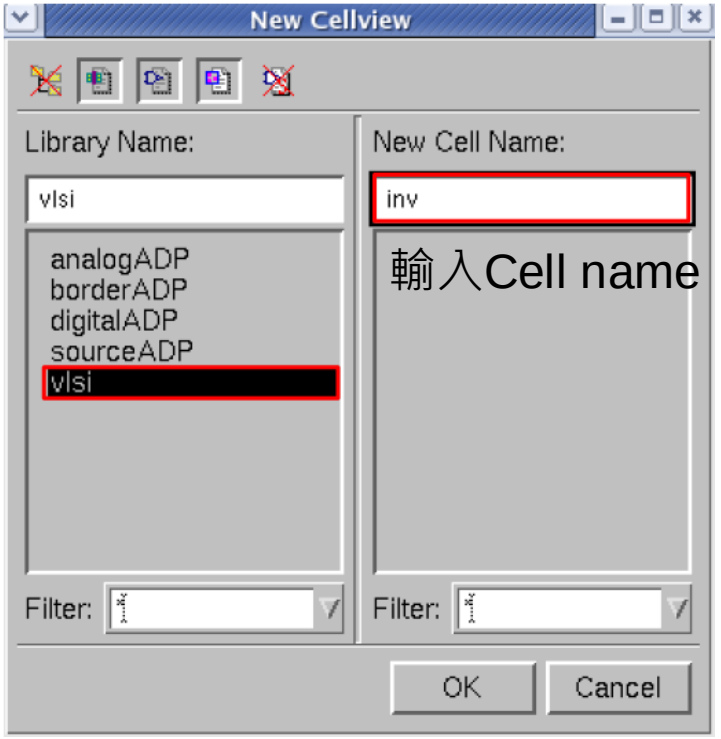
- **ssh –X vlsicad5**
- **cp –r /home/user2/vlsi17/vlsi1780/Lab9 .**
- **進入 Lab9 之後解壓縮，開啟Laker之前**
  - 在終端機輸入 source /usr/cad/mentor/CIC/calibre.cshrc
  - 在終端機輸入 source /usr/cad/synopsys/CIC/laker.cshrc
- **執行Laker**
  - 輸入 laker &

LAKER

- **Create New Library (Library->NEW)**
- **Create New Cell (Cell->NEW)**







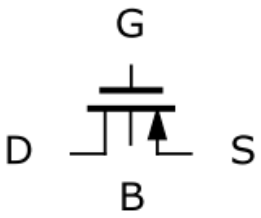
LALER 快捷指令

將Layout table 叫到左邊：window → layout table → attach left

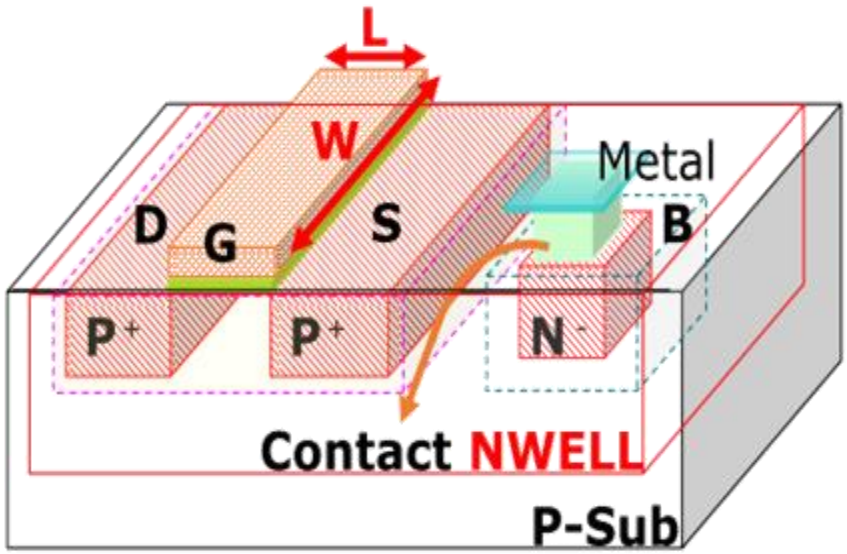
快捷鍵	說明	快捷鍵	說明
Shift G	叫 NGR/PGR	K / shift K	尺規/消除尺規
Ctrl M	叫 PMOS/NMOS	M	移動
A	對齊	S	伸長或縮短
A f3	設定相距多少	R	畫圖
O	叫 CONTACT	U	復原
P f3		C	複製
Q	元件內部屬性	L	打腳位
F	顯示全圖	Shift Z	縮小
Ctrl Z	放大	I	呼叫元件

LAKER – EXAMPLE (1/3): PMOS

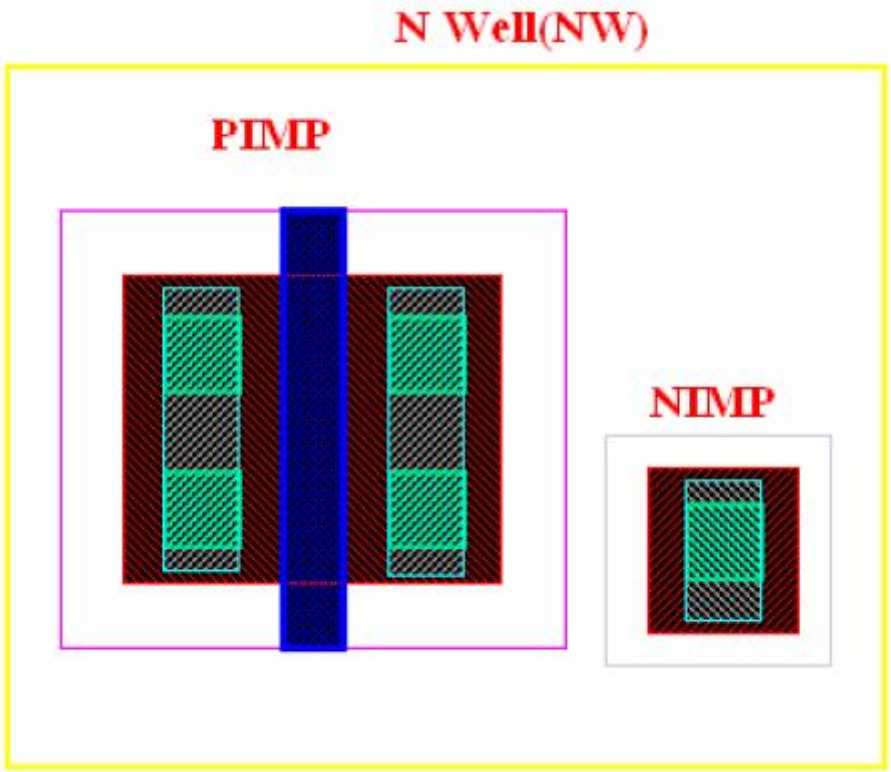
- **SYMBOL**



- **PROCESS**

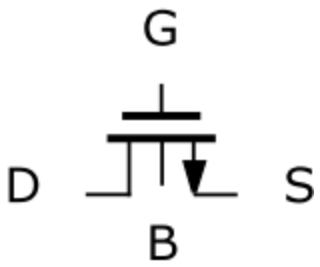


- **LAYOUT VIEW**

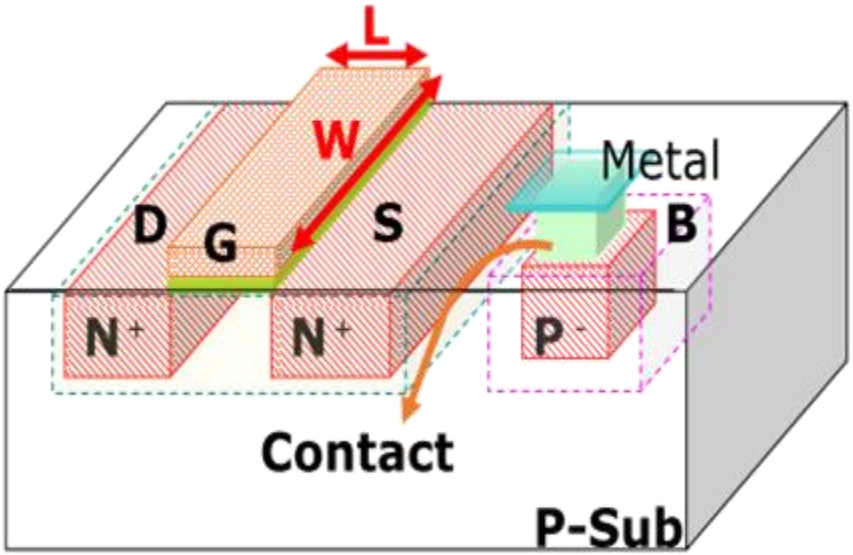


LAKER – EXAMPLE (2/3): NMOS

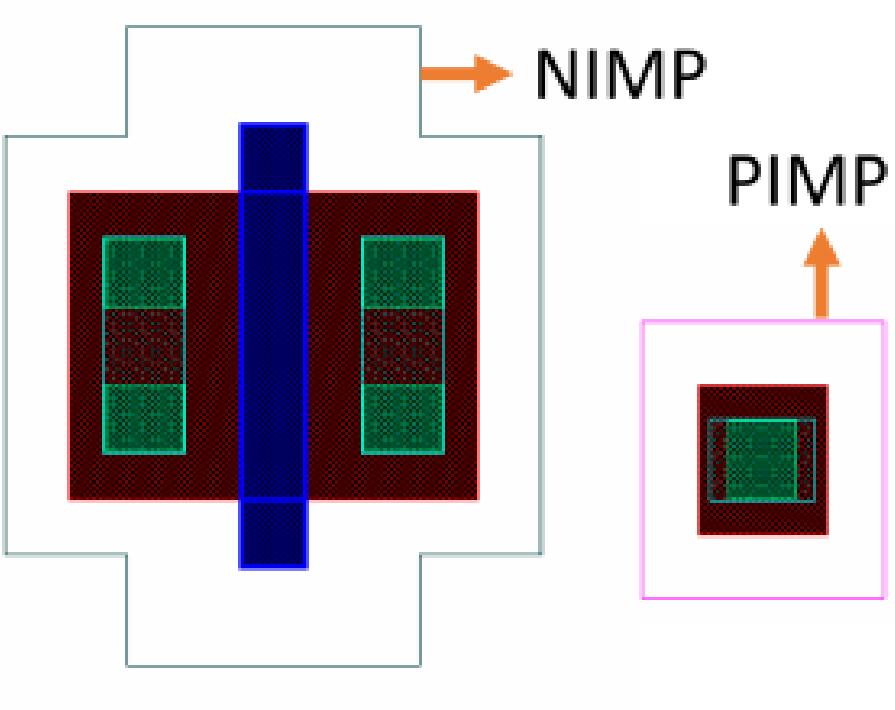
- **SYMBOL**



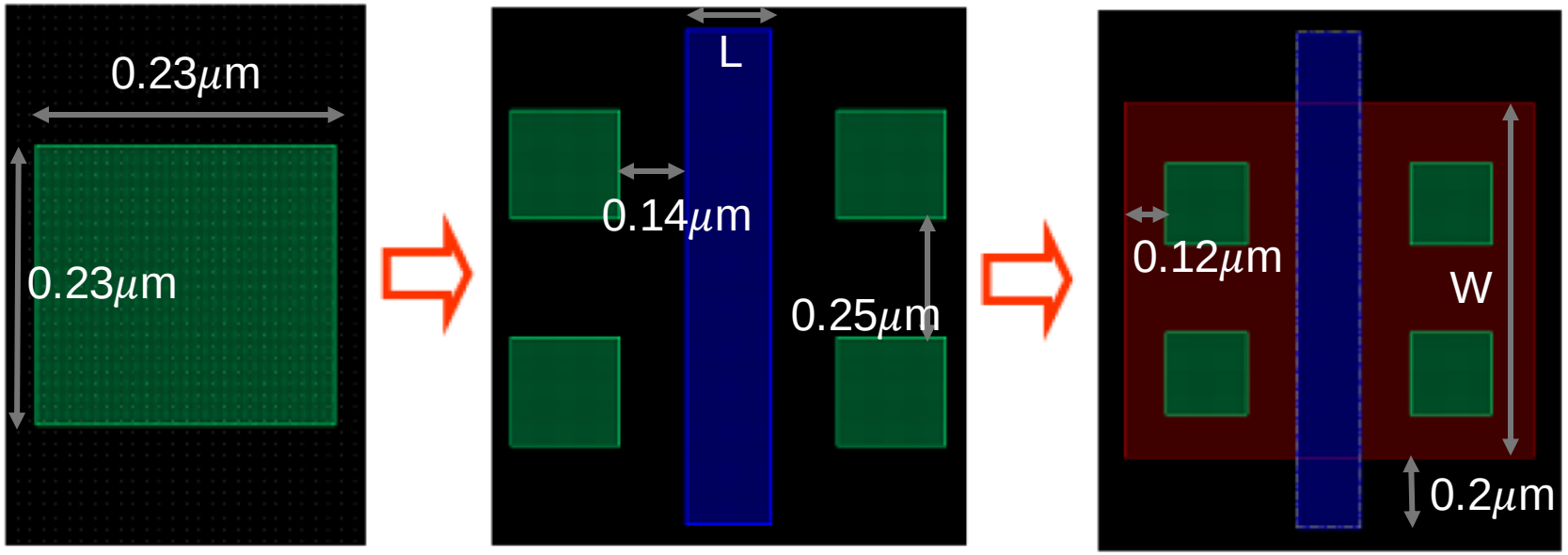
- **PROCESS**



- **LAYOUT VIEW**



LAKER – EXAMPLE (3/3): INVERTER

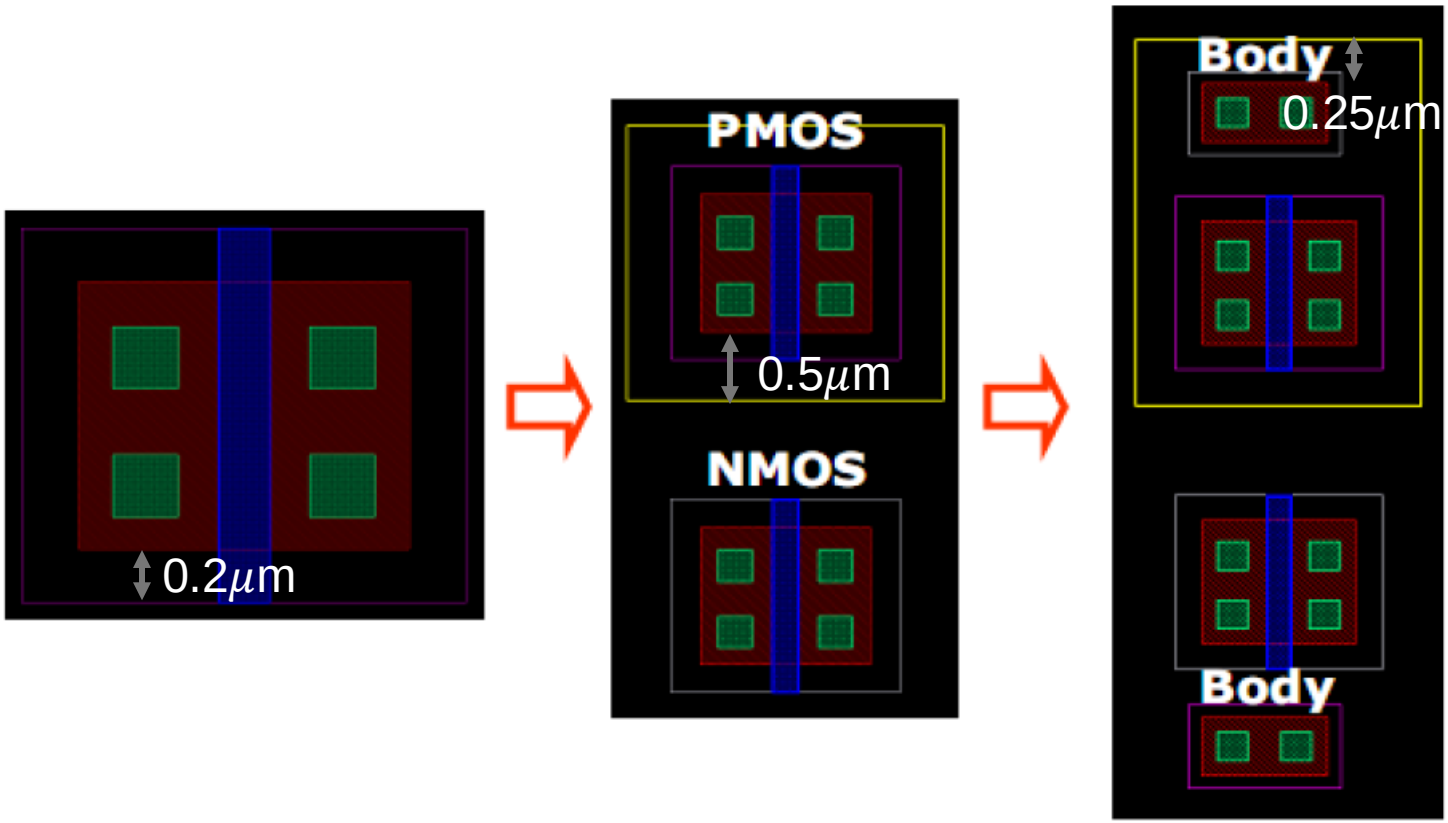


Create a contact(CONT)

Create a poly(PO1)

Add a diffusion layer(DIFF)

LAKER – EXAMPLE (3/3): INVERTER



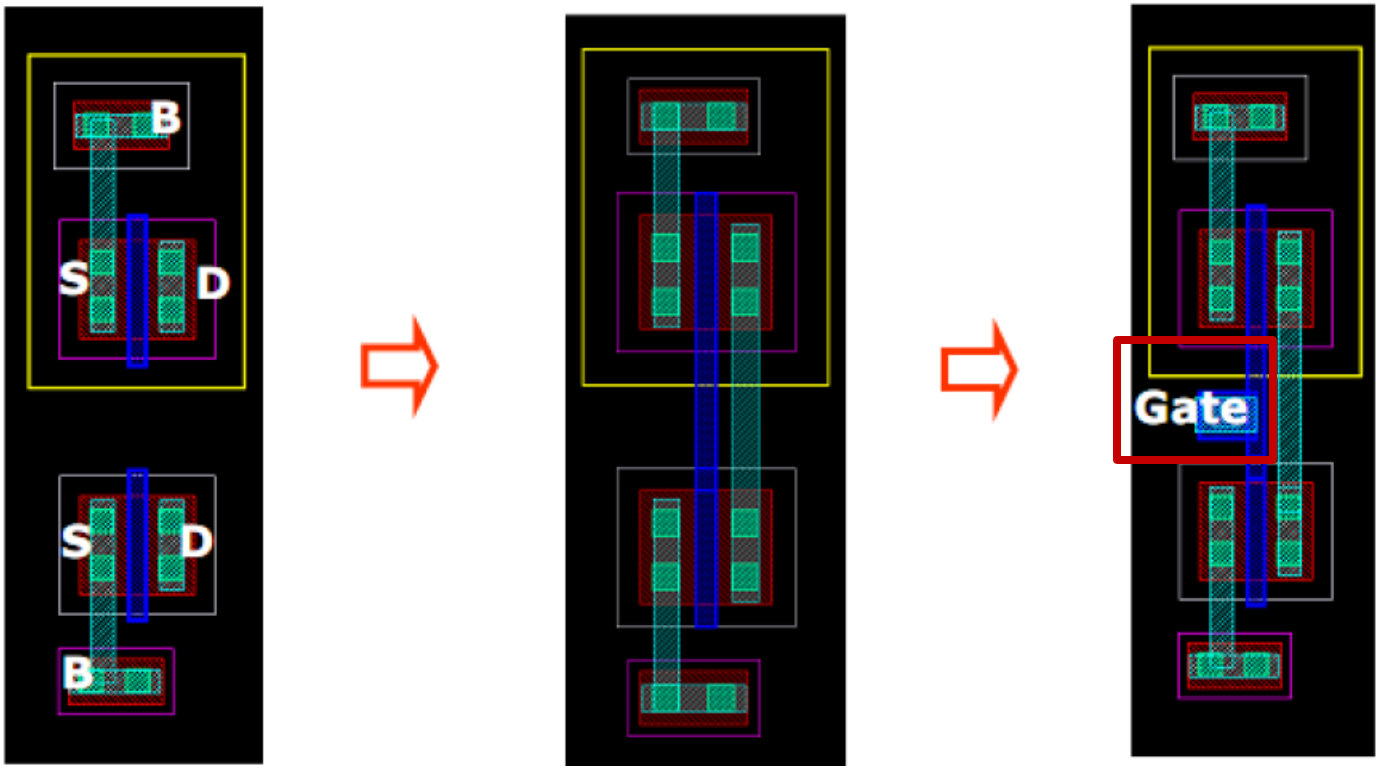
Add P implantation(PIMP)

Create a PMOS and a NMOS

Create bodies

LAKER – EXAMPLE (3/3): INVERTER

Gate
CONT(0.23μm*0.23μm)
PO1
ME1



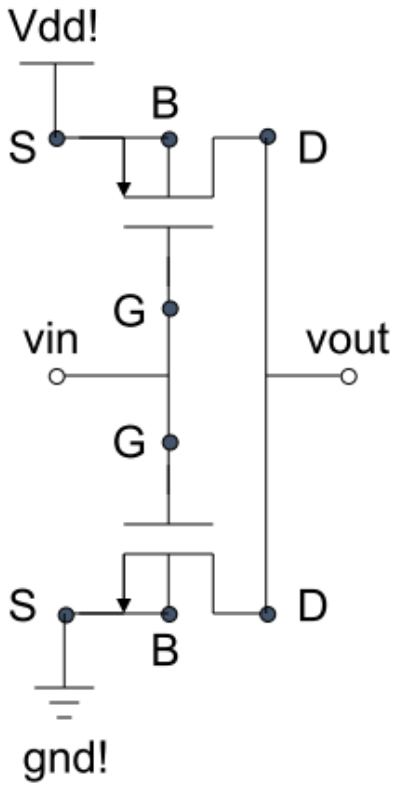
Use metal(ME1) to connect source and body

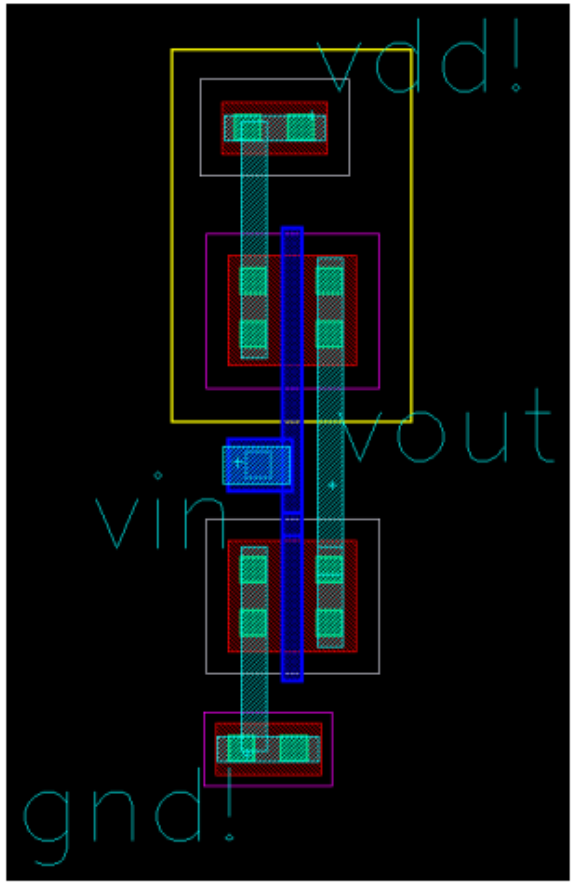
Connect the drains and gates of two MosFETs

Add gates

LAKER – EXAMPLE (3/3): INVERTER

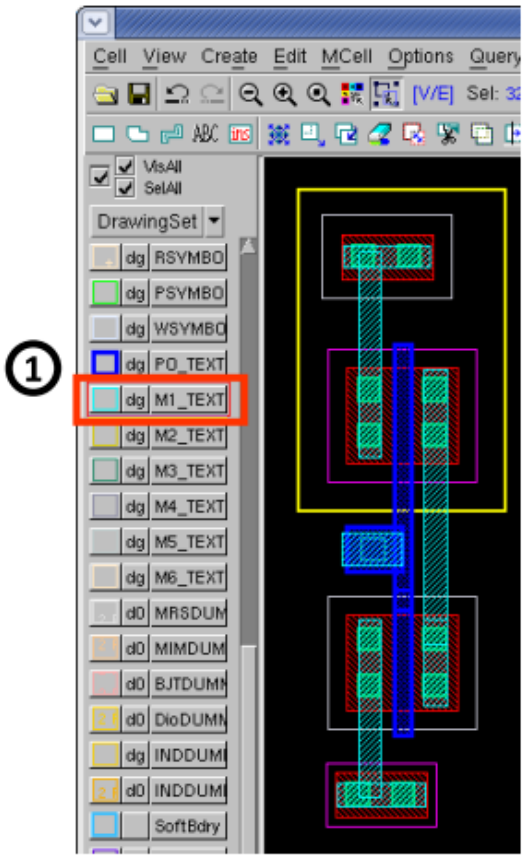
- **Add pin names**





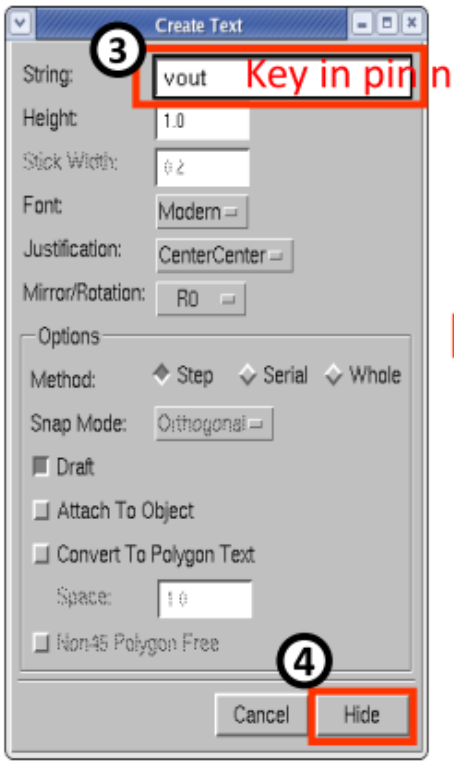
LAKER – EXAMPLE (3/3): INVERTER

Pin Name
Pin name should be the same as the pin name in spice document(.sp).



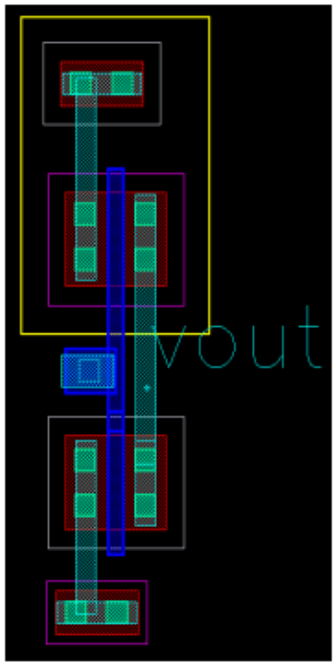
① M1_TEXT

② ABC Create text
Hot key: l



③ Key in pin name

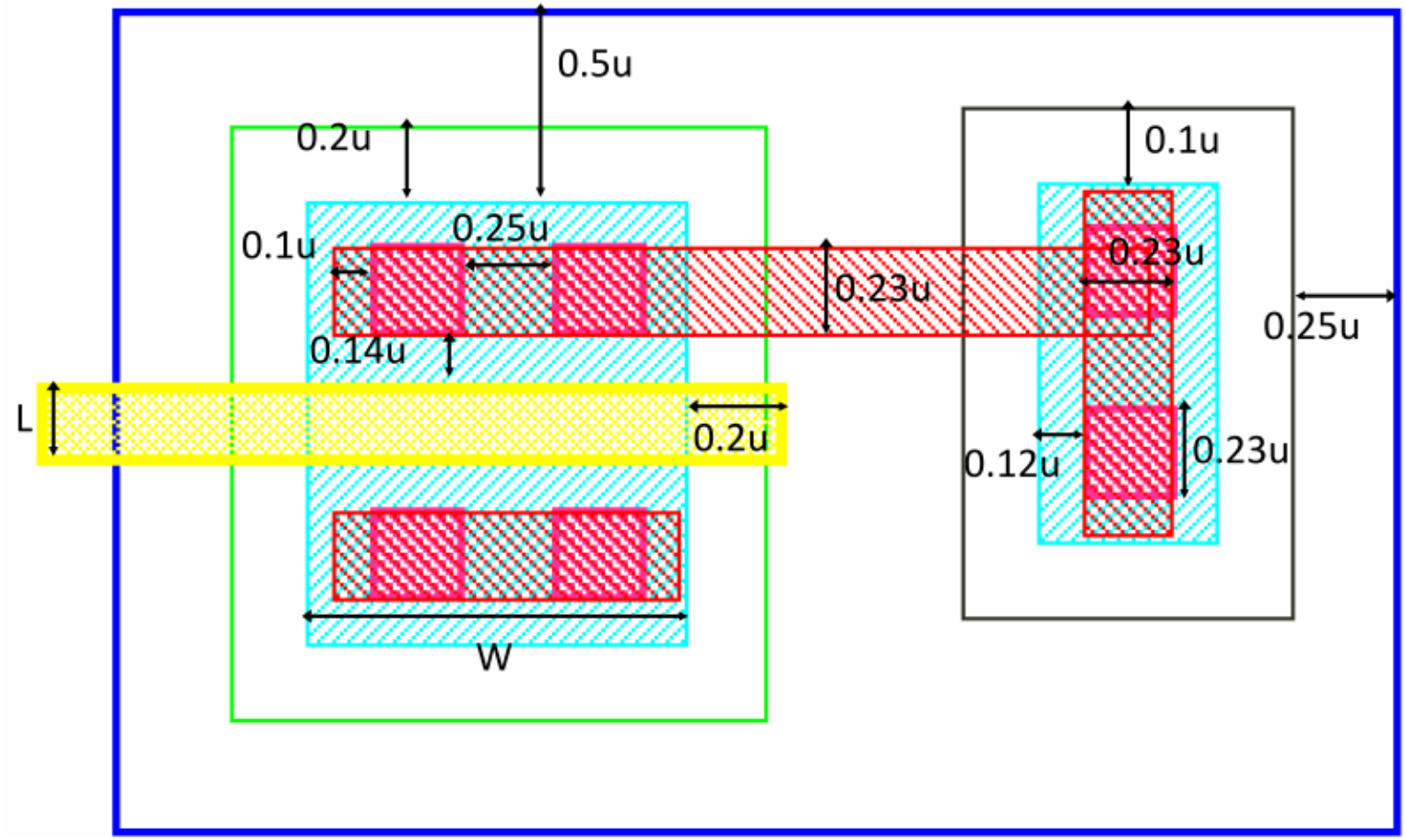
④ Hide



LAKER DESIGN RULE

Term	Explanation
W	Width
L	Length
DIFF	Diffusion (Drain/Source)
PO1	Poly silicon (Gate)
PIMP	P implantation
NIMP	N implantation
NW	N WELL

LAKER DESIGN RULE

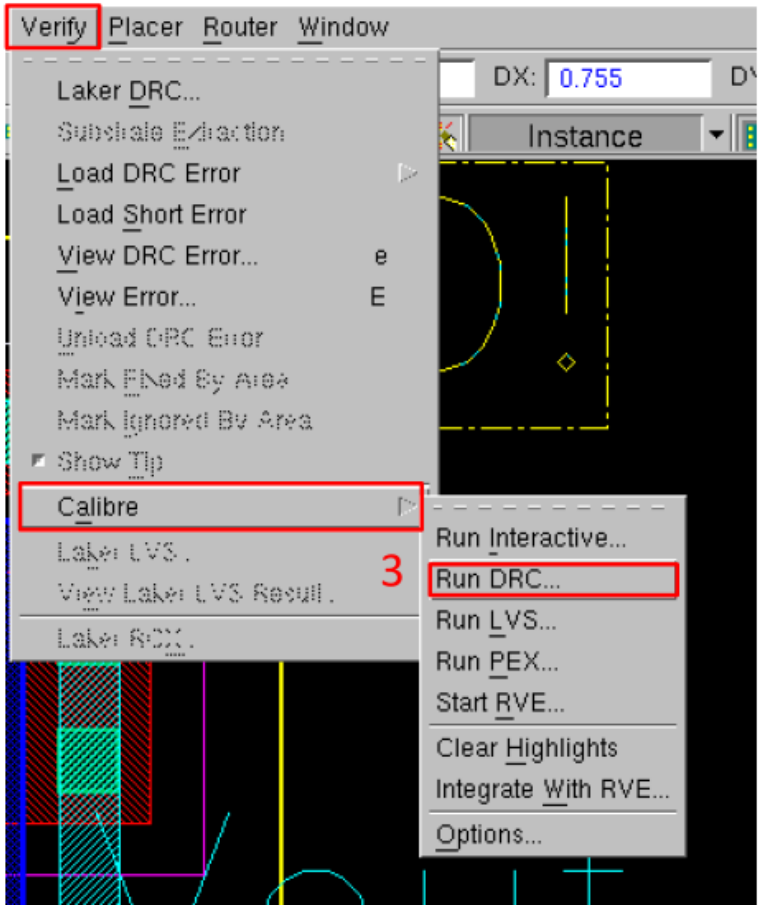


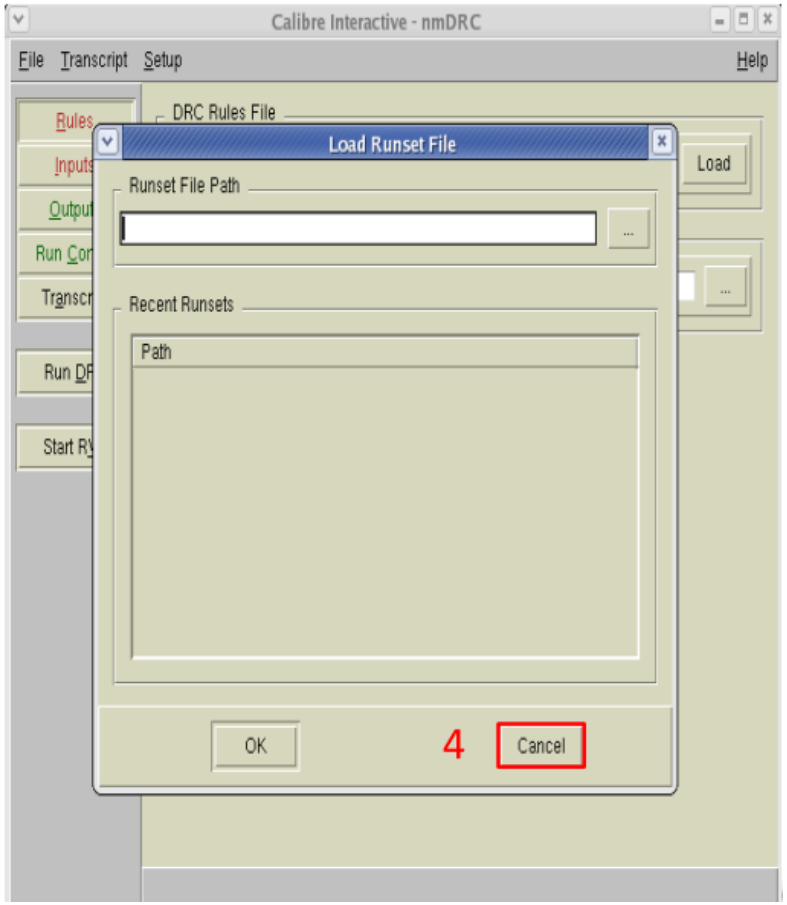
LAKER DESIGN RULE

1. PIMP(NIMP)距離DIFF爲0.1u
2. PIMP距離NIMP爲0u
3. PIMP距離PIMP爲0.45u
4. NIMP距離NIMP爲0.45u
5. POLY超出DIFF距離爲0.2u
6. MT1距離MT1爲0.24u
7. MT2距離MT2爲0.27u
8. DIFF距離DIFF爲0.3u
9. NWELL距離NWELL爲1.6u

DRC CHECK

- **Verify (Calibre->Run DRC)**

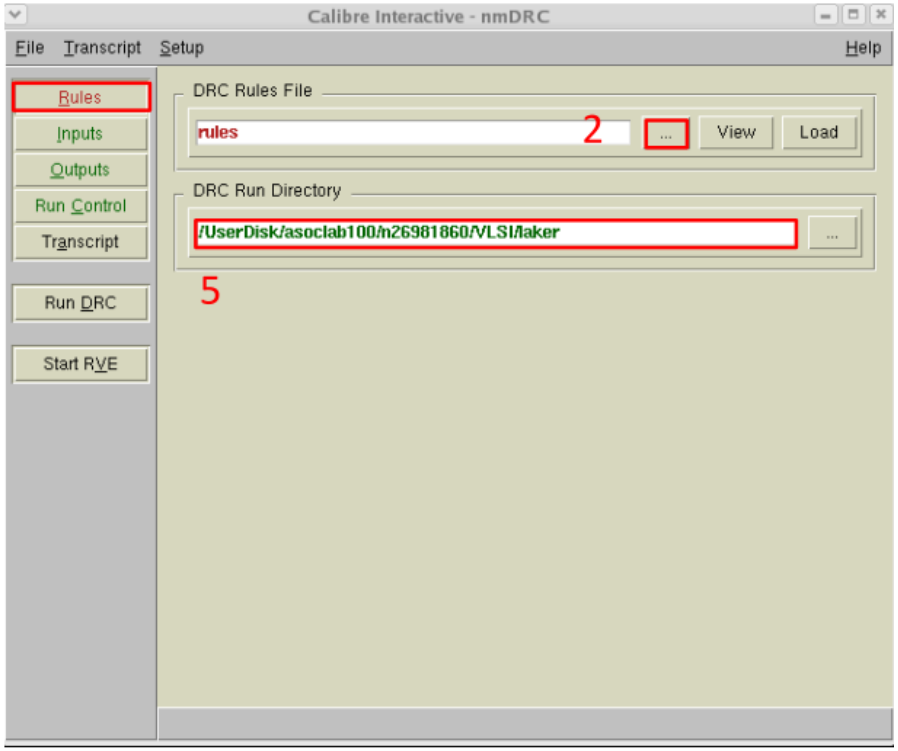


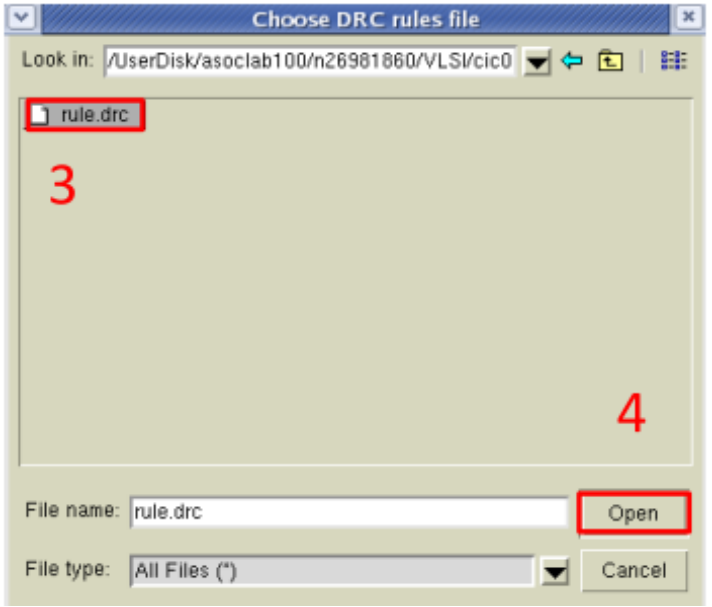


DRC CHECK

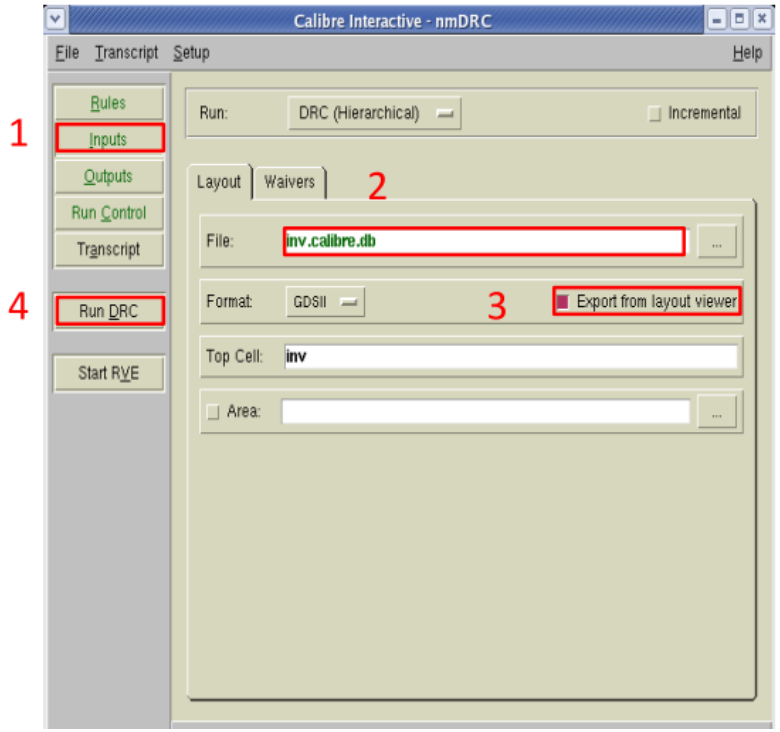
- **Verify (必須輸入rule.drc檔位置**

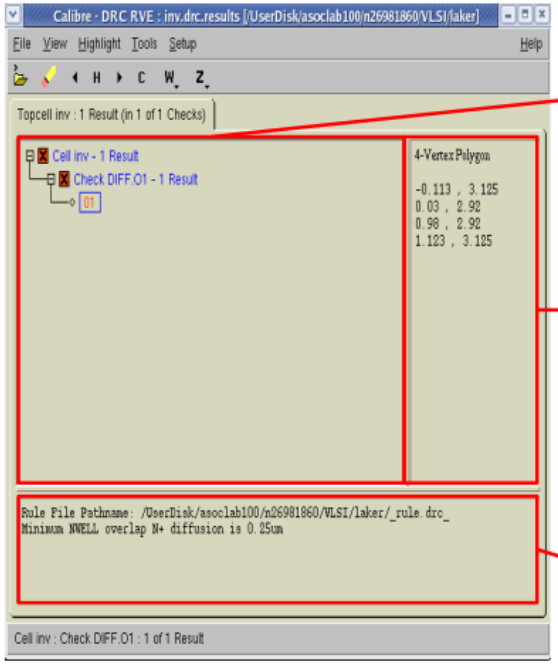
(cic018->caliber->Calibre_DRC->rule.drc))





DRC CHECK



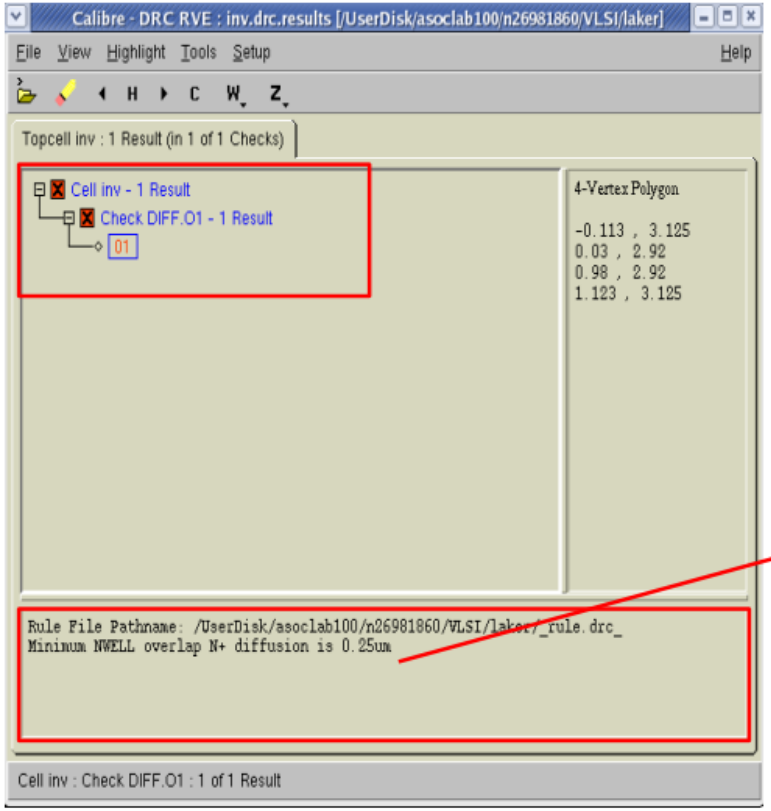


Error table

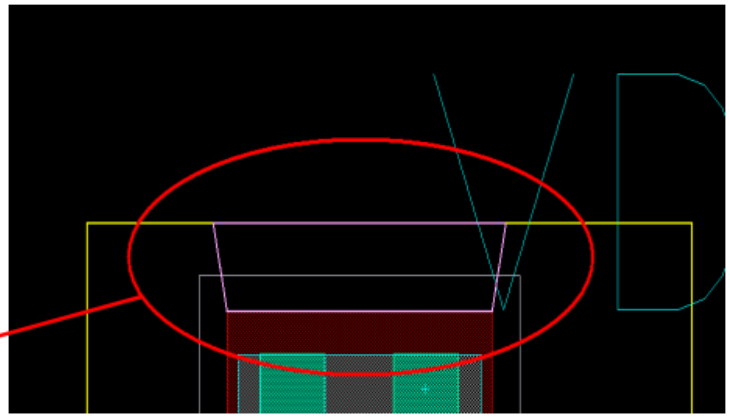
Axis

Error Massage

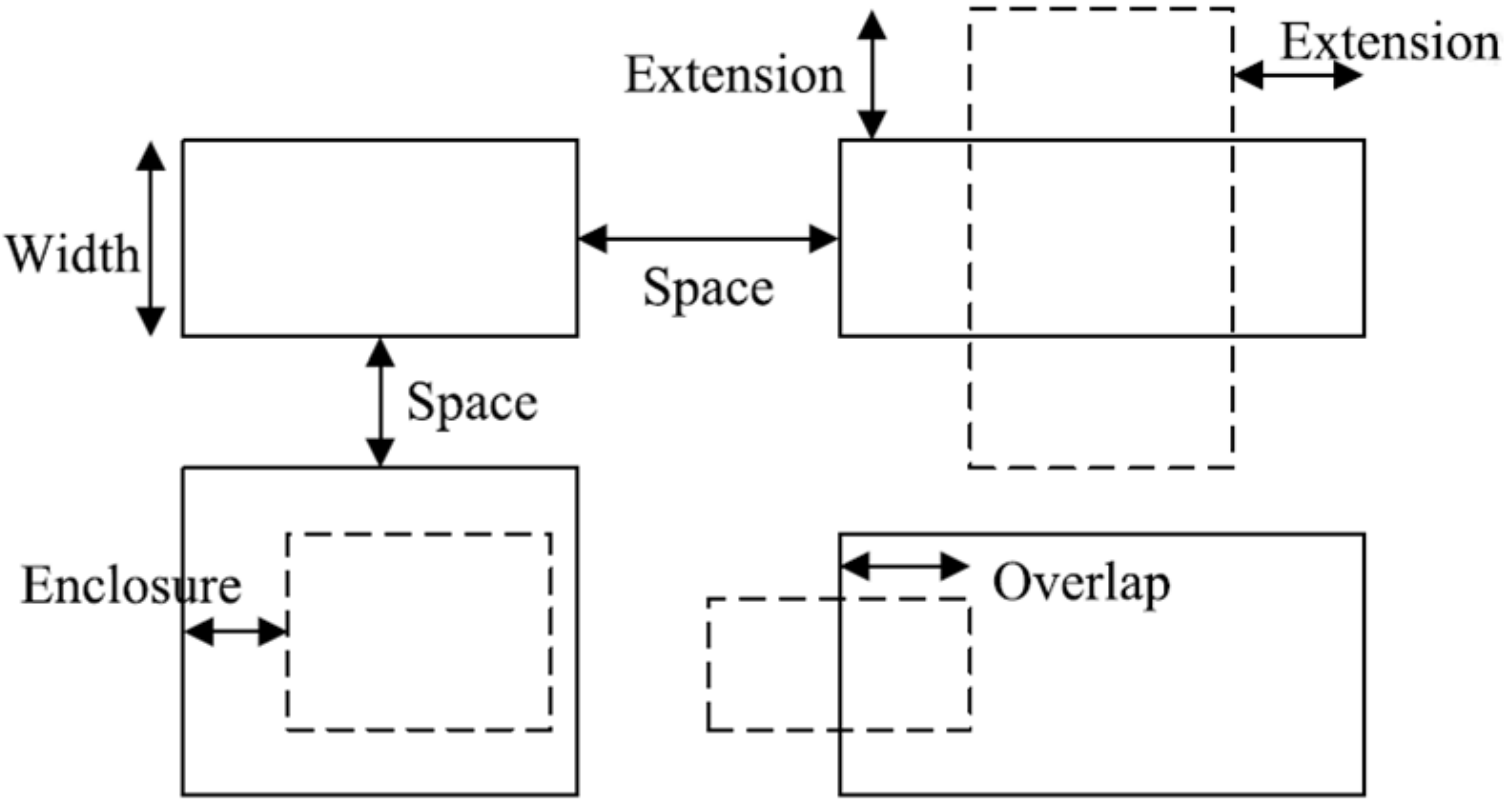
DRC CHECK



下圖紅色橢圓為 Error Massage 描述的錯誤訊息

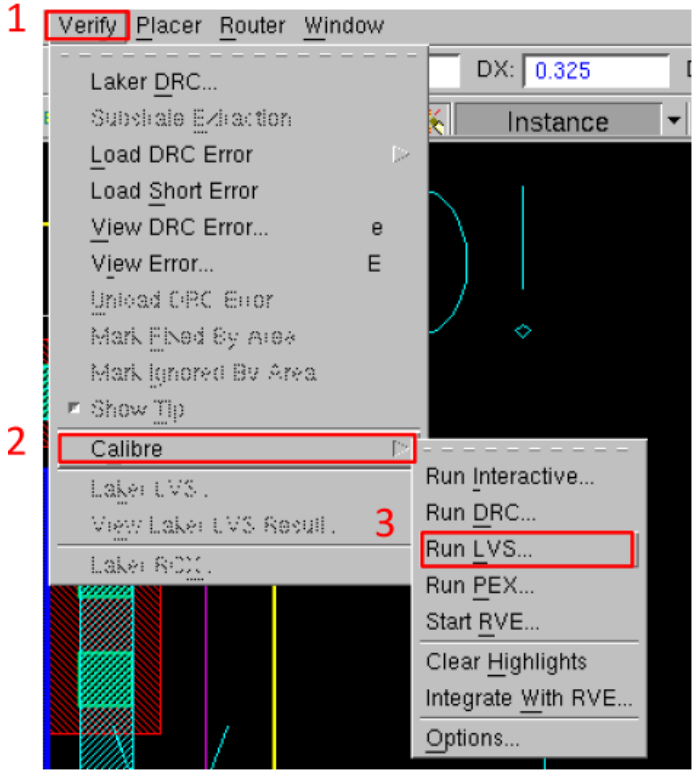


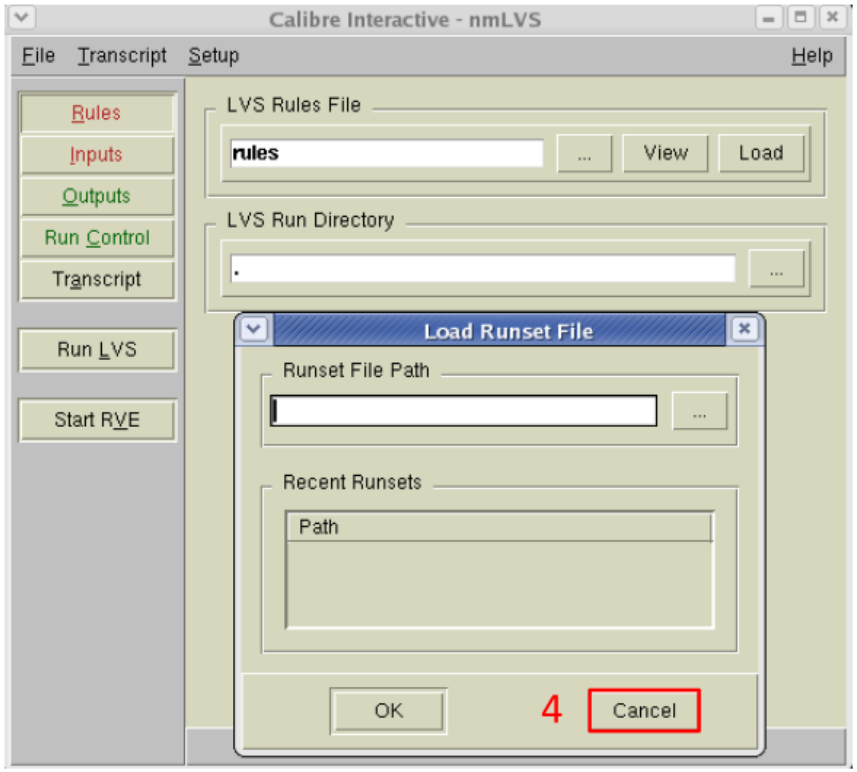
DRC CHECK



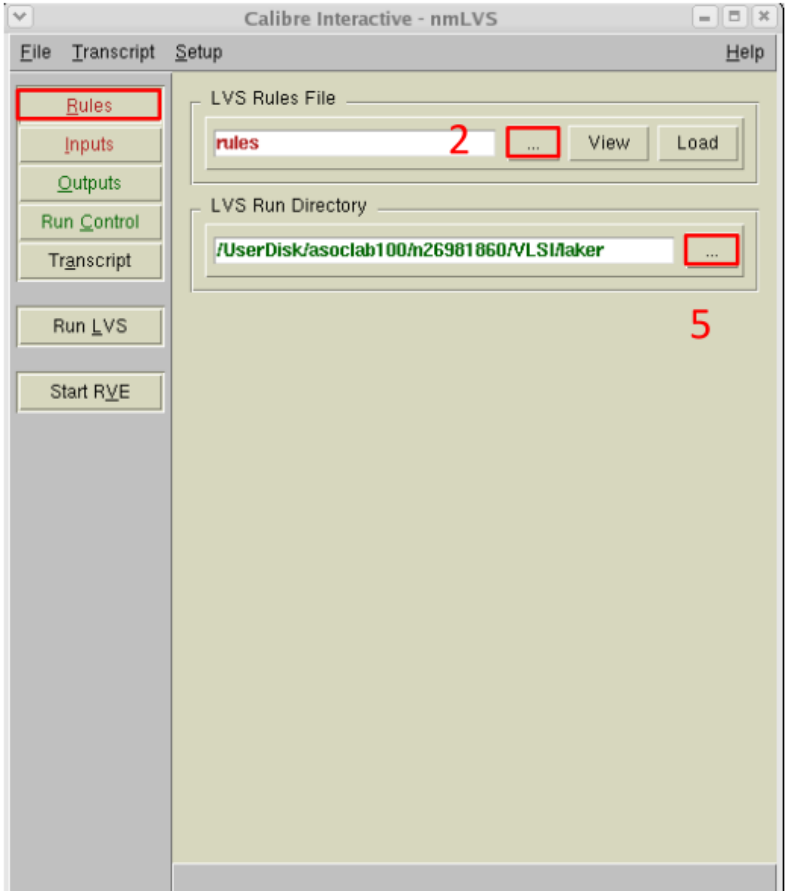
LVS CHECK

- **Verify (Calibre->Run LVS)**

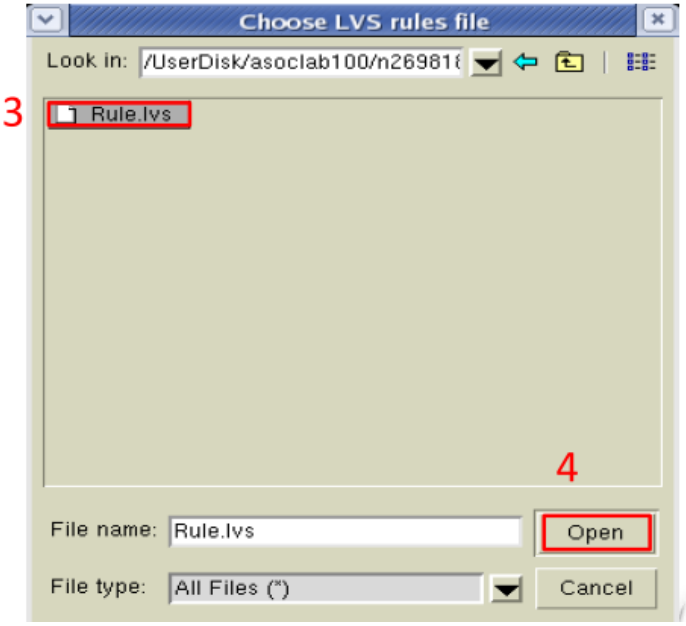




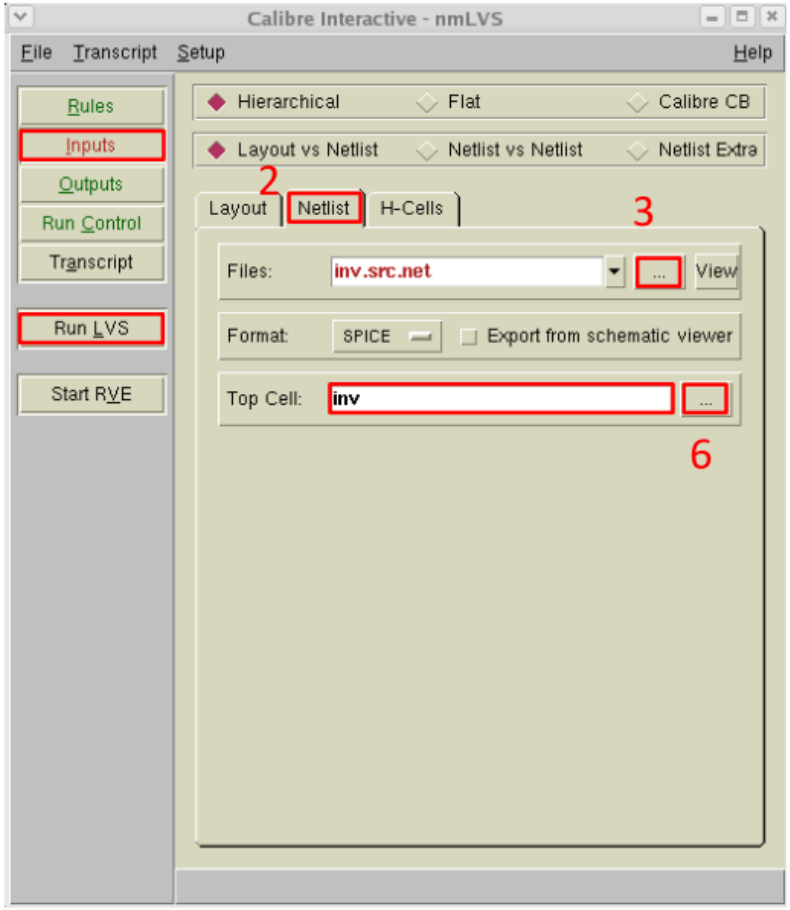
LVS CHECK



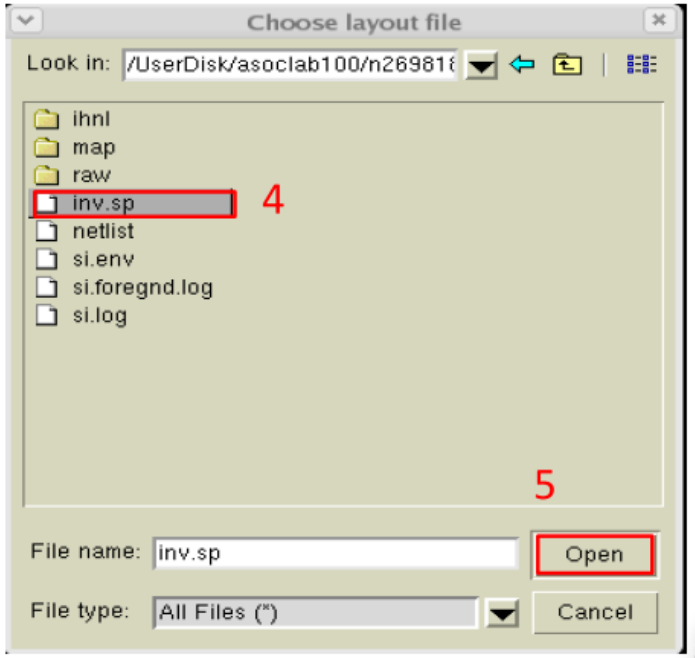
注意:
必須輸入rule.drc檔位置
(cic018->calibre->Calibre_LVS
->Rule.lvs)
請注意輸出檔案位置



LVS CHECK

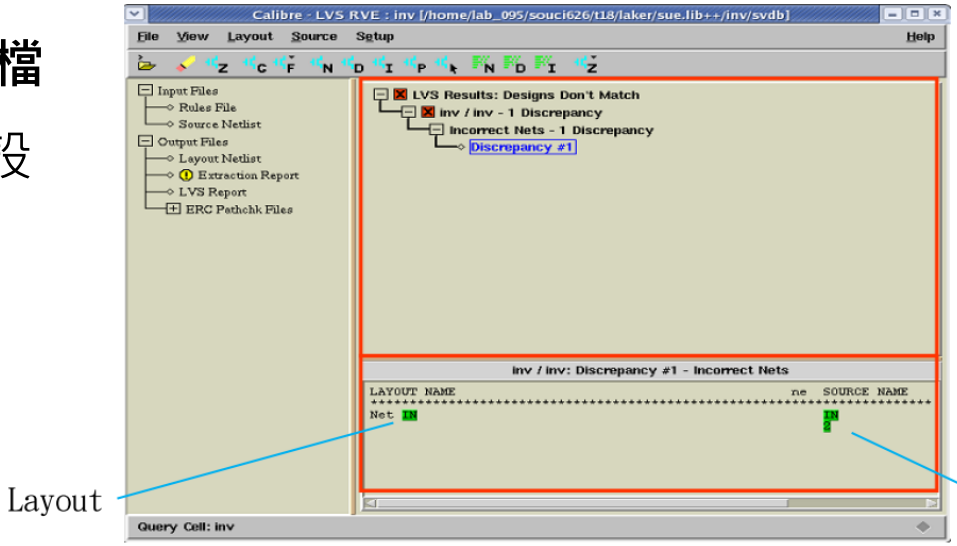


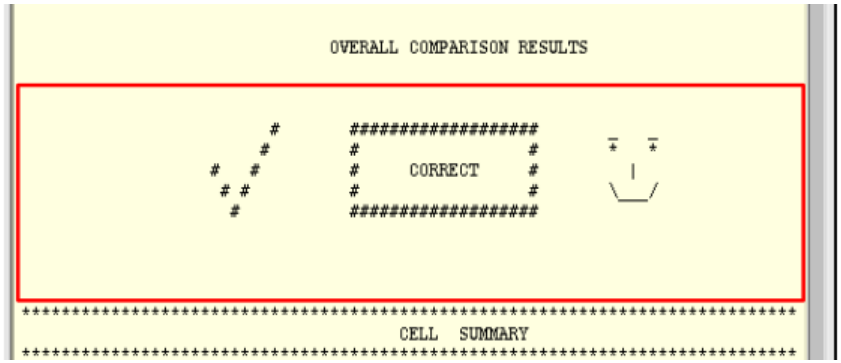
注意：
必須輸入的.sp檔為SCHEMATIC轉出的.sp檔



LVS CHECK

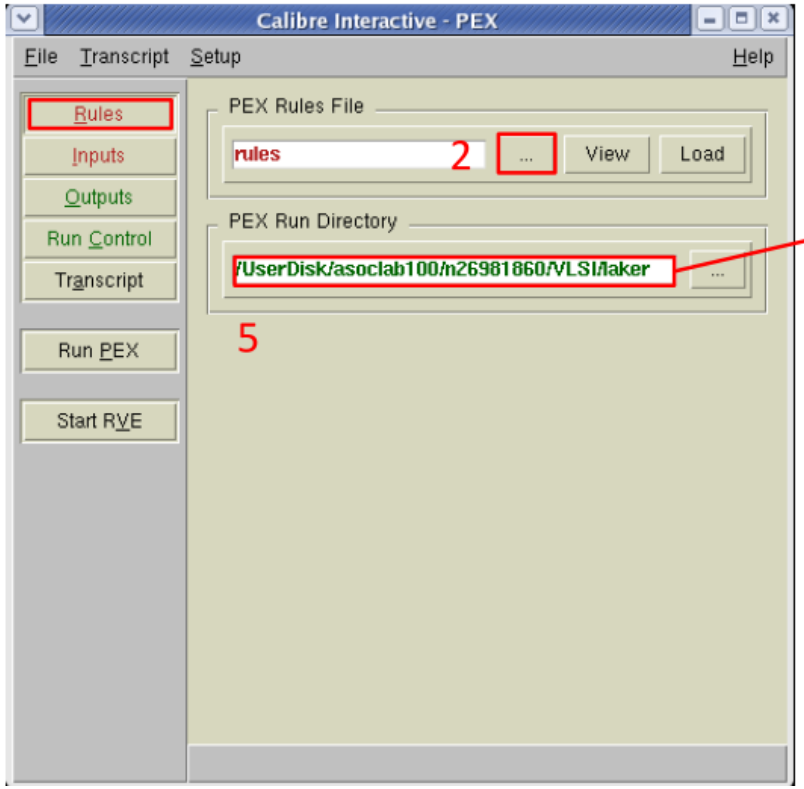
- 打開LVS所產生的.sp檔
  - 確認pin腳位與原設計是否相同





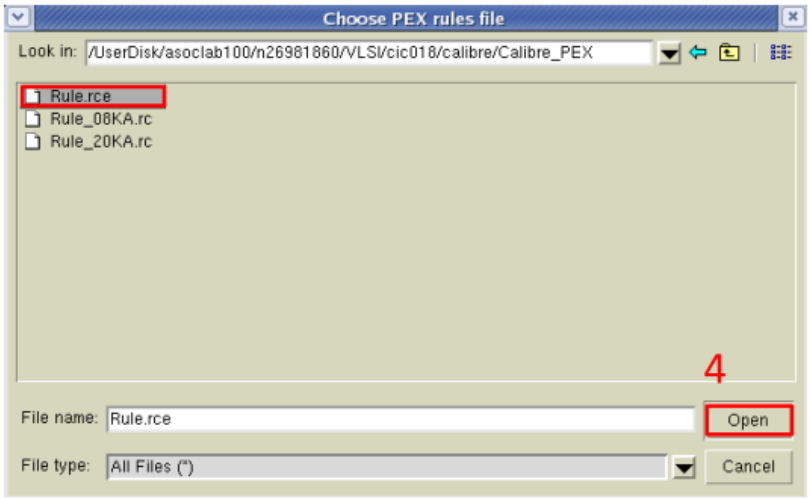
PEX

- **Verify (Calibre->Run PEX)**

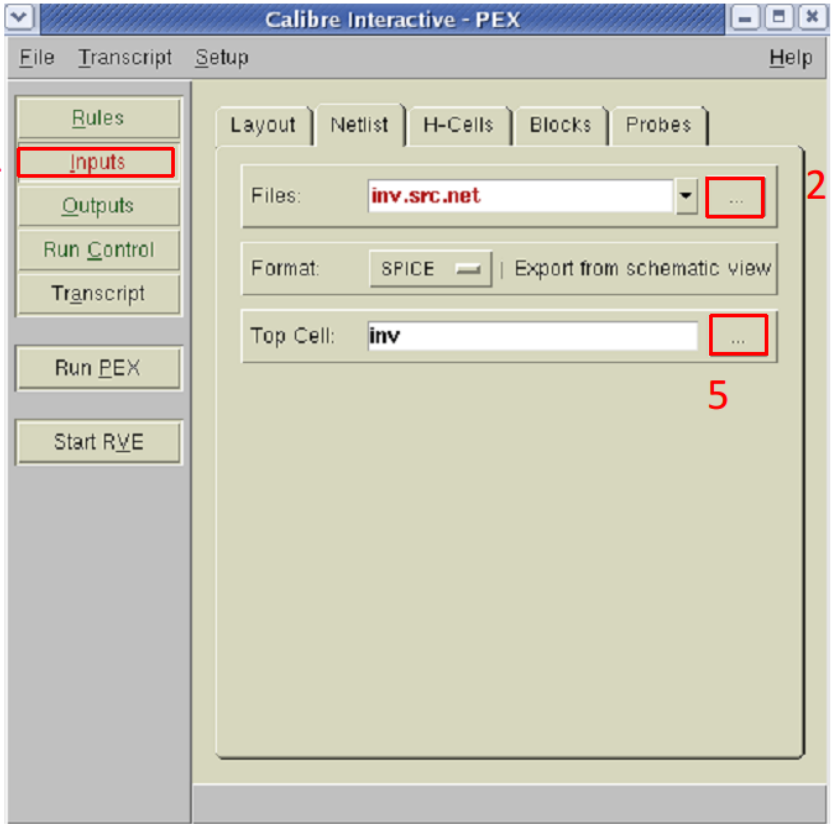


注意:
必須輸入rule.drc檔位置
(cic018->calibre->Calibre_PEX
->Rule.rce)

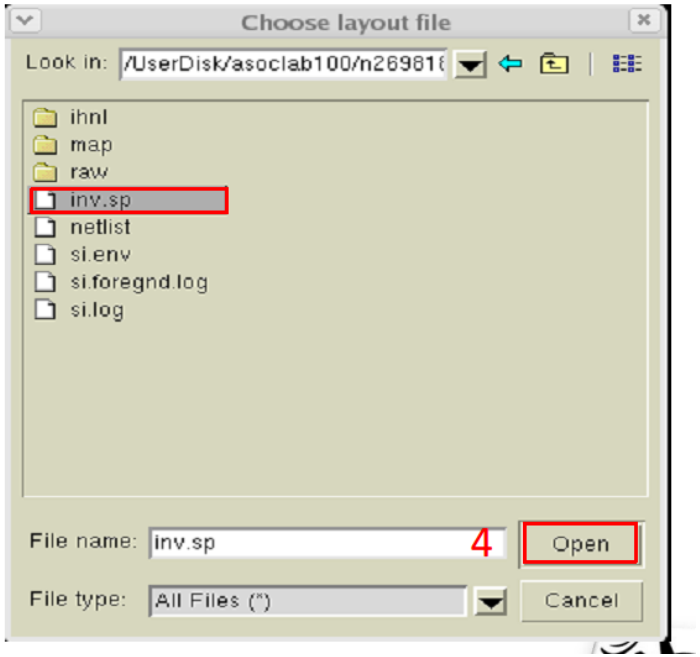
指定路徑下必須含有PEX的rule



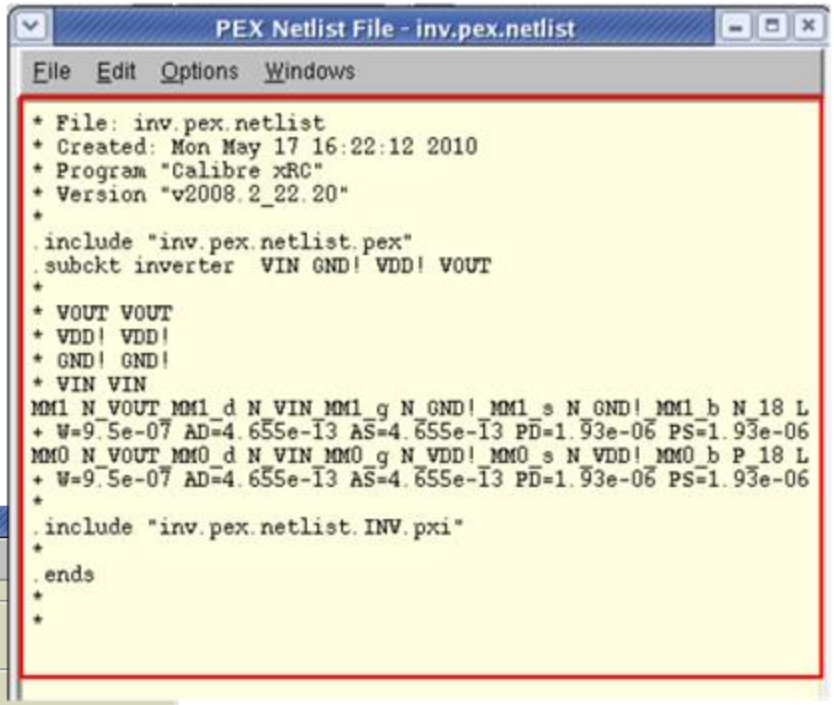
PEX

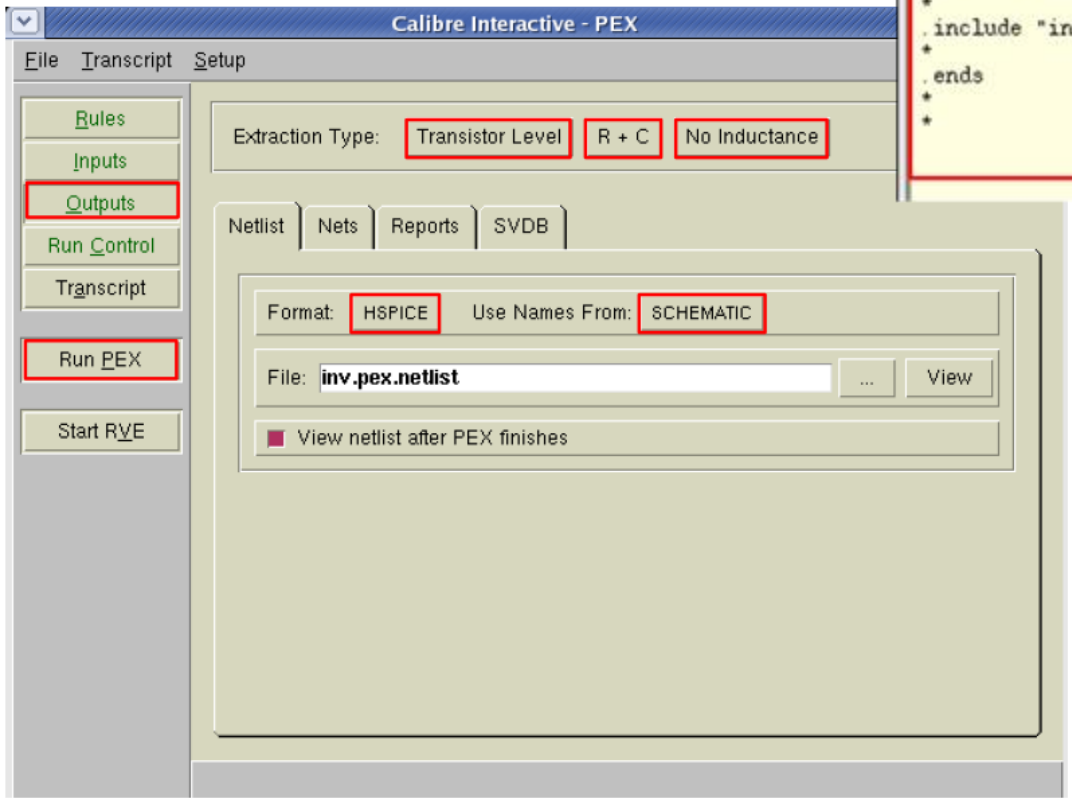


注意：
必須輸入的.sp檔為LVS轉出的.sp檔



PEX


PEX Netlist File - inv.pex.netlist
File Edit Options Windows
* File: inv.pex.netlist
* Created: Mon May 17 16:22:12 2010
* Program "Calibre xRC"
* Version "v2008.2_22.20"
*
.include "inv.pex.netlist.pex"
.subckt inverter VIN GND! VDD! VOUT
*
* VOUT VOUT
* VDD! VDD!
* GND! GND!
* VIN VIN
MM1 N_VOUT_MM1_d N_VIN_MM1_g N_GND!_MM1_s N_GND!_MM1_b N_18_L
+ W=9.5e-07 AD=4.655e-13 AS=4.655e-13 PD=1.93e-06 PS=1.93e-06
MM0 N_VOUT_MM0_d N_VIN_MM0_g N_VDD!_MM0_s N_VDD!_MM0_b P_18_L
+ W=9.5e-07 AD=4.655e-13 AS=4.655e-13 PD=1.93e-06 PS=1.93e-06
*
.include "inv.pex.netlist.INV.pxi"
*
.ends
*
*


Calibre Interactive - PEX
File Transcript Setup
Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
Start RVE
Extraction Type: Transistor Level R + C No Inductance
Netlist Nets Reports SVDB
Format: HSPICE Use Names From: SCHEMATIC
File: inv.pex.netlist ... View
View netlist after PEX finishes

PEX

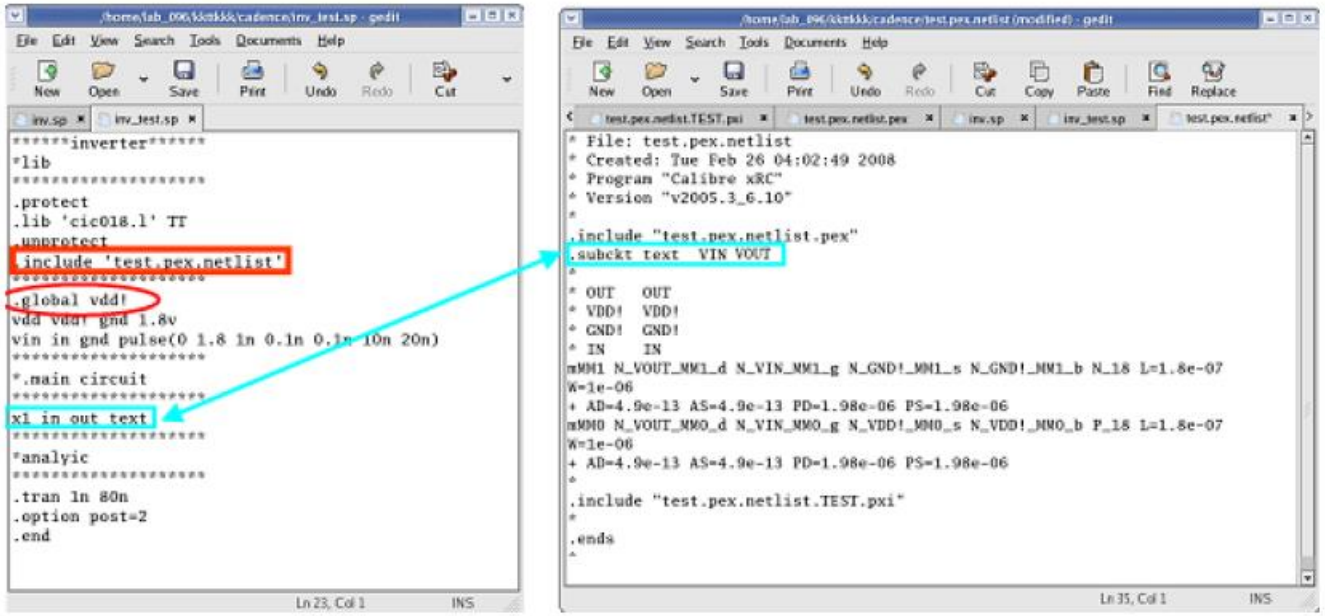
testbench.sp裡面，電路最外面的pin腳位名稱跟腳位順序跟"pex.netlist"檔裡的一樣，但電路名稱的順序沒差。

跑postsim的時候，要把下面三個檔案拉出來跟cic018.l以及testbench.sp一起run，反正就是要在同一個資料夾內就是了。

- **PEX產生的檔案**

Three output filse

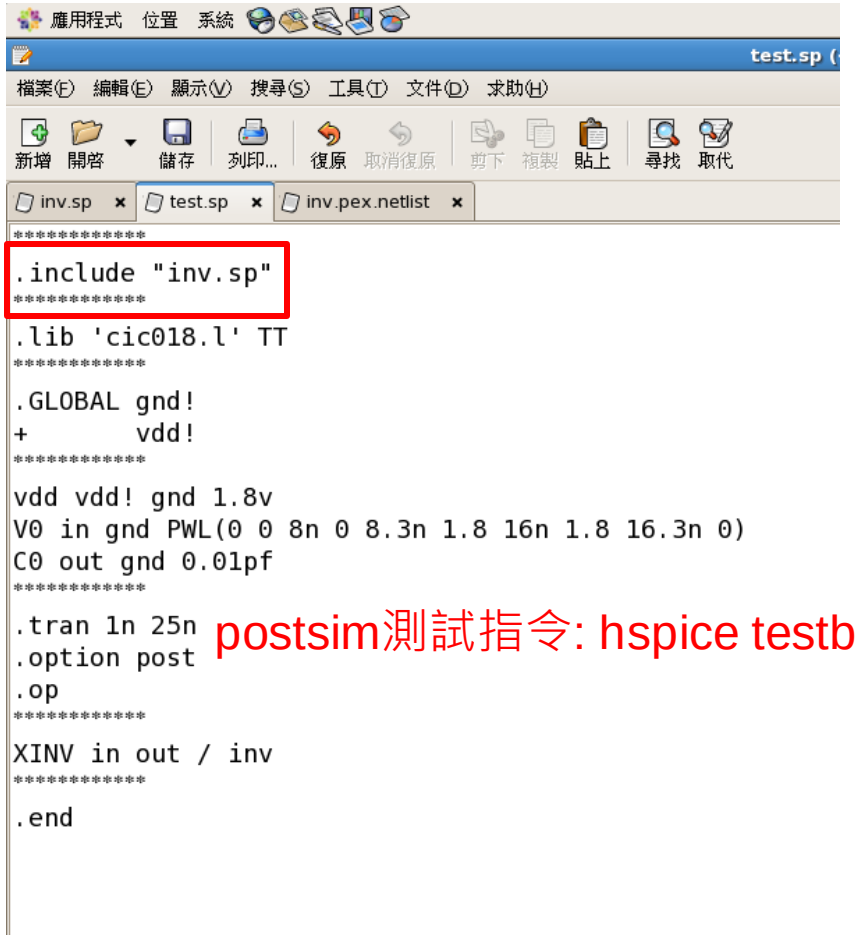
xxx.pex.netlist	Top circuit	(ex : test.pex.netlist)
xxx.pex.netlist.pex	Subcircuit	(ex : test.pex.netlist.pex)
xxx.pex.netlist.xxx.pxi	Connection	(ex : test.pex.netlist.TEST.pxi)



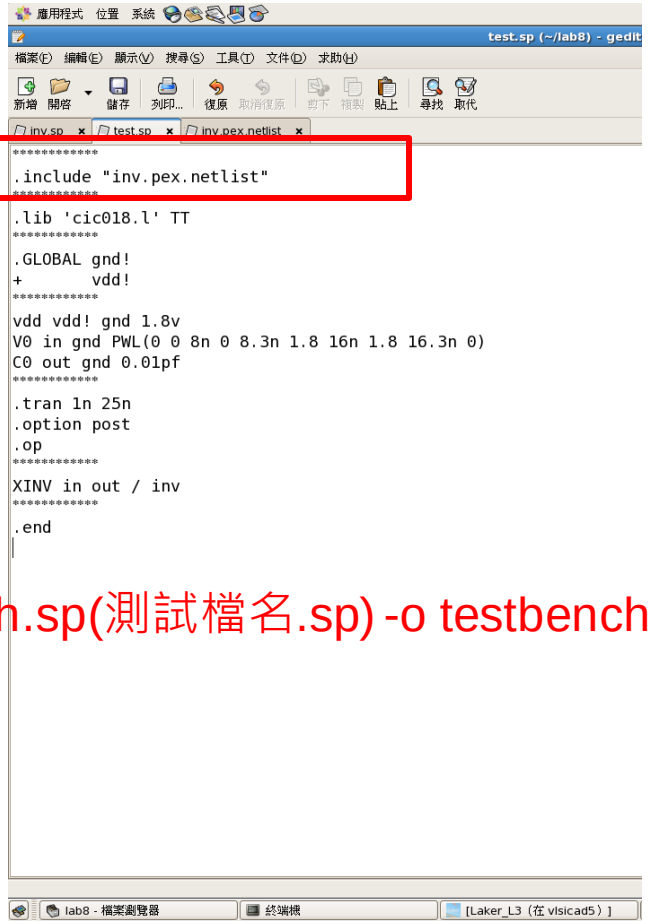
testbench.sp裡面ivclude的sp檔改成pex萃取出來的".pex.netlist"，因為要測試最真實的電路。

HSPICE

- **Pre-simulation**



- **Post-simulation**



postsim測試指令: hspice testbench.sp(測試檔名.sp) -o testbench.lis