# Goal

Computer Organization, Spring 2021

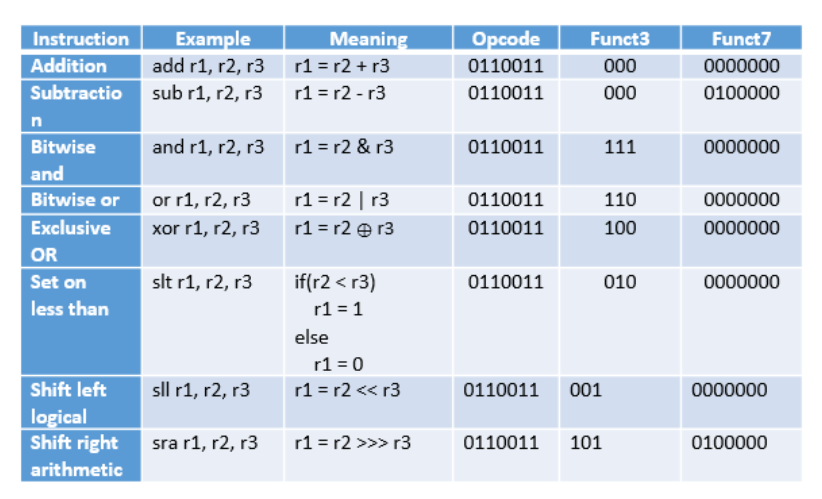
**Lab 3: Single-Cycle CPU (Simple Version)**

**Due: 2021/04/29**

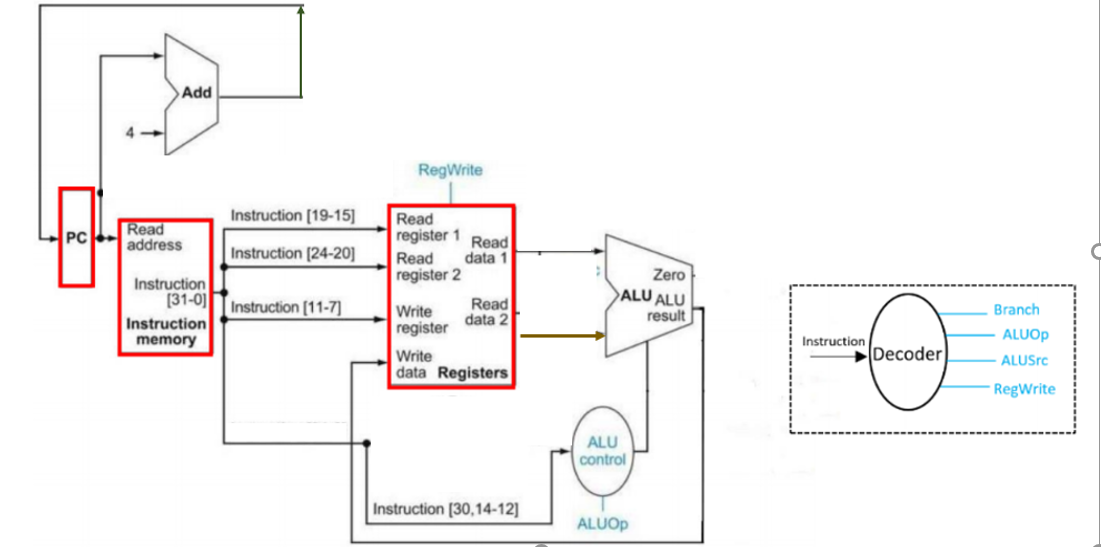
Utilizing the ALU in Lab2 to implement a Simple Single-Cycle CPU. CPU is the most important unit in computer system. Read the document carefully and do the Lab, and you will have the elementary knowledge of CPU.

# HW Requirement

* 1. Please use ISE as you HDL simulator.
  2. Please attach your names and student IDs as comment at the top of each file.
  3. Please use the Program Counter, Instruction Memory, Register File and Testbench we provide you.
  4. Basic instruction set



# 3.Architecture Diagram

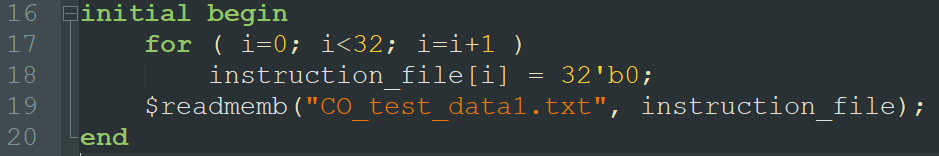


1. **Testbench**

There contain 10 test pattern, CO\_test\_data1.txt ~ CO\_test\_data10.txt.

The default pattern is the first one. Please edit the line 19 in the file “Instr\_Memory.v” to test the other cases.

Line 19: $readmemb("CO\_test\_data1.txt", instruction\_file);



The following are the assembly code for the test pattern:

Initially, in all case, r1=1 , r2=2

|  |  |  |
| --- | --- | --- |
| **Test data 1** | **Test data 2** | **Test data 3** |
| xor r1,r1,r1  add r2,r2,r1  or r3,r2,r1  sll r4,r3,r2  sub r5,r3,r4 | sra r6,r2,r1  sub r4,r4,r2  sub r4,r4,r2  sra r5,r4,r2 | slt r4,r2,r3  sub r3,r3,r2  slt r5,r2,r3 |
| **Final result** | **Final result** | **Final result** |
| r1=0 ,r2=2,r3=2 ,  r4=8 ,r =-6 | r1=1, r =2,r4 =-4  ,r5 = -1 ,r6 =1 | r1=1,r2=2,r3=-2  ,r4=0 , r5=0 |

“CO\_Result.txt” will be generated after Run -All  the testbench. Check you answer with it.

# Grade

* 1. instructions score: 80 points.
  2. Report: 20 points – format is in CO\_Report.docx.
  3. Late submission: 10 percent penalty per day
  4. No plagiarism, or you will get 0 point.

# Hand in

* 1. Zip your folder and name it as “GroupID\_ID1\_ID2.zip” (e.g. G1\_0816001\_0816002.zip) before uploading to newe3. Other filenames and formats such as \*.rar and \*.7z are NOT accepted! Multiple submissions are accepted, and the version with the latest time stamp will be graded.
  2. Please include ONLY Verilog source codes (\*.v) and your report (\*.docx or \*.pdf) in the zipped folder.

# Q&A

For any questions regarding Lab 3, please contact

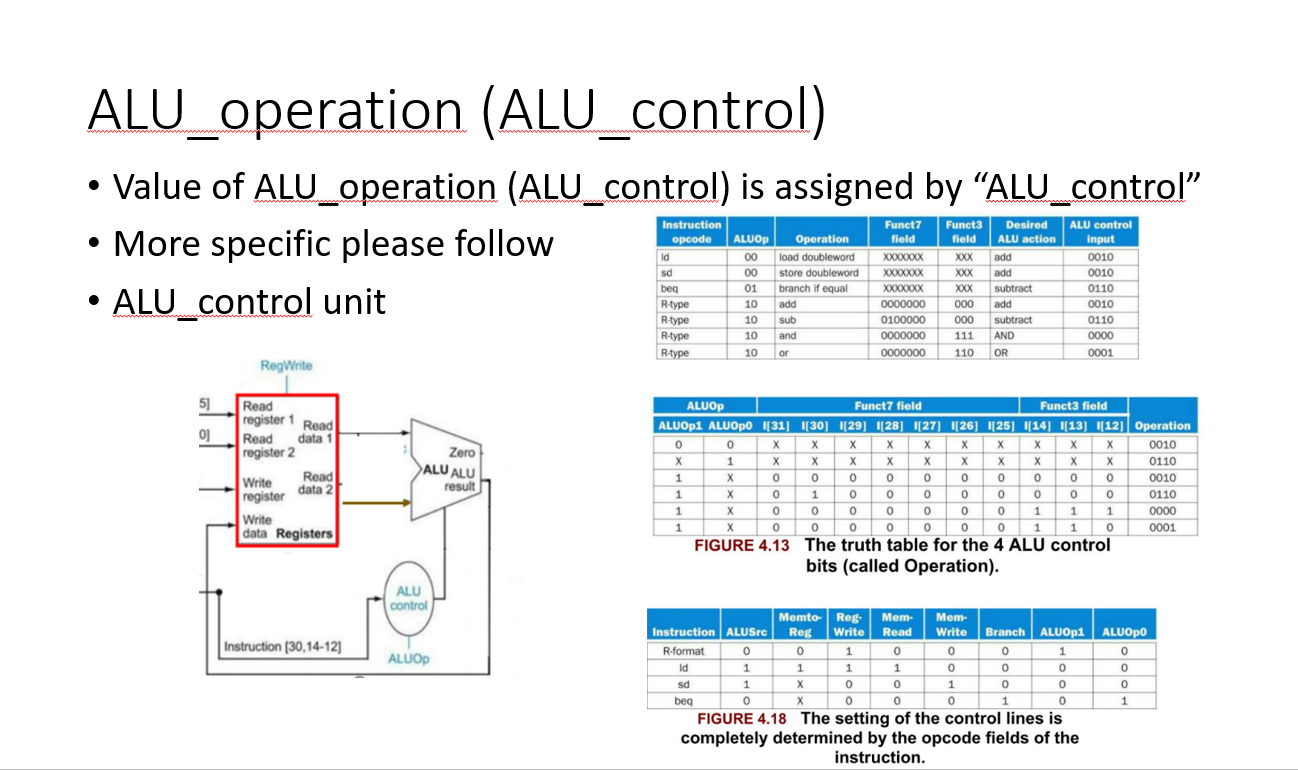
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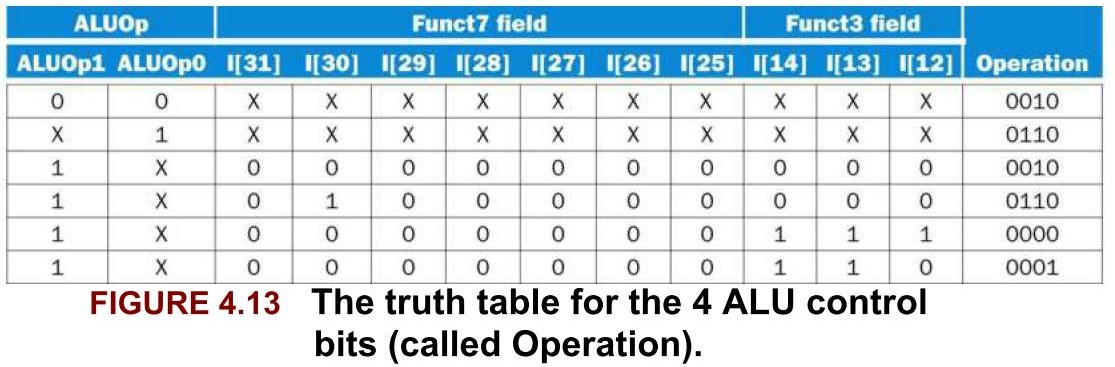
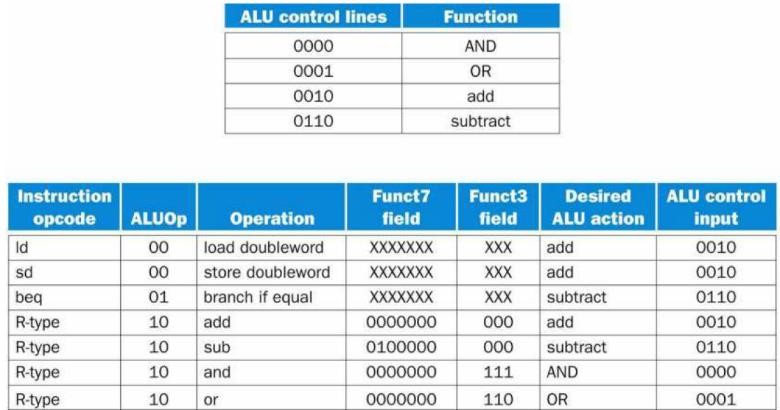
# References

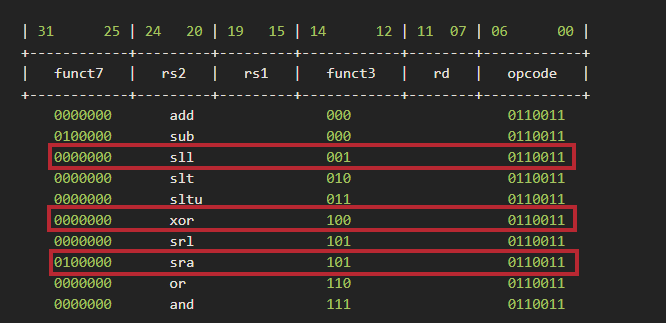


**sll 邏輯左移**

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**ALU Control**





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**XOR:0011**

**Decoder**

