CS6135 VLSI Physical Design Automation

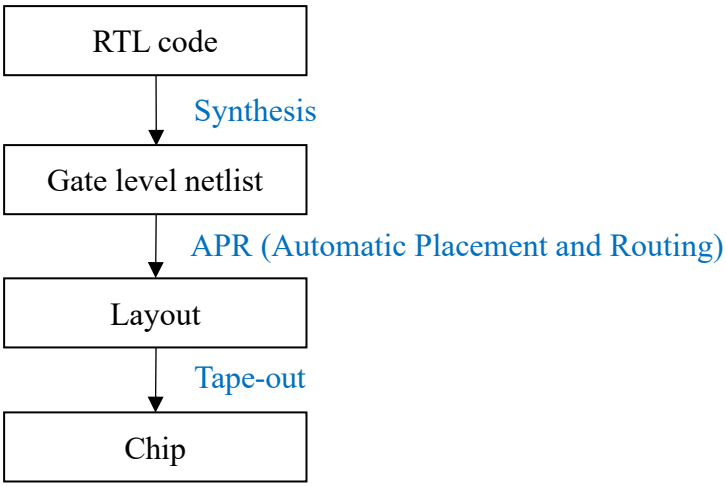
Homework 1: P&R Tool

Due: 23:59, March 13, 2025

1. Introduction

In this homework, you will use Cadence Innovus to complete the Place and Route (P&R) flow for a given synthesized standard-cell design. This assignment aims to familiarize you with Innovus and the P&R process. Additionally, you are encouraged to optimize timing, chip area, and wire length. The quality of your optimization will affect your score, so strive for the best performance in all metrics.

Please follow the procedures in **Section 6** and use Cadence Innovus for automated place and route (APR) to generate the layout.



2. Objectives

- Optimize the timing by adjusting the clock period in the *sdc/sha256.sdc* file.
  - Default clock period: `600`
  - In .sdc: `create_clock -name "clk" -period 600 [get_ports clk]`
- Optimize the area by adjusting the core utilization in the floorplan stage.
  - Default Core Utilization: `0.4`
- Try to achieve non-negative slack and zero DRC violations.

3. Report

Your report should at least contain the following contents.

(1) Your name and student ID

(2) Record different configurations of the core utilization, clock period, DRC violations, slack, chip area, and wire length. Furthermore, explain the observation of the experiment. (Try more than 5 different configurations to get full points in this question.)

Core Utilization	Clock Period	DRC violations	Slack	Chip Area	Wire length

(3) Explain how the adjustments of the clock period and the core utilization affect the metrics (DRC violations, slack, chip area, and wire length).

(4) Explain the purpose of inserting well tap cell.

(5) Show the configuration from your best result. The information to be included in the configuration is listed below. Please try to maintain non-negative slack and zero DRC violations.

i. Clock period (in file *sha256.sdc*)

ii. Slack time (in generated file *timing.rpt*)

iii. Total area of chip (in generated file *summary.rpt*)

iv. Total wire length (in generated file *summary.rpt*)

v. DRC violations (in generated file *drc.rpt*).

(6) Show the final chip layout of your best result generated by Innovus (use print-screen to save the final layout and paste on the report)

4. Grading

- ✓ 50%: The completeness of your submitted report
- ✓ 50%: The quality (For all the following attributes, lower values indicate better performance.)
  - clock period (in file *sha256.sdc*)
  - Total area of chip (in generated file *summary.rpt*)
  - Total wire length (in generated file *summary.rpt*)

5. File Submission

Download the *file_submission_example.zip* from eeclass, unzip it, and follow its folder structure for your submission.

```
$ unzip file_submission_example.zip
```

Name your folder *CS6135_HW1_{STUDENT_ID}*, compress it into a *.zip* file name *CS6135_HW1_{STUDENT_ID}.zip*, and submit it to eeclass. The details below describe the contents of each folder.

(1) *CS6135_HW1_{STUDENT_ID}.tar.gz*

- An archive containing your post P&R design

  ```
  $ tar -zcvf CS6135_HW1_{STUDENT_ID}.tar.gz HW1/
  ```

  For example:

  ```
  $ tar -zcvf CS6135_HW1_ 113000000.tar.gz HW1/
  ```

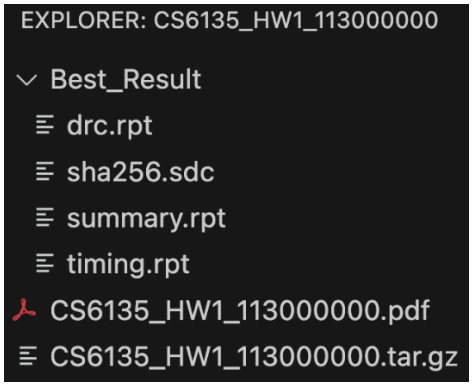
(2) *CS6135_HW1_{STUDENT_ID}_report.pdf*

- Your report

(3) A *Best_Result* folder

- Contain *drc.rpt*, *sha256.sdc*, *summary.rpt*, and *timing.rpt*

The folder structure would be like the following figure:



6. Procedures

Follow the steps below to complete the physical implementation of the given design. Note that the provided figures are for reference only, and your results may differ.

Before proceeding, ensure you have a basic understanding of the command-line interface (CLI). If you are unfamiliar with shell commands or Vim, refer to the *Shell Tutorial.pdf* uploaded to eeclass.

A. Design Preparation

Step 1. Log in to the workstation (using MobaXterm for ease)

Please download *HW1.tar.gz* from eeclass, and upload the file to the server nthucad.cs.nthu.edu.tw.

```
$ scp HW1.tar.gz {YOUR_ACCOUNT}@nthucad.cs.nthu.edu.tw:.
```

("$" is a prompt, not a command, so don't type it. "scp" stands for **s**ecure **c**o**p**y.)

Next, log in to the server nthucad.cs.nthu.edu.tw using the ssh command in a terminal application (e.g., PuTTY, Cygwin, MobaXterm, Terminal.app). After logging in, change your password by entering the command "yppasswd".

("ssh" stands for **s**ecure **sh**ell. "-XY" means to enable X11 forwarding to see GUI.)

```
$ ssh -XY {YOUR_ACCOUNT}@nthucad.cs.nthu.edu.tw
$ yppasswd
```

The server nthucad.cs.nthu.edu.tw functions as a proxy (relay) server used to access other servers within a private network. It provides only basic services, so you must log into a Linux-based workstation server (e.g., ic53) to run Innovus.

```
$ ssh -XY ic53
```

You can also enter "lab_uptime" to check the load on each available server. It is recommended to login to a server with fewer active users for better performance.

```
nthucad:~> lab_uptime
--------users---load average------------------users---load average---
ic21 (l): 3   0.00, 0.04, 0.05   ||   ic22 (l): 0   0.01, 0.02, 0.05
ic51 (l): 8   8.23, 8.68, 9.49   ||   ic53 (l): 3   0.05, 0.03, 0.05
ic55 (l): 2   0.00, 0.01, 0.05   ||   ic56 (l): 3   0.01, 0.06, 0.06
last updated: 公曆 20廿五年 二月 十八日 週二 十七時九分二秒
(l) Linux, (s) SunOS, (D) Shutdown
```

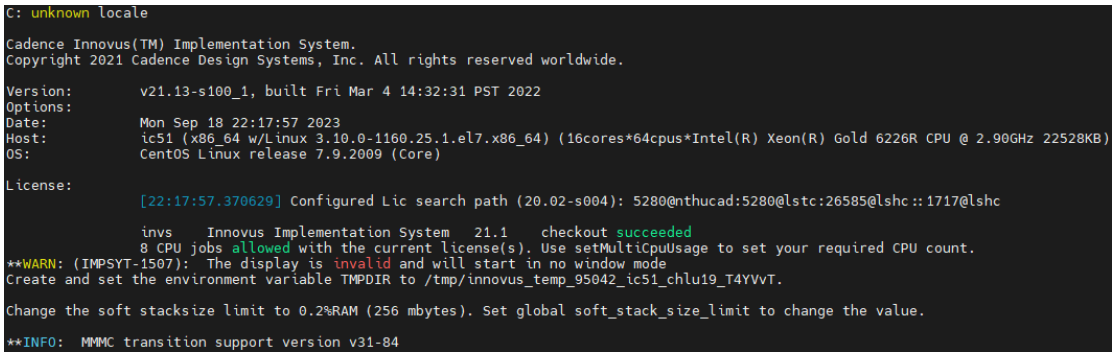
Step 2. Invoke Innovus

```
$ tar -zxvf HW1.tar.gz                    # untar the archive
$ cd HW1/scripts
```

Before launching Innovus with the GUI, ensure an X server (e.g., Xming or X-Win32) is installed on your computer. If you are using MobaXterm (Windows) or XQuartz (macOS), you can skip this step. Otherwise, you must manually set the DISPLAY environment variable to your IP address.

```
$ innovus                                 # invoke Innovus
```

(If you didn't set up a X server on your PC and forward X11 to the workstation properly, you will get the following error.)



B. Design Setup

First, we need to import the given design and read in all required files. Each time you enter a command, it's very important for you to check whether the error messages show in the console.

Step 1. Set CPU Usage, Process Node, and Technology

Navigation bar > Tools > Set Multiple CPU Usage …

Local Machine

Number of Local CPU(s)	8

click **OK**

```
innovus> setDesignMode -process 7 -node N7
```

Step 2. Import Design

Navigation bar > File > Import Design…

Netlist

Verilog	Selected
Files	../design/sha256.v
Top Cell	Select "Auto Assign"

Technology/Physical Libraries

* Note that the order of the .lef files matter *

LEF Files	Selected
LEF Files	../lef/asap7_tech_4x_201209.lef ../lef/asap7sc7p5t_28_L_4x_220121a.lef ../lef/asap7sc7p5t_28_SL_4x_220121a.lef

Power

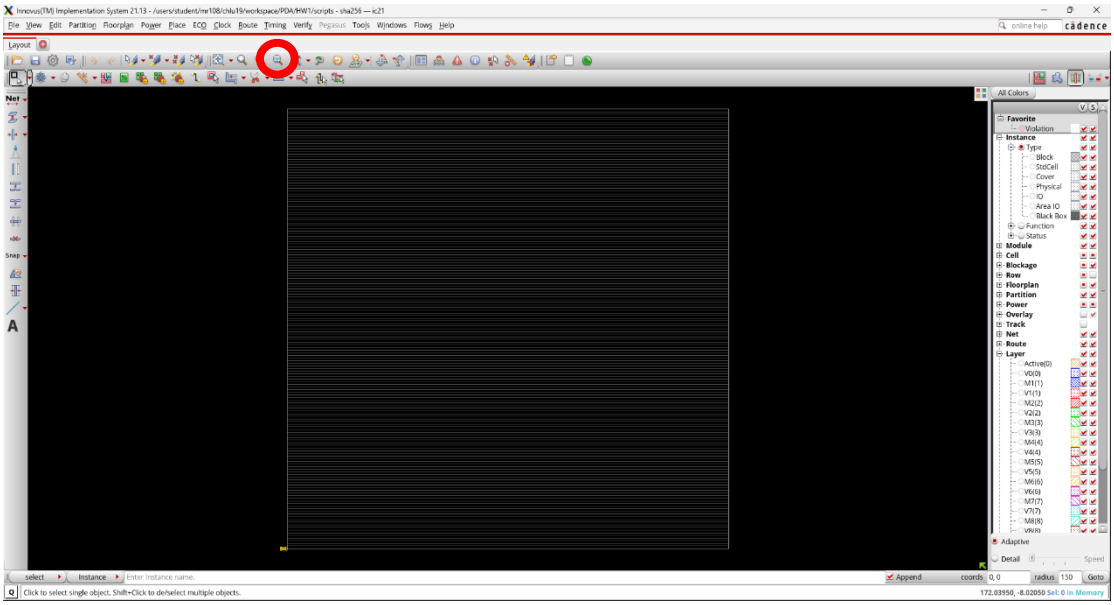
Power Nets	VDD
Ground Nets	VSS

Analysis Configuration

MMMC View Definition File	mmmc.view

click **OK**

A layout window similar to the figure below will open. Click the highlighted button first to fit the design to the window size.



Routing layer

```
innovus> setDesignMode -bottomRoutingLayer 2
innovus> setDesignMode -topRoutingLayer 7
```

Step 3. Save design

Navigation bar > File > Save Design…

Data Type	Select “Innovus”
File Name	setup

click **OK**

Restore design

P.S. You cannot restore a design when another design is opened

Navigation bar > File > Restore Design…

Data Type	Select “Innovus”
Files of type	All Files (*)
Restore Design File	setup (Your saved design)

click **OK**

After restoring the design, please make sure you are in the "Physical view" rather than the "Floorplan view." You can find the view mode buttons at the upper-right corner.

C. Pre-power planning and Floorplan

Step 1. Connect Global Net

Navigation bar > Power > Connect Global Net…

Power Ground Connection > Connect

Pin	Selected
Pin Name(s)	VDD

Power Ground Connection > Scope

Apply All	Selected

Power Ground Connection

To Global Net	VDD

click **Add to List**

Power Ground Connection > Connect

Pin	Selected
Pin Name(s)	VSS

Power Ground Connection > Scope

Apply All	Selected

Power Ground Connection

To Global Net	VSS

click **Add to List**

Click **Apply** and **close the pop-up window**

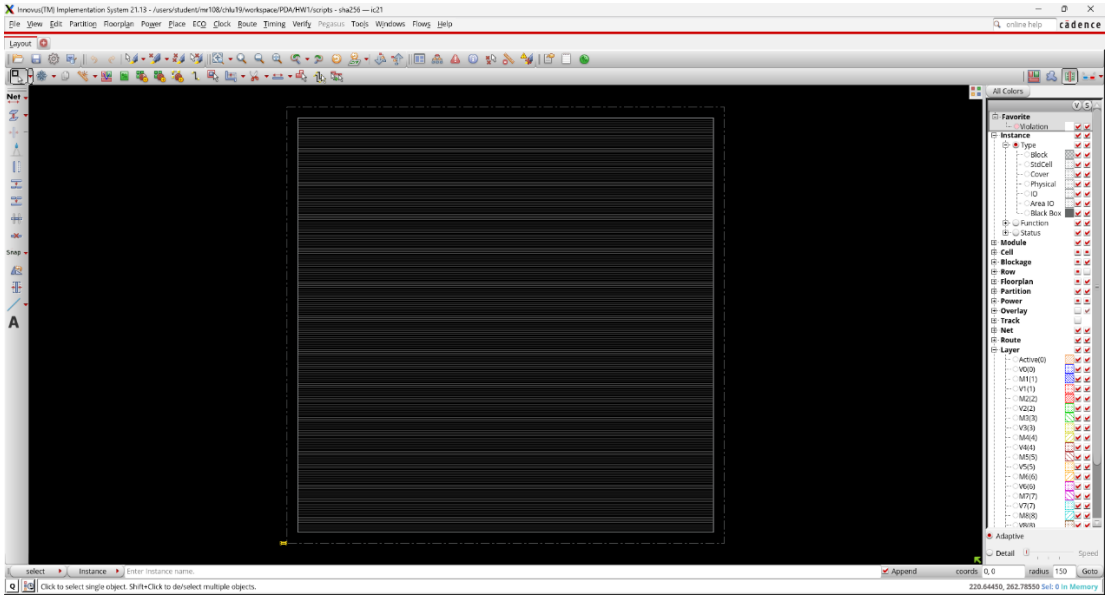
Step 2. Initialize floorplan (specify a region and put our design in it.)

Navigation bar > Floorplan > Specify Floorplan… > Basic

Specify By	Select “Size”	
Core Size by	Select “Aspect Ratio”	
Ratio (H/W)	1.0	
Core Utilization	0.4 (Depends on you, 0 < utilization < 1)	
Core Margins by	Select “Core to Die Boundary”	
Core to Die Boundary	Core to Left: 6.22	Core to Top: 6.22
	Core to Right: 6.22	Core to Bottom: 6.22

click **OK**

The initial floorplan should be like the following figure. The gray solid rectangle is the core area in which you will put all your standard cells.



D. Insert Well Tap Cells and Tracks

Now, use *.tcl* scripts instead of relying solely on the GUI to complete the next steps. A *.tcl* script functions like a shell script, recording all the procedures you want to execute on the layout.

```
innovus> source add_well_tap_and_track.tcl
```

E. Pin Adjustment

```
innovus> source pin_adjustment.tcl
```

F. Power planning

Step 1. Construct Power Network

Navigation bar > Power > Power Planning > Add Ring…

Basic

Net(s)	VDD VSS

Ring Configuration

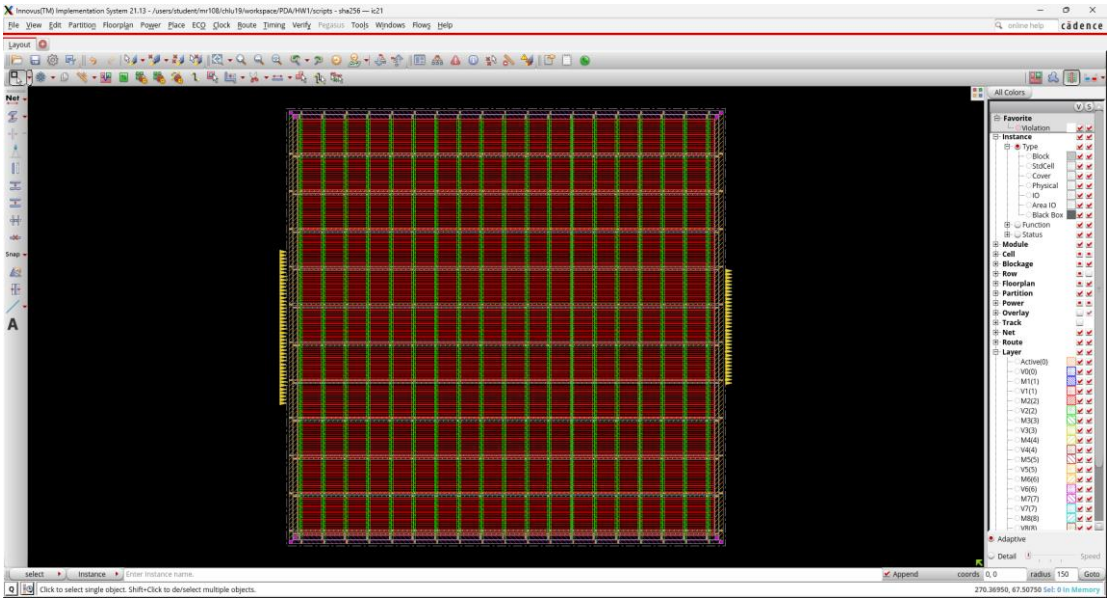
	Layer	Width	Spacing	Offset
Top	M7(7) V	2.176	0.384	0.384
Bottom	M7(7) V	2.176	0.384	0.384
Left	M6(6) H	2.176	0.384	0.384
Right	M6(6) H	2.176	0.384	0.384

click **OK**

Add Stripe

```
innovus> source add_stripe.tcl
```

After completing these steps, you will see the power planning results as shown below. Make sure to check the "Net" checkbox.



Step 2. Special Route

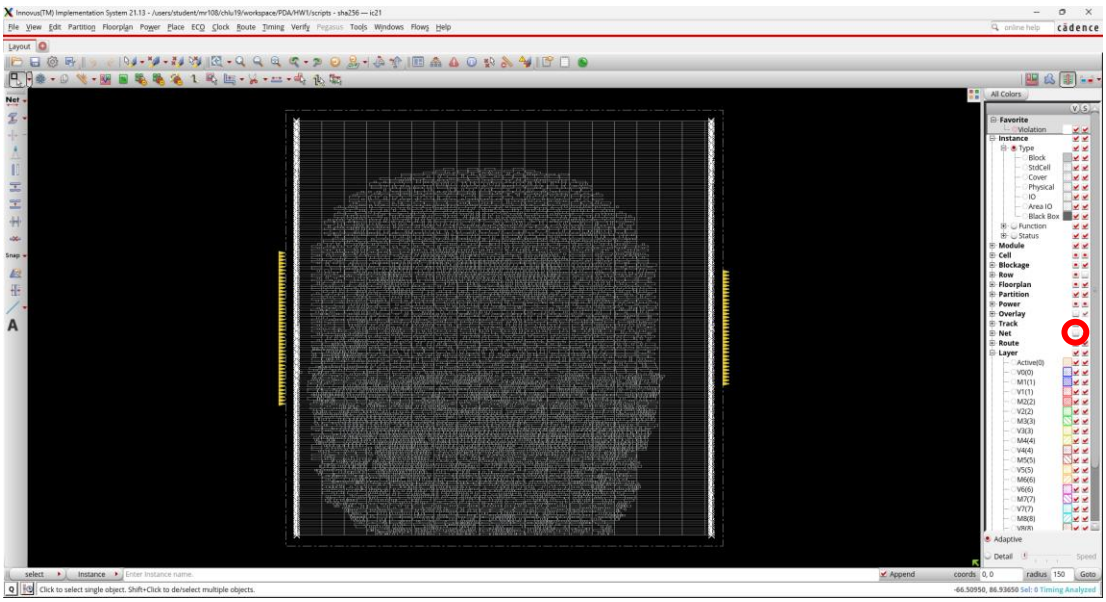
```
innovus> source special_route.tcl
```

G. Placement

Step 1. Place standard cell

```
innovus> place_opt_design
```

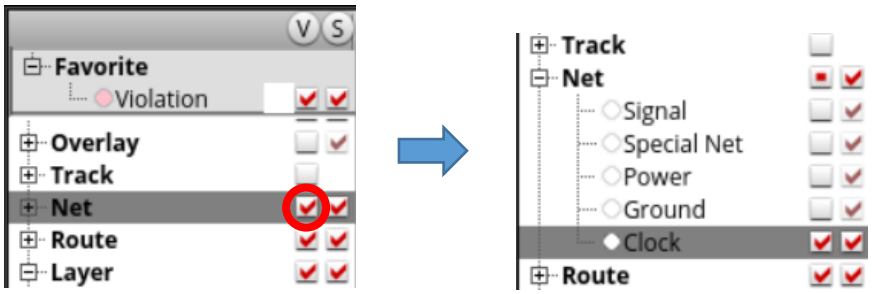
In order to see the placed standard cell, please remember to uncheck the marked checkbox to hide the routing net. You can use the zooming utility to observe the layout.



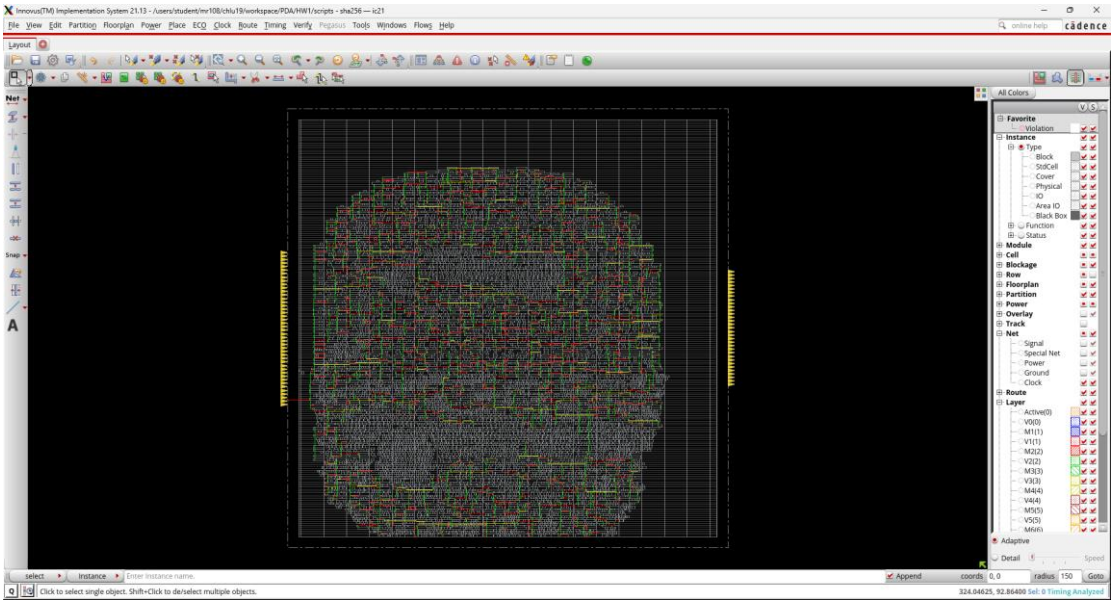
H. Clock Tree Synthesis (CTS)

You can see the clock tree by doing the following instruction:

1. Make sure “Route” checkbox is checked and uncheck the “Net” checkbox.
2. Double click on the “Net” and then check the “Clock” checkbox.



After completing these steps, you will see a result similar to the image below, displaying the clock tree.



Save design

Navigation bar > File > Save Design…

Data Type	Select “Innovus”
Path Name	placement

click **OK**

I. Route (Clock Nets and Signal Nets)

Step 1. Route Design

```
innovus> source route.tcl
```

Step 2. Analyze timing (setup and hold) and check routability

```
innovus> report_timing
```

Is there any timing violation (slack < 0)?

(slack = required time - arrival time. If slack < 0, it is failed.)

(Optional step) Optimize routing results

*** This command will usually work at other cases, but it may ruin this case. ***

*** Not recommend for running the following commands on this case. ***

If there is any timing violation, you can try to fix them by following command:

```
innovus> setAnalysisMode -analysisType onChipVariation
innovus> optDesign -postRoute
```

Step 3. Fix DRC violations

Check if there are any DRC violations in the current design by the following command:

```
innovus> verify_drc
```

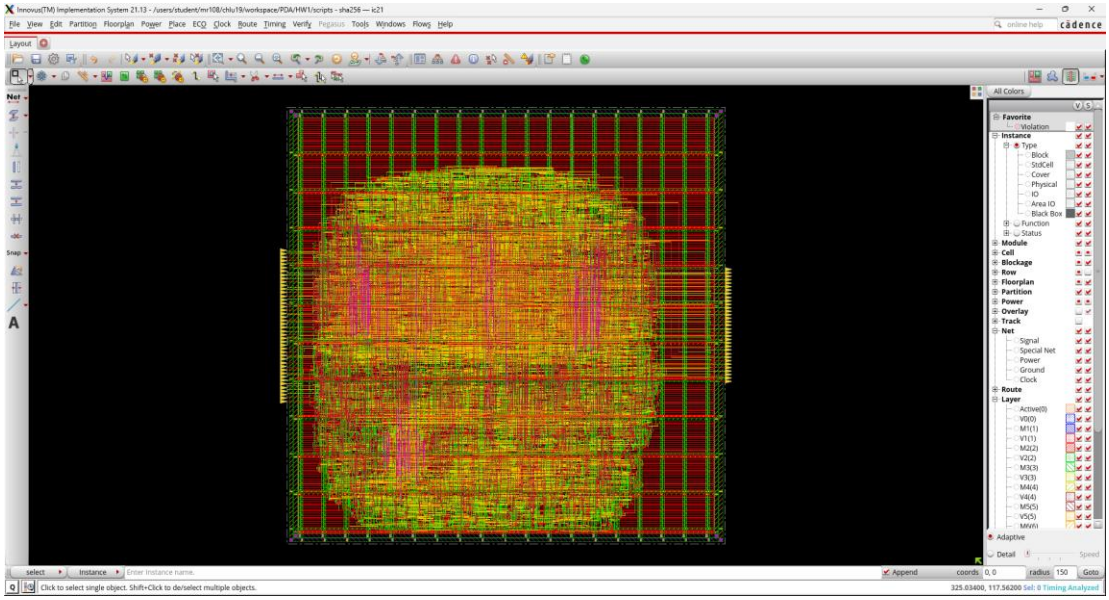
(Optional step) Optimize routing results with ecoRoute

If there are any DRC violations, you can try to fix them by the following command:

```
innovus> ecoRoute -fix_drc
```

If there are still any DRC violations, you should attempt to reduce core utilization during the floorplan stage and then redo all the steps mentioned above.

After completing these steps, you will see the routing result image as below.



Step 4. Save design

Navigation bar > File > Save Design…

Data Type	Select “Innovus”
Path Name	route

click **OK**

J. Output and Record

Step 1. Dump report

```
innovus> report_timing > ../timing.rpt
innovus> summaryReport -noHtml -outfile ../summary.rpt
```

You can find the total area of chip (`Total area of Chip`) and total wire length (`Total wire length`) in the summary.rpt file.

```
innovus> verify_drc > ../drc.rpt
```

Step 2. Take a snapshot of your final layout

Paste this layout figure into your report.

Step 3. Exit

```
innovus> exit
```

(Tip) Save .tcl

When the last time you exit the Innovus, all your operations are translated as commands and are stored in the file *innovus.cmd[index]*. You can rename it to *apr.tcl* and store it for further use. Also, you can open Innovus with the option *-no_gui*. It will significantly reduce running time since GUI needs time to render components.

(Tip) Open innovus with *-no_gui*

```
$ innovus -no_gui
```

(Tip) Execute *apr.tcl*

```
innovus> source apr.tcl
```