EDA HW1 Report

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Configuration Settings

Core Utilization	Clock Period	DRC Violation	Slack time	Chip Area(um^2)	Wire Length(um)
0.2	800	0	53.012	122090.914	191045.2880
0.4	600	0	5.169	62888.348	187162.82
0.6	800	0	42.953	42877.797	186532.9280
0.6	600	1	2.200	42877.797	185763.1880
0.7	780	0	35.127	37121.981	175034.3040
0.8	800	7	50.424	32789.090	163750.944
0.9	200	102	-349.400	29387.764	186623.388

Effect of Clock Period and Core Utilization

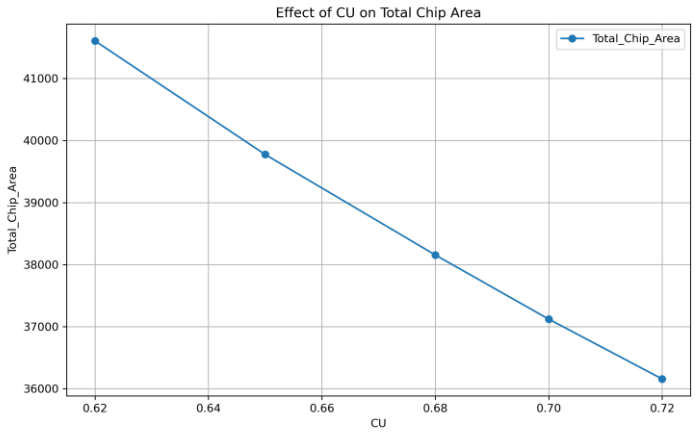

Figure 1

Figures 1, 2, and 3 illustrate the effects of varying core utilization (CU) on chip design metrics, with a constant clock period (CP) of 700. Figure 1 depicts total chip area, Figure 2 shows total wire length, and Figure 3 presents slack time. Observations from Figures 1 and 2

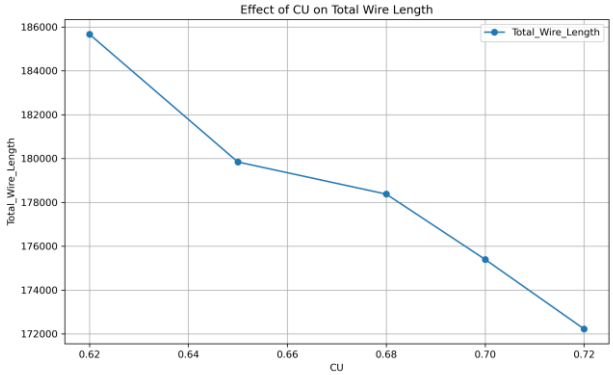

Figure 2

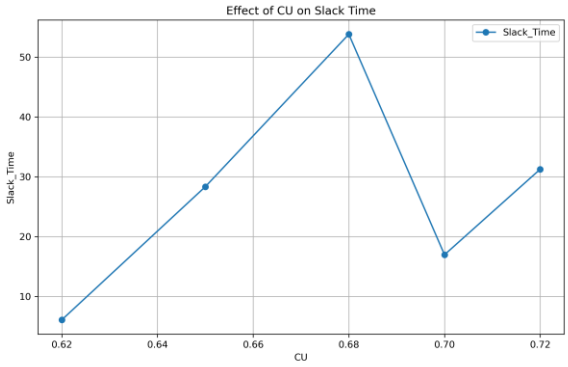

Figure 3

reveal that higher CU reduces both total chip area and wire length. However, the relationship differs between the two: the effect of CU on chip area is linear, whereas its impact on wire length is nonlinear. In contrast, Figure 3 indicates no significant correlation between CU and slack time.

Figures 4, 5, and 6 explore the influence of varying clock periods (CP) at a fixed CU of 0.62. Figure 4 shows total wire length, Figure 5 displays total chip area, and Figure 6 presents slack time. Clock period affects both wire length and slack time, but not chip area. Specifically, for clock periods between 400 and 550, shorter clock periods increase wire length, though this effect disappears outside this range. For slack time, the result shows shorter clock periods consistently reduce slack time.

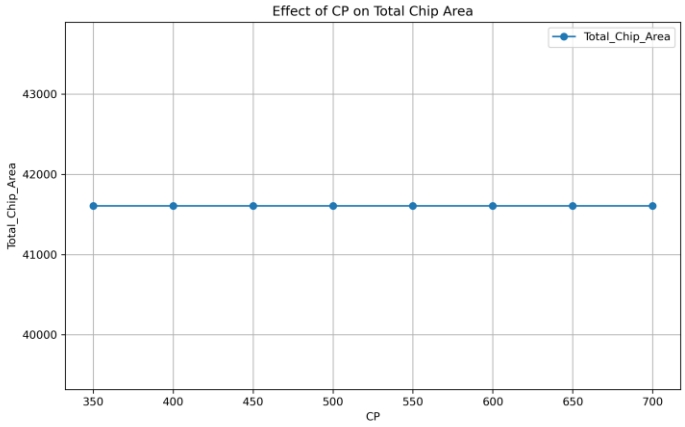

Figure 4

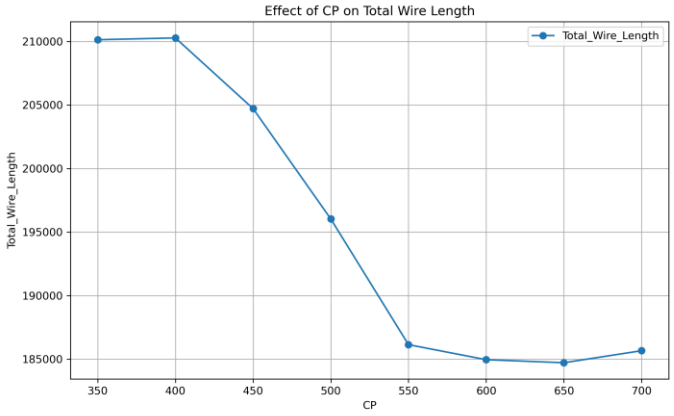

Figure 5

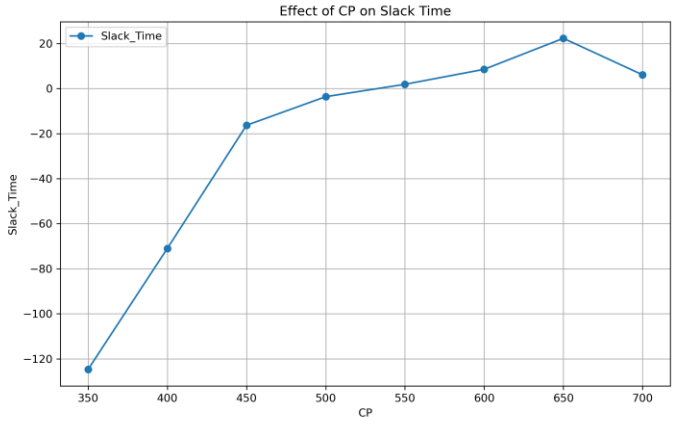

Figure 6

Purpose of Inserting Well Tap Cell

The purpose of inserting well tap cells before placing standard cells is that we can use tapless standard cells which are smaller than normal cells. If we don’t insert well tap cells and use tapless standard cells, it will cause latch-up. Latch-up occurs when parasitic PNPN thyristors in CMOS circuits create a low-impedance path between VDD and VSS, leading to high current flow and possible chip failure.

Best Configuration

Core Utilization	Clock Period	DRC Violation	Slack time	Chip Area(um^2)	Wire Length(um)
0.7	780	0	35.127	37121.981	175034.3040

Final Chip Layout