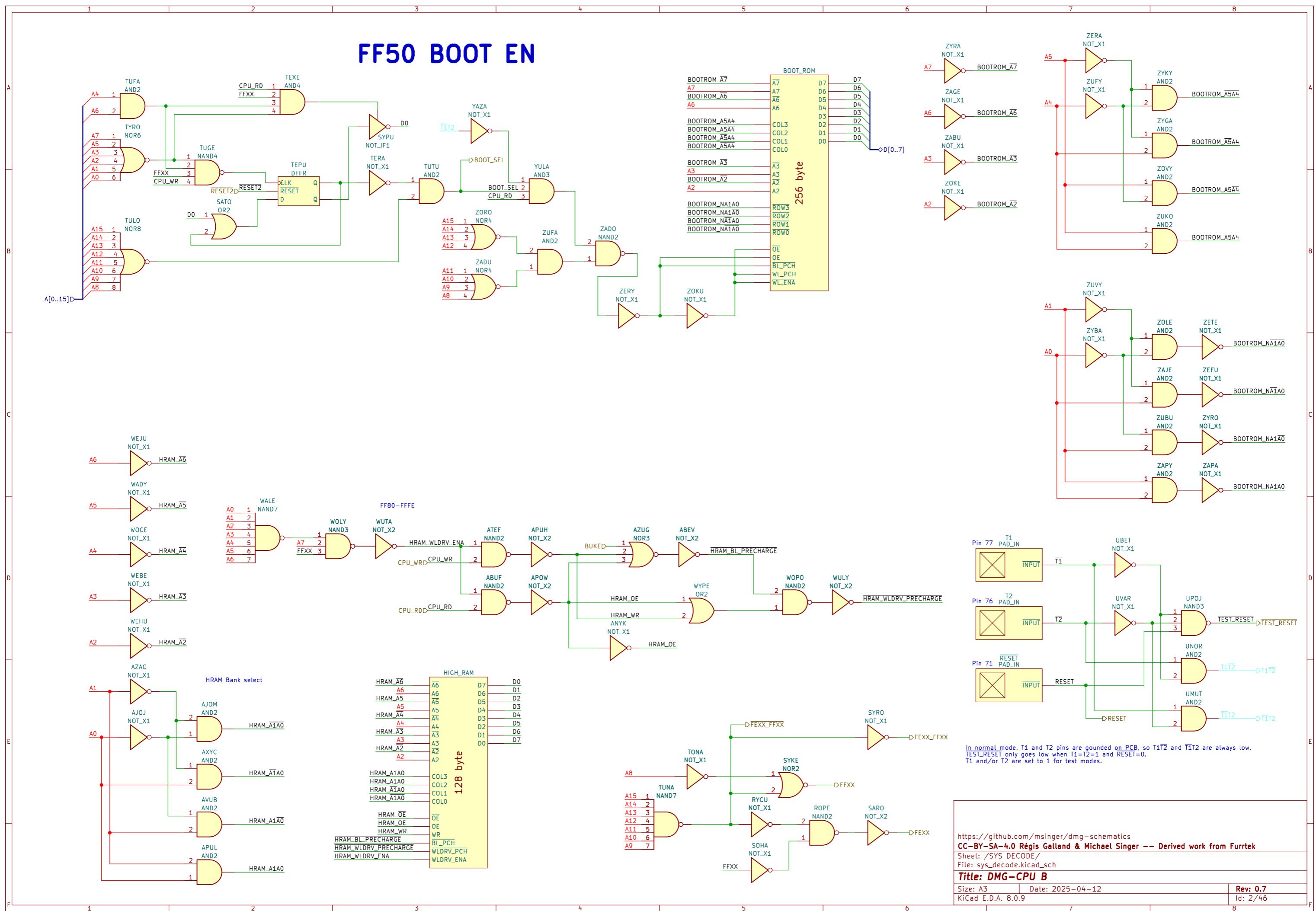
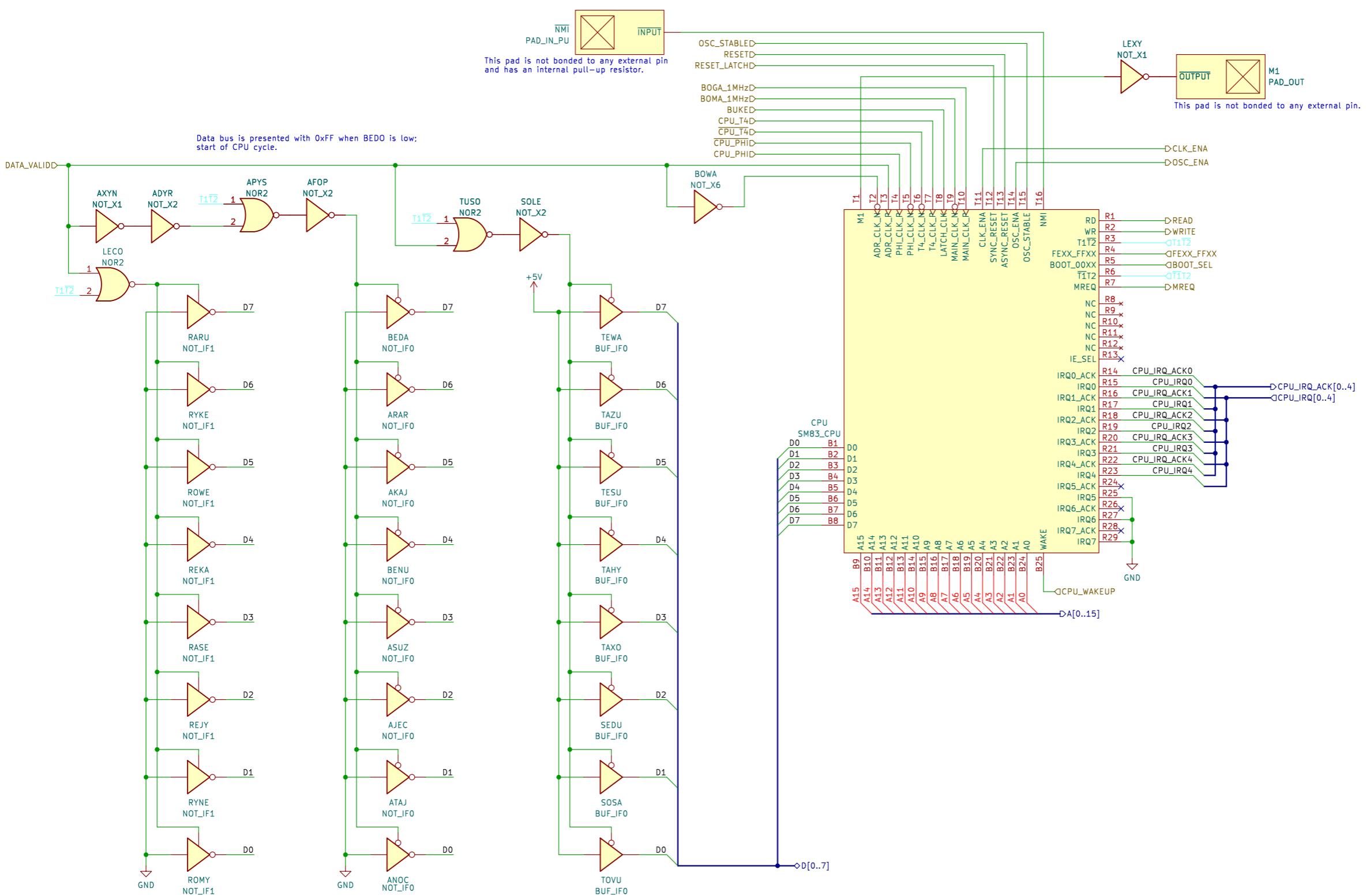


Green boxes contain 10 pins  
Red boxes contain sub sheets

<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek  
 Sheet: / File: dmg\_cpu\_b.kicad\_sch  
**Title: DMG-CPU B**  
 Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9 Rev: 0.7  
 Id: 1/46

FF50 BOOT EN





<https://github.com/msinger/dmg-schematics>  
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Sheet: /CPU/

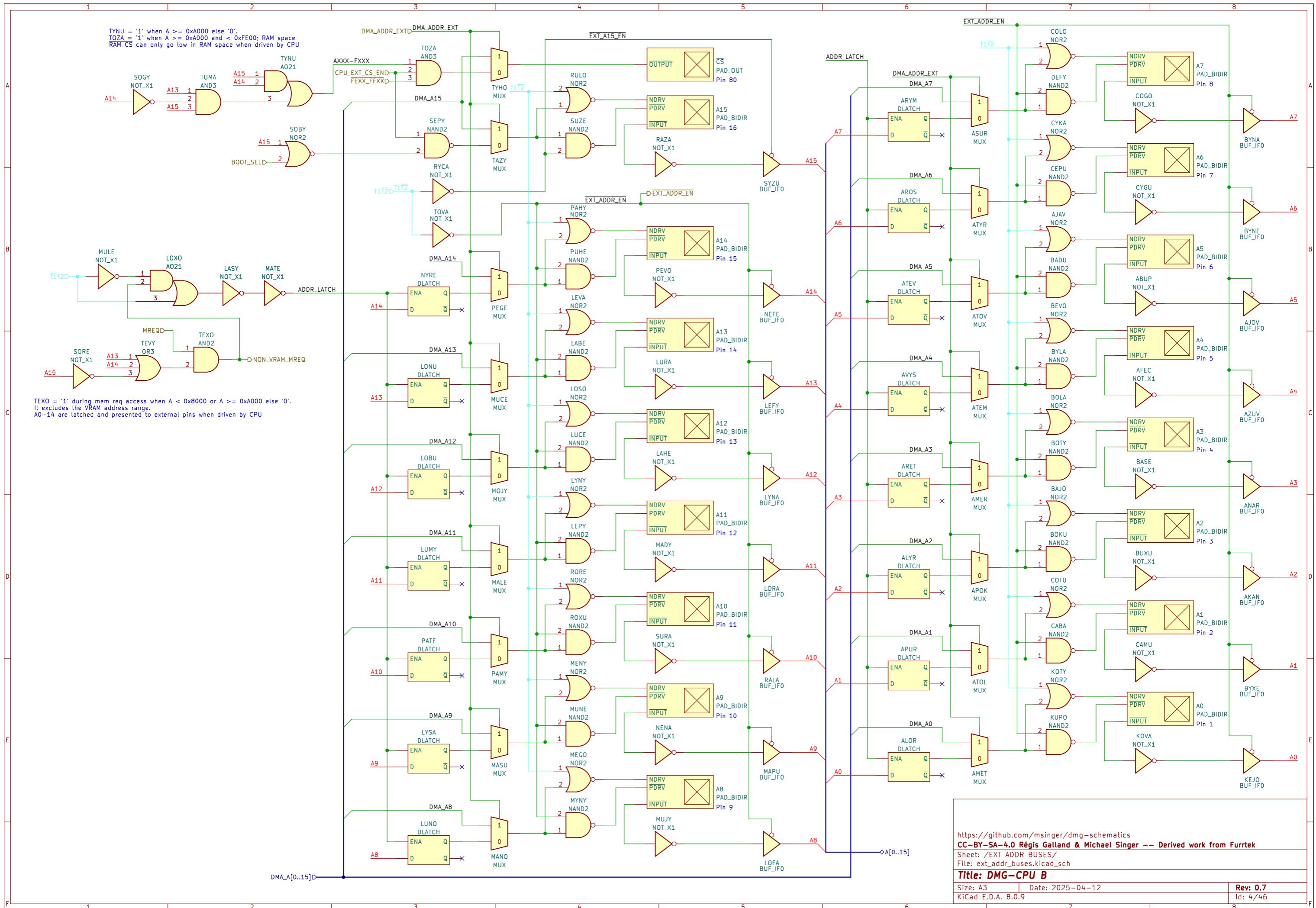
File: cpu.kicad\_sch

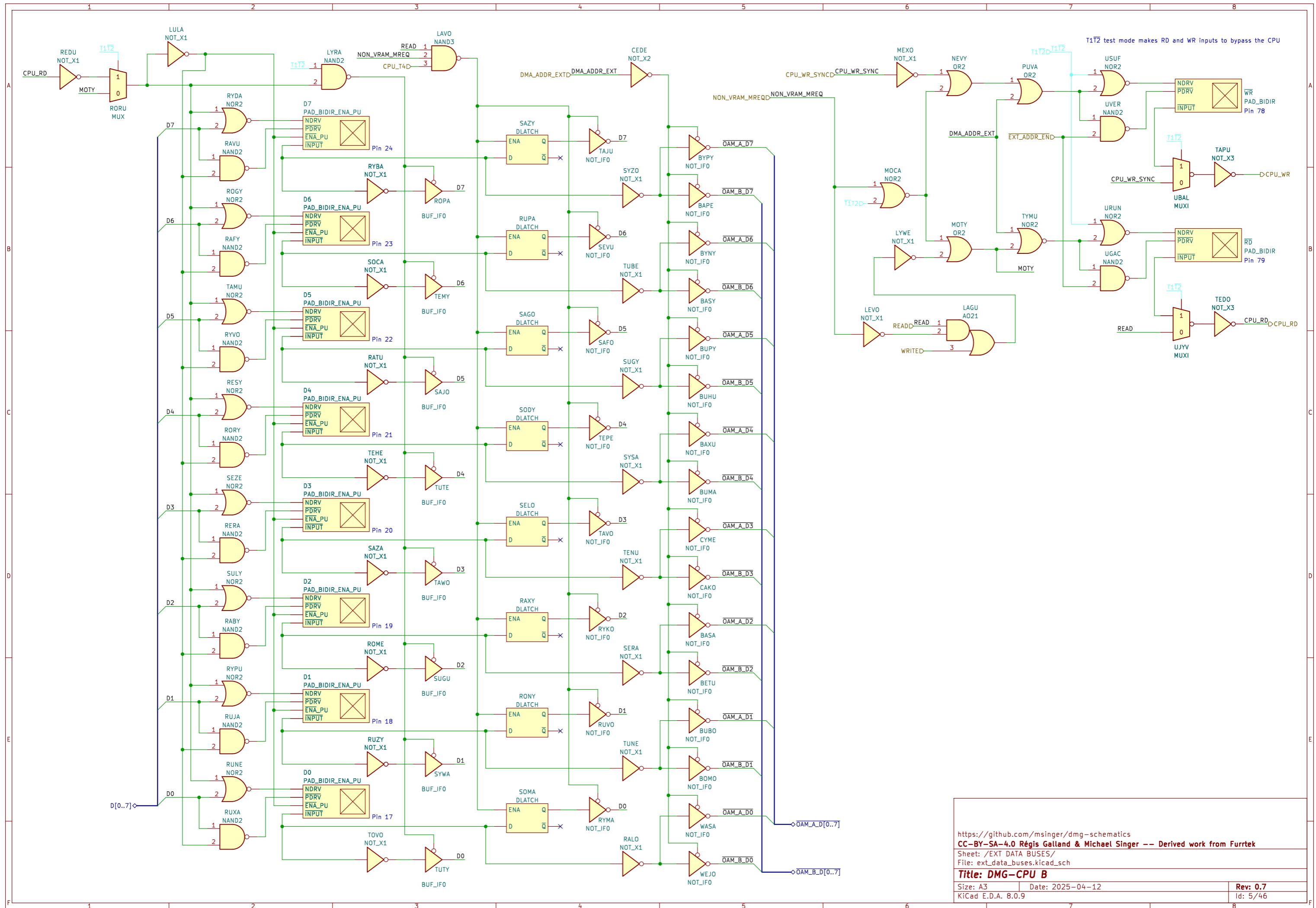
## Title: DMG-CPU B

Size: A3 Date: 2025-04-12  
KiCad EDA 8.0.0

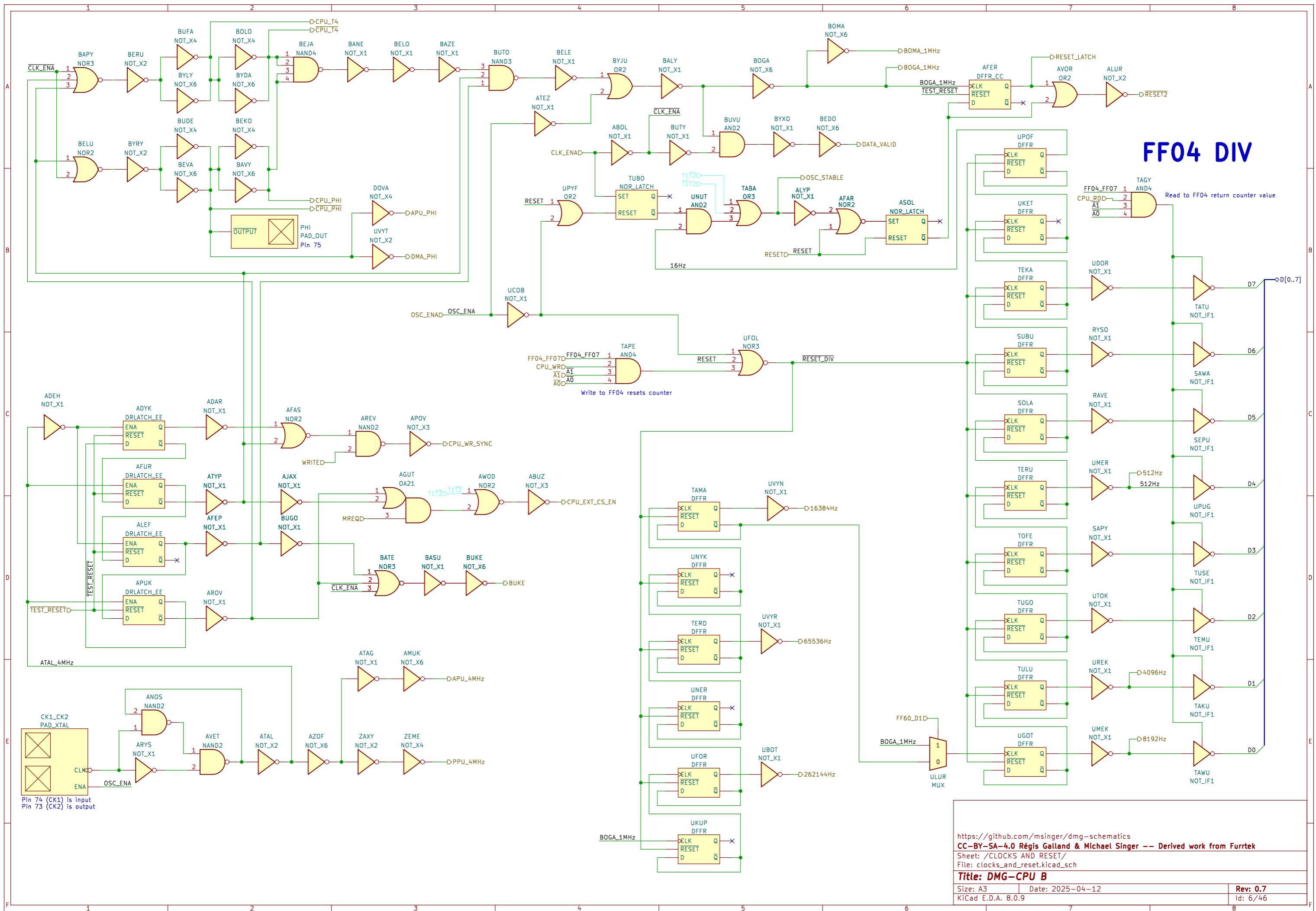
KiCad E.D.A. 8.0.9

Rev: 0.7

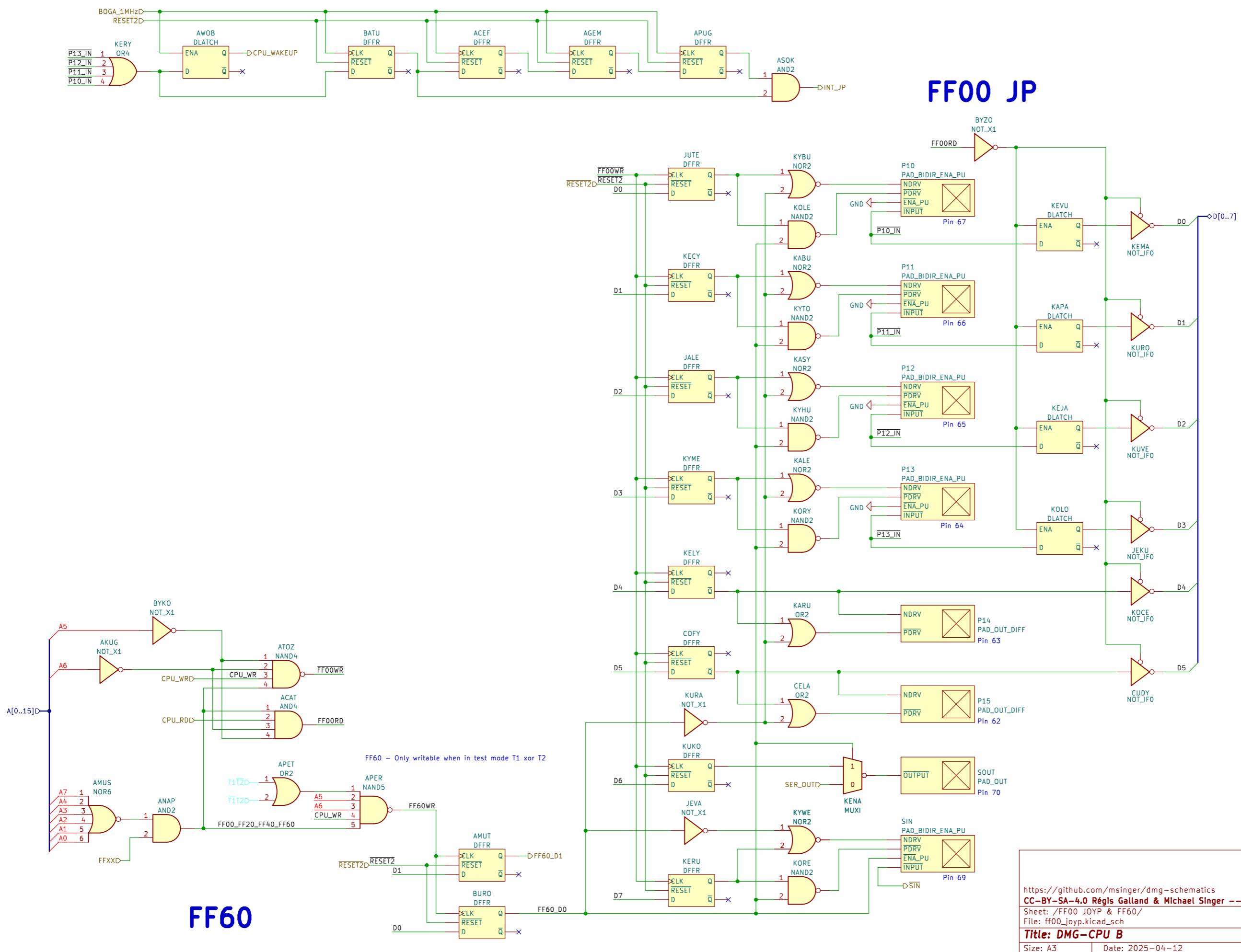




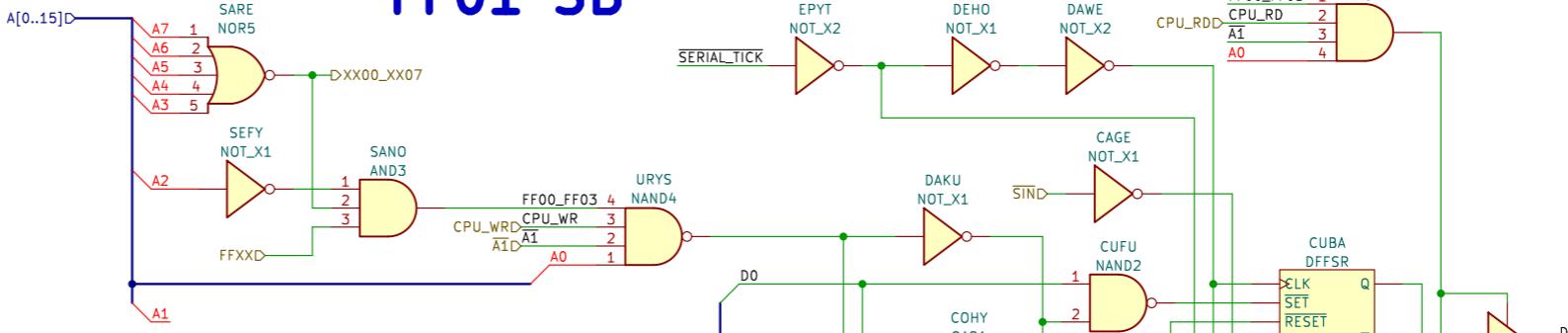
# FF04 DIV



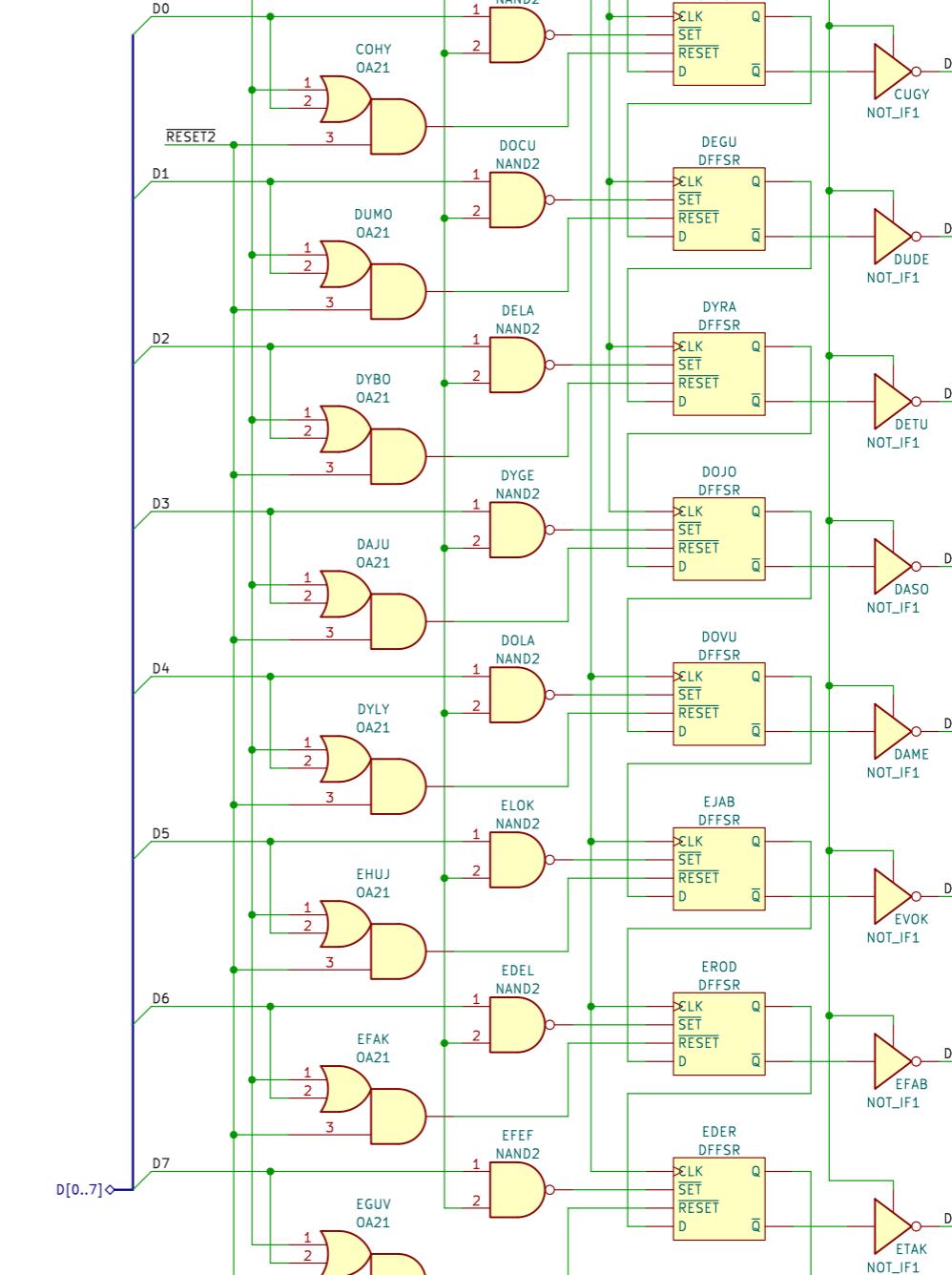
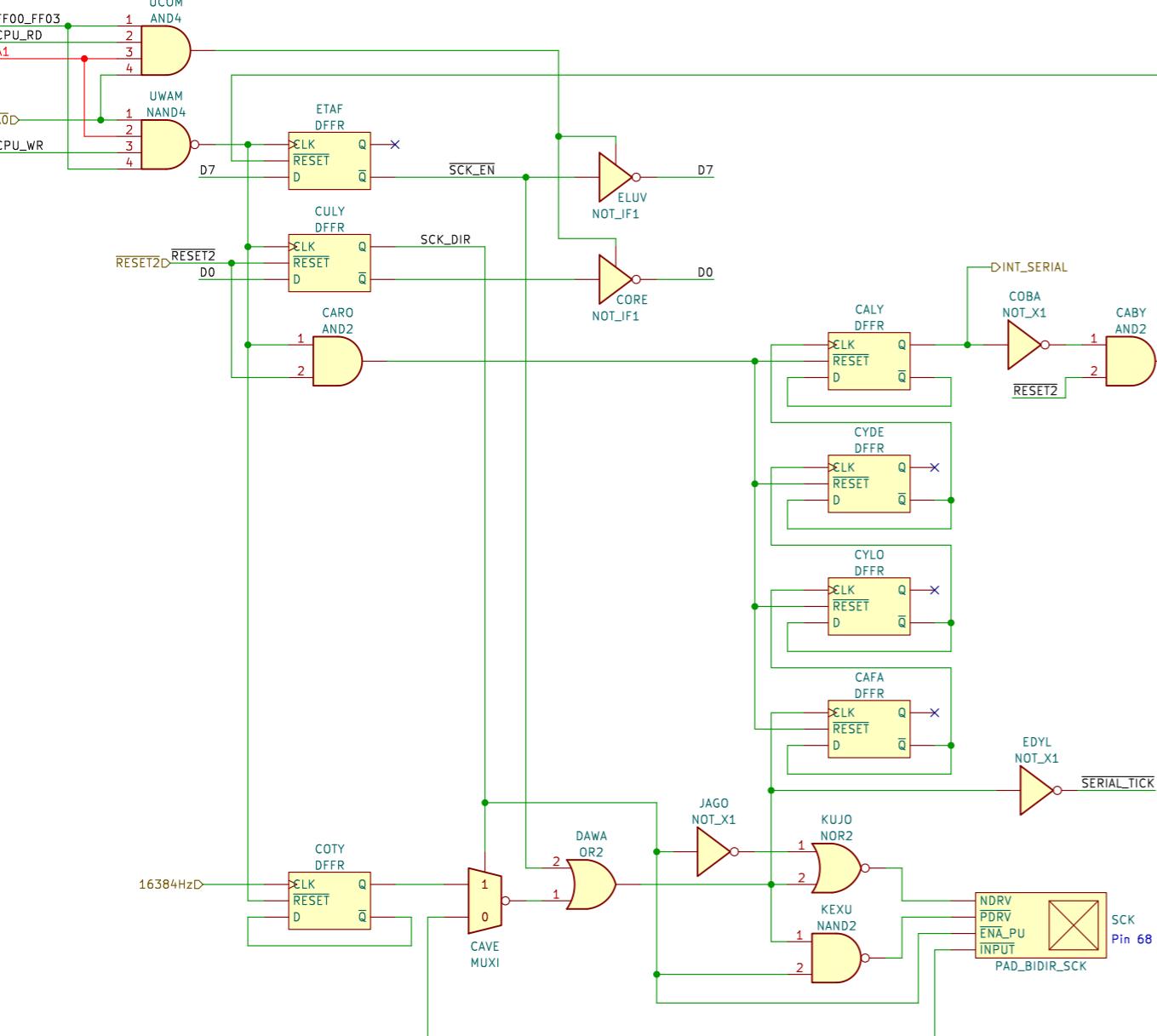
# FF00 JP



# FF01 SB



# FF02 SC



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Sheet: /FF01-02 SERIAL LINK/

File: ff01-02\_serial.kicad\_sch

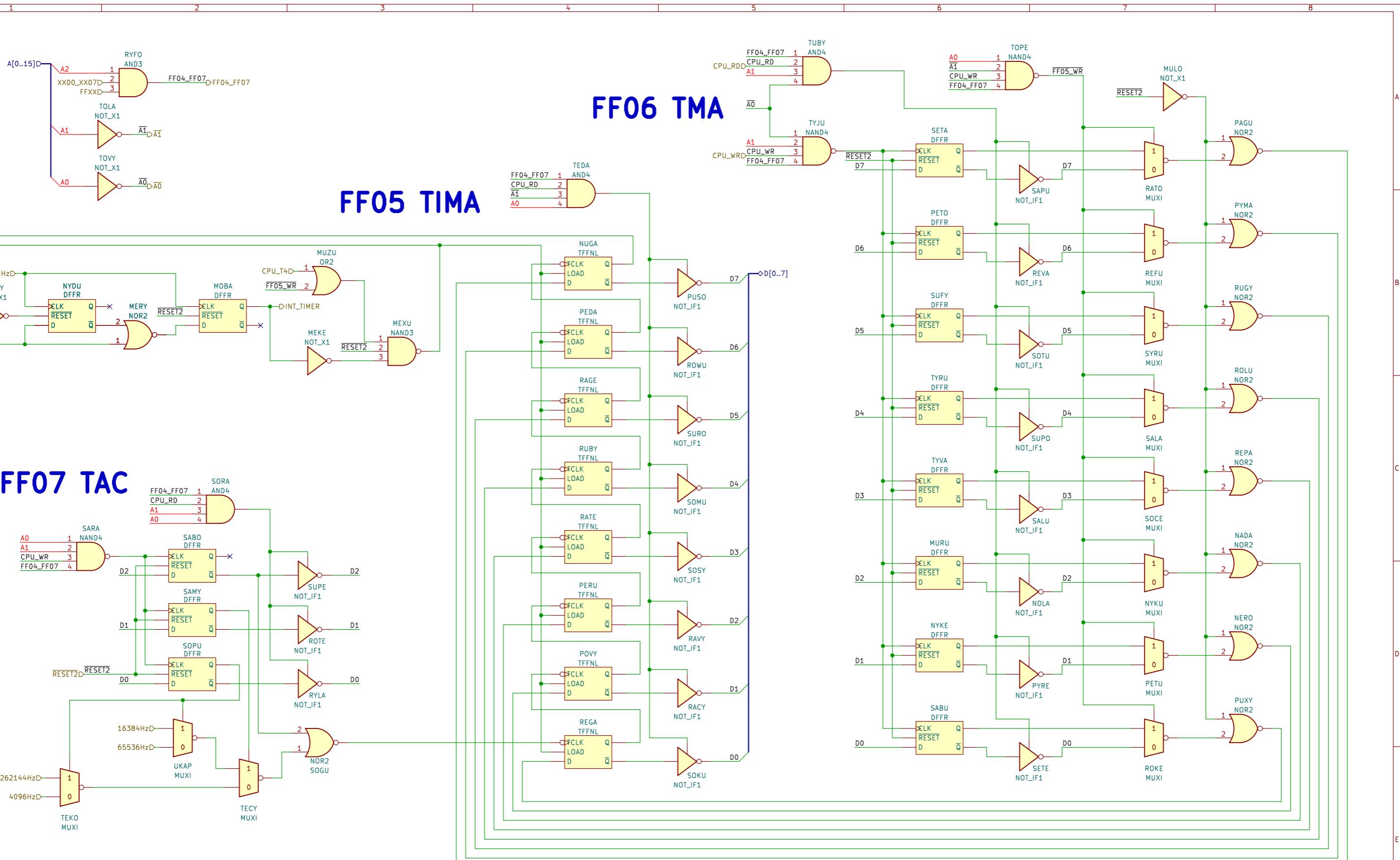
Title: DMG-CPU B

Size: A3 Date: 2025-04-12

KiCad E.D.A. 8.0.9

Rev: 0.7

Id: 8/46



<https://github.com/msinger/dmg-schematics>  
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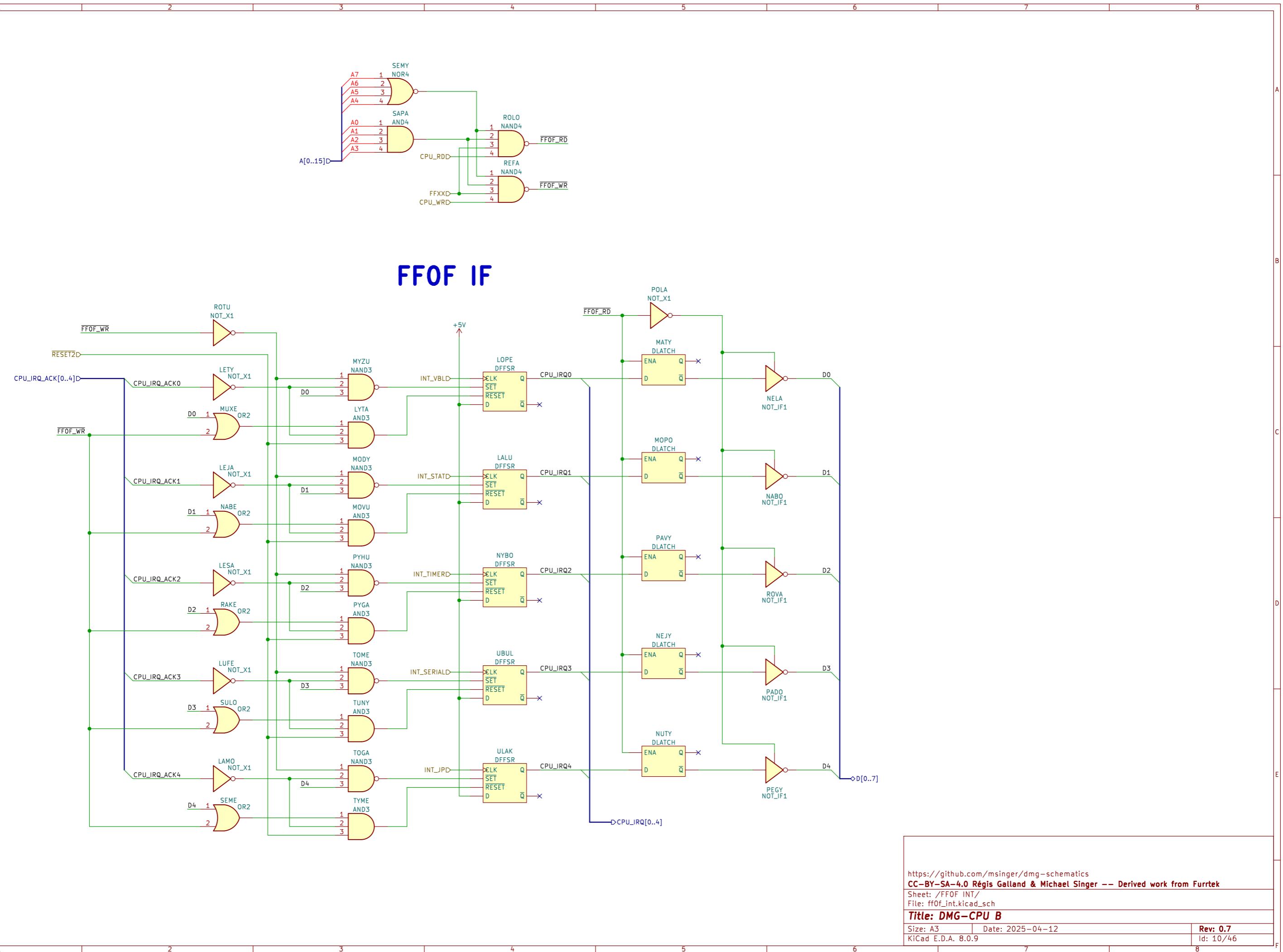
Sheet: /FF05-07 TIMER/  
 File: ff05-07\_timer.kicad\_sch

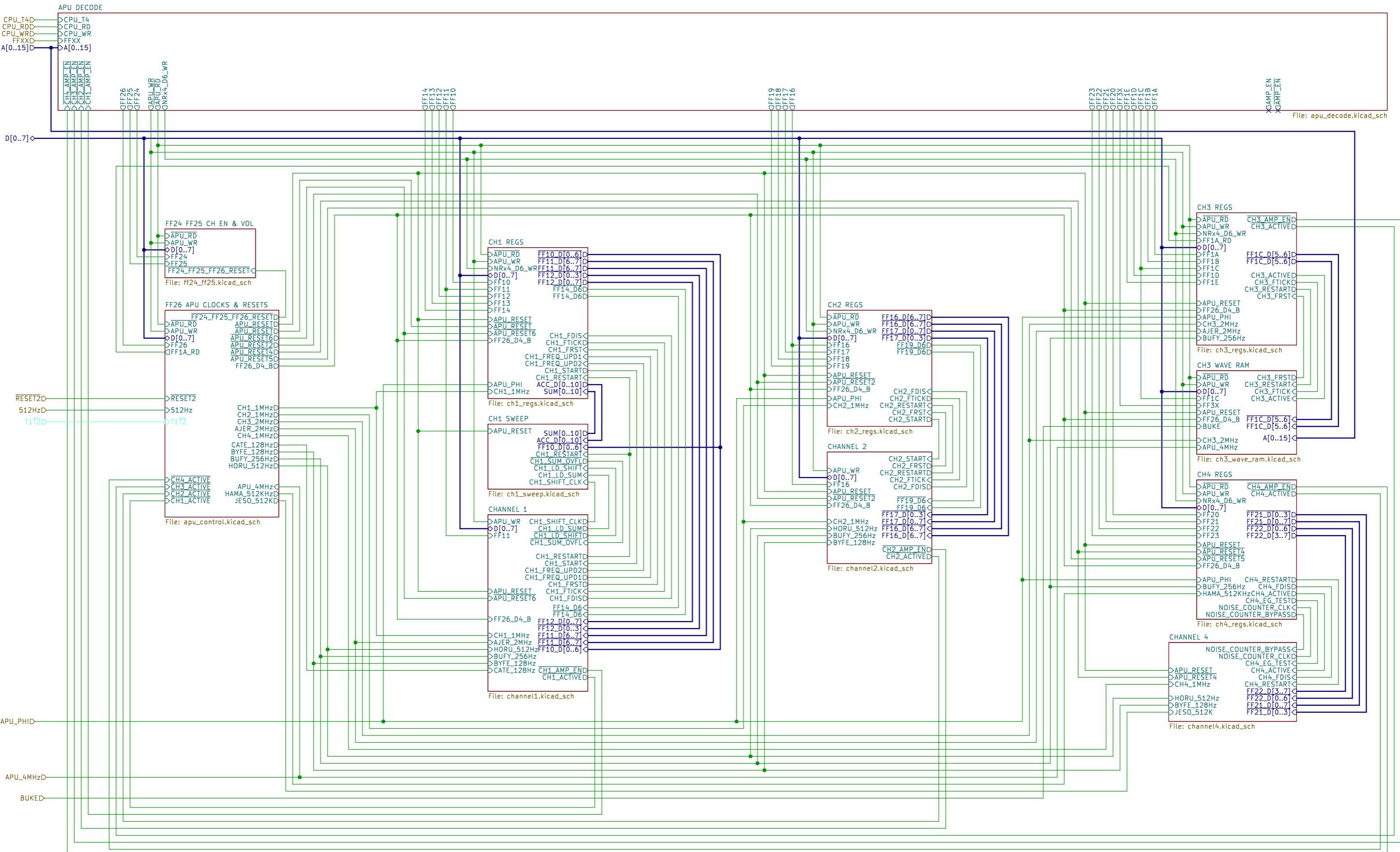
**Title: DMG-CPU B**

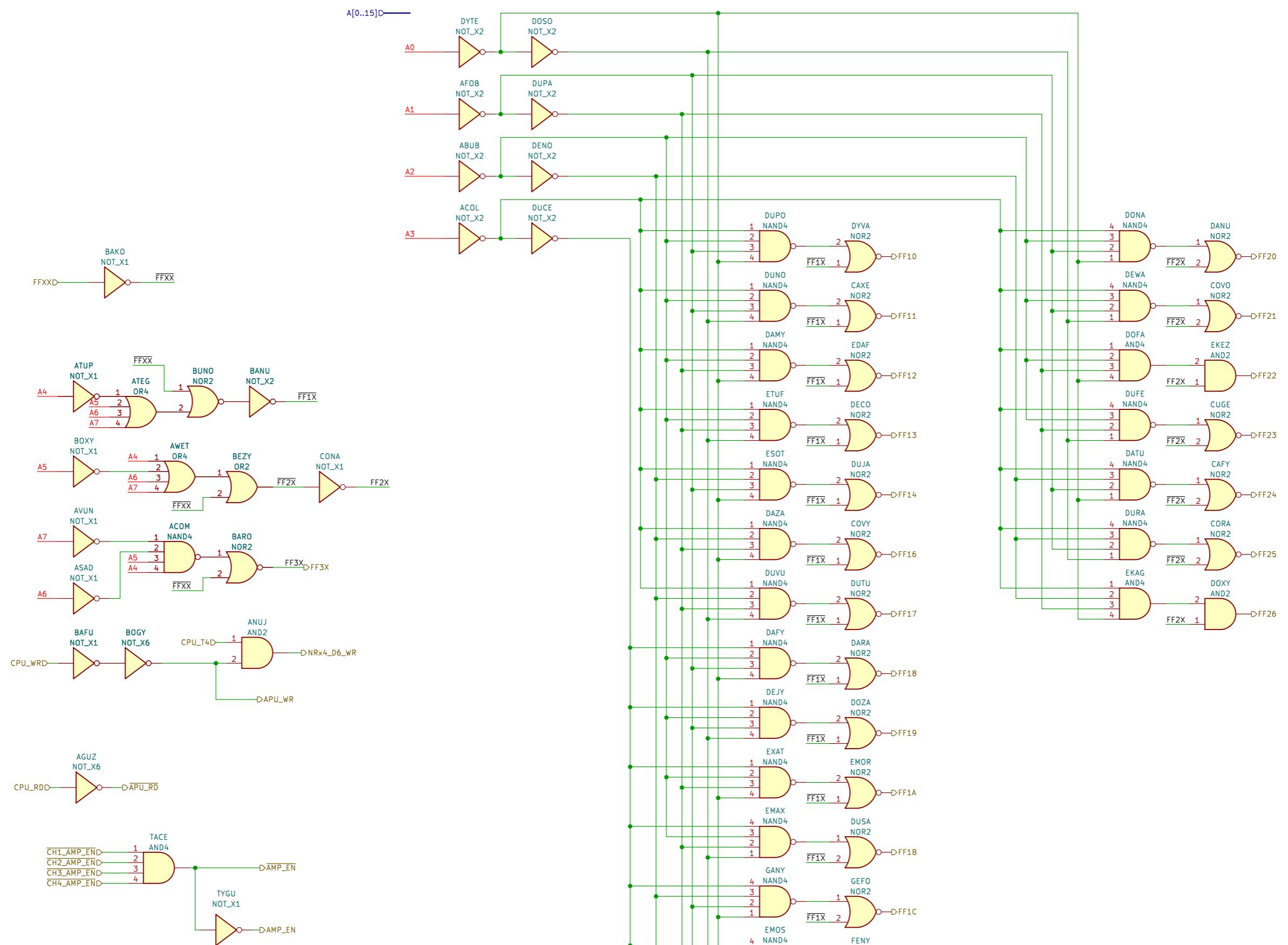
Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7

Id: 9/46







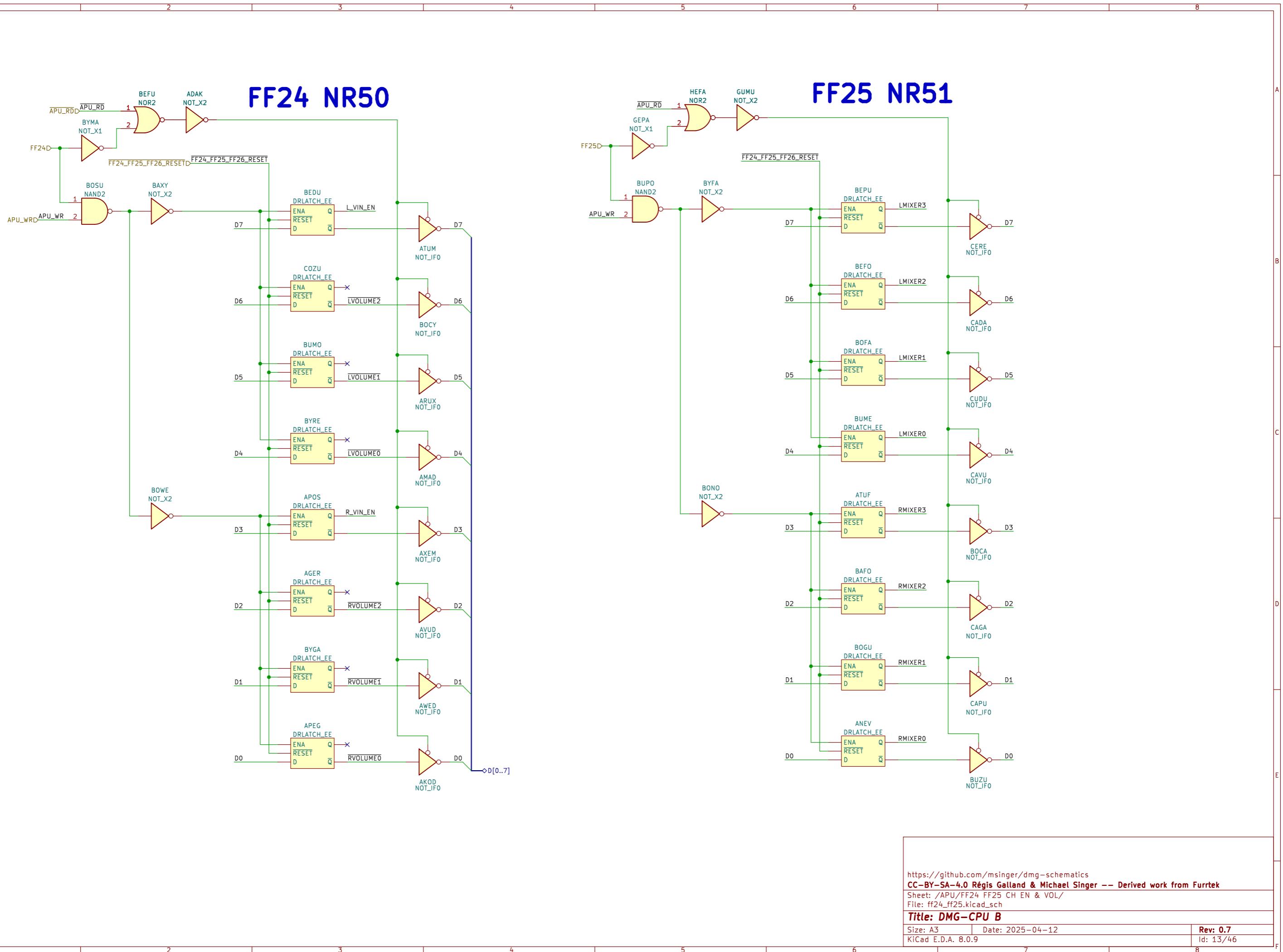
<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek

Sheet: /APU/APU\_DECODE/  
 File: apu\_decode.kicad\_sch

**Title: DMG-CPU B**

Size: A3 | Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7  
 Id: 12/46



<https://github.com/msinger/dmg-schematics>  
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Sheet: /APU/FF24\_FF25\_CH\_EN & VOL/  
 File: ff24\_ff25.kicad\_sch

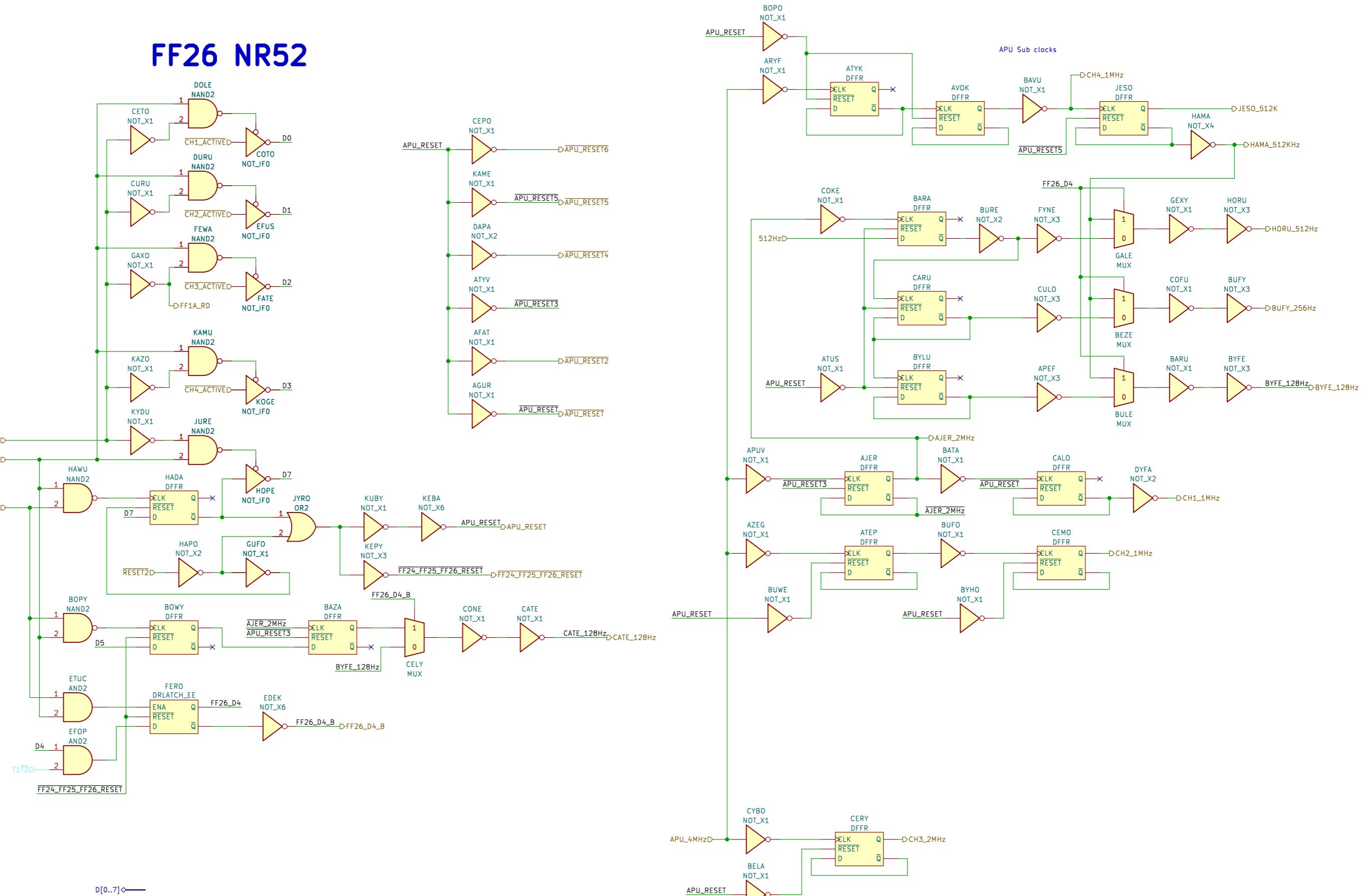
**Title: DMG-CPU B**

Size: A3 | Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7

Id: 13/46

# FF26 NR52



<https://github.com/msinger/dmg-schematics>  
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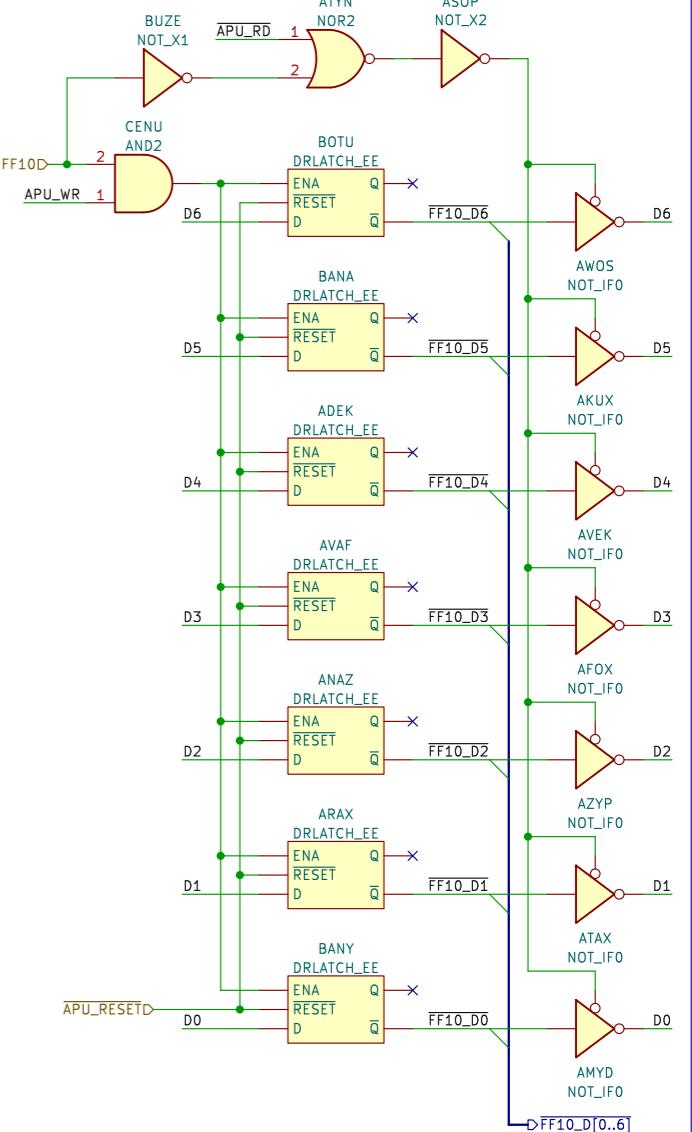
Sheet: /APU/FF26 APU CLOCKS & RESETS/  
File: apu\_control.kicad\_sch

**Title: DMG-CPU B**

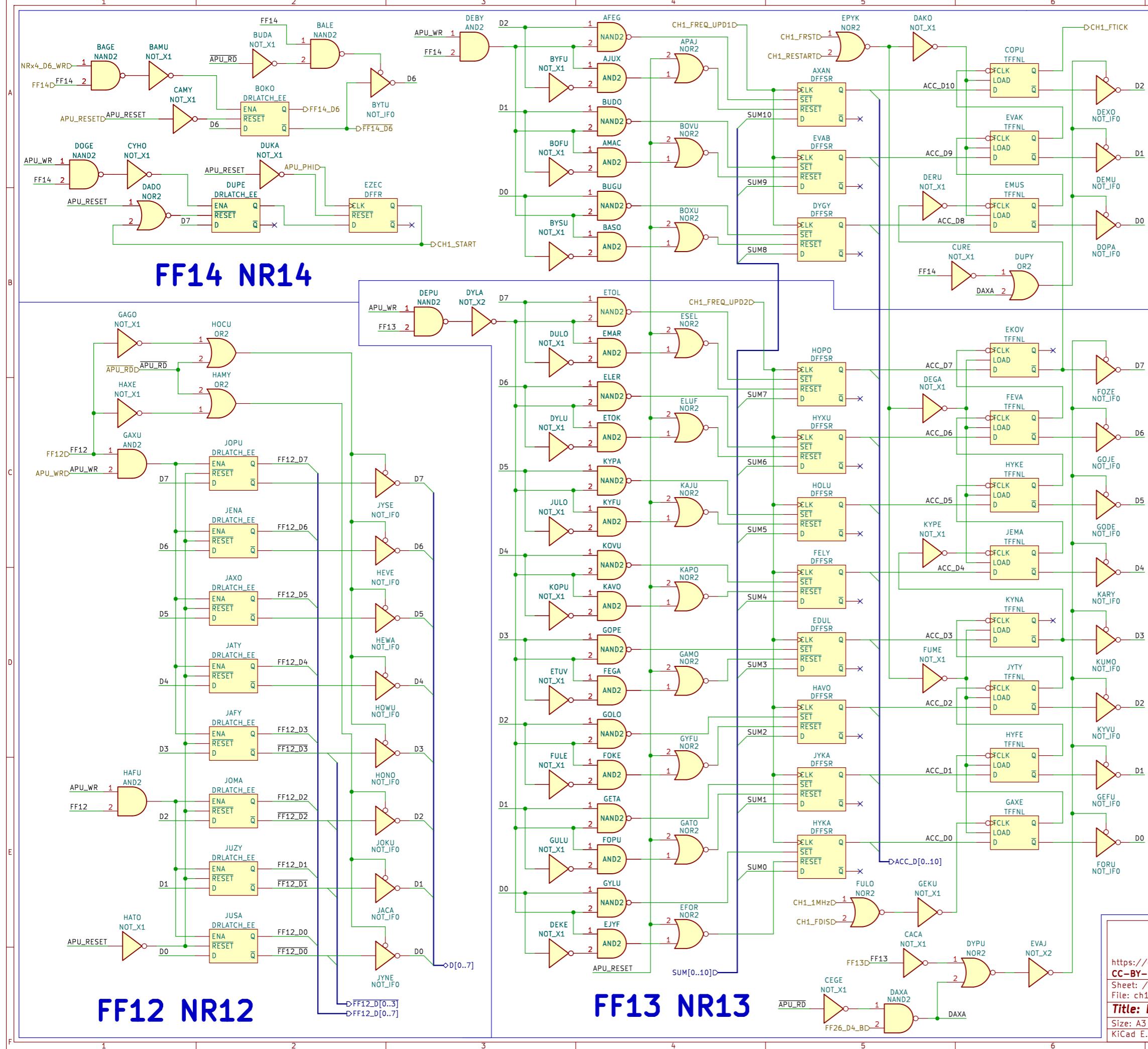
Size: A3 Date: 2025-04-12  
KiCad E.D.A. 8.0.9

Rev: 0.7  
Id: 14/46

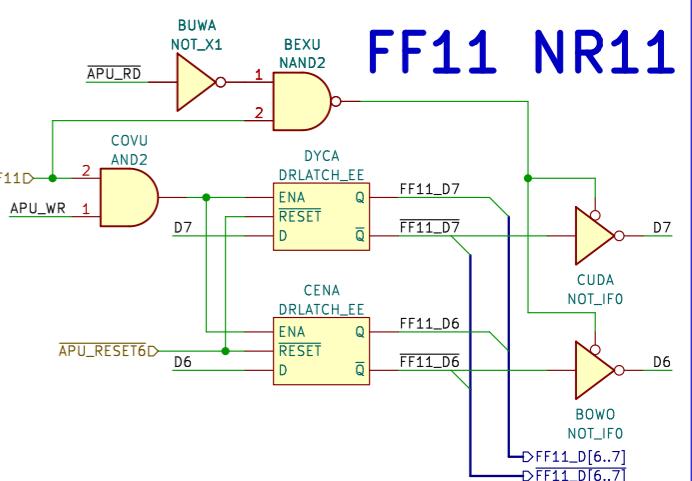
# FF10 NR10



# FF14 NR14

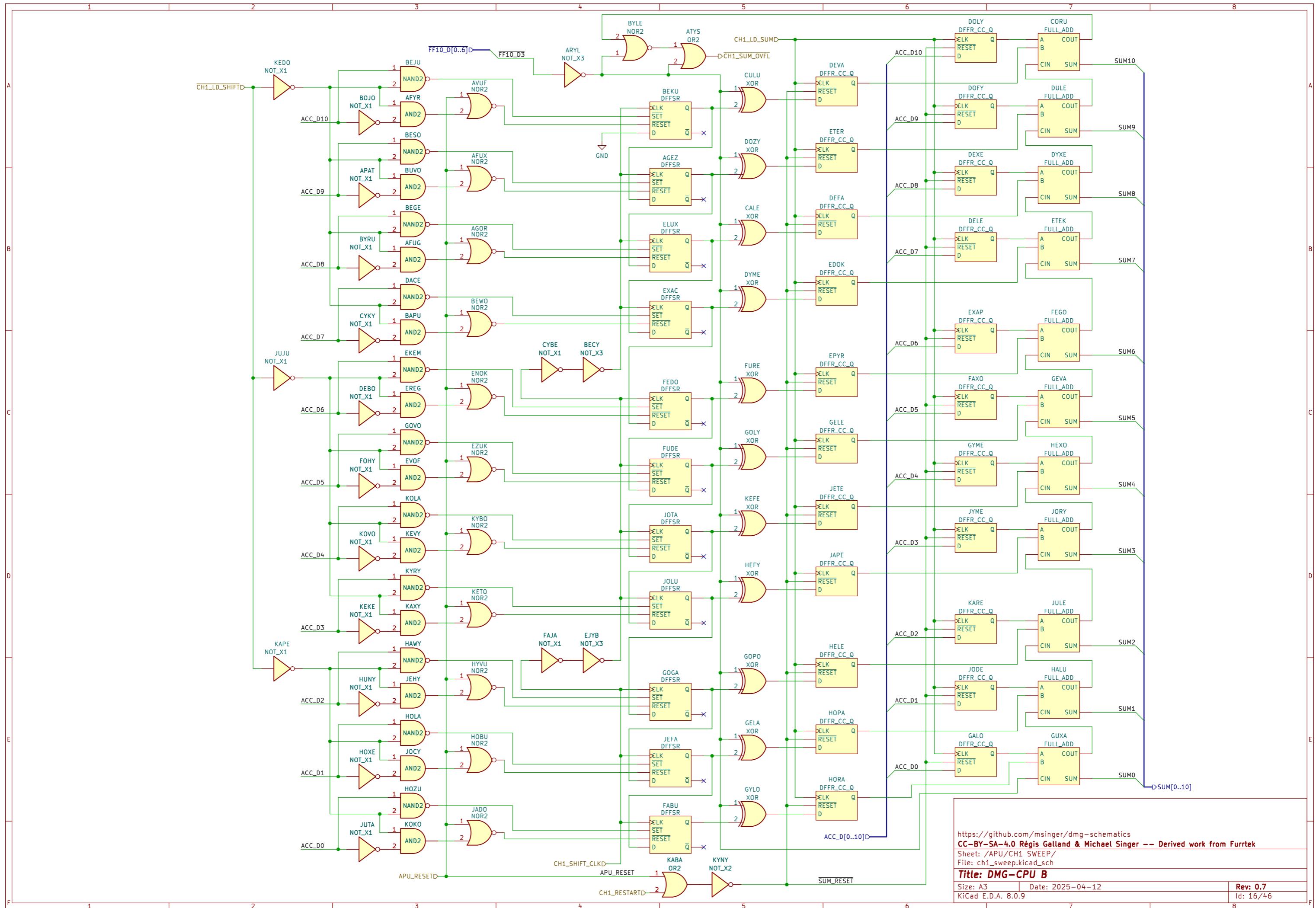


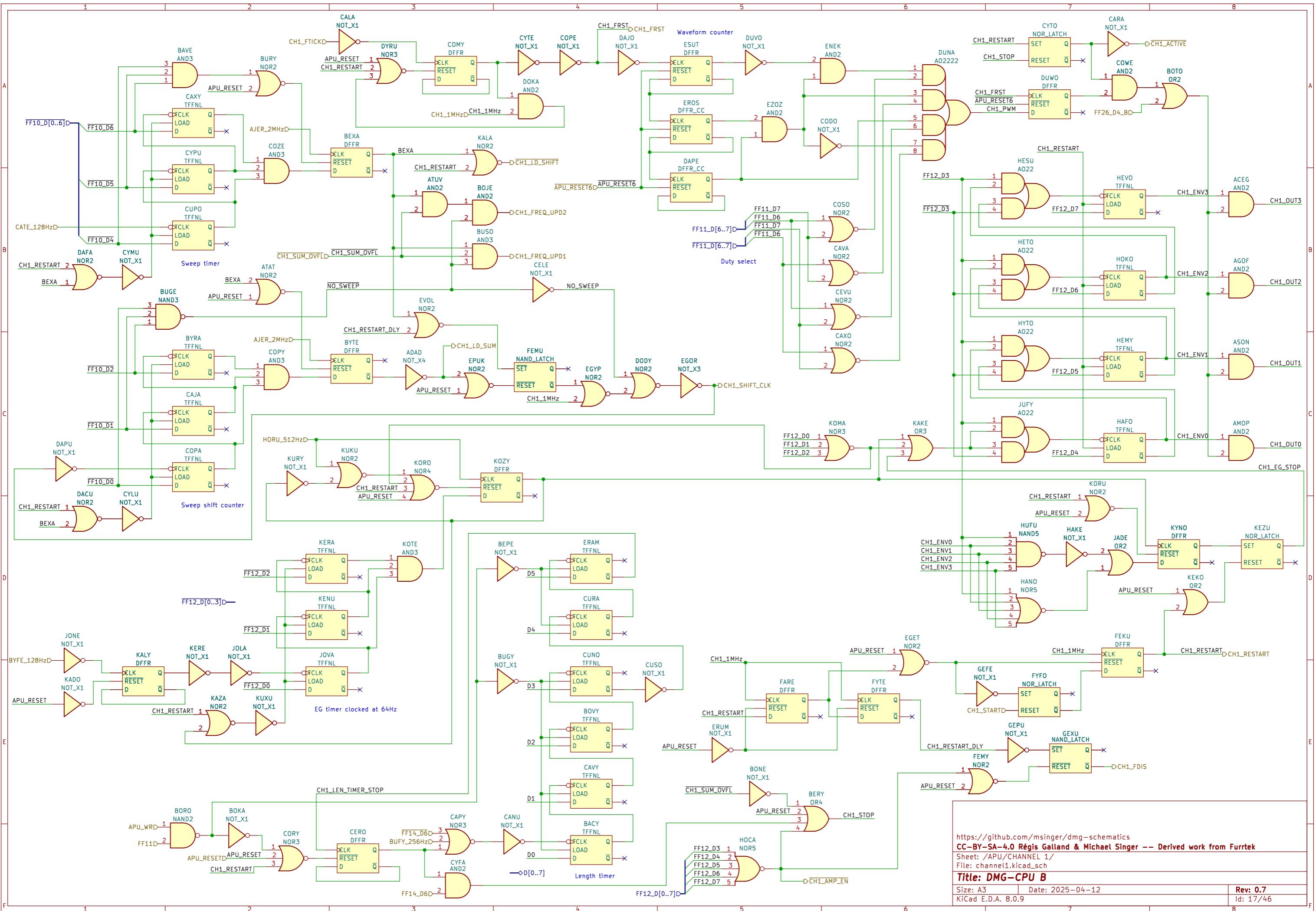
# FF12 NR12

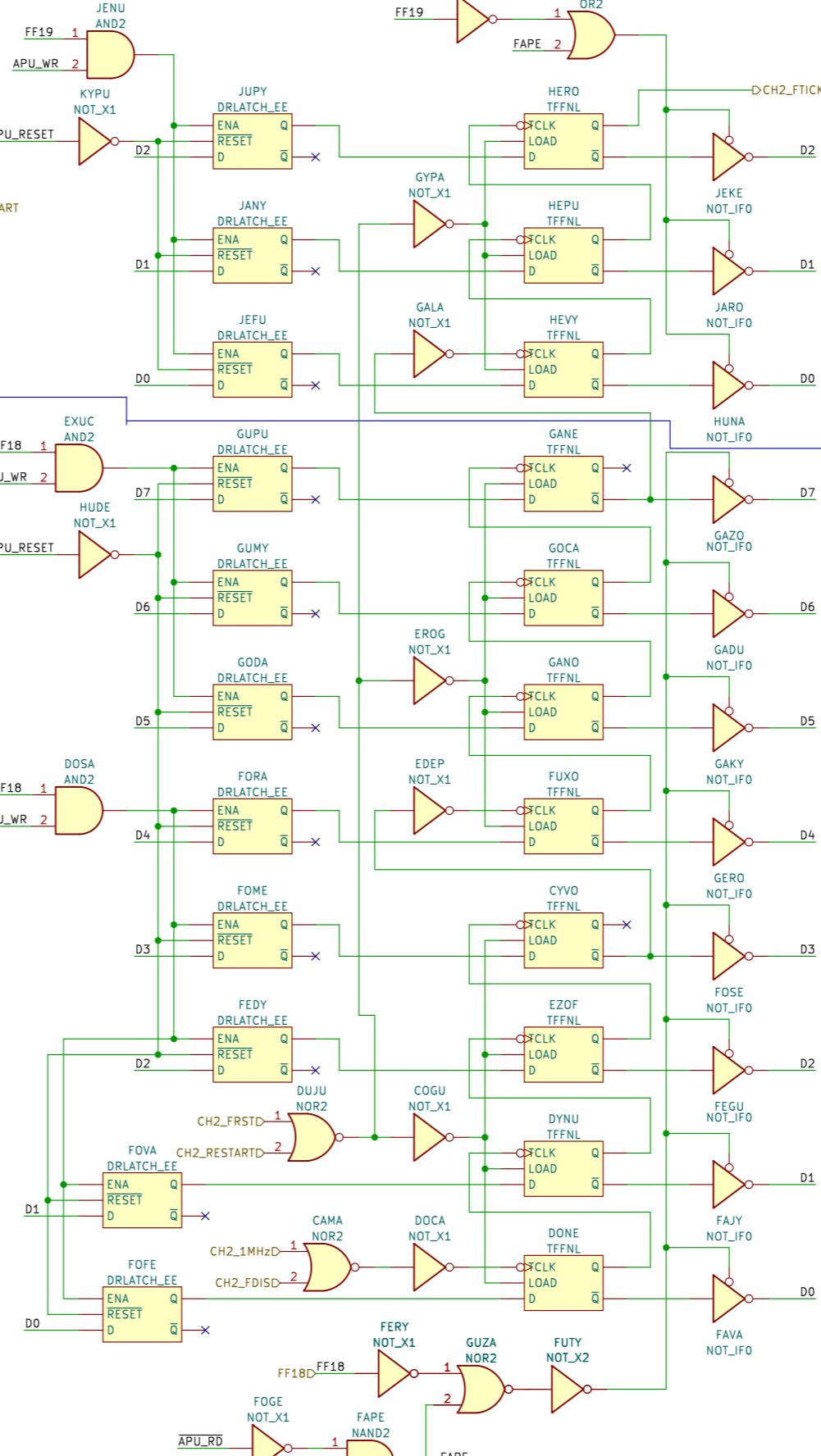
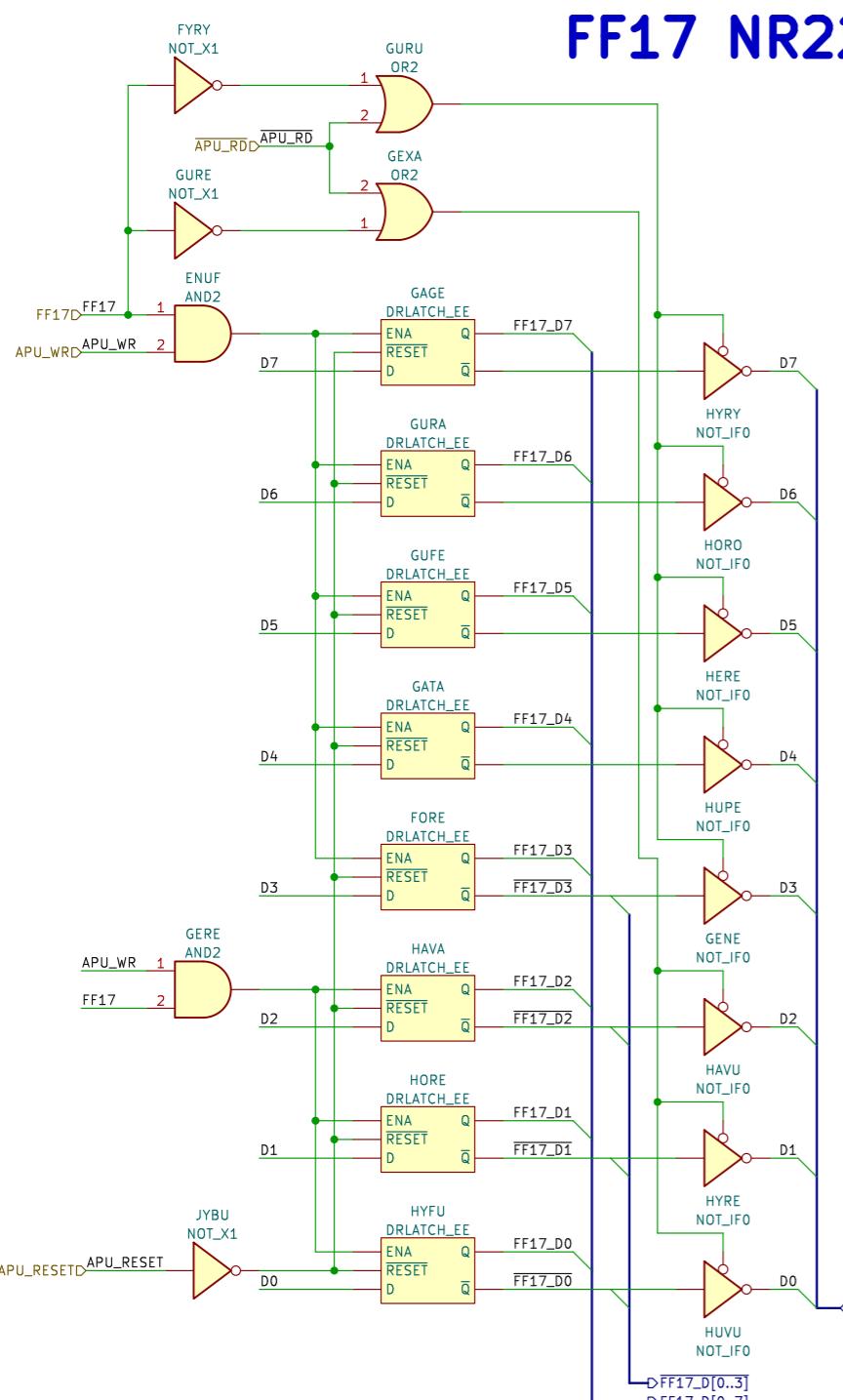
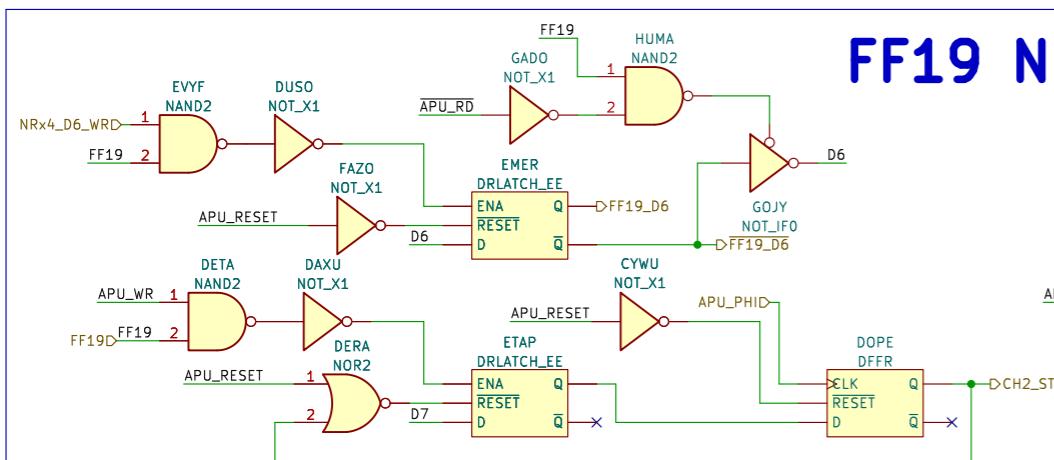


# FF13 NR13

<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek  
 Sheet: /APU/CH1\_REGS/  
 File: ch1\_regs.kicad\_sch  
**Title: DMG-CPU B**  
 Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9 Rev: 0.7  
 Id: 15/46







<https://github.com/msinger/dmg-schematics>  
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Sheet: / At 0/ ch2\_REGS/  
File: ch2\_regs.kicad\_sch

## Title: DMG-CPU B

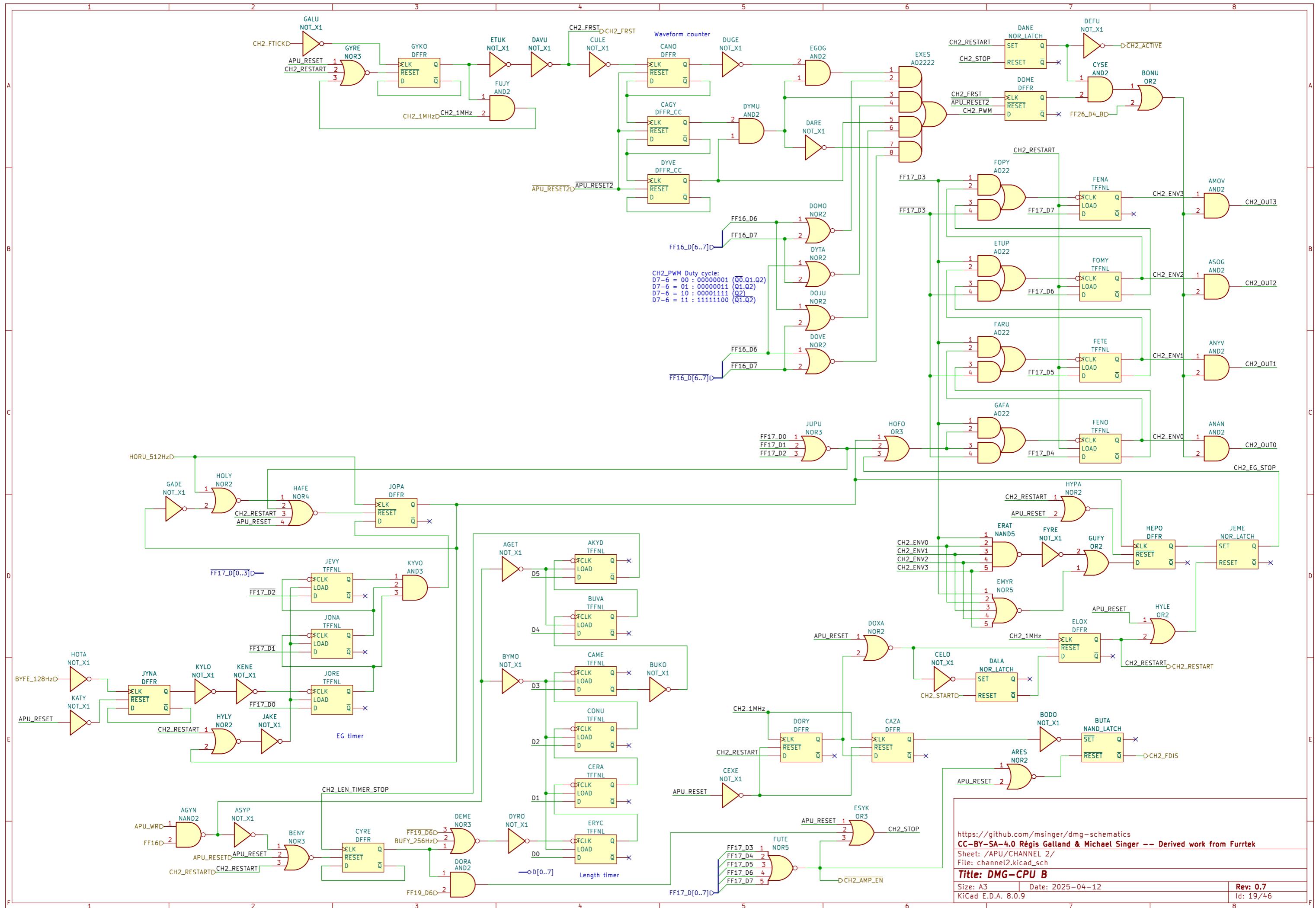
Size: A3 Date: 2023-06-06

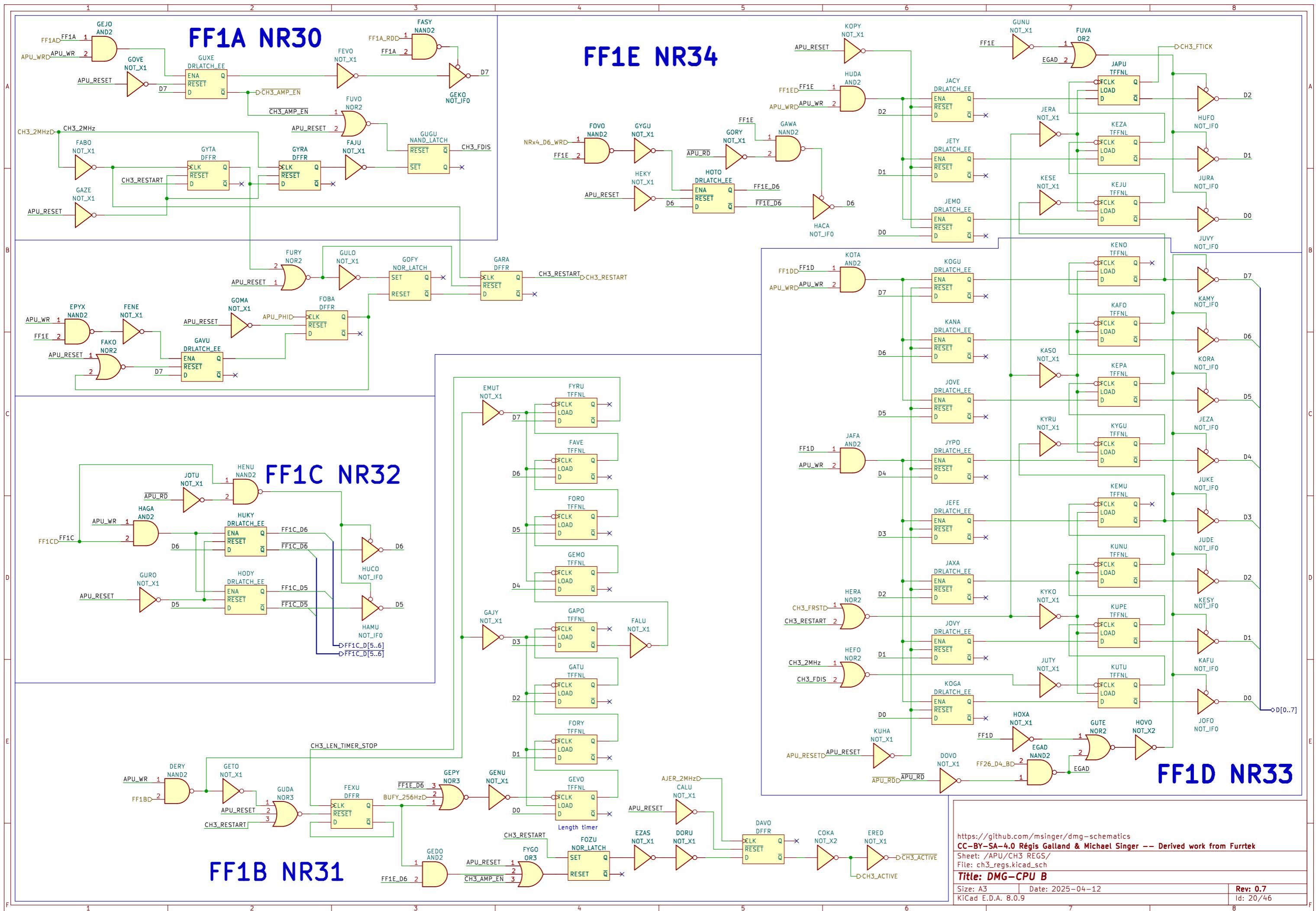
KiCad E.D.A. 8.0.9

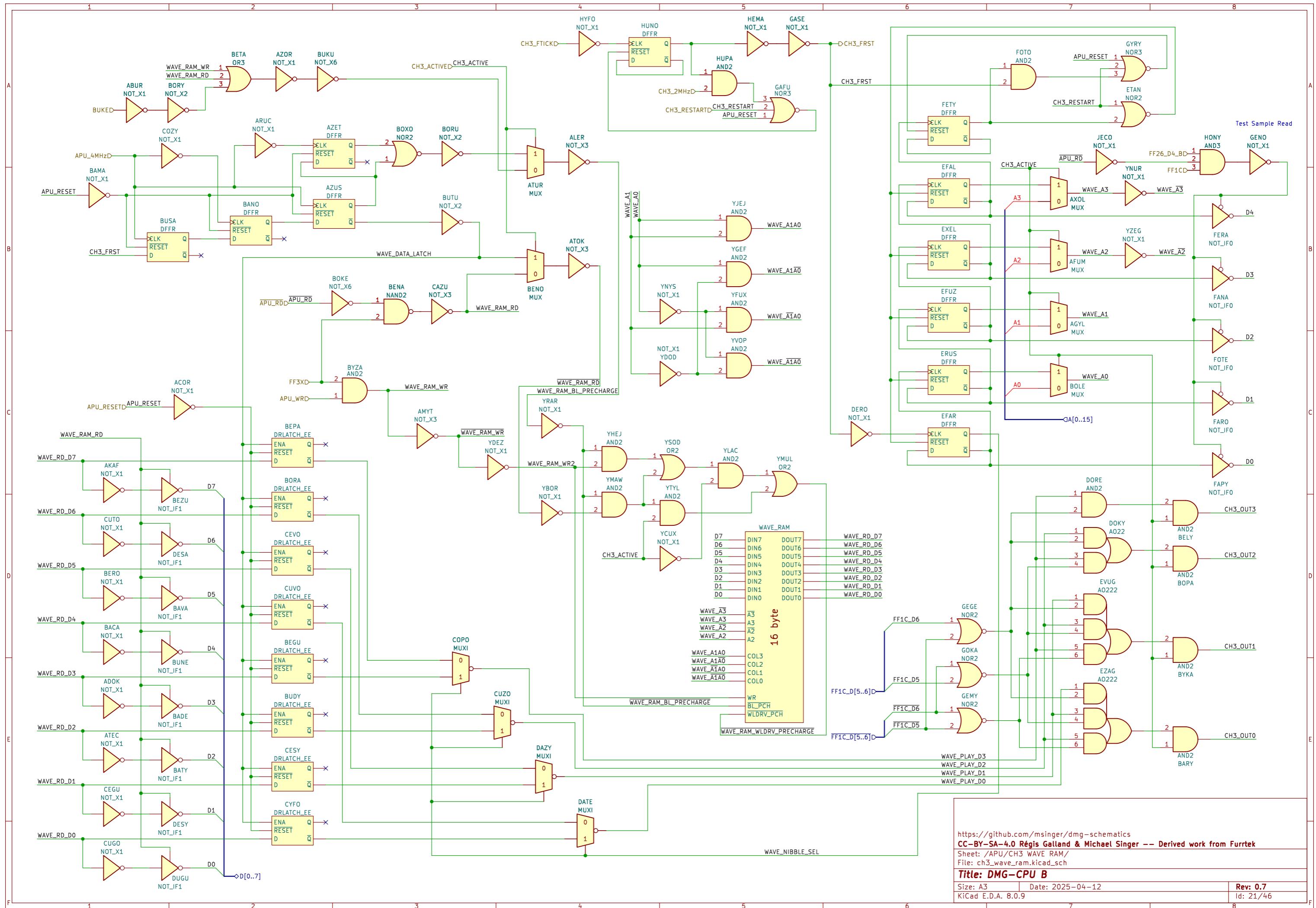
\_\_\_\_\_ | \_\_\_\_\_

Id: 18/4

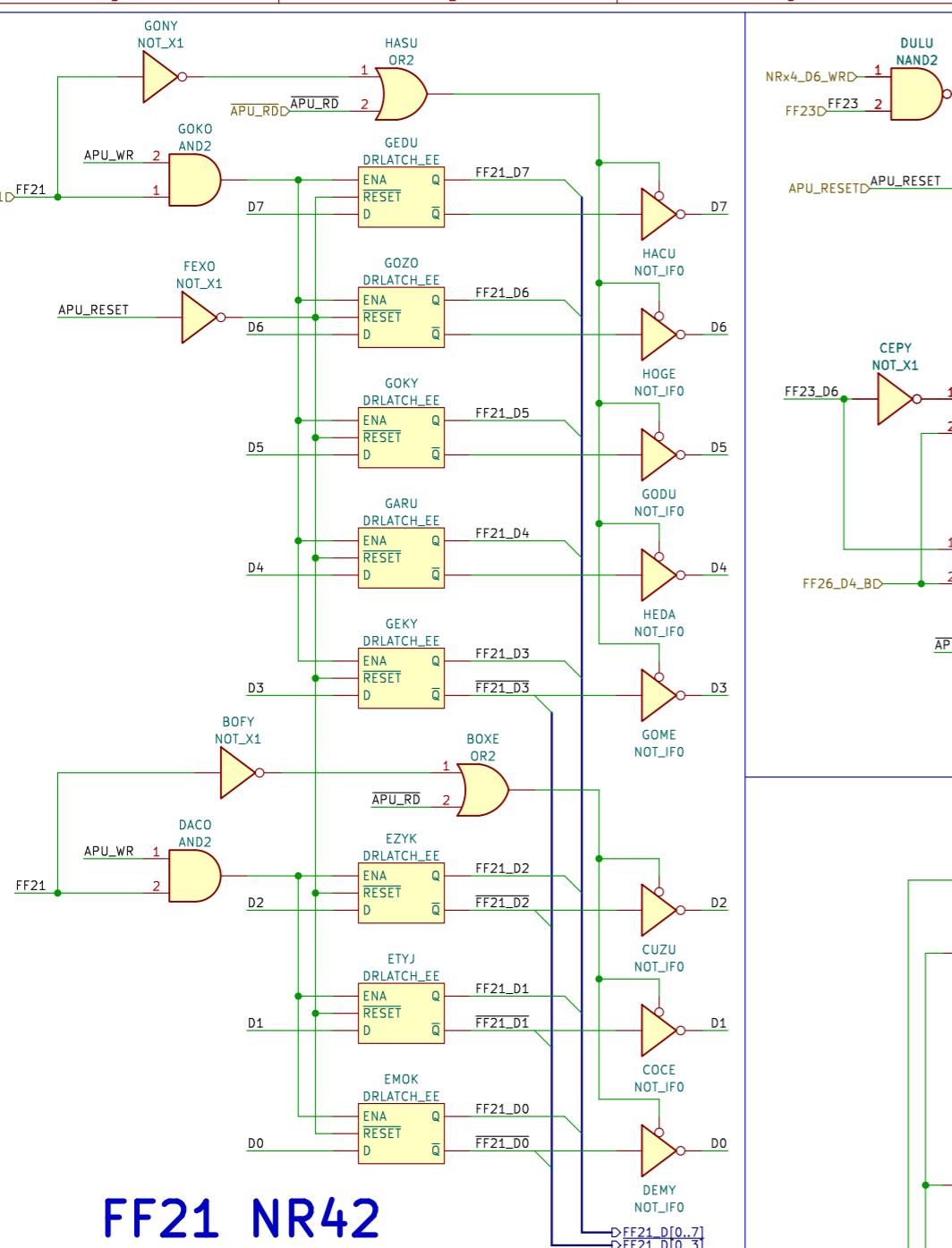
3



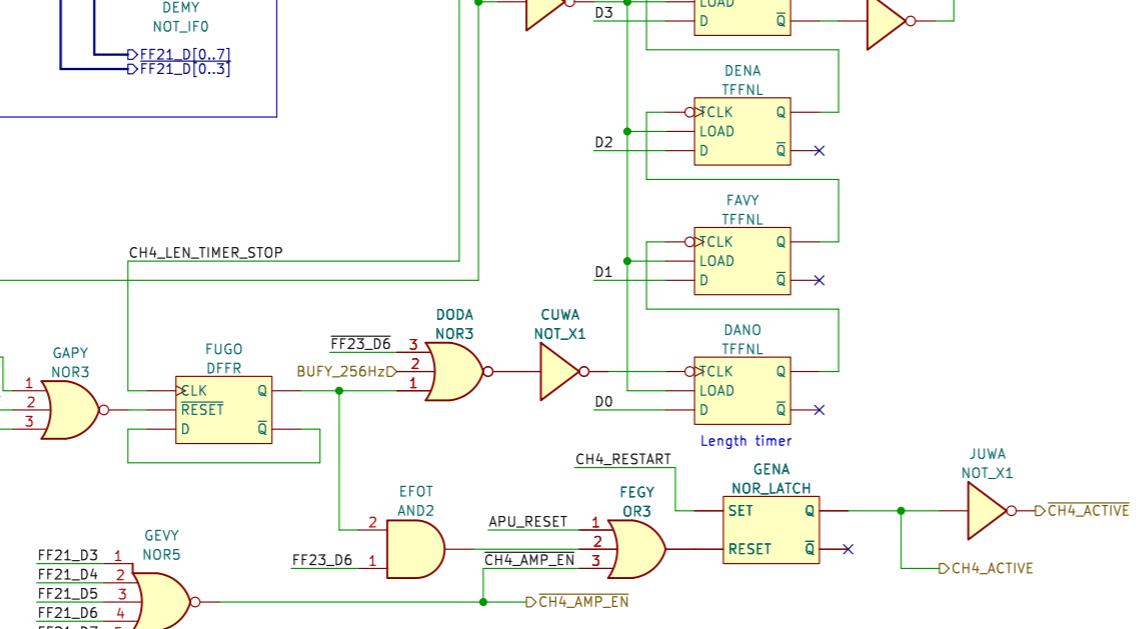




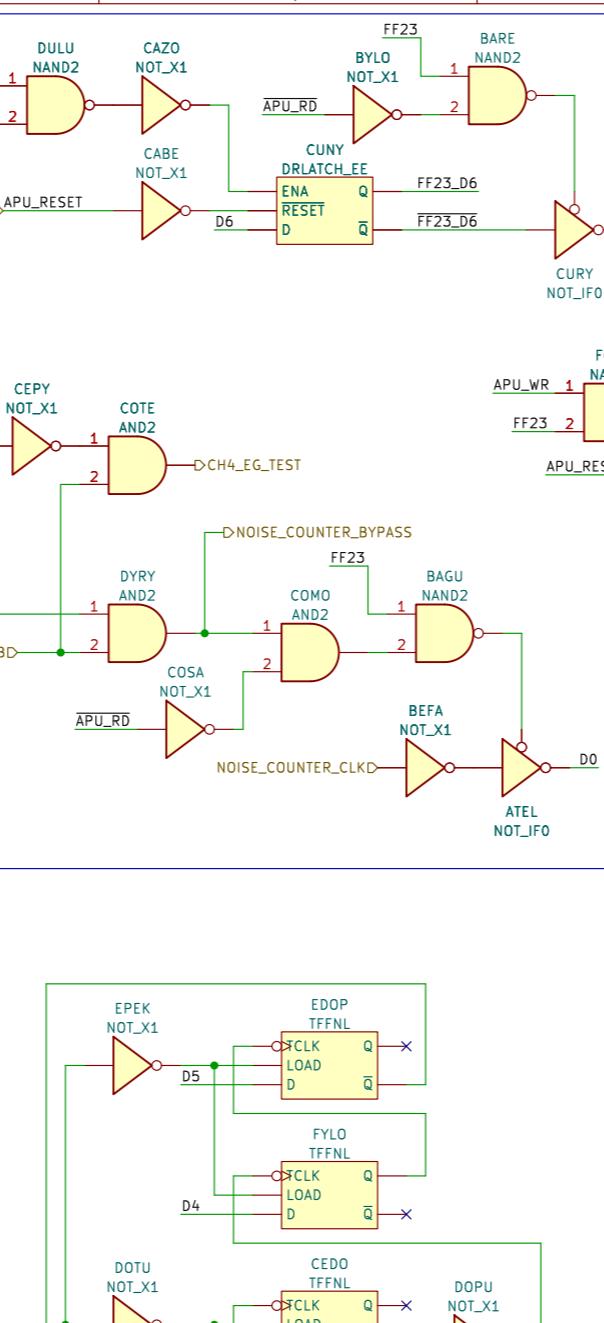
## FF21 NR42



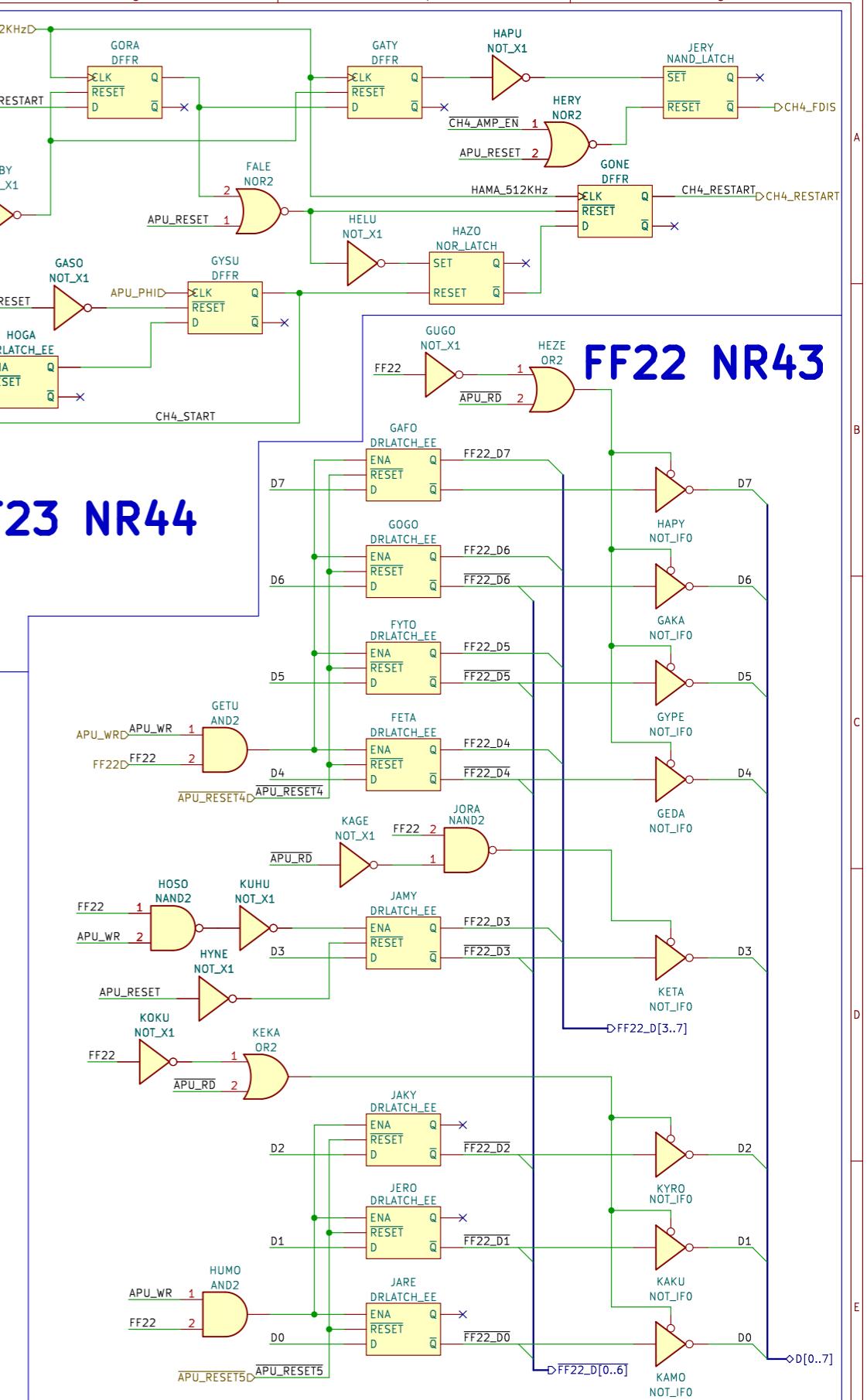
## FF20 NR41



## FF23 NR44



## FF22 NR43



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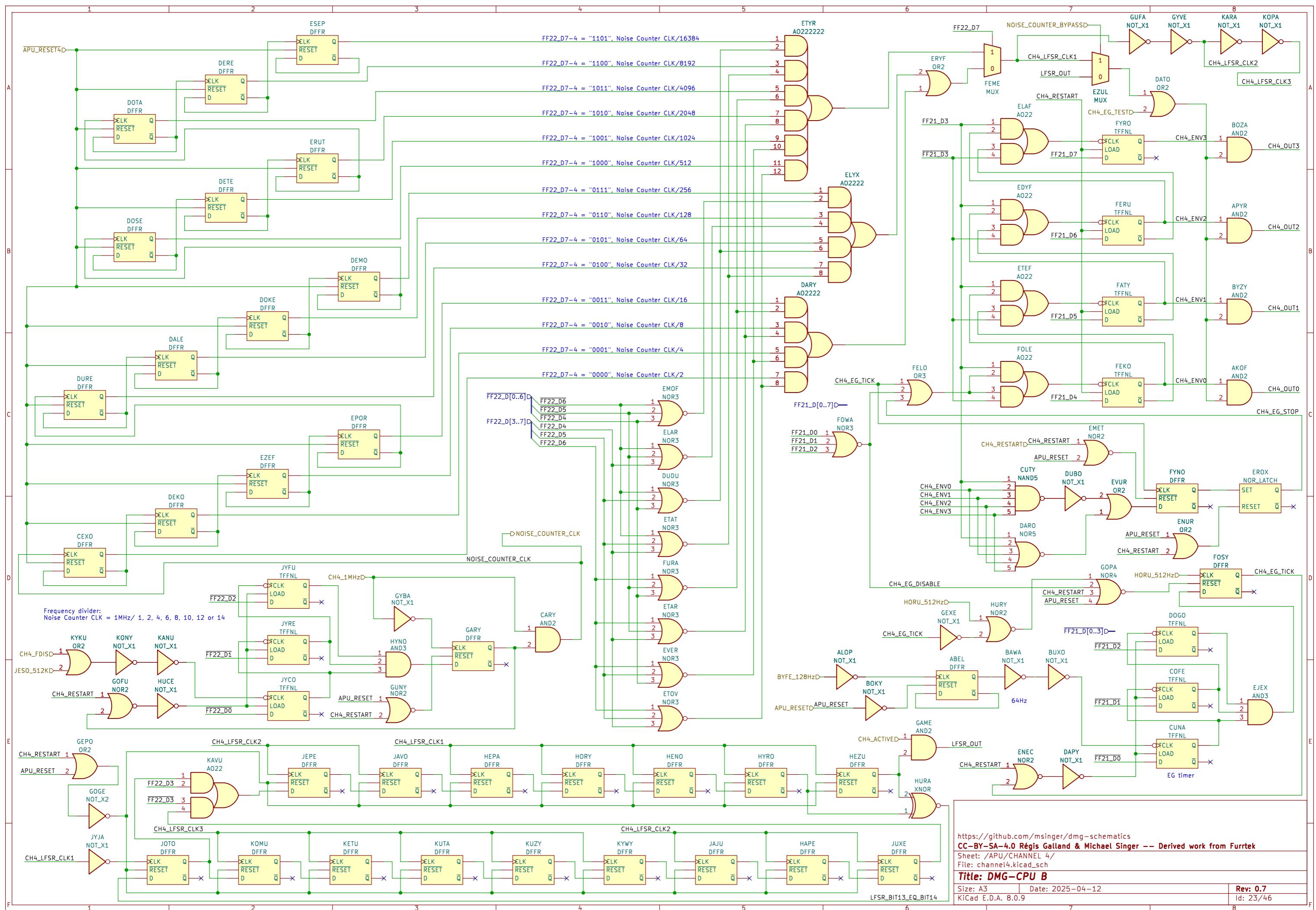
Sheet: /APU/CH4\_REGS/  
 File: ch4\_regs.kicad\_sch

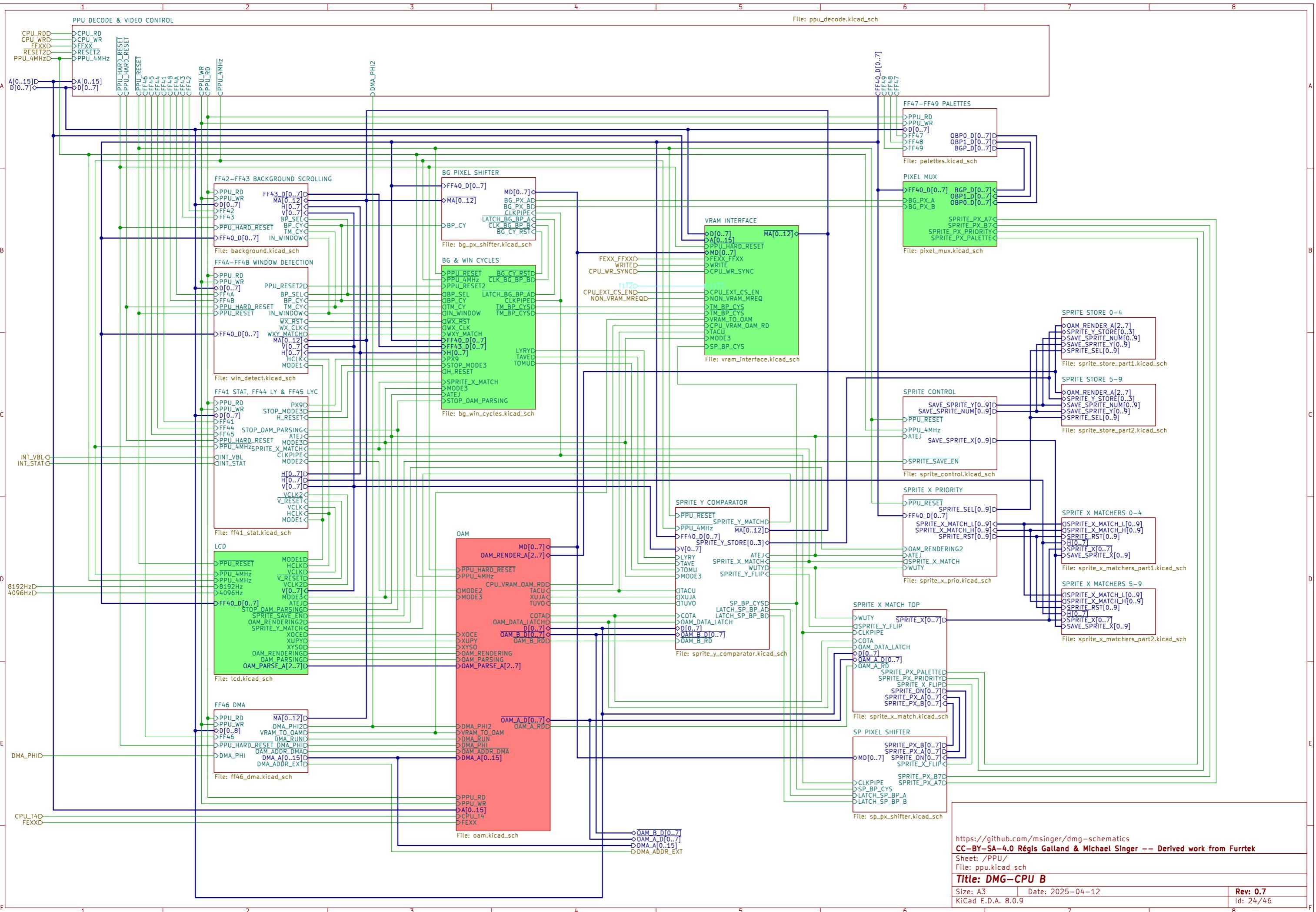
Title: DMG-CPU B

Size: A3 Date: 2025-04-12

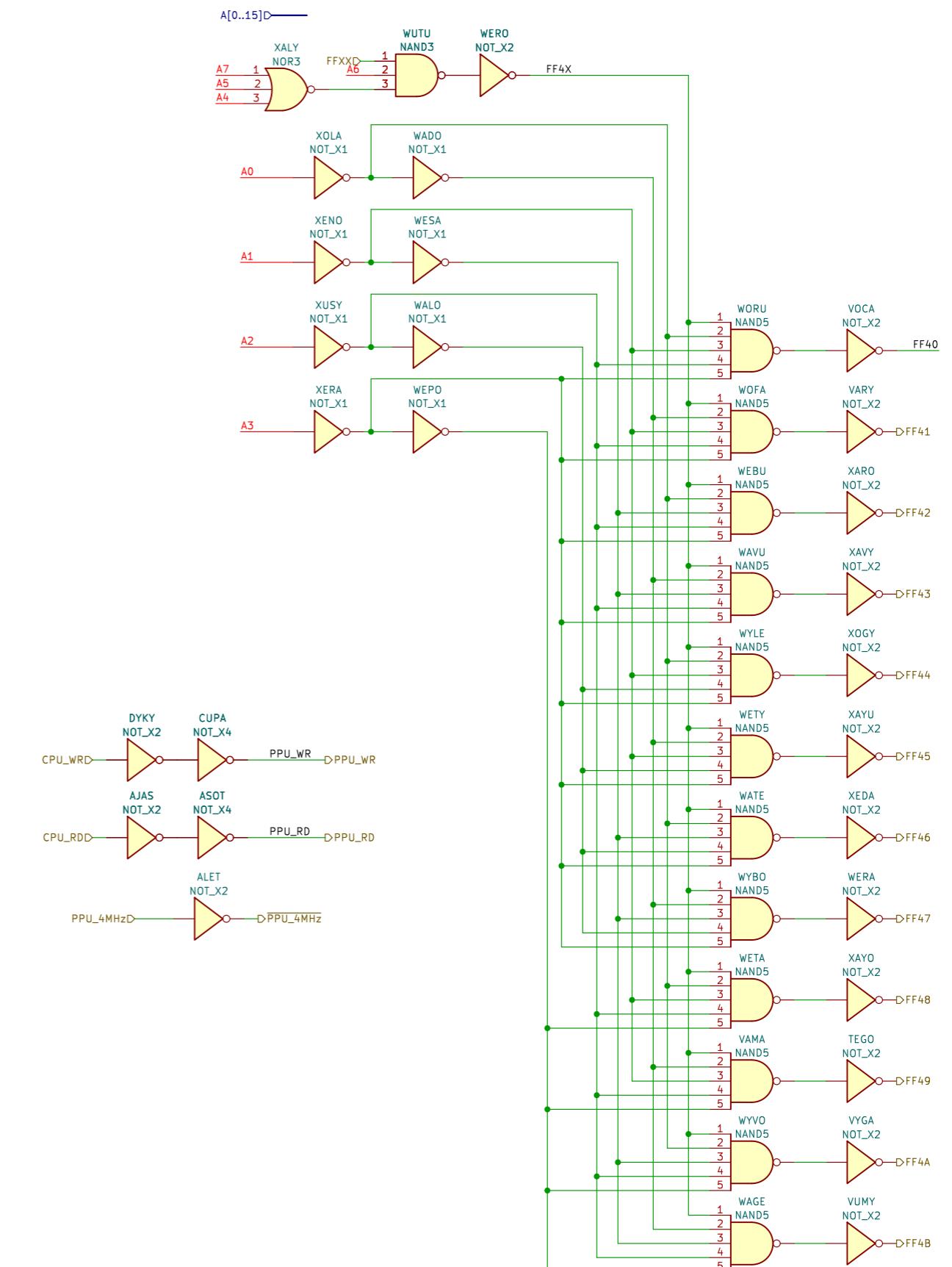
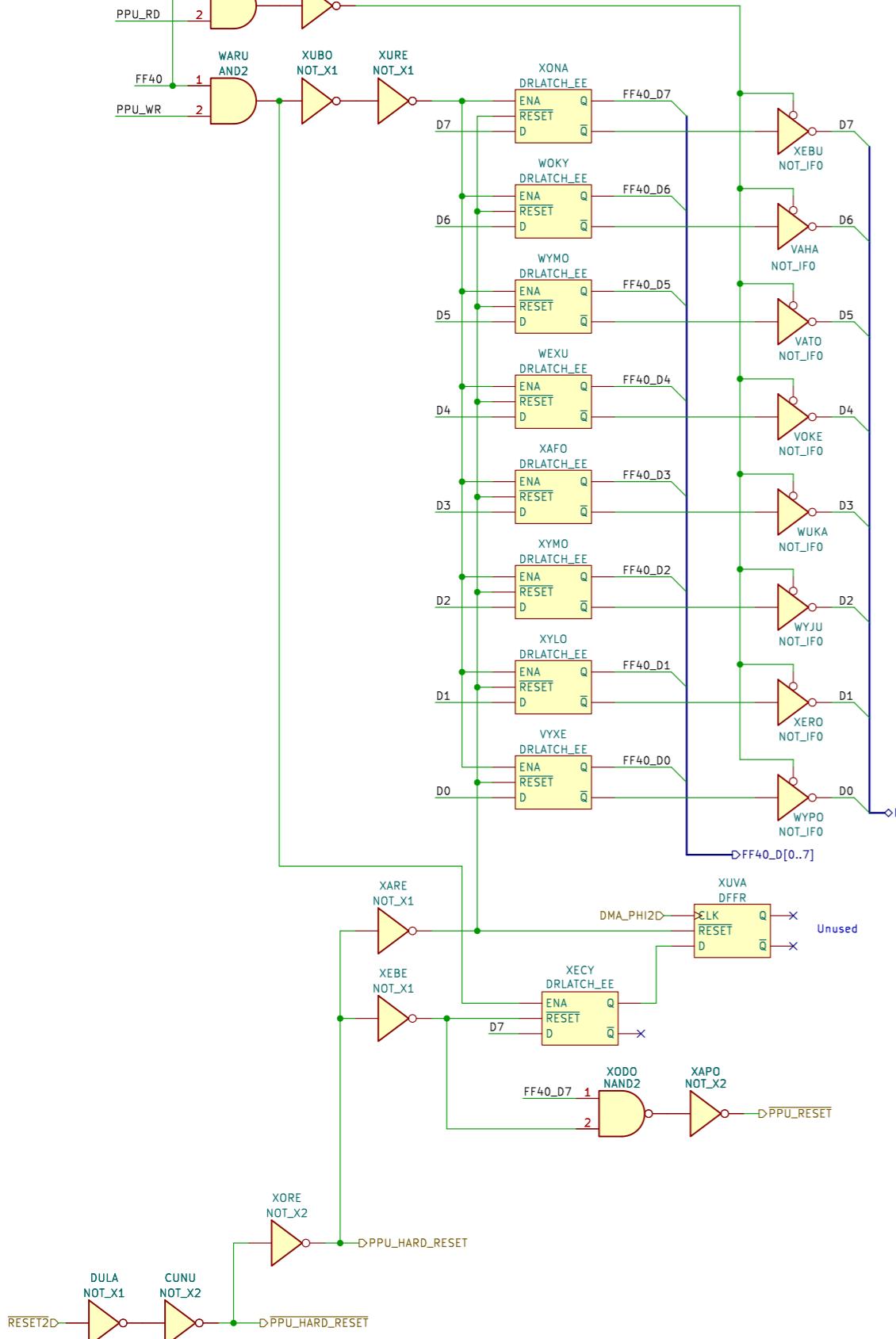
KiCad E.D.A. 8.0.9 Rev: 0.7

Id: 22/46





# FF40 LCDC



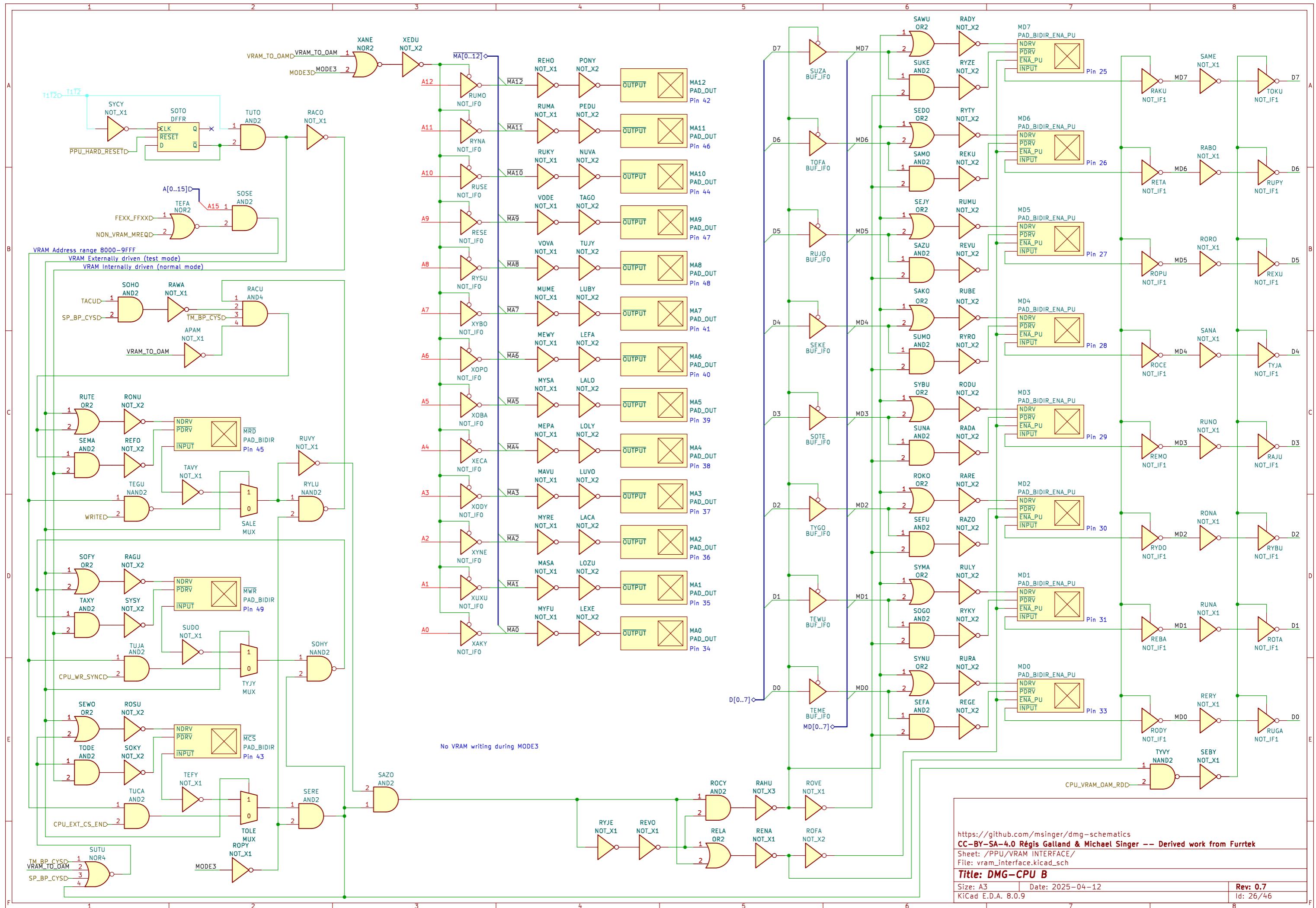
<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek

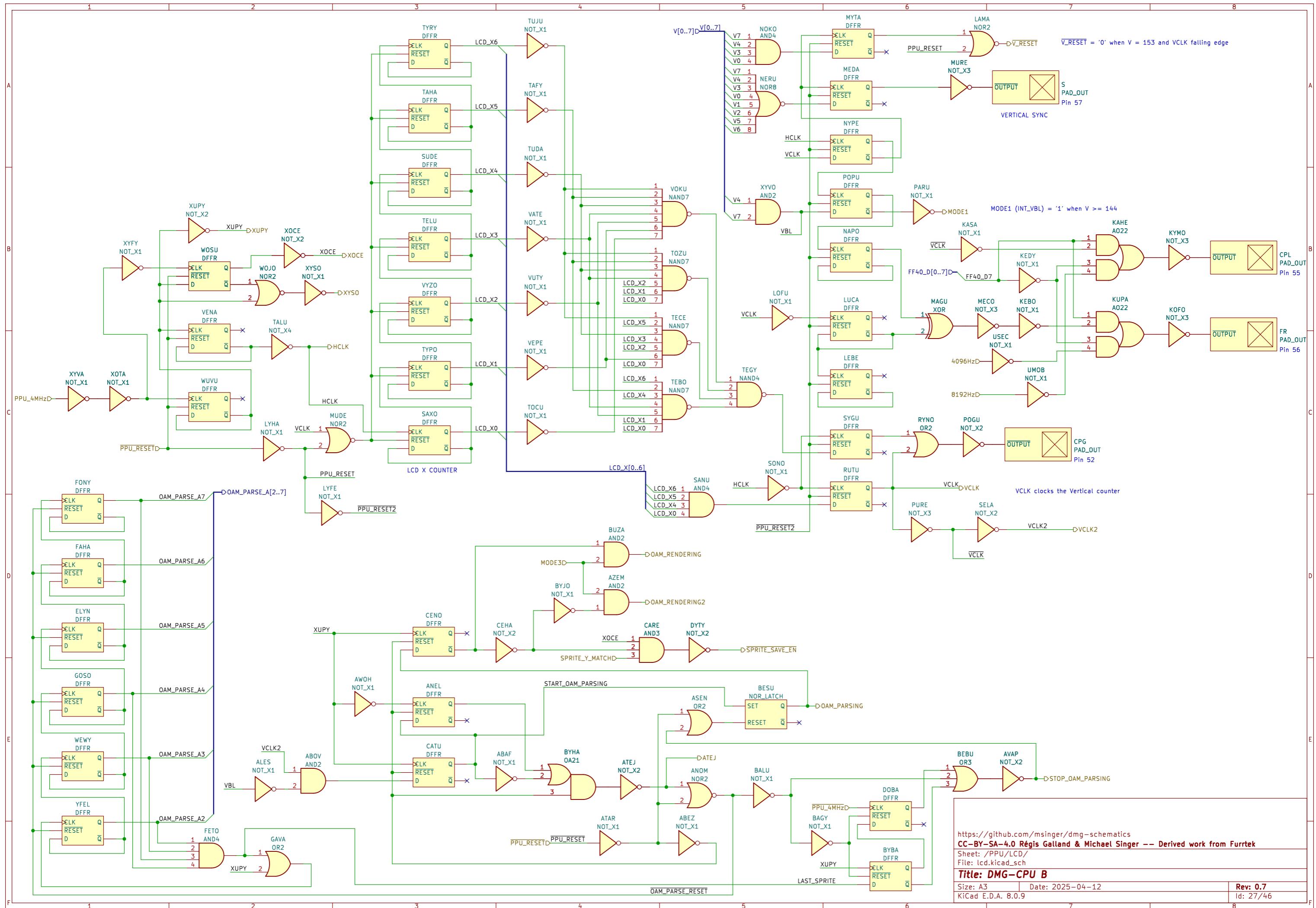
Sheet: /PPU/PPU DECODE & VIDEO CONTROL/  
 File: ppu\_decode.kicad\_sch

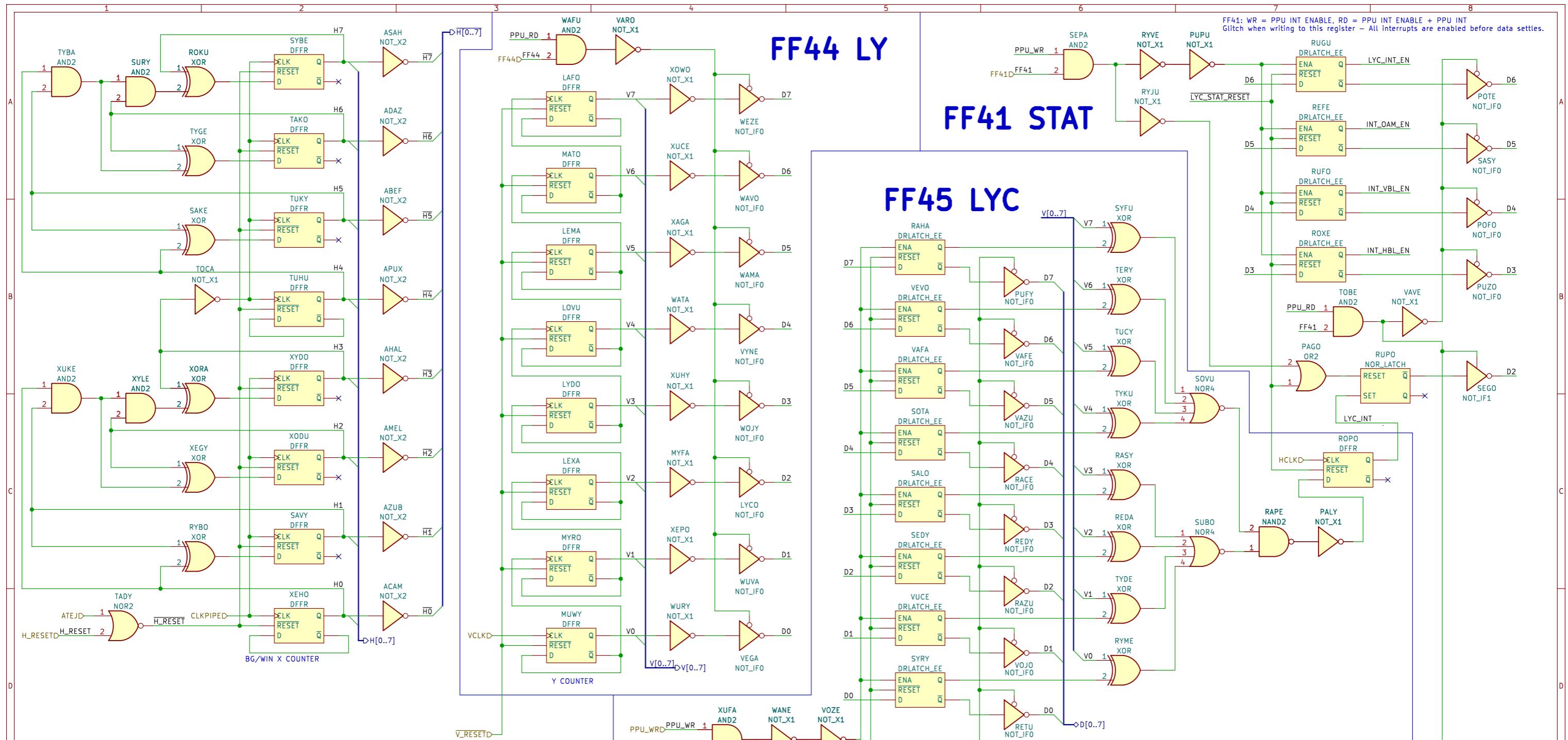
Title: DMG-CPU B

Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

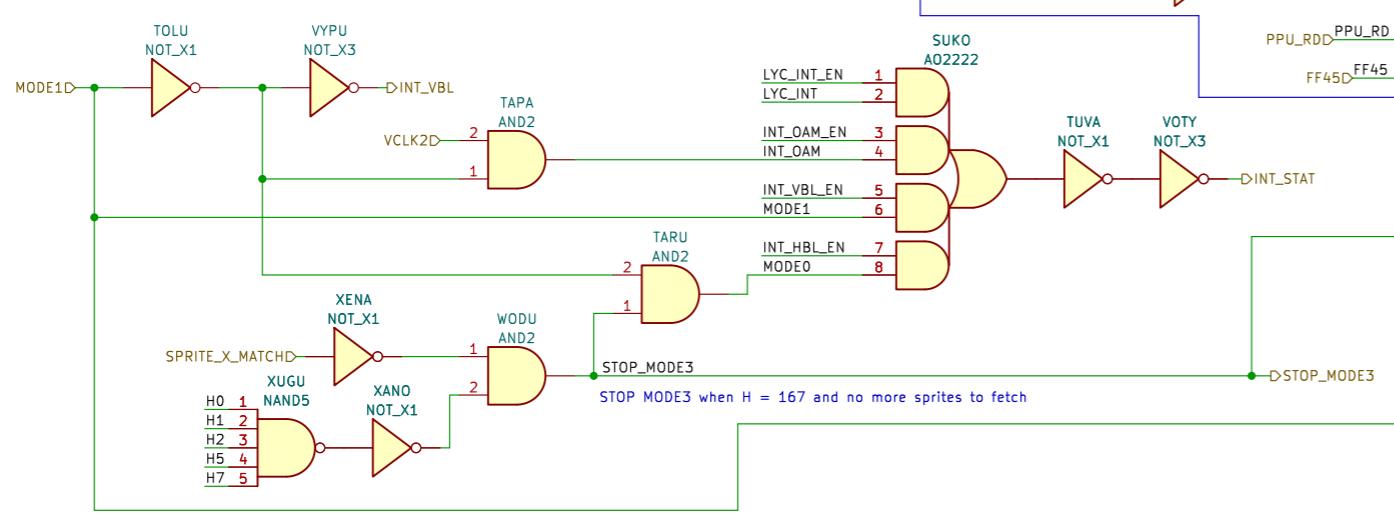
Rev: 0.7  
 Id: 25/46







When all interrupts are enabled,  
INT\_STAT = '1' when LY = LYC (whole line), VBLANK (MODE1), HBLANK (MODE0),  
and Only for a few cycles at the start of OAM parsing when VCLK is high.



**FF44 LY**

**FF41 STAT**

**FF45 LYC**

FF41: WR = PPU INT ENABLE, RD = PPU INT ENABLE + PPU INT  
Glitch when writing to this register – All interrupts are enabled before data settles.

<https://github.com/msinger/dmg-schematics>  
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Sheet: /PPU/FF41\_STAT, FF44 LY & FF45 LYC/  
File: ff41\_stat.kicad\_sch

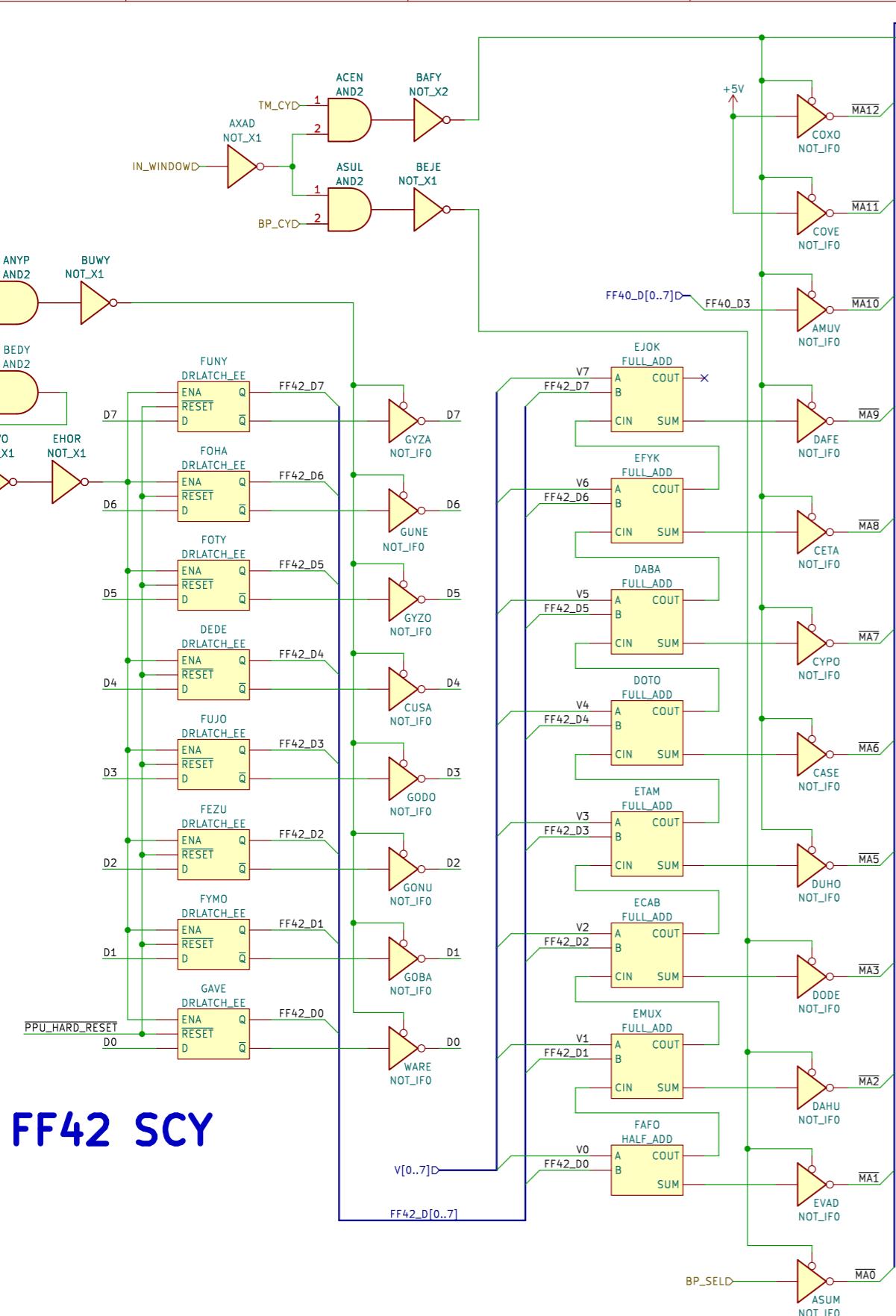
**Title: DMG-CPU B**

Size: A3 Date: 2025-04-12  
KiCad E.D.A. 8.0.9

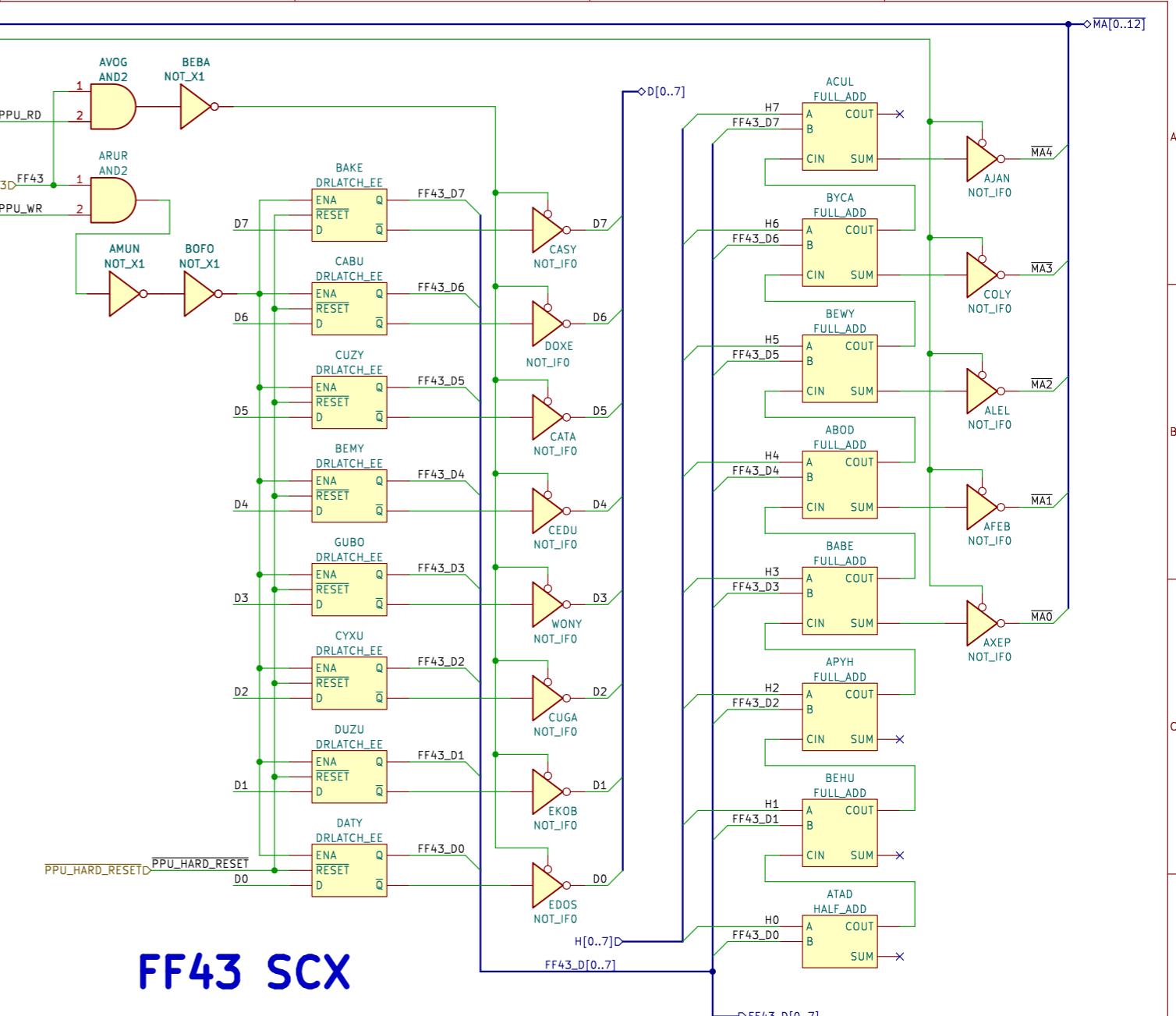
Rev: 0.7

Id: 28/46

## FF42 SCY



## FF43 SCX



<https://github.com/msinger/dmg-schematics>  
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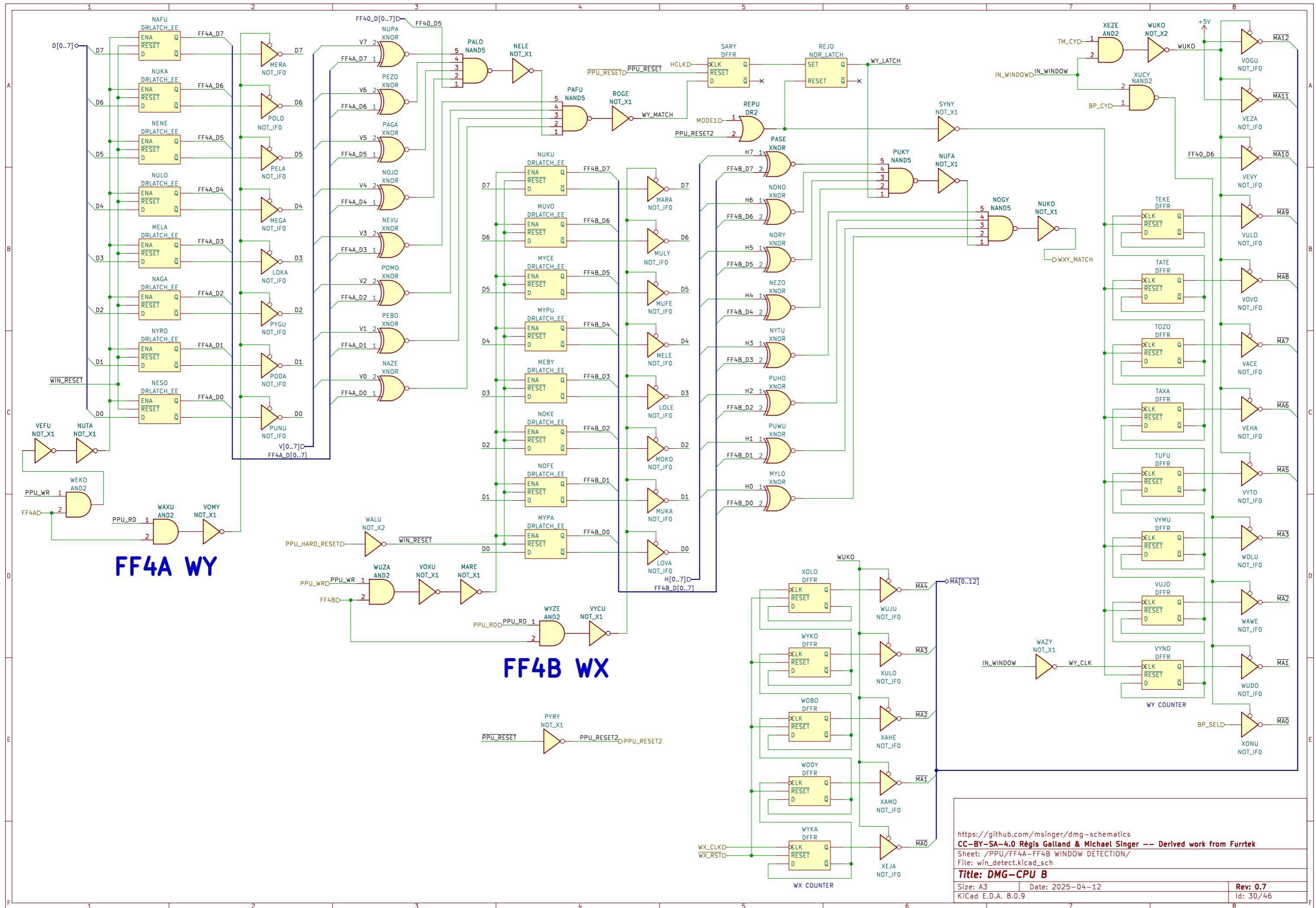
Sheet: /PPU/FF42-FF43 BACKGROUND SCROLLING/  
File: background.kicad\_sch

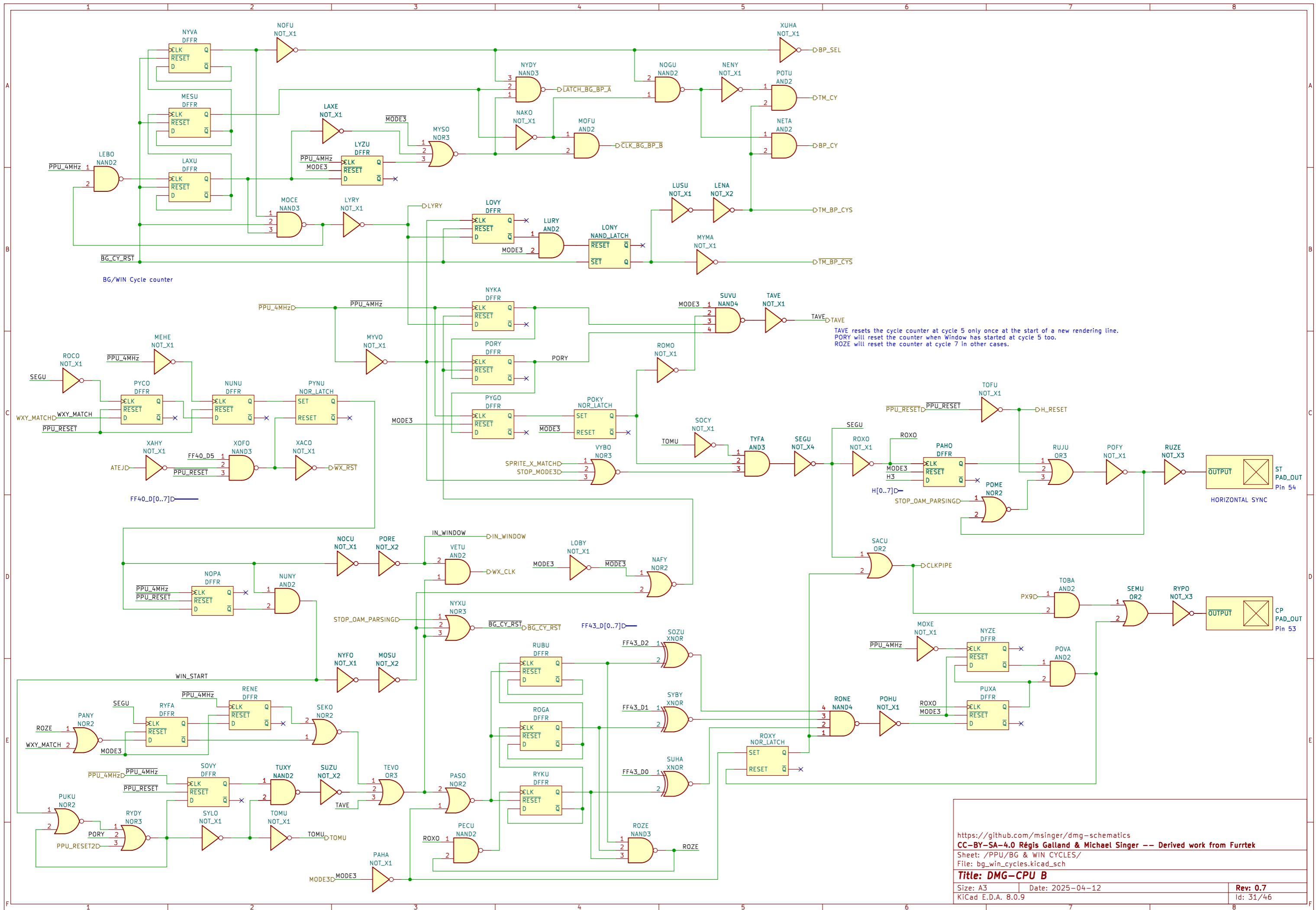
Title: DMG-CPU B

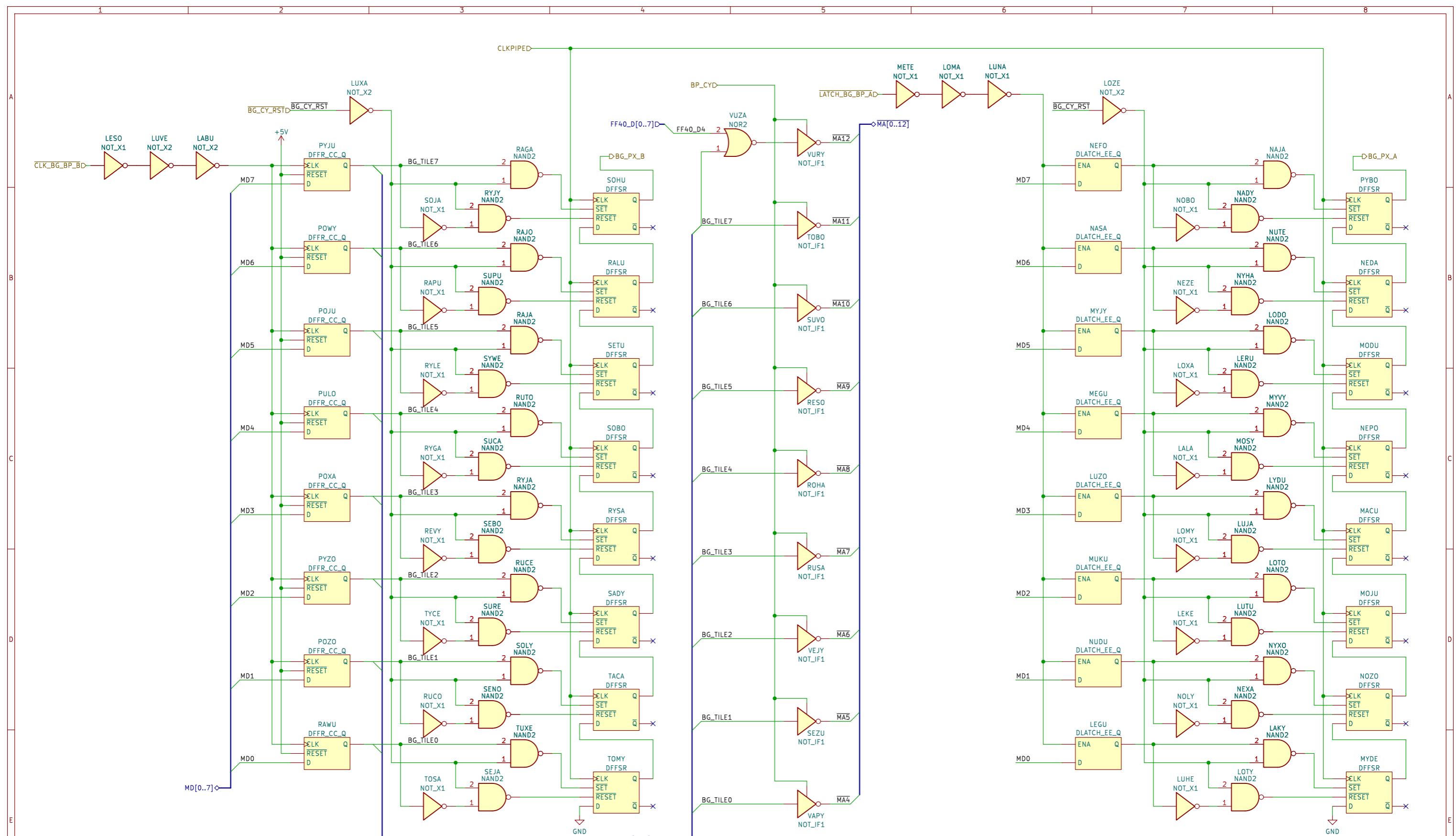
Size: A3 Date: 2025-04-12  
KiCad E.D.A. 8.0.9

Rev: 0.7

Id: 29/46







MA bit 3-0 comes from BG or WIN sheets which gives the y offset in the tile

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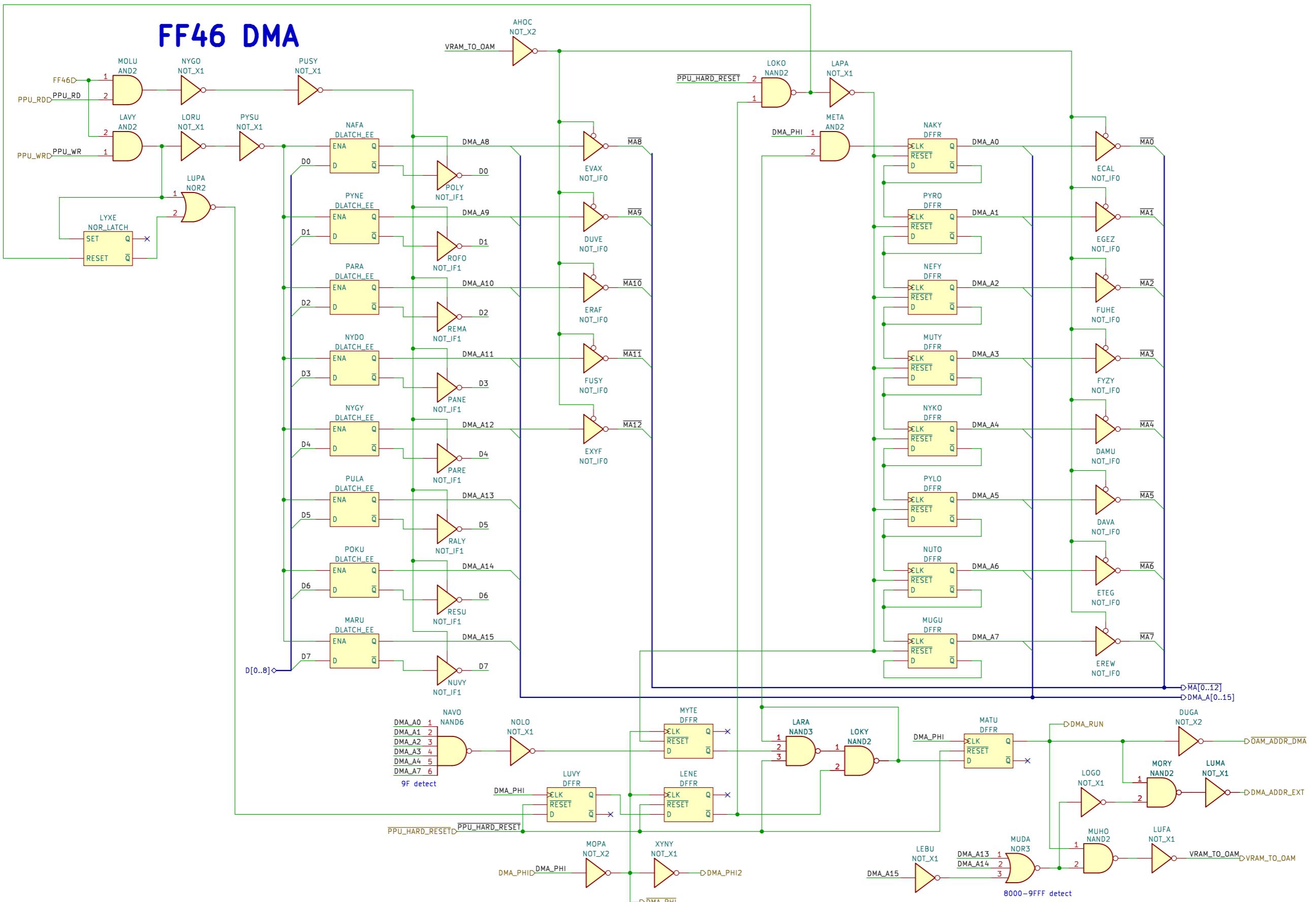
Sheet: /PPU/BG PIXEL SHIFTER/

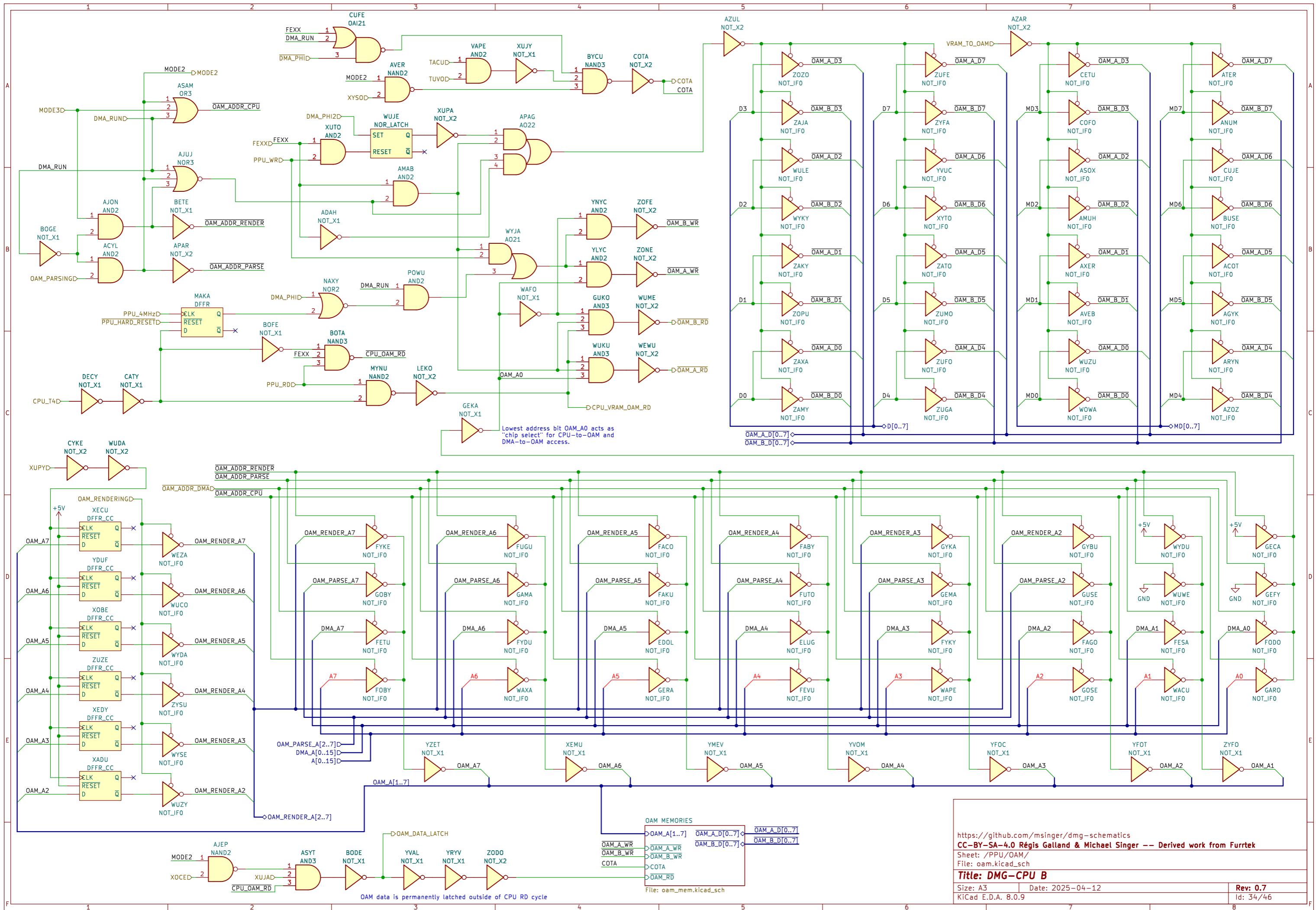
File: bg\_px\_shifter.kicad\_sch

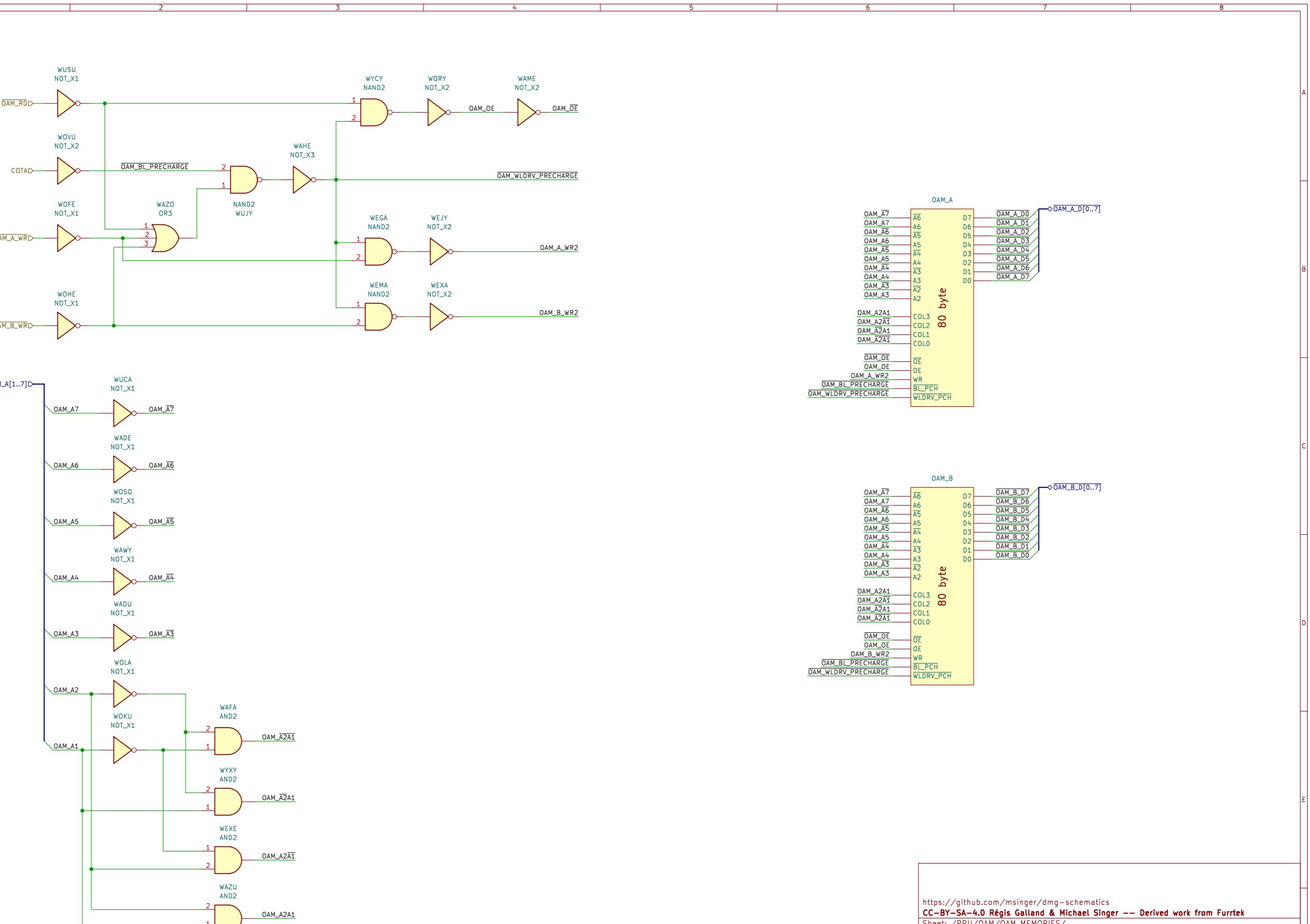
Title: DMG-CPU B

Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7  
 Id: 32/46







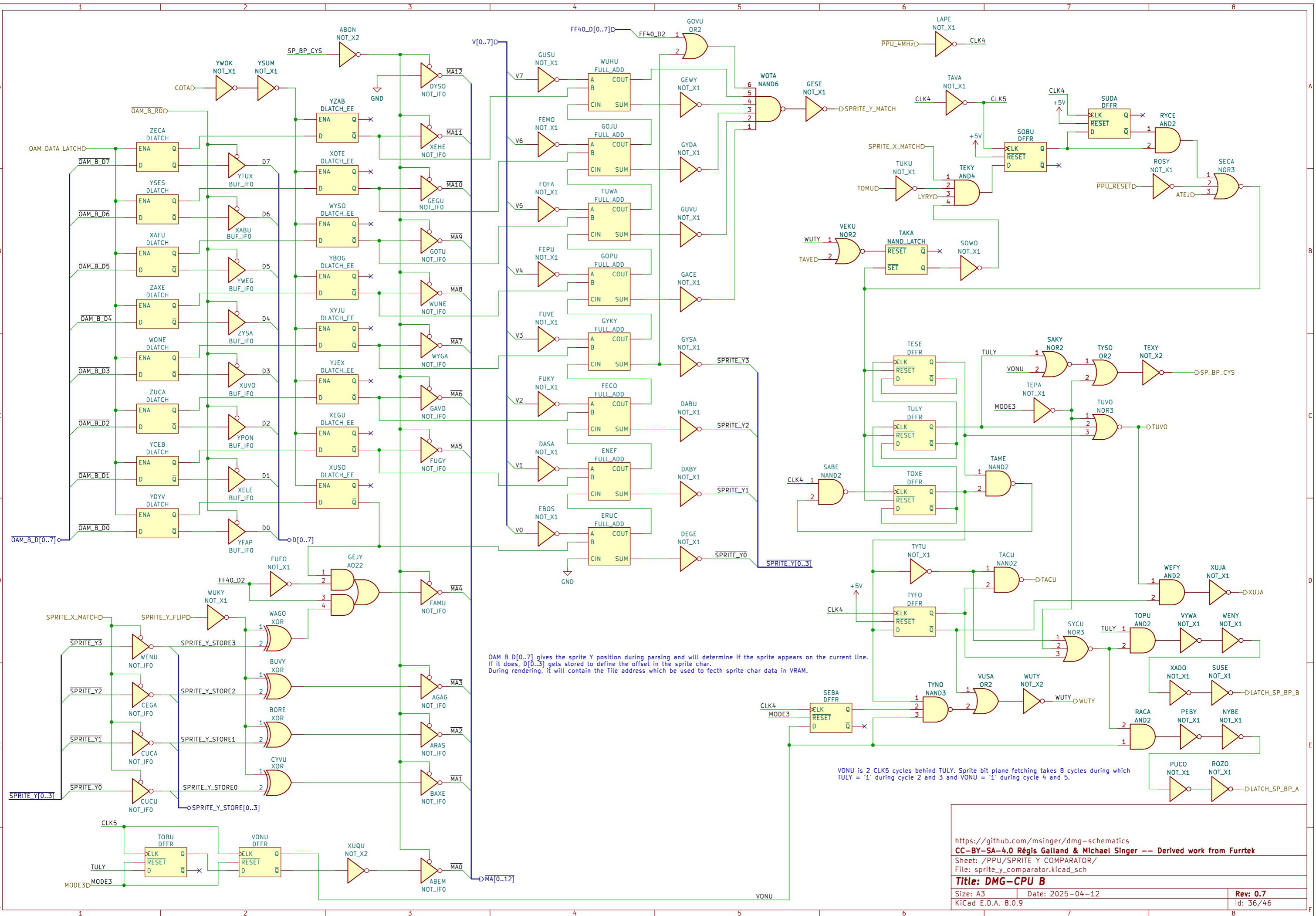
<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek

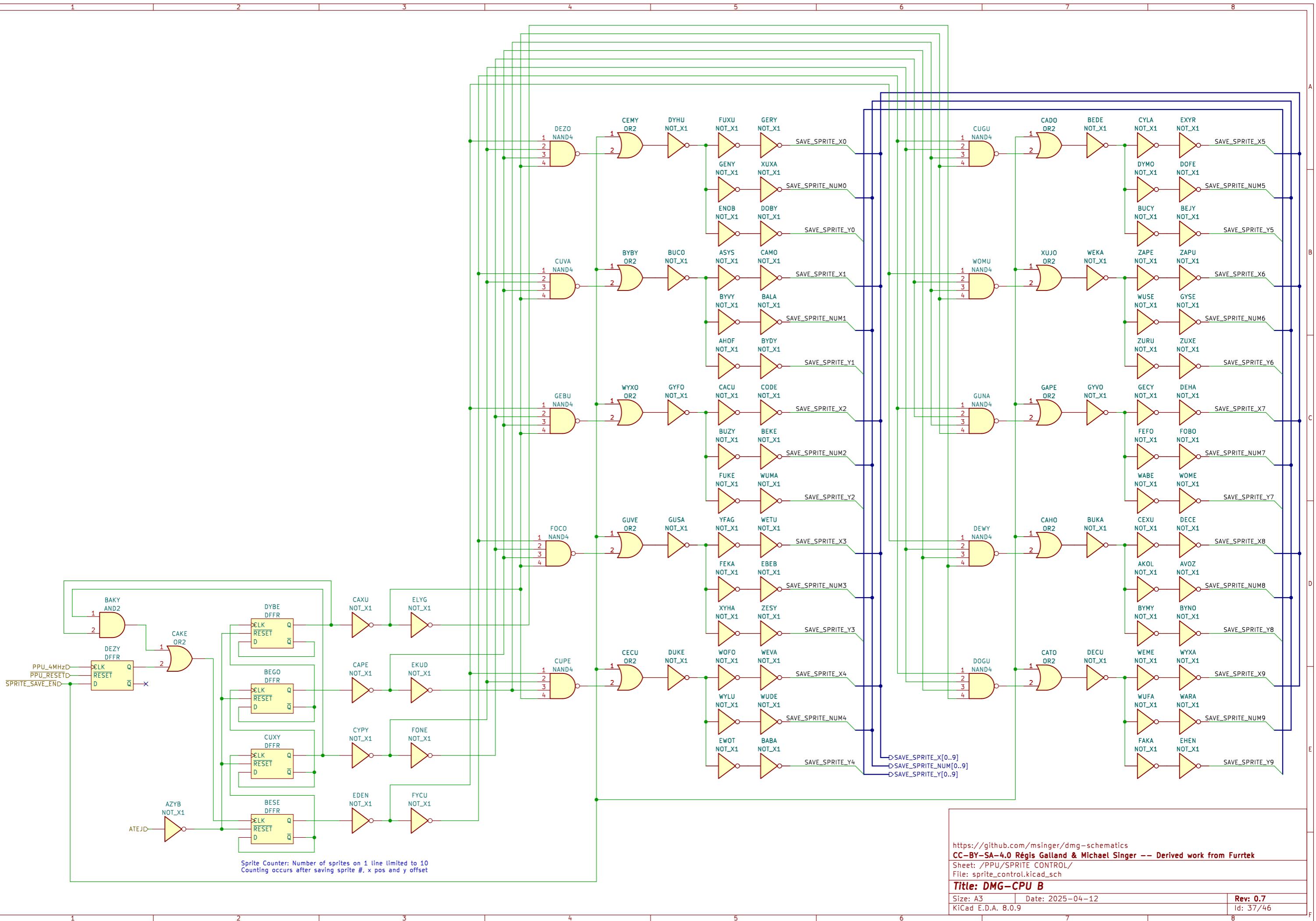
Sheet: /PPU/OAM/OAM MEMORIES/  
 File: oam\_mem.kicad\_sch

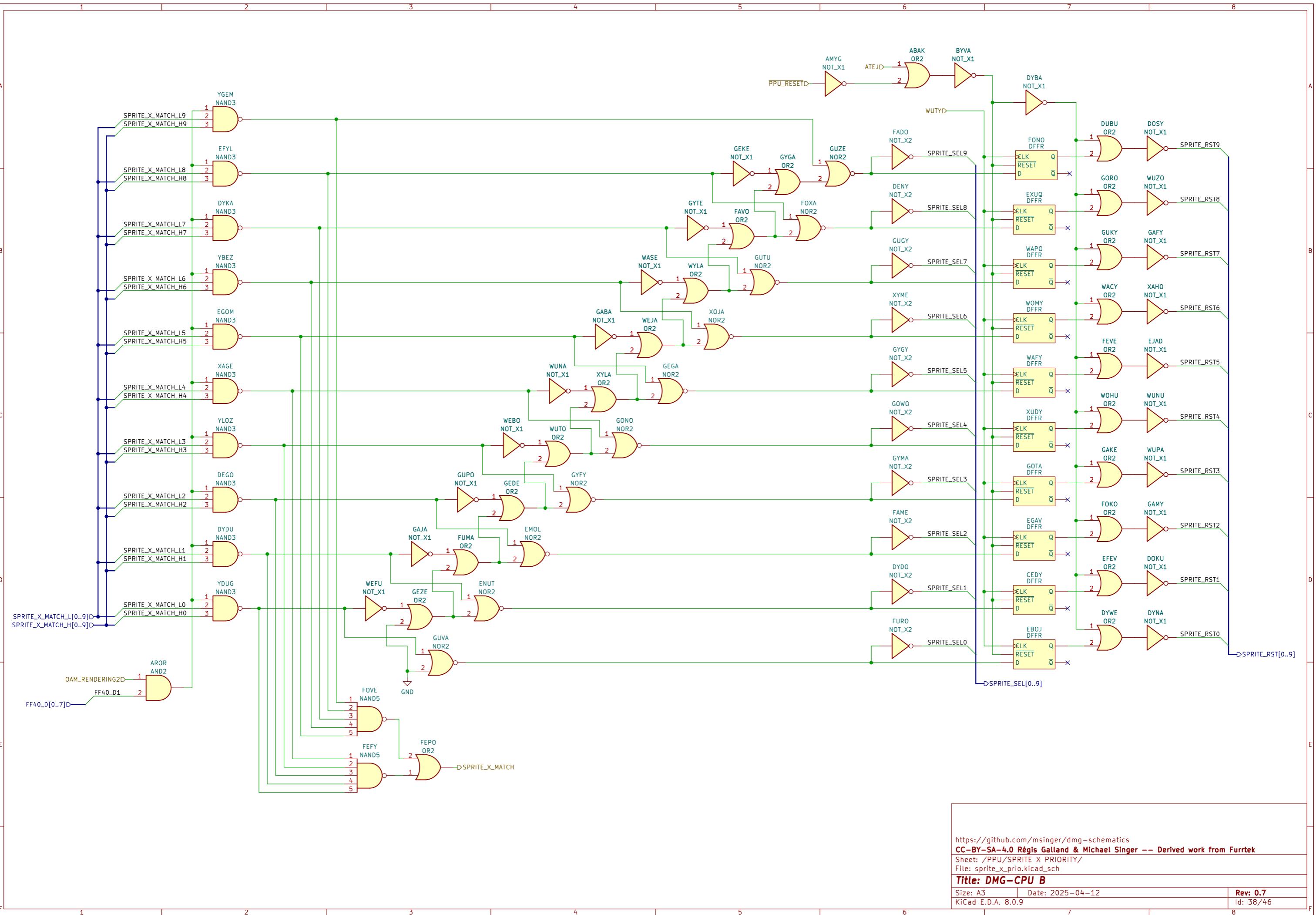
**Title: DMG-CPU B**

Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7  
 Id: 35/46







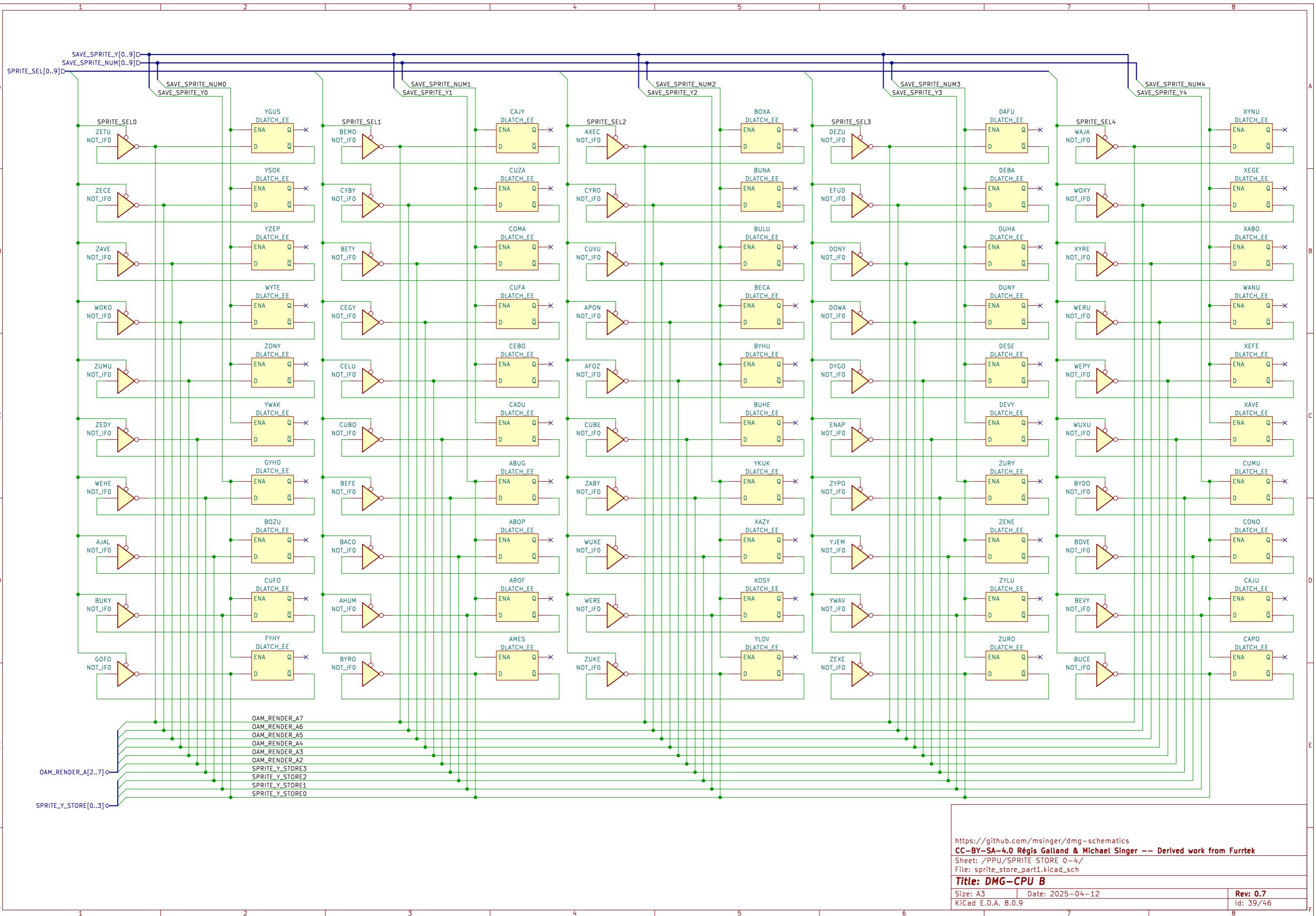
<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek  
 Sheet: /PPU/SPRITE\_X\_PRIORITY/  
 File: sprite\_x\_prio.kicad\_sch

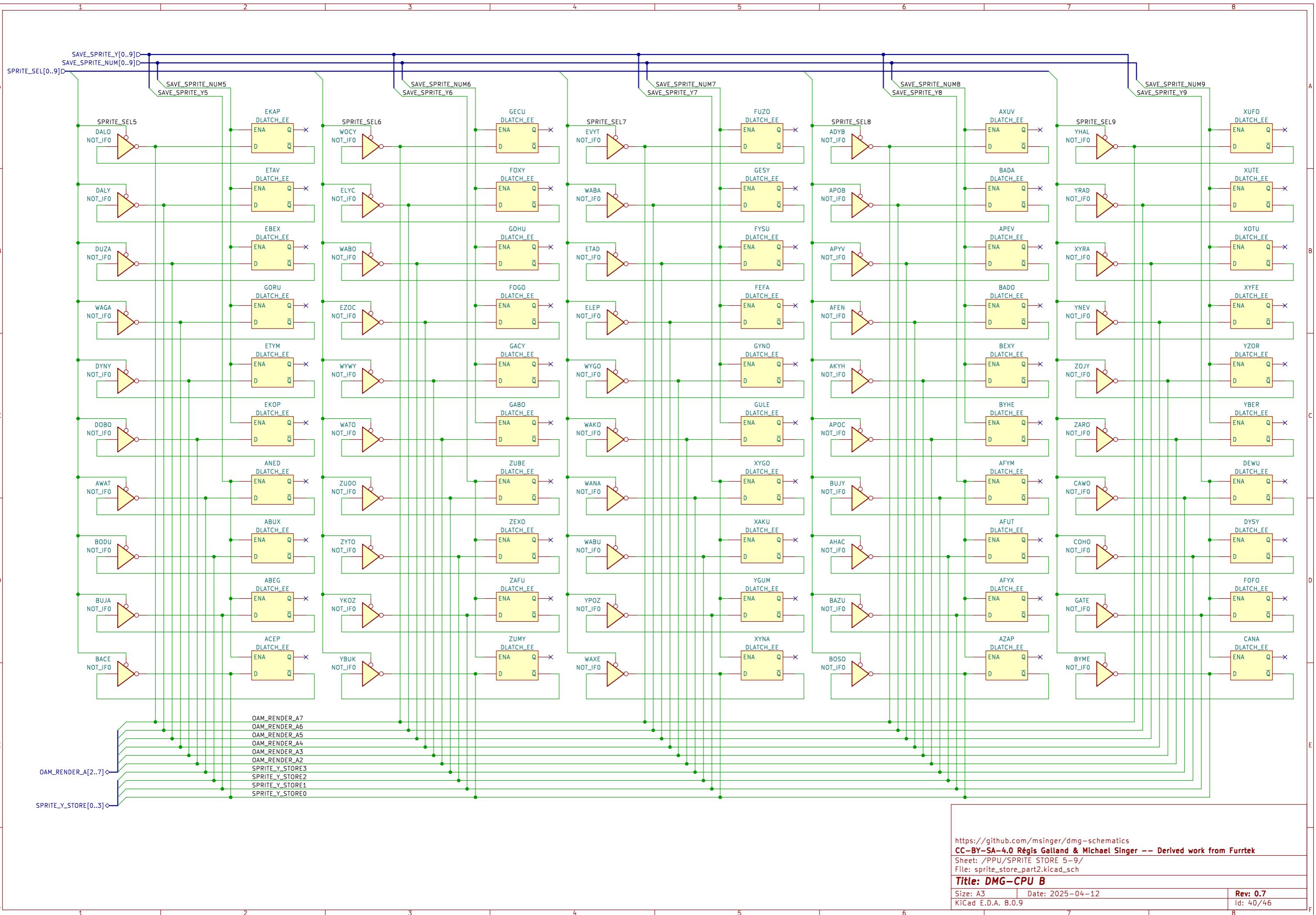
**Title: DMG-CPU B**

Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7

Id: 38/46



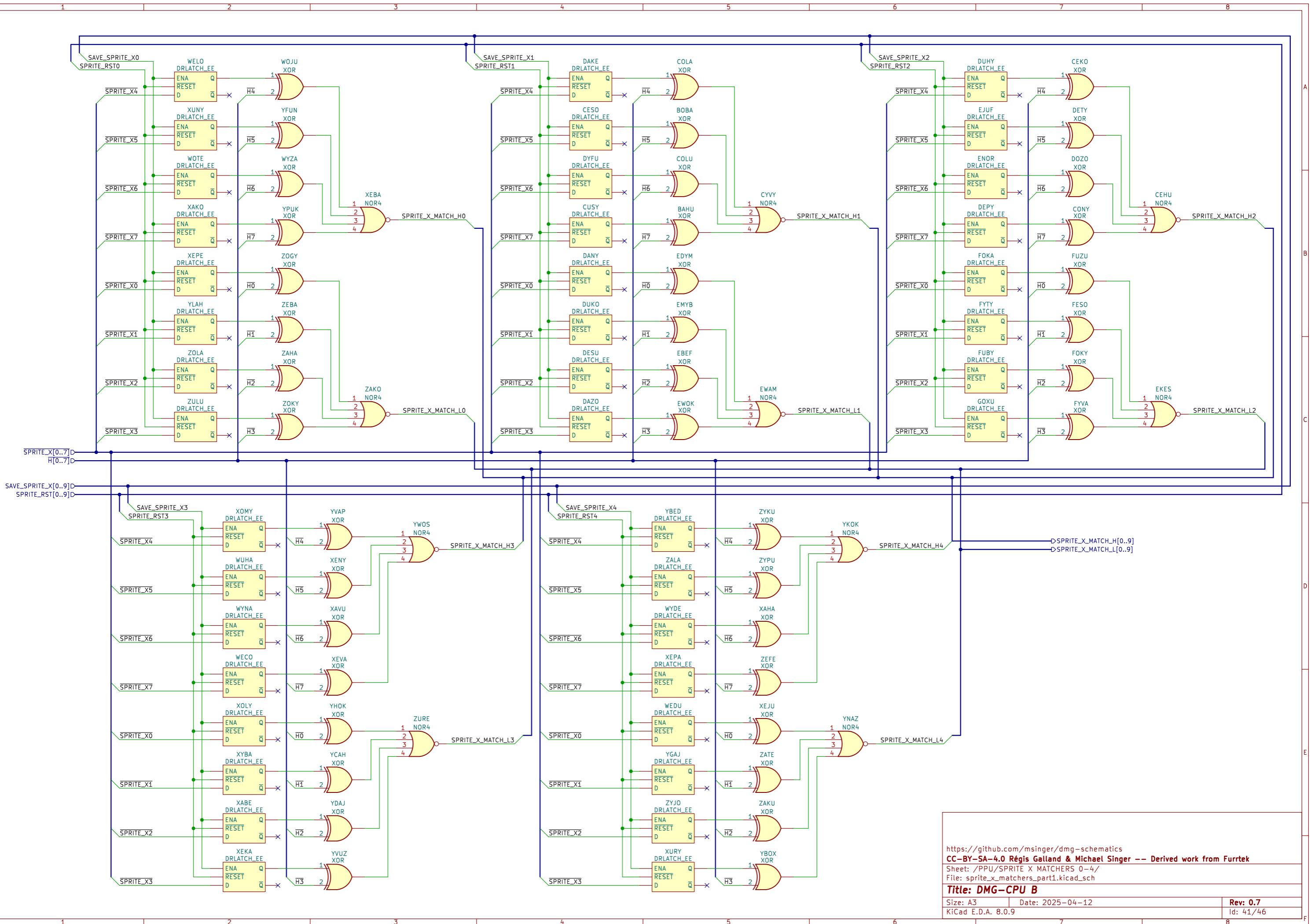


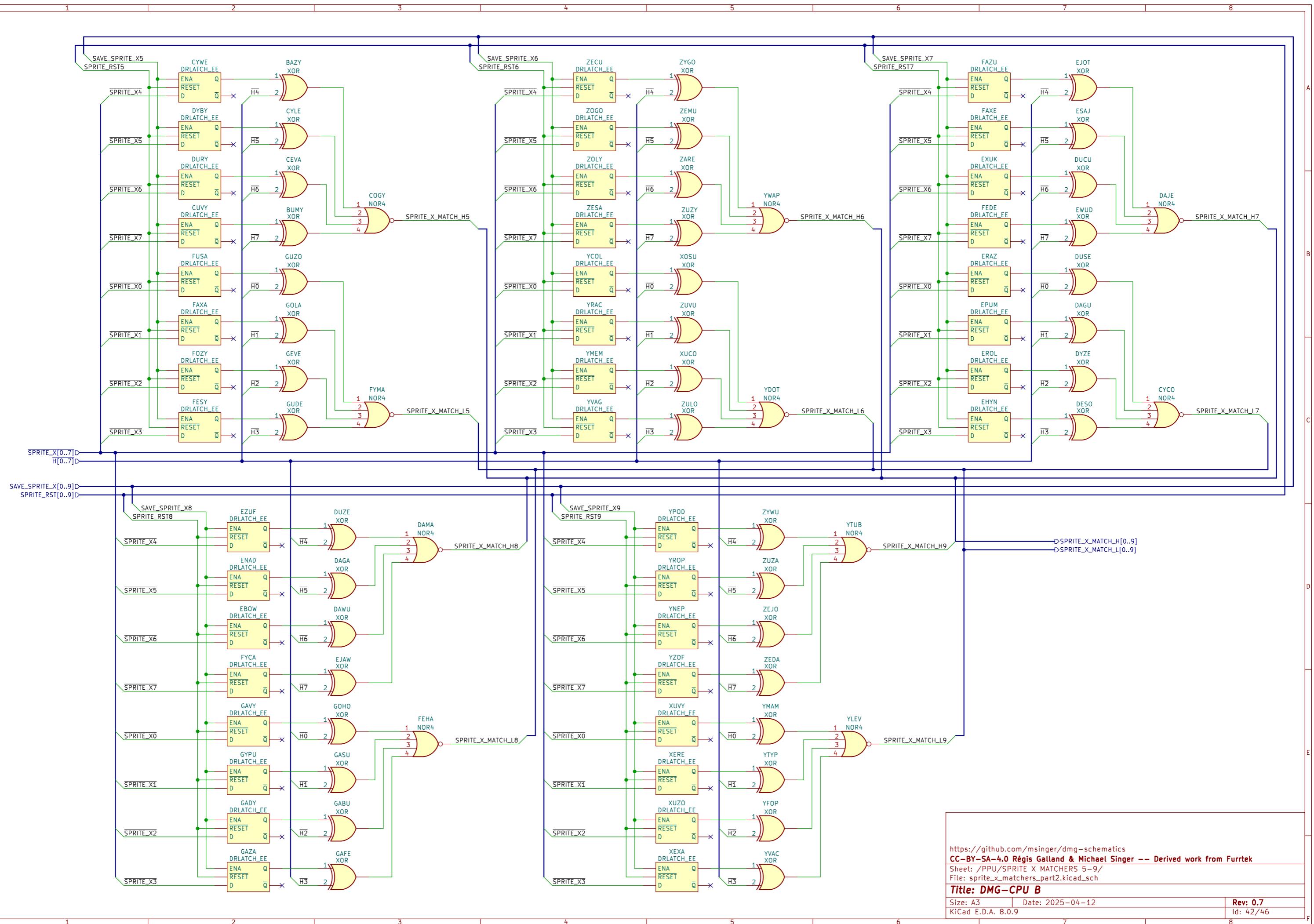
<https://github.com/msinger/dmg-schematics>  
 CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furtek

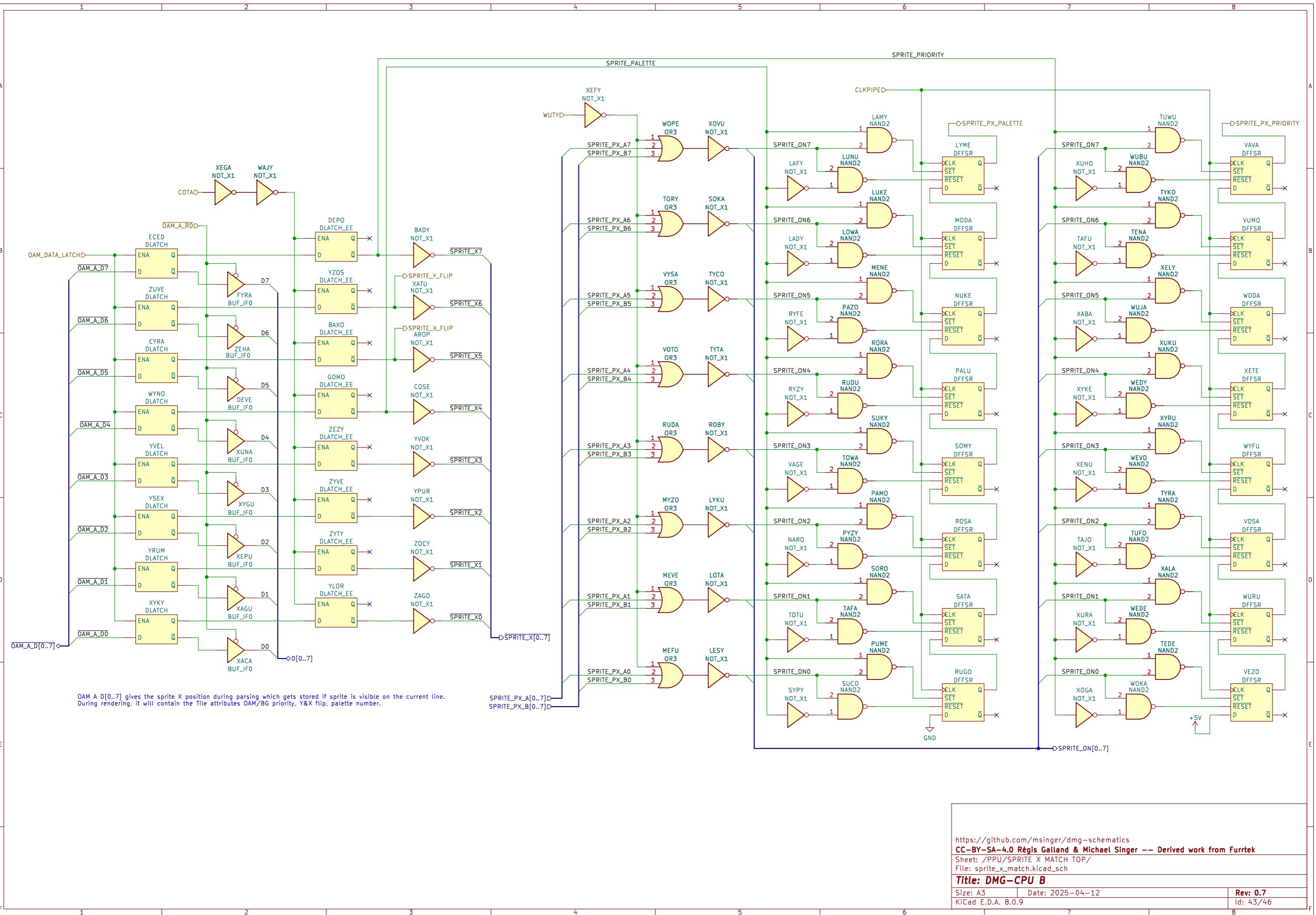
Sheet: /PPU/SPRITE STORE 5-9/  
 File: sprite\_store\_part2.kicad\_sch  
**Title: DMG-CPU B**  
 Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

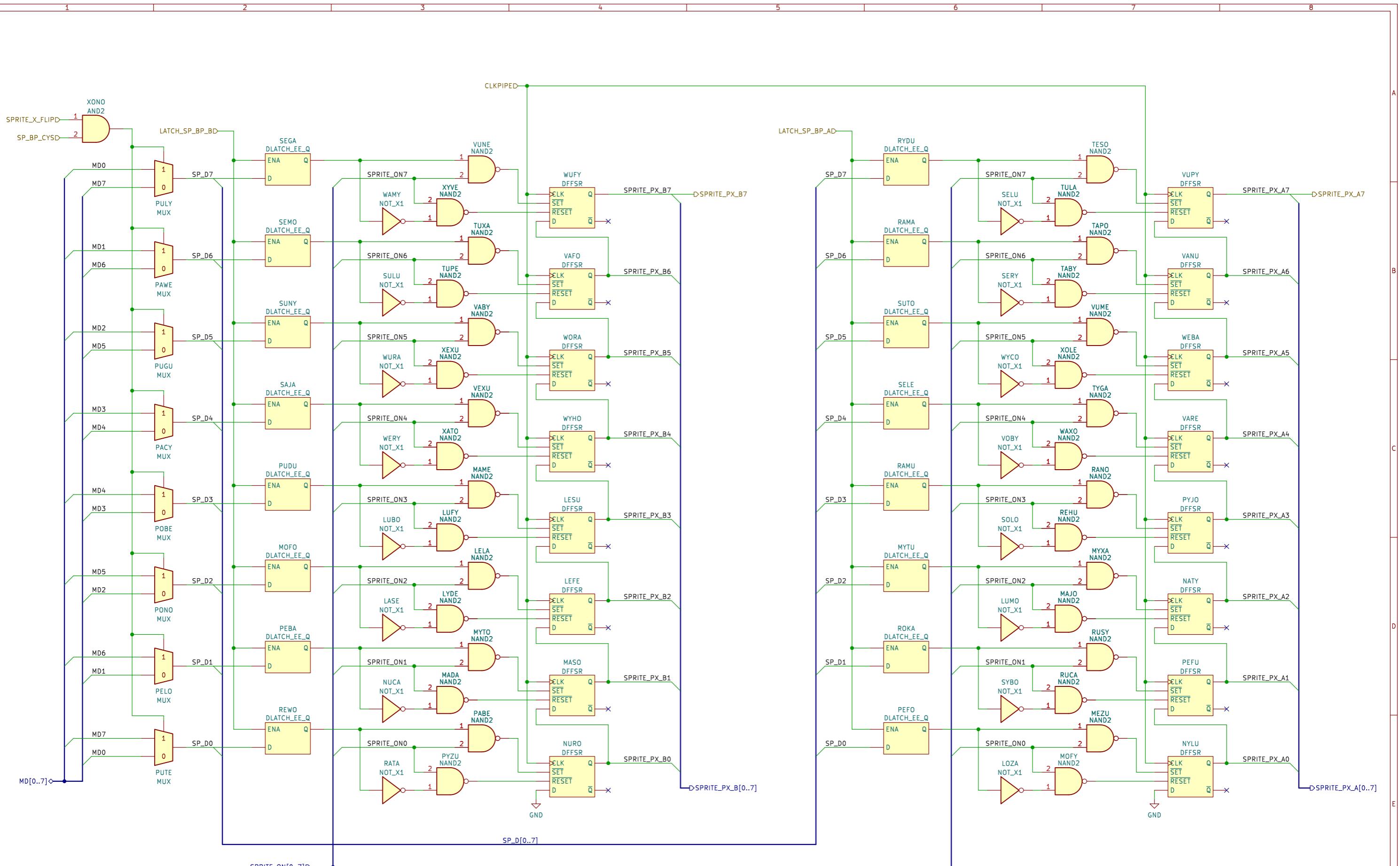
Rev: 0.7

Id: 40/46









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 Sheet: /PPU/SP PIXEL SHIFTER/  
 File: sp\_px\_shifter.kicad\_sch

**Title: DMG-CPU B**

Size: A3 Date: 2025-04-12  
 KiCad E.D.A. 8.0.9

Rev: 0.7  
Id: 44/46

