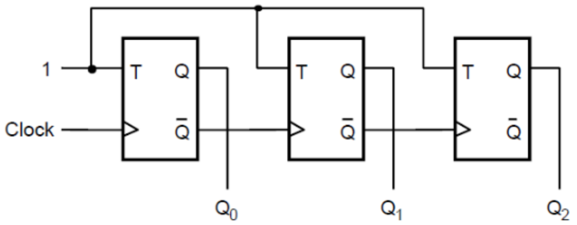
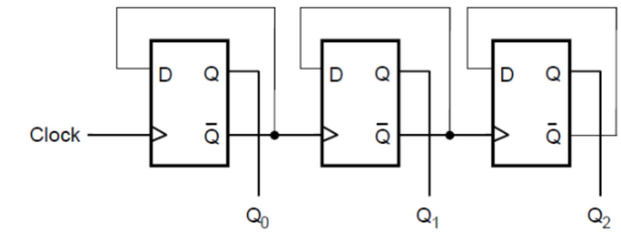
# VE270 Lecture 8 Counter

## Asynchronous Binary Counter

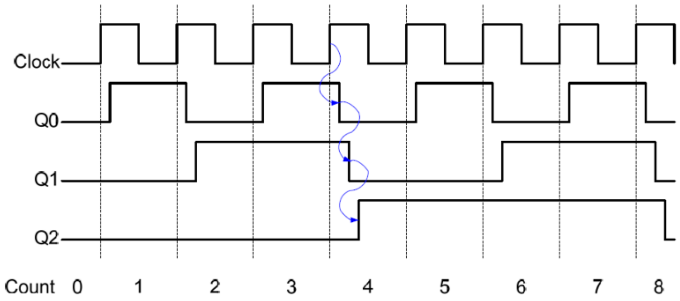
### T-Flip-Flops implementation



### D-Flip-Flops implementation

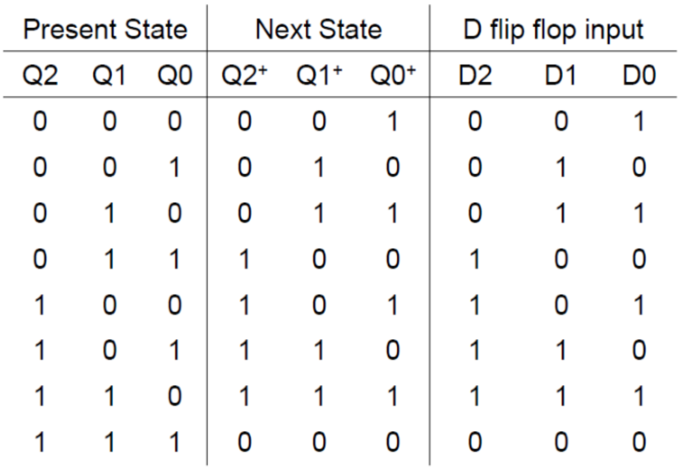


### Problem: Delays



# Synchronous Binary Counter

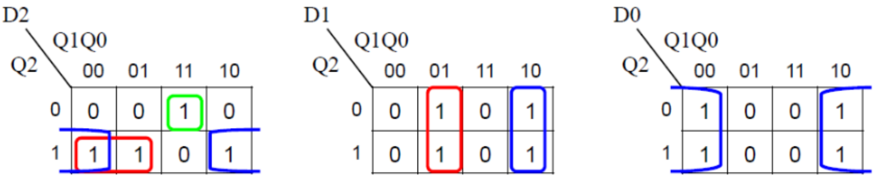
## Design (With D-Flip-Flop)



| Present State | | | Next State | | | D flip flop input | | |
|---|---|---|---|---|---|---|---|---|
| Q2 | Q1 | Q0 | Q2⁺ | Q1⁺ | Q0⁺ | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

With the Present State as the D flip flop output.

Apply K-Map method:



D2

| Q2 \ Q1Q0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

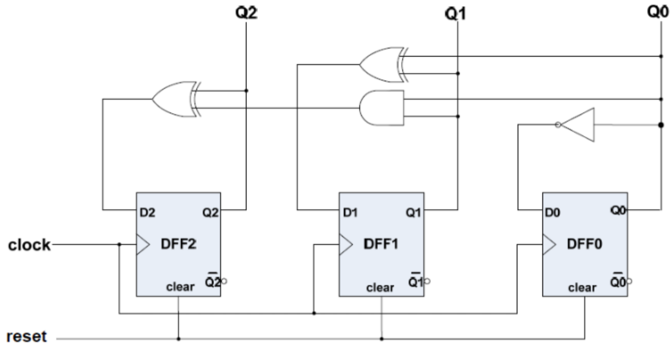
D1

| Q2 \ Q1Q0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |

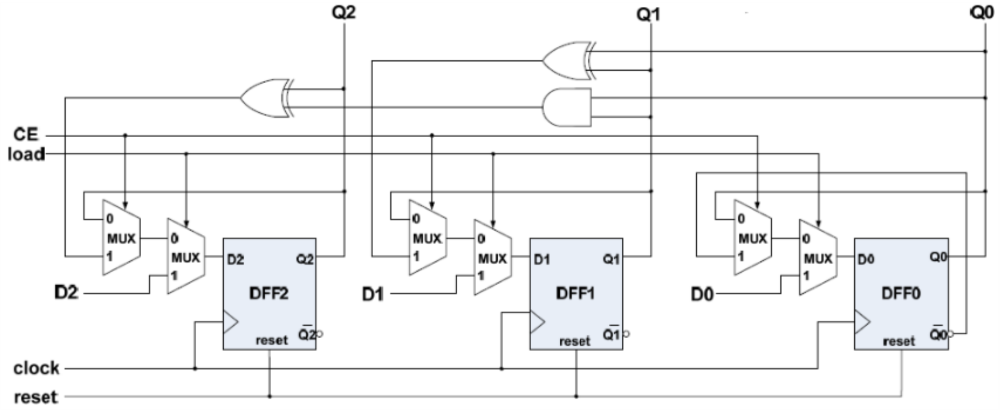
D0

| Q2 \ Q1Q0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |

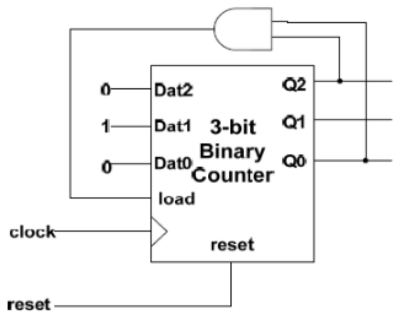
So we get $D_n = Q_n \oplus (Q_{n-1} \cdots Q_n)$

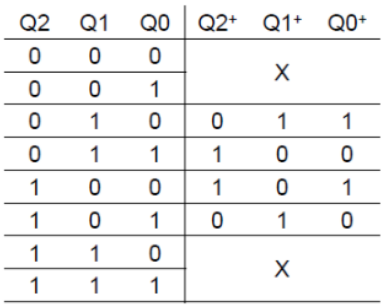


## External Control



## Customize Counting Sequence

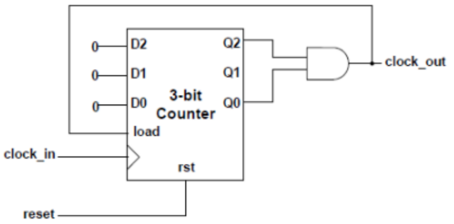


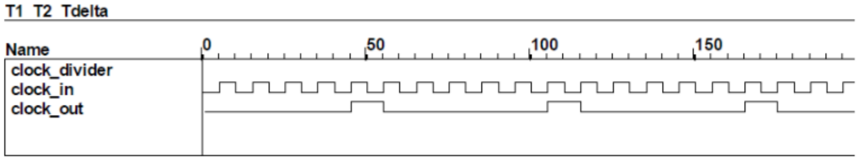


| Q2 | Q1 | Q0 | $Q2^+$ | $Q1^+$ | $Q0^+$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | | X | |
| 0 | 0 | 1 | | | |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | | X | |
| 1 | 1 | 1 | | | |

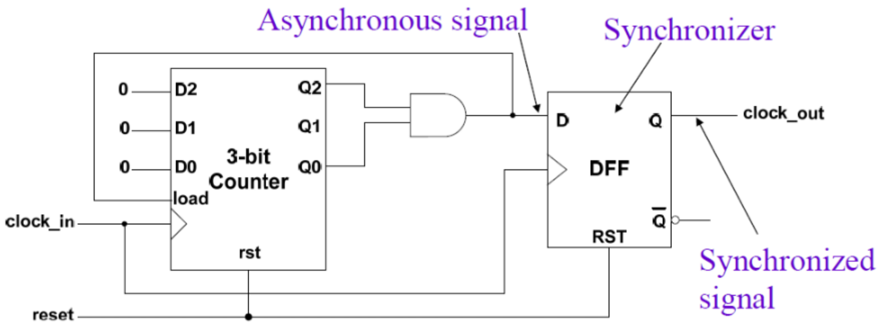
## Clock Divider

Divide by $n$, let the load is activated by $n-1$.





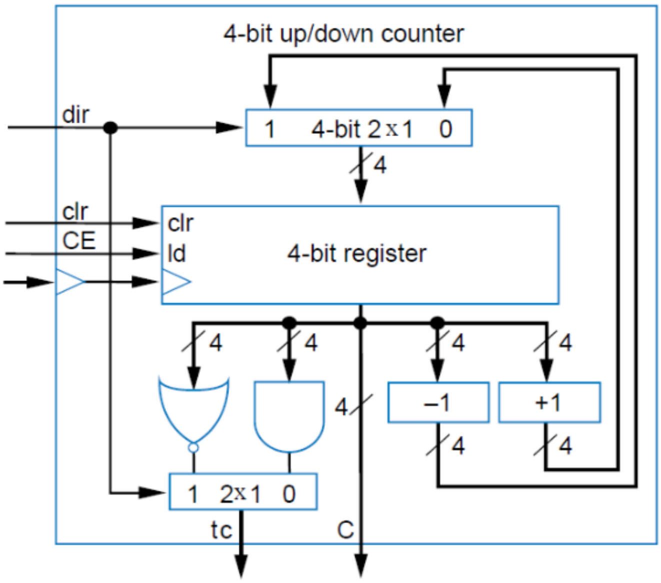
## Output Synchronization



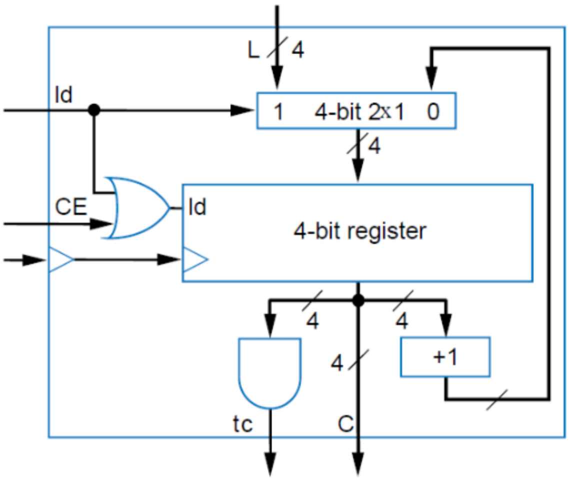
Since the output clock signal may have delay by the gate, so we give a D-Flip-Flop to synchronize the signal to the output.

The output still have delay, but the delay is smaller, not deleted.

## Up/Down Counter



## Alternative Design Counter with Control


L
4
ld
1
4-bit 2x1
0
4
CE
ld
4-bit register
4
4
4
+1
tc
C