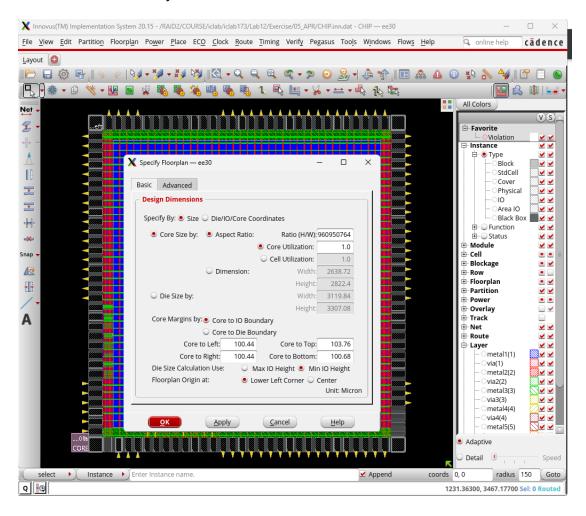
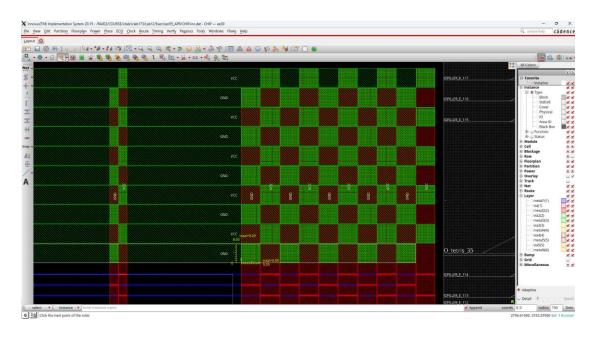
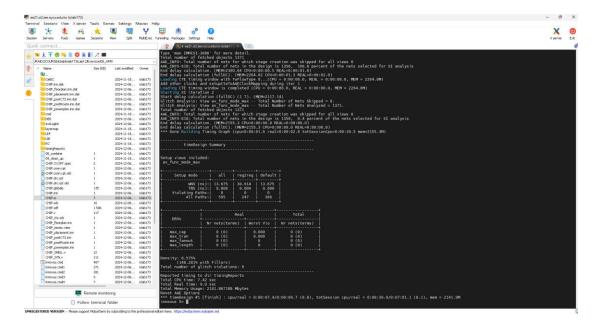
1. Core to IO boundary:



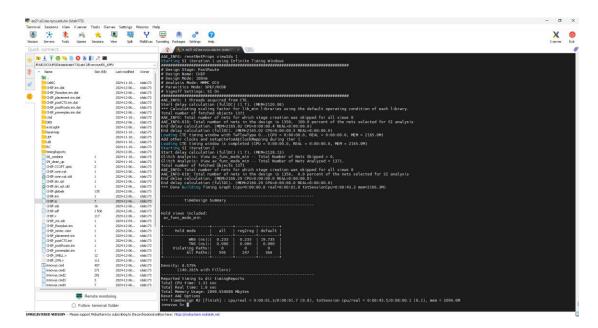
2. Core Ring:



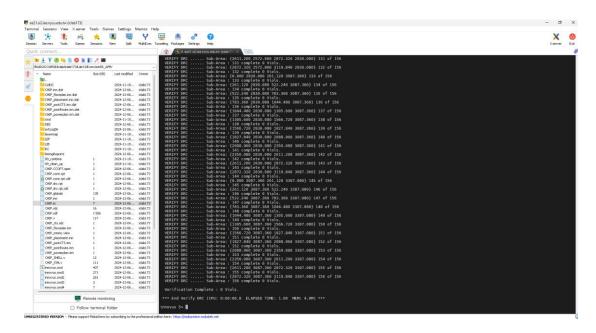
3. Post-Route setup time analysis :



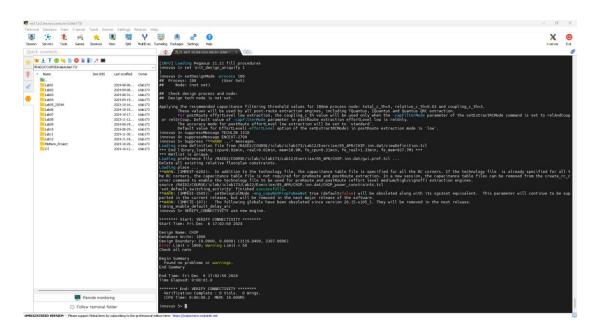
4. Post-Route hold time analysis:



5. DRC result:



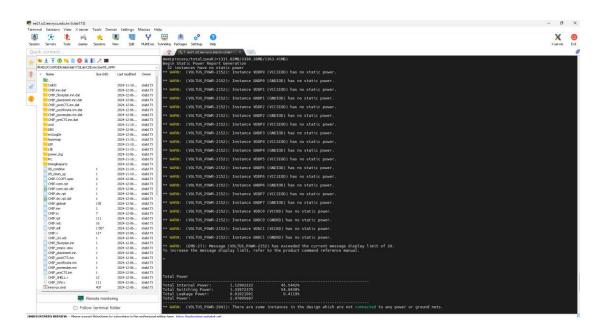
6. LVS result:



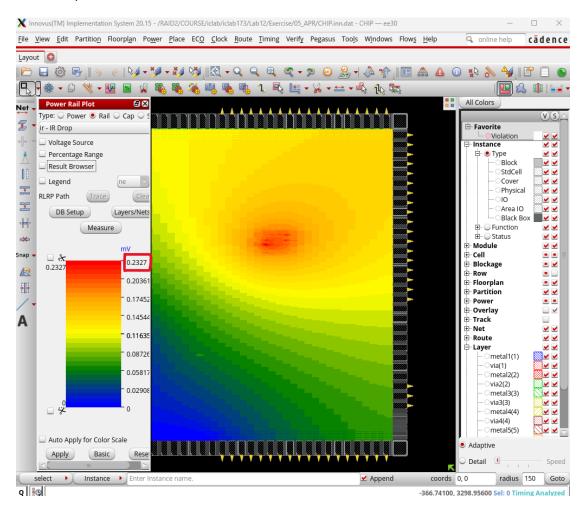
7. Post Layout simulation result:

```
| Rest | Company | Company
```

8. Power result:



9. IR Drop Results:



我在每邊都加上 4 個 VCC 來減少 IR drop 的問題