2023 NYCU EE VLSI Lab Report

Lab04 4-Bit Multiplier

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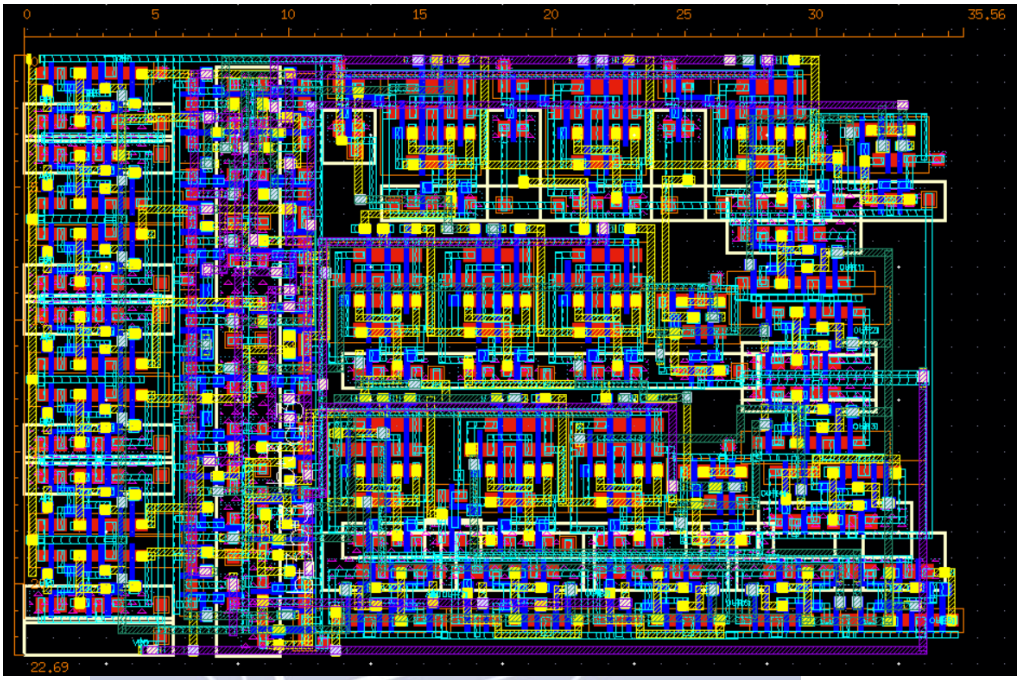
I. Layout result

1. Layout picture with ruler

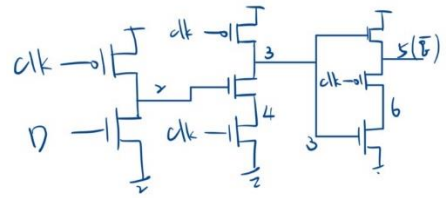


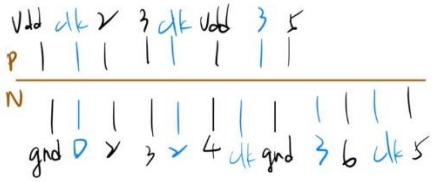
2. Design concept

(1) Circuit Schematic

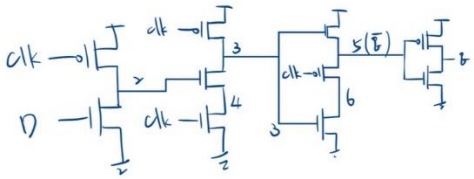
DFFN（DFF 變形，輸出訊號會和輸入訊號相反）、FAS（FA 變形，輸出是~COUT 和 SUM）、FAC（FA 變形，輸出是 COUT 和~SUM）、FAN（FA 變形，輸出是~COUT 和~SUM）、HAC（HA 變形，輸出是 COUT 和~SUM）、HAN（HA 變形，輸出是~COUT 和~SUM）。

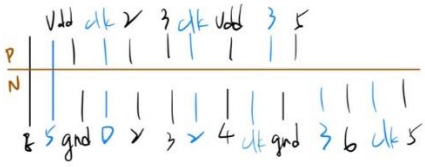
DFFN (DFF_noInv)



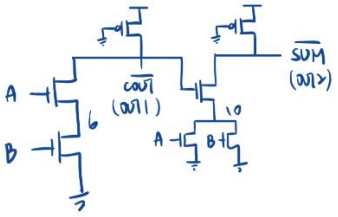


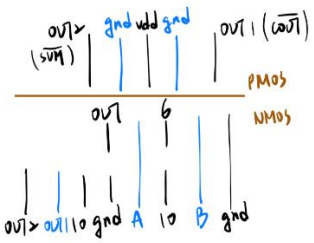
DFF (DFF_inv)



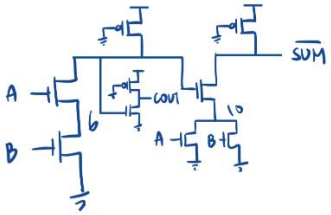


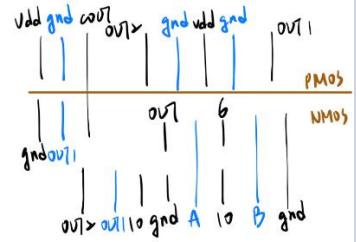
HAN (HA_noInv)



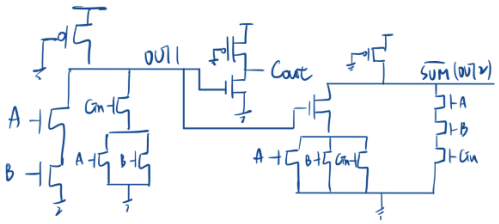


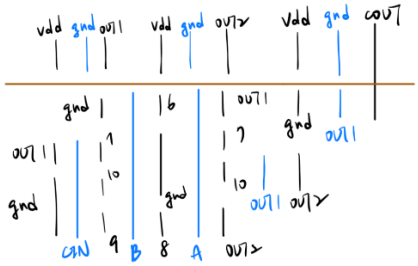
HAC (HA_withInvForCout)



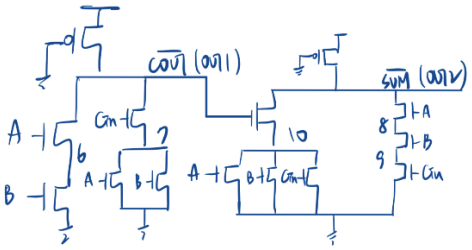


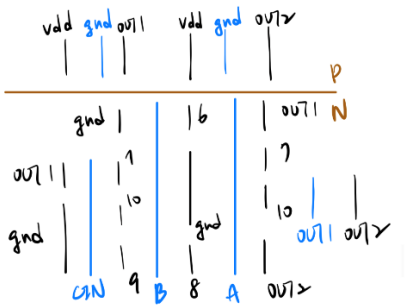
FAC (FA_withInvForCout)

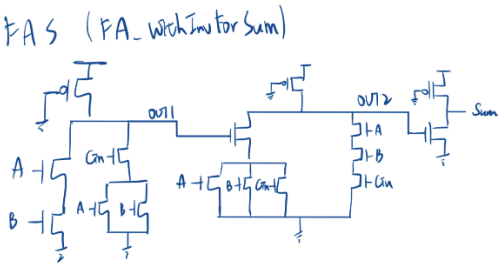


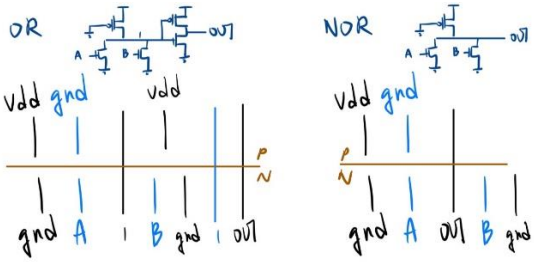


FAN (FA_noInv)





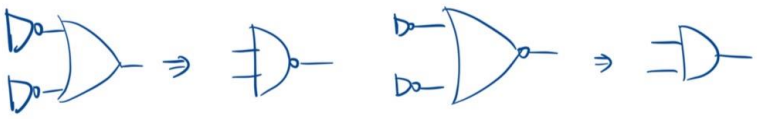




(2) Summary of structure (number of transistor / logic gate is used)

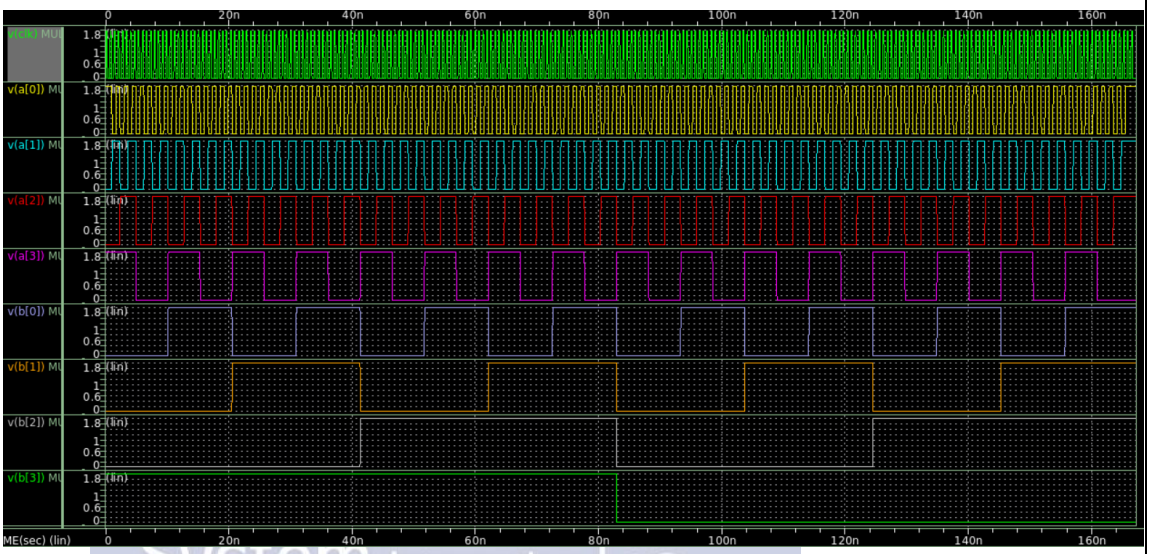
Logic gate	Number	PMOS(/logic gate)	NMOS(/logic gate)
DFF	3	4	6
DFFN	13	3	5
HAC	1	3	6
HAN	2	2	5
FAS	3	3	13
FAC	1	3	13
FAN	5	2	12
NOR	11	1	2
OR	5	2	3

總共用了 101 顆 PMOS 和 248 顆 NMOS。用 NOR, OR 去實現 AND, NAND，是為了減少 inverter 的使用，所以輸入端的 DFF 都輸出反向訊號。

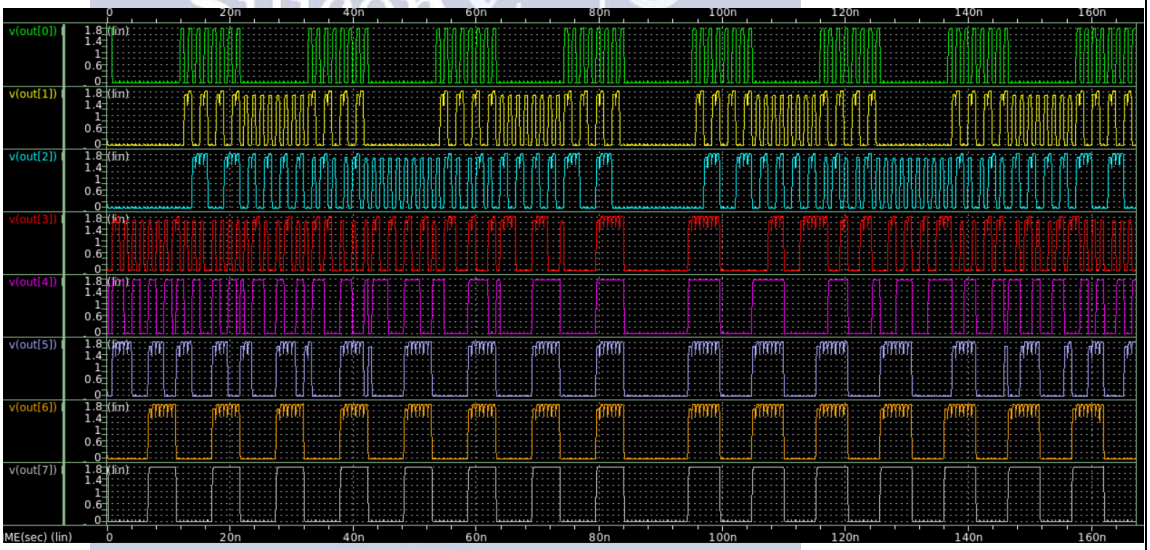


II. Simulation result

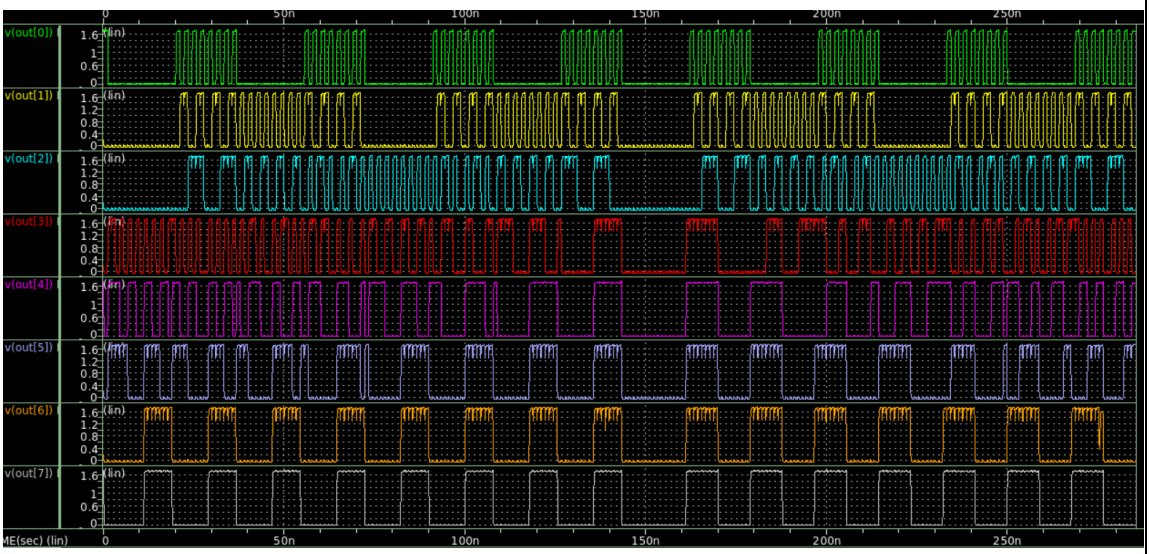
1. **Output waveform** (with input from MULT4.vec)



(1) Pre-sim



(2) Post-sim

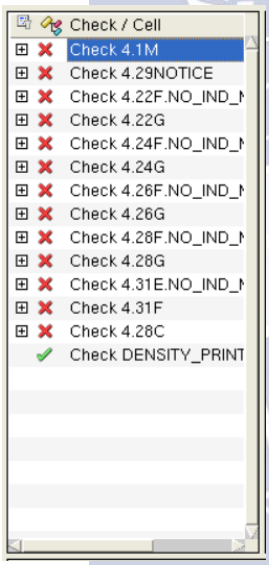


(3) Performance list (TT case under worst case input pattern)

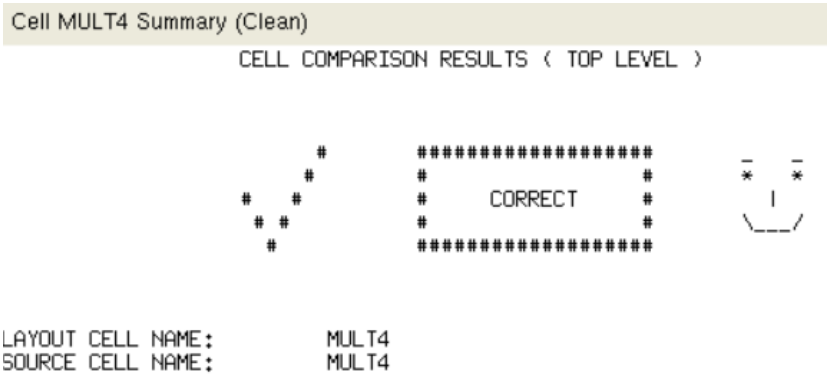
Maximum operation frequency	Pre-sim: 0.65ns
	Post-sim: 1.11ns
Average power	Pre-sim: 7.040e-3
	Post-sim: 6.357e-3
Layout area	35.56*22.69 = 806.8564
Multiplier and adder structure	Wallace tree
Glitch control (Yes/No)	No

III. Verification result

1. DRC

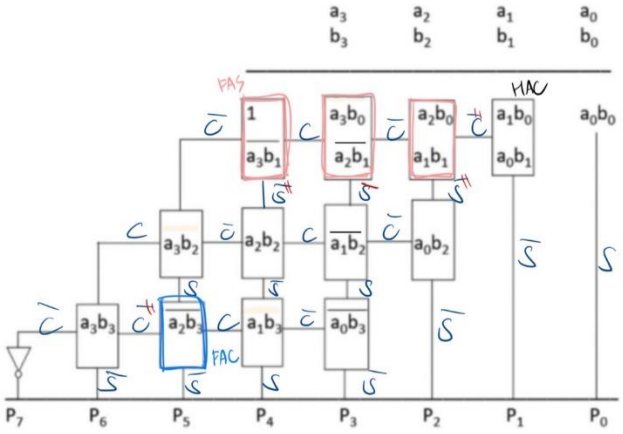


2. LVS



IV. Discussion

1. Sketch your partial product



2. Show your critical path