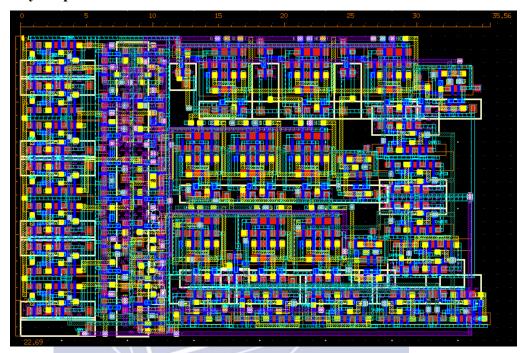
2023 NYCU EE VLSI Lab Report

Lab04 4-Bit Multiplier

Student ID: 110511254 Name: 徐煜絨 Date: 2023/12/13

I. Layout result

1. Layout picture with ruler

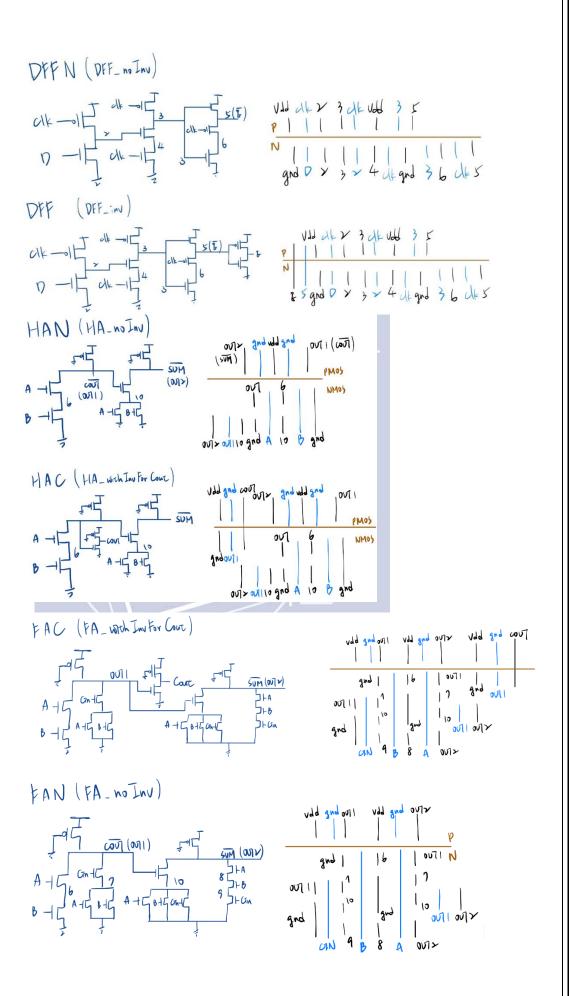


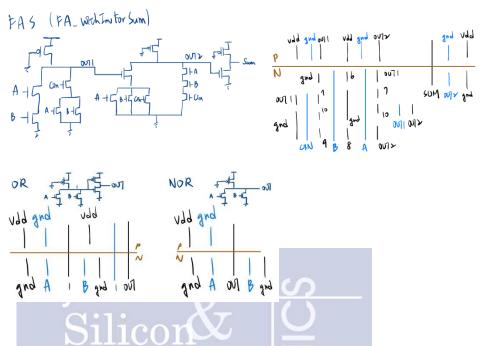
2. Design concept

(1) Circuit Schematic

DFFN (DFF 變形,輸出訊號會和輸入訊號相反)、FAS (FA 變形,輸出是~COUT 和 SUM)、FAC (FA 變形,輸出是 COUT 和~SUM)、FAN (FA 變形,輸出是~COUT 和~SUM)、HAC (HA 變形,輸出是COUT 和~SUM)。

DFFN (BU))	(asbi) OR	OR	(arbi)	FAS FAS FAS HAC
DEFN (AL3)	(a, b.) NOR	NOR	(arbo)	DEEN (OUL)
DEEN (B(0))	(a,b) NOR			FAN FAN FAN HAN DFFN (ONT)
V.	(a.b.) NOR	NOR	(asbr)	DEEN (OUT[3])
DEFN (ACA)	(aob) NOR	MOR	(arbr)	FAN FAC FAN HAN DEF (00164)
DEEN (BED)	(abb) OR	NOR	(asb3)	Vrr (witer)
DFFN (AU)	(ab) NOR	OR	(a, b)	DEFN DEF DEFN DEFN
DEFN (BEST)	(a.b.) NOR	OR	(a.b)	(ALO) (OUT[1]) (OUT[0]) (OUT[6]) (OUT[6])

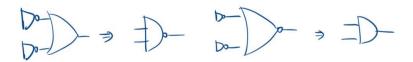




(2) Summary of structure (number of transistor / logic gate is used)

Logic gate	Number	PMOS(/logic gate)	NMOS(/logic gate)
DFF	3	43CO (()	6
DFFN	13	3	5
HAC	1	3	6
HAN	2	2 700 nCS / LLI	5
FAS	3 Vetwork	3	13
FAC	1	3	13
FAN	5	2	12
NOR	11	1	2
OR	5	2	3

總共用了 101 顆 PMOS 和 248 顆 NMOS。用 NOR, OR 去實現 AND, NAND,是為了減少 inverter 的使用,所以輸入端的 DFF 都輸出反向 訊號。

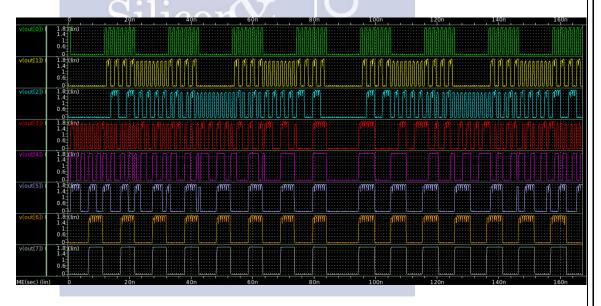


II. Simulation result

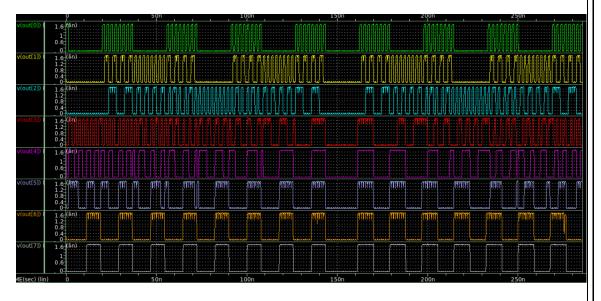
1. Output waveform (with input from MULT4.vec)



(1) Pre-sim



(2) Post-sim

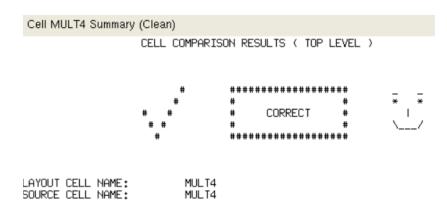


(3) Performance list (TT case under worst case input pattern)

Manianana ananting for an an	Pre-sim: 0.65ns	
Maximum operation frequency	Post-sim: 1.11ns	
A	Pre-sim: 7.040e-3	
Average power	Post-sim: 6.357e-3	
Layout area	35.56*22.69 = 806.8564	
Multiplier and adder structure	Wallace tree	
Glitch control (Yes/No)	No	

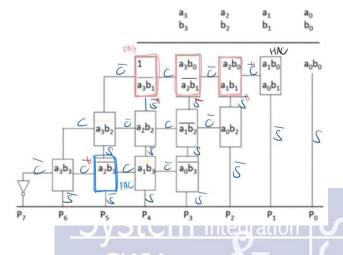
Verification result III. em Integration o 1. **DRC** con 🖺 🍕 Check / Cell ★ Check 4.29NOTICE ★ Check 4.28F.NO_IND_N ★ Check 4.28C Check DENSITY_PRINT

2. LVS



IV. Discussion

1. Sketch your partial product



2. Show your critical path

