Homework #2

(Due date: 2022/12/30)

1. MOESI is a popular coherence protocol. The cache state will be changed based on the request sources (i.e., from the processor or from the bus). Please design the corresponding Finite State Machine (FSM) to present the behavior of MOESI protocol.

2. Can we ensure the correctness of the computing result as soon as ensuring cache coherence? Please explain your perspective and propose a potential solution if not.

3. If we have a 32-core processor, each processor generates 4 loads and 2 stores per cycle. The processor cycle time is 2.167ns, and the SRAM cycle time is 15ns. How many memory banks needed to allow all processors to run at full memory bandwidth?

4. Figure 1 shows a 5-stage pipelined MIPS CPU to support a simple code in Figure 2. We need to spend one clock cycle to complete all tasks in each pipeline stage.

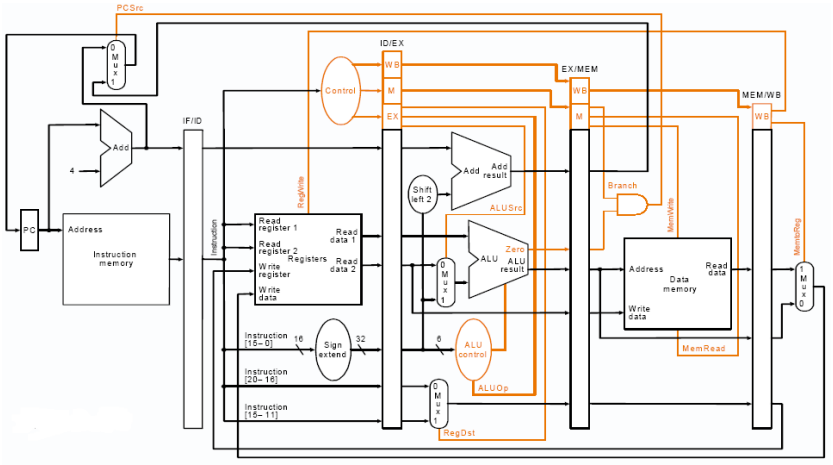

Fig. 1

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sub  $2, $1, $3
and  $12, $2, $5
or   $13, $6, $2
add  $14, $2, $2
sw   $15, 100($2)
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Fig. 2

a. Do we need to stall this architecture in Figure 1 to run the code in Figure 2? If yes, please determine how many cycles we should stall and explain your reasons. If not, please describe your reason.
b. Is it possible to move the Adder from the third pipeline stage to the second pipeline stage? If yes, please explain your re-design strategy. If not, please describe your reason.