COM519000: Digital Communication Integrated Circuits

Homework #4

Deadline : 2025/11/25 23:00

Verilog HDL IP design of an OFDM receiver

Please design an OFDM receiver based on the fixed-point simulation results in homework #3. Program Steps 1-7 are the same as those in homework #2. Please design an OFDM receiver (Step 8-10) using Verilog HDL.

1. **Bitstream generation:** The generator's output is a random binary stream with 2^25=33,554,432 bits. You can use the function of Matlab or C/C++ library as the generator. You can also design a random generator by yourself.
2. **QAM mapping:** Mapping the binary stream to a stream with 2^24=16,777,216 QPSK symbols.
3. **Serial to 64xParallel:** Grouping 64 QPSK symbols.
4. **IFFT:** 64-point OFDM modulation
5. **64xParallel to serial:** Converting to time-domain OFDM symbols.
6. **CP insertion:** Copying 1/4 OFDM to the guard interval and connecting time-domain OFDM symbols with CP as stream data.
7. **AWGN channel:** Perform additive white Gaussian noise generation (AWGN) and add AWGN to serial time-domain OFDM symbols.
8. **OFDM symbol synchronization (Digital Circuits):** Performing autocorrelation to search for the OFDM symbol boundary (FFT boundary).
9. **FFT (Digital Circuits):** Using the detected OFDM symbol boundary to do 64-point OFDM demodulation.
10. **QAM demapping (Digital Circuits):** Converting each QPSK symbol to two binary bits.
11. **Bit error rate calculation**: comparison of bit differences between the demapped bits and the generated bits in the transceiver by

    BER = Number of error bits/ Number

Program lab (60%)

Design and simulate an OFDM receiver (Step 8-10) using Verilog HDL

1. Use the word-lengths determined in the fixed-point simulation (Homework #3) to design an OFDM receiver using Verilog HDL. You can use either Single-Delay-Feedback or Multiple-Delay Commutate architecture to realize an FFT

processor for OFDM demodulation. Please draw the detailed circuit diagram of your OFDM receiver including timing synchronization circuit, OFDM demodulation circuit (FFT processor), and QAM de-mapping circuit. Please also draw the finite-state-machine that control your FFT and OFDM receiver.

2. Simulate your Verilog HDL code and **compare its outputs with those of the fixed-point simulation results** including
   (a) Synchronization circuit outputs that show at least three peaks for symbol timing.
   (b) OFDM demodulation circuit outputs of an OFDM symbol (64 points)
   (c) De-mapping circuit outputs that show the bit-stream of an OFDM symbol. (64x2 bits for QPSK, 64x4 bits for 16QAM)

Report (25%)

Please hand in your Verilog HDL and a Word report (no page limit). Please add comments on the circuit details in the Verilog HDL code. Report must include your OFDM receiver architecture and detailed circuits. More discussions about your discoveries in the simulation are preferred in the report.

Bonus (15%)

Please synthesize the Verilog HDL of the OFDM receiver by using an FPGA (Xilinx Vivado Design Suite) or using Design Compiler Logic Synthesizer with Synopsis Virtual Library. Please report logic/memory costs, and the clock speed (MHz) and throughput in bits/sec of your OFDM receiver.

Hand in

Please upload your homework to eeclass course website before the deadline. Please compress all your files into a zip file and type in your student ID number and name in the file name (studentID_name.rar, example: 11464536_王小明.zip). Otherwise, you will be regarded as no hand in. If you want to upload a newer version, please upload you file name as 11464536_王小明_v1.zip for example.