1.0   (MEM / WB forward only)

EX to 1st   ~~add~~ add $t0   IF ID EX MEM. WB.   (+1 stall)
               add $t3   IF ID ID ↘EX MEM WB.

MEM to 1st   lw $t0   IF ID EX   MEM   WB
               add $t3   IF ID   ID   EX MEM WB   (+1 stall)

EX to 2nd   add $t0   ~~IF~~ ID EX MEM. WB.
               add $t3   IF ID EX \MEM WB   (+0 stall)
               add $t6   IF ID ↗EX   MEM WB

MEM to 2nd   lw $t0   IF ID EX MEM WB.   (+1 stall)
               add $t3   IF ID EX MEM WB
               add $t6   IF IF ID   EX MEM WB

EX to 1st   lw $t1   IF ID EX MEM WB.
& MEM to 2nd   add $t9   IF ID EX MEM WB   (+1 stall)
               add $s1   IF IF ID EX MEM WB

RAW (no hazard, +0 stall)

→
$\sum$ stall cycles = EX to 1st + MEM to 1st + MEM to 2nd + (EX to 1st & MEM to 2nd)
                    = 0.1 + 0.25 + 0.1 + 0.15
                    = $\boxed{0.6}$

2.0   Full forwarding, branch pridict -token, branch resolues in EX

Cycle	IF	ID	EX	MEM	WB	
1	lw$r₂					
2	beq $r₂	lw$r₂				
3	sw $r₁	beq $r₂	lw$r₂			
4	sw $r₁	beq $r₂	(bubble)	lw$r₂		
5	after	sw $r₁	beq$r₂	(bubble)	lw$r₂	(not taken once)
6	lw$r₃	(bubble)	(bubble)	beq$r₂	(bubble)	
7	beq$r₃	lw$r₃	(bubble)	(bubble)	beq$r₂	
8	beq$r₂	beq$r₃	lw$r₃	(bubble)	(bubble)	
9	beq$r₂	beq$r₃	(bubble)	lw$r₃	(bubble)	
10	sw$r₁	beq$r₂	beq$r₃	(bubble)	lw$r₃	(taken)
11		sw$r₁	beq$r₂	beq$r₃	(bubble)	(taken)
12			sw$r₁	beq$r₂	beq$r₃	
13				sw$r₁	beq$r₂	
14					sw$r₁	

⤷ | Total cycles = 10 |

3.0.1. Each mispredicted always-taken branch causes
2\$ stall cycles $\Rightarrow 3 \times (1 - 0.4)(0.2) = \boxed{0.36}$ $\boxed{0.29}$

3.0.2

Each mispredicted 2-bit branch cause 2\$ stall cycles.
$CPI_{ALL} = CPI_{Branch}$

$CPI_{without\ conversion} = 1 + 2\$ \times (1-0.8) \times 0.2 = 1.48 \times 12 \ 1.008 \ \boxed{1.08}$

$CPI_{with\ conversion} = 1 + 2\$ \times (1-0.8) \times 0.2 \times 0.5 = 1.08 \ 1.016 \ \boxed{1.04}$

$SpeedUp = \dfrac{CPI_{without}}{CPI_{with}} = \dfrac{1.12}{1.016} = \boxed{1.102} \quad \dfrac{1.08}{1.04} = \boxed{1.038}$.

4.0

```
loop:        lw   $t3,  0($S1)          ⎫
             lw   $t4,  0($S2)          ⎬  Single loop without
             mul  $t1,  $t3, $t4        ⎪  iteration.
             add  $S0,  $t1, $S0        ⎭
             lw   $t3,  -8($S1)         ⎫
             lw   $t4,  -8($S2          ⎬  ~~first~~ loop body after
             mul  $t1,  $t3, $t4        ⎪  1st iteration
             add  $S0,  $t1, $S0        ⎭
             lw   $t3,  -16($S1)        ⎫
             lw   $t4,  -16($S2         ⎬  2nd '' iteration
             mul  $t1,  $t3, $t4        ⎪
             add  $S0,  $t1, $S0        ⎭
             lw   $t3,  -24, ($S1)      ⎫
             lw   $t4,  -24, ($S2)      ⎪  3rd  ''
             mul  $t1,  $t3,  $t4       ⎬
             add  $S0,  $t1,  $0        ⎭
             addi $S1,  $S1, 32         ⎫  Correct iterator
             addi $S2,  $S2, -32        ⎭
             beq  $S1,  $zero,  Loop
```

$t3 ∈ 10:12
$t4 ∈ 13:15
$t1 ∈ 20:22

Cycle		
1	lw $t3, 0($S1)	lw $10, -8($S1)
2	lw $11, -16($S1)	lw $12, -24($S1)
3	lw $t4, 0($S2)	lw $13, -8($S2)
4	lw $14, -16($S2)	lw $15, -24($S2)
5	mul $t1, $t3, $t4	mul $20, $10, $13
6	mul $21, $11, $14	mul $22, $12, $15.
7	add $S0, $t1, $S0	add $S0, $20, $S0
8	add $S0, $21, $S0	add $S0, $22, $S0.
9	addi $S1, 32	addi $Se, -32
10	beq $S1, $zero, loop	→ ⟨11 cycle⟩
11		
12		