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1.0)

1.0.1) variables i & j are repeatedly used.
Also, for each "i" iteration, ~~A[i][1]~~ A[i][1] is used for 8000 times
→ A[i][1] is a temporal locality

1.0.2
~~A[i][1] is exhibit exhibit spatial locality because~~
Since the elements are executed / stored in "Row Major Format",
B[i,j] exhibit spatial locality because B[i][j] and B[i][j+1] are ~~relatively~~ "close".
A[j][i] does not exhibit spatial locality because A[j][i] and A[j+1][
are not "close" because there is 8000 elements (j iteration) between those

2.0)

2.0.1) Cache capacity, $C = (\text{Number of Blocks}) \times (\text{Block size})$
$= (\text{Number of set}) \times (\text{Number of ways}) \times (\text{Block Size})$
$= \boxed{S \times N \times b \ (\text{words})}$
$= \boxed{4 S \times N \times b \ (\text{bytes})}$ (one word = 4 bytes)

2.0.2).
- In full associative, whole block in cache is considered as one set.
  → $S = 1$. Hence, word in the main memory can be saved in any block
- $C = \overset{1}{S} \times N \times b = Nb$
  → $\boxed{N = C/b}$

3.0)
3.0.1)

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3.0.1) Block size = 1 word
Blocks = 16 Blocks.

3.~~0.2~~) # Offset bit = $\log_2$ (# words in a block) = $\log_2 1$ = 0 offset bit
Index bit = $\log_2$ (# Blocks) = $\log_2 16$ = 4 Index bit
Tag bit = 28-bit remaining (MSB).

Address	Tag (28-MSB).	Index (4 LSB).	Data ~~Hit/Miss~~	Hit/Mi
0x0000 0074	0x0000 007	0x4	M[0x74]	Miss
0x000000A0	0x0000 00A	0x0	M[0xA0]	Miss
0x0000 0078	0x0000 007	0x8	M[0x78]	Miss
0x0000038C	0x0000 038	0xC	M[0x38C]	Miss
0x0000 00AC	0x0000 00A	0xC	M[0xAC]	Miss
0x0000 0084	0x0000 008	0x4	M[0x84].	Miss
0x00000088	0x0000 008	0x8	M[0x88]	Miss
0x0000008C	0x0000 008	0xC	M[0x8C]	Miss
0x0000007C	0x0000 007	0xC	M[0x7C]	Mis
0x0000 0034	0x0000 003	0x4	M[0x34]	Miss
0x0000 0038	0x0000 003	0x8	M[0x38]	Mis
0x0000 013C	0x0000 013	0xC	M[0x13C]	Mis
0x00000388	0x0000 038	0x8	M[0x388]	Mis
0x0000 018C	0x0000 018.	0xC	M[0x18C]	Mis

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3.0.2 ~~Offset bit~~ Block Size = 2 word
#Blocks = 32 Blocks

Offset bit = $\log_2(\text{\# words in a block}) = \log_2 2 = 1$ offset bit
Index bit = $\log_2(\text{\#Blocks}) = \log_2 32 = 5$ index bit
Tag bit = 26 - bit remaining {MSB}

Address (Hex/Binary)	Tag	Index	Data	Miss /Hit.
0x74 /...0000 0111 0100	...0000 001	11010	M[0x74]	Miss
0x A0 /...0000 1010 0000	...000010	10000	M[0xA0]	Miss
0x 78 /...0000 0111 1000	...000001	11100	M[0x78]	Miss
0x38C /...0011 1000 1100	...001110	00110	M[0x38C]	Miss
0x AC /...0000 1010 1100	...000010	10110	M[0xAC]	Miss
0x 84 /...0000 1000 0100	...000010	00010	M[0x84].	Miss
0x 88 /...0000 1000 1000	...000010	00100	M[0x88]	Miss
0x 8C /...0000 1000 1100	...000010	00110	M[0x8C].	Miss
0x 7C /...0000 0111 1100	...000001	11110	M[0x7C].	Miss
0x 34 /...0000 0011 0100	...000000	11010	M[0x34]	Miss
0x 38 /...0000 0011 1000	...000000	11100	M[0x38].	Miss
0x 13C /...0001 0011 1100	000100	11110	M[0x13C].	Miss
0x 388 /...0011 1000 1000	...001110	00100	M[0x388]	Miss
0x 18C /...0001 1000 1100	...000110	00110	M[0x18C].	Miss

Index offset

Tag

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4.0.1, $t_{cache} = {}^{1cycle}/_{2.5GHz} = 0.4ns$

~~4.0.1~~.

AMAT, Average memory access time $= 0.4 + 0.07 \times 45ns = \boxed{\cancel{4.45 (ns)}}\ \boxed{3.55ns}$

4.0.2

~~The average CPI for bench mark =~~

Non-ideal memory system:

load instruction requires 4ns for memory access and 4ns for load

→ 8 ns for load

$CPI_{load} = (4 \underset{mem}{\overset{cycle}{\cancel{ns}}} + \underset{load}{\overset{4\ cycle}{\cancel{4ns}}}) = 8$ cycle

$CPI_{store} = (\underset{mem\ \cancel{acc}}{4\ cycle} + \underset{store.}{3\ cycle}) = 7$ cycles

$CPI_{branch} = 3$ cycles.

$CPI\ data = 4$ cycles.

→ Average CPI for bench mark $= (0.25 \times 8) + (0.15 \times 7) + (0.1 \times 3) + (0.5 \times 4)$
$= \boxed{5.35ns}$

4.0.3

Average $CPI_{bench\ mark} = 5.35ns + (0.03 \times 45ns) = \boxed{6.7ns}$