

DisplayPort 1.4 Link Layer Compliance

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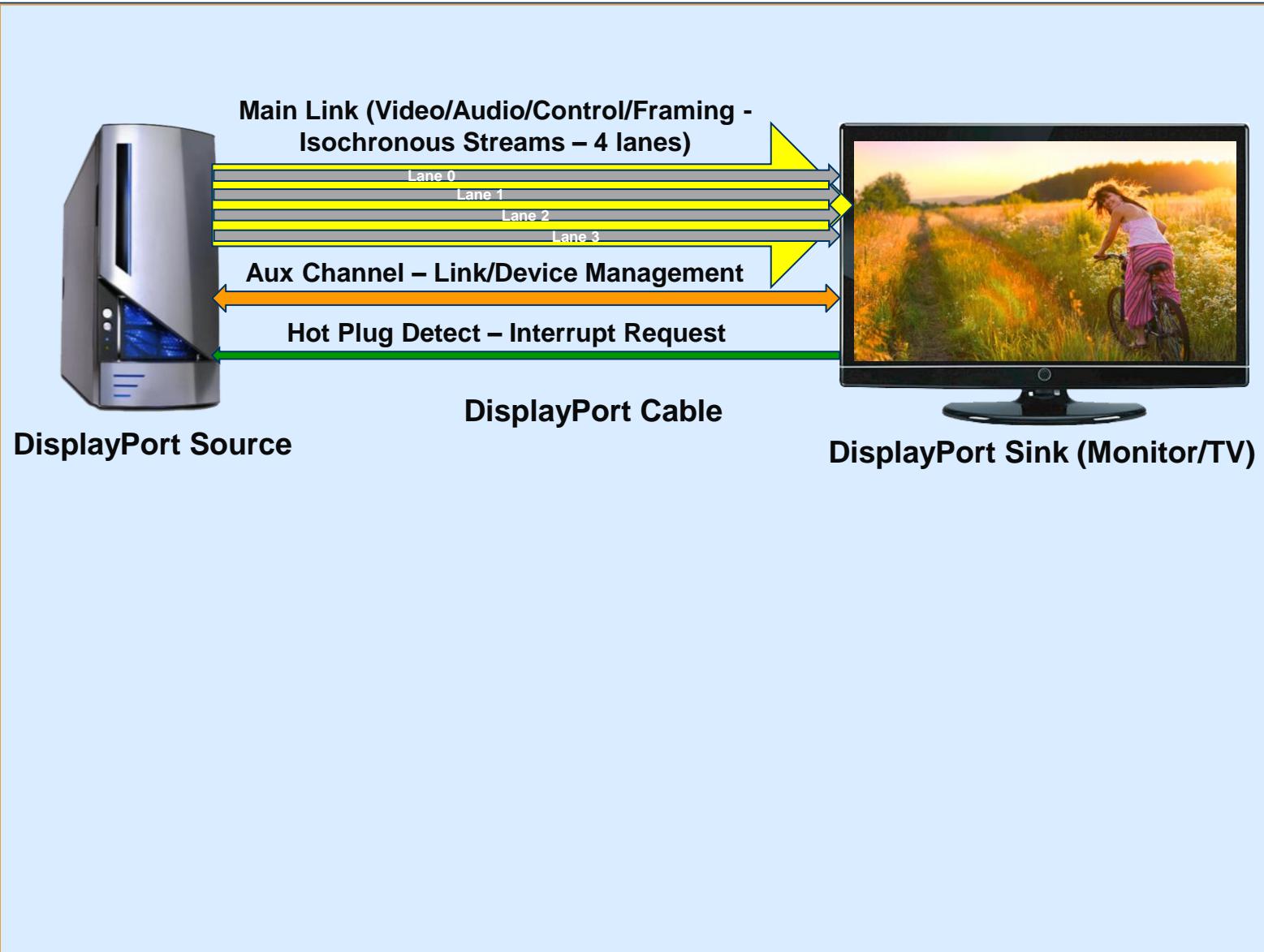


Agenda

- ◆ DisplayPort 1.4 Source Link Layer Compliance Test samples (4 sample tests)
- ◆ DisplayPort 1.4 Sink Link Layer Compliance Test samples (3 sample tests)

- ◆ Please Check out our DisplayPort “Essentials of” Webinars:
 - ◆ [Essentials of DisplayPort Protocols](#)
 - ◆ [Essentials of HDCP 2.2 Protocols](#)
 - ◆ [Essentials of DisplayPort Display Stream \(DSC\) Protocols](#)

DisplayPort Anatomy



- **Main Link:** Unidirectional, high-bandwidth channel used to transport video, audio and metadata and protocol control elements.
- Main Link 1, 2 or 4 Lane Configurations.
- Main Link 4 link rates:
 - 1.62Gbps (Reduced Bit Rate)
 - 2.7Gbps (High Bit Rate)
 - 5.4Gbps (High Bit Rate 2)
 - 8.1Gbps (High Bit Rate 3)
- **No clock channel.** Sink recovers clock using link transitions. Pixel clock recovered from the link symbol clock using Mvid/Nvid in the MSA.
- **Aux Channel:** Bidirectional, half duplex channel with a data rate of 1Mbps. Link Training, DPCD Register status, HDCP authentication & EDID.
- No separate clock for aux channel.
- Hot plug lead:
 - Connection Detection.
 - Interrupt mechanism with link failure.

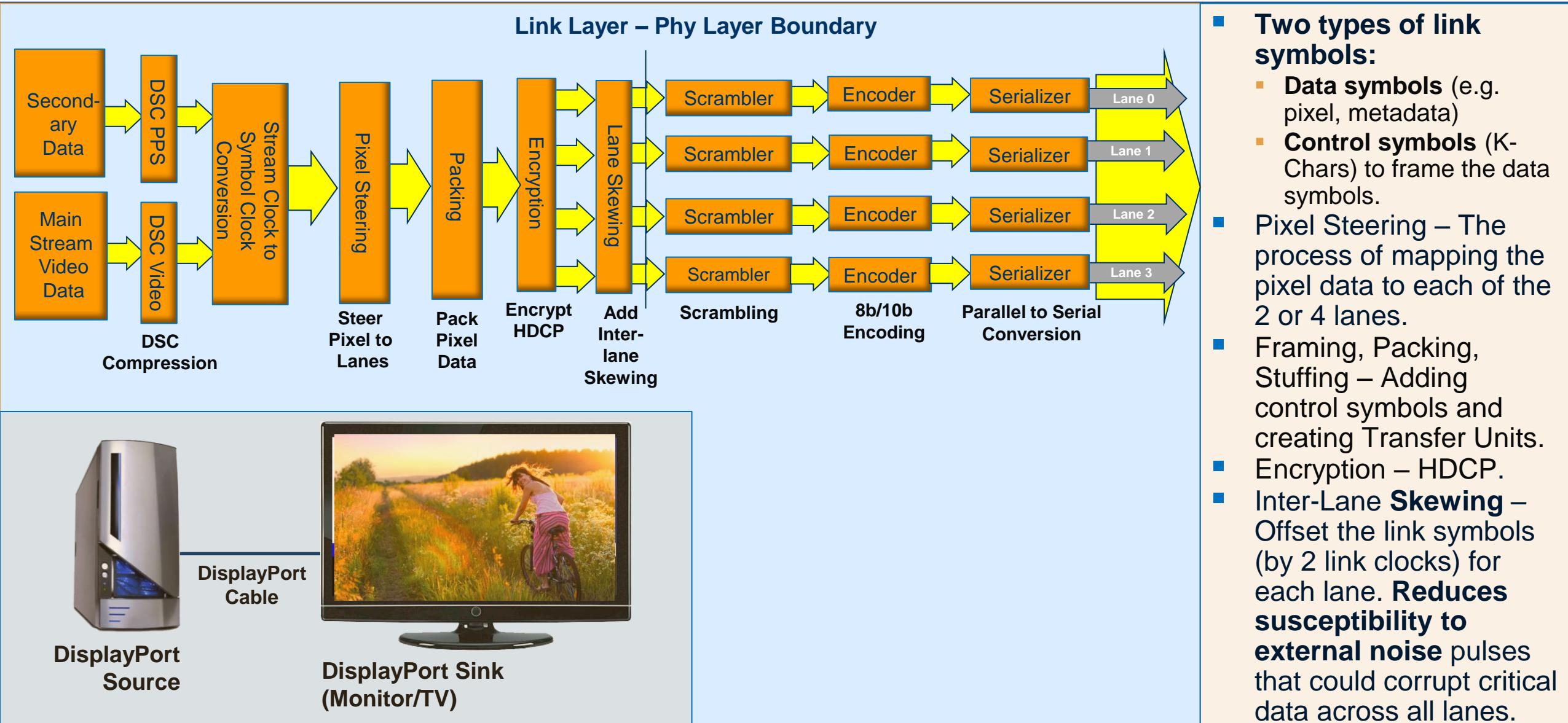
DisplayPort Main Link Protocol – One Video Frame



- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period.
- There is a lot of **over capacity**. **Fill characters** are zeros for filling up (stuffing) the unused link symbols.

Video	Fill Characters
Metadata	Control Symbols
Audio	Control VBID w/ Compression
PPS	EoC

DisplayPort Main Link Stream Generation – Packing and Stuffing



Display Port Connection Sequence – EDID, DPCD Link Training, HDCP, DSC



- Hot Plug. Indication to the Source that there is a Display device connect to it.
- EDID read. EDID is a data structure provided by a DisplayPort display that describe its capabilities to a DisplayPort video source.
- DPCD read. DPCD is a data structure provided by a DisplayPort device that describe its link & DSC capabilities to a DisplayPort source.
- Link Training. Link training establishes the physical link parameters (number of lanes, link rate, voltage swing, pre-emphasis, equalization) used for transmission of video and audio over the main link.
- Link Training has two phases:
 - Clock Recovery and
 - Channel Equalization which includes Symbol Lock and Inter-Lane alignment.
- If the video/audio content is flagged for content protection, the High-bandwidth Digital Content Protection (HDCP) authentication protocol is used.
- Compressed, encrypted video transmission is initiated. Picture Parameter (PPS) metadata is transmitted, VB-ID compressed flag is set.

Source Link Layer Compliance Tests



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Emulating DisplayPort Sink to Run Link Layer Source Compliance Tests

DisplayPort Source



DisplayPort Cable



DisplayPort 1.4 Reference Sink
Example: Teledyne LeCroy
quantumdata 980 Test Platform
with DP 1.4 Video Generator /
Protocol Analyzer

Filling Out the Capabilities Declaration Form (CDF)

Entering the CDF Information – General

DP 1.4 Source CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Open New Save CDF File: <not saved>

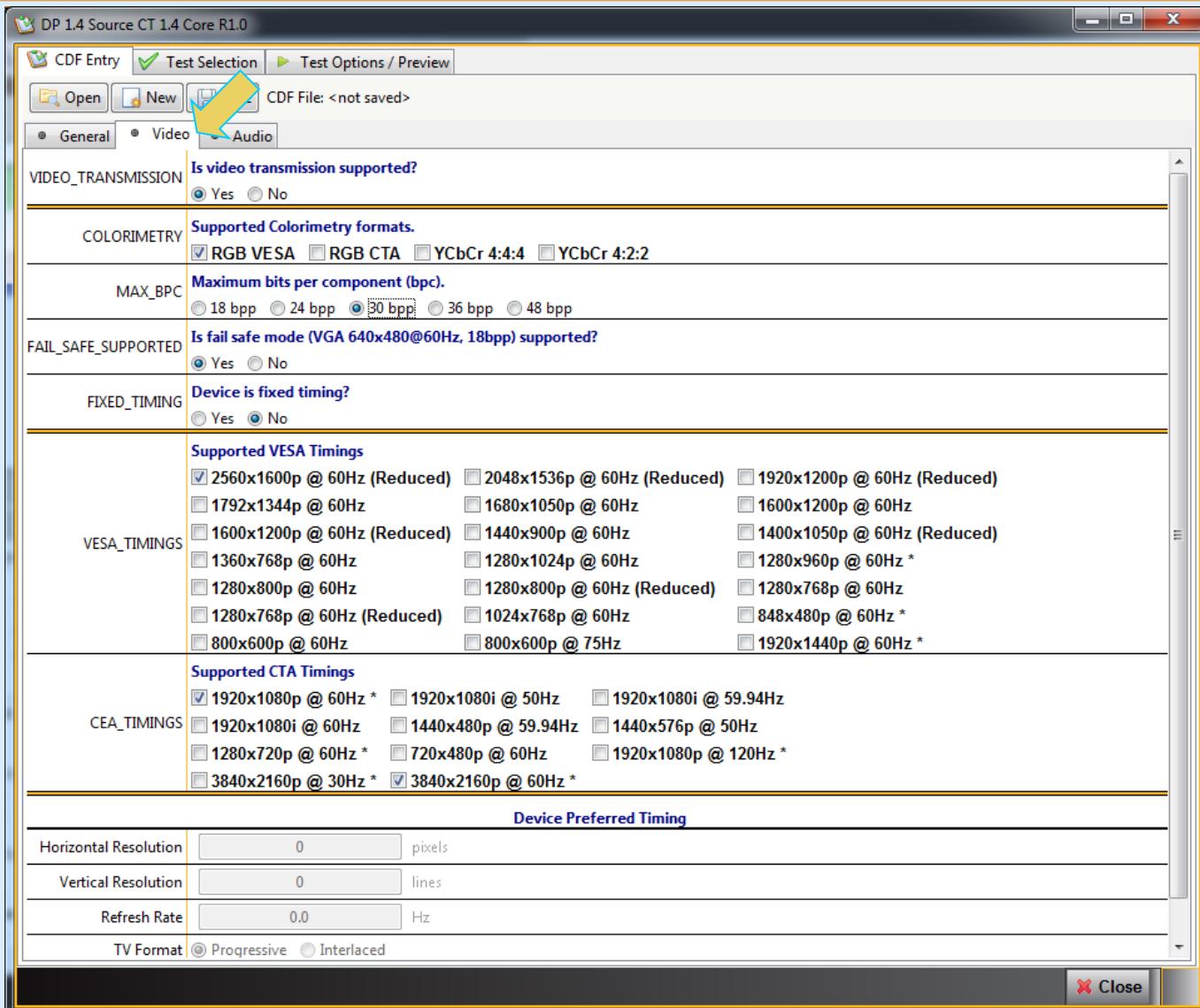
General Video Audio

Manufacturer	What is the product manufacturer's name? ACME
Model	What is the model name/number of the product? XYZ
Port_Tested	What port is being tested? 1
MAX_LANE_COUNT	What is the maximum lane count supported? <input type="radio"/> 1 <input type="radio"/> 2 <input checked="" type="radio"/> 4
MAX_LINK_RATE	What is the maximum link rate supported? <input type="radio"/> 1.62 (RBR) <input type="radio"/> 2.70 (HBR) <input type="radio"/> 5.40 (HBR2) <input checked="" type="radio"/> 8.10 (HBR3)
DRIVE_LEVEL3_SUPPORTED	Is drive level 3 (1.2V) supported? <input checked="" type="radio"/> Yes <input type="radio"/> No
PREEMP_LEVEL3_SUPPORTED	Is pre-emphasis level 3 (9.5dB) supported? <input checked="" type="radio"/> Yes <input type="radio"/> No
DEVICE_READY_INDICATOR	How does this device indicate it is ready to accept test requests? <input type="radio"/> (1) No event required. <input type="radio"/> (2) Completion of EDID read. <input type="radio"/> (3) End of link training (write of TRAINING_PATTERN_SET to 00b) <input checked="" type="radio"/> (4) Start of video stream (default)
SPRD_SPEC_CLK	Is spread spectrum clocking supported? <input checked="" type="radio"/> Yes <input type="radio"/> No
V_FMT_CHNG_NO_RETRAIN	Is video format change without link re-training supported? <input type="radio"/> Yes <input checked="" type="radio"/> No
LC_RED_NO_RETRAIN	Is lane count reduction without re-training supported? <input type="radio"/> Yes <input checked="" type="radio"/> No
TEST_DELAY	Time to wait between tests 0 seconds

Close

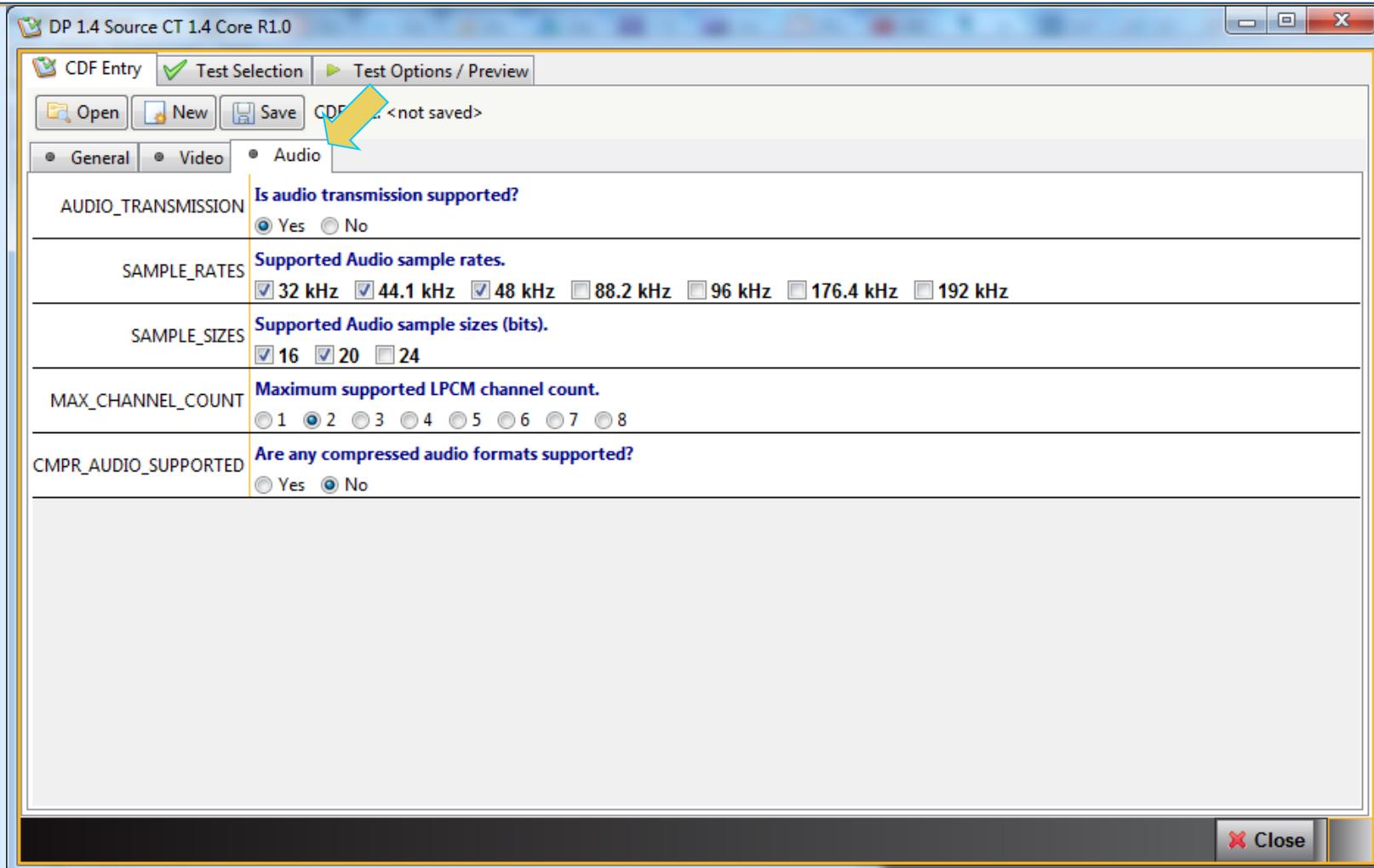
- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF is used by the reference sink to know which Link Layer related source features to test.
- There are three (3) tabs:
 - General Tab - Describes the link capabilities of the source device.
 - Video – Described in next slide(s).
 - Audio – Described in next slide(s).

Entering the CDF Information – Source Video Parameters



- Video – Described video capabilities of the source device.

Connection Sequence – Link Layer Compliance Tests



- Audio – Described audio capabilities of the source device.

Source Link Layer Compliance

List of Current Tests

Source Link Layer Compliance Tests – List of Current Tests

DP 1.4 Source CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

All Execute Tests Cards...

Category / Test Name

Link Training

- 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.
- 4.3.1.2: Successful Link Training Upon HPD Plug Event.
- 4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.
- 4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence.
- 4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence.
- 4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).
- 4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & Channel Equalization

Link Maint.

- 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.
- 4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.
- 4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock.
- 4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.
- 4.3.2.5: Lane Count Reduction and Increase.

Video

- 4.3.3.1: Video Time Stamp Generation

Audio

- 4.4.4.3: Audio Time Stamp Generation

Link Training (1.4)

- 400.1.1: Source Device HPD Event Pulse Length Test
- 400.1.2: Source Device IRQ HPD Pulse Length Test
- 400.1.3: Source Device Inactive HPD / Inactive AUX Test
- 400.2.1: Source Device Link Training CR Fallback Test
- 400.2.2: Source Device Link Training EQ Fallback Test

Close

Source Link Layer Compliance – Test 4.3.1.1 Successful Link Training

Compliance Test Results Viewer
DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 03_27_2018_15_01_26 Manufacturer:
Date Tested: March 27, 2018 3:01 PM Model Name:
Overall Status: CTS 1.4 Core R1.0 - Fail Port Tested: 1 [HTML Report](#)

Test Name / Details

4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Iter 01:

- 01: [1] Link Training test for lane count = 1 and lane rate = 1.62
- 02: [2] Link Training test for lane count = 2 and lane rate = 1.62
- 03: [3] Link Training test for lane count = 4 and lane rate = 1.62
- 04: [4] Link Training test for lane count = 1 and lane rate = 2.70
- 05: [5] Link Training test for lane count = 2 and lane rate = 2.70
- 06: [6] Link Training test for lane count = 4 and lane rate = 2.70
- 07: [7] Link Training test for lane count = 1 and lane rate = 5.40
- 08: [8] Link Training test for lane count = 2 and lane rate = 5.40
- 09: [9] Link Training test for lane count = 4 and lane rate = 5.40
- 10: [10] Link Training test for lane count = 1 and lane rate = 8.10
- 11: [11] Link Training test for lane count = 2 and lane rate = 8.10
- 12: [12] Link Training test for lane count = 4 and lane rate = 8.10

Source DUT start link training..
Source DUT sets link bw and lane count before TP1 is set.
Source DUT sets same link bw for link rate under test.
Source DUT sets correct lane count for lane count under test.
Source DUT sets TP1 on all active lanes.
Source DUT starts with voltage swing 0 on all active lanes.
Source DUT starts with pre-emphasis 0 on all active lanes.
CR Lock succeeded on all active lanes.
Training pattern 2 or 3 or 4 detected after Training pattern 1.
For HBR3 source Training pattern 4 detected.
Equalization succeeded on all active lanes.
Symbol lock succeeded on all active lanes.
All Lanes are Aligned and skewed.
Link compliance training test completed successfully.

Link training completed in 20.00 ms, which exceeds the 10ms guideline.

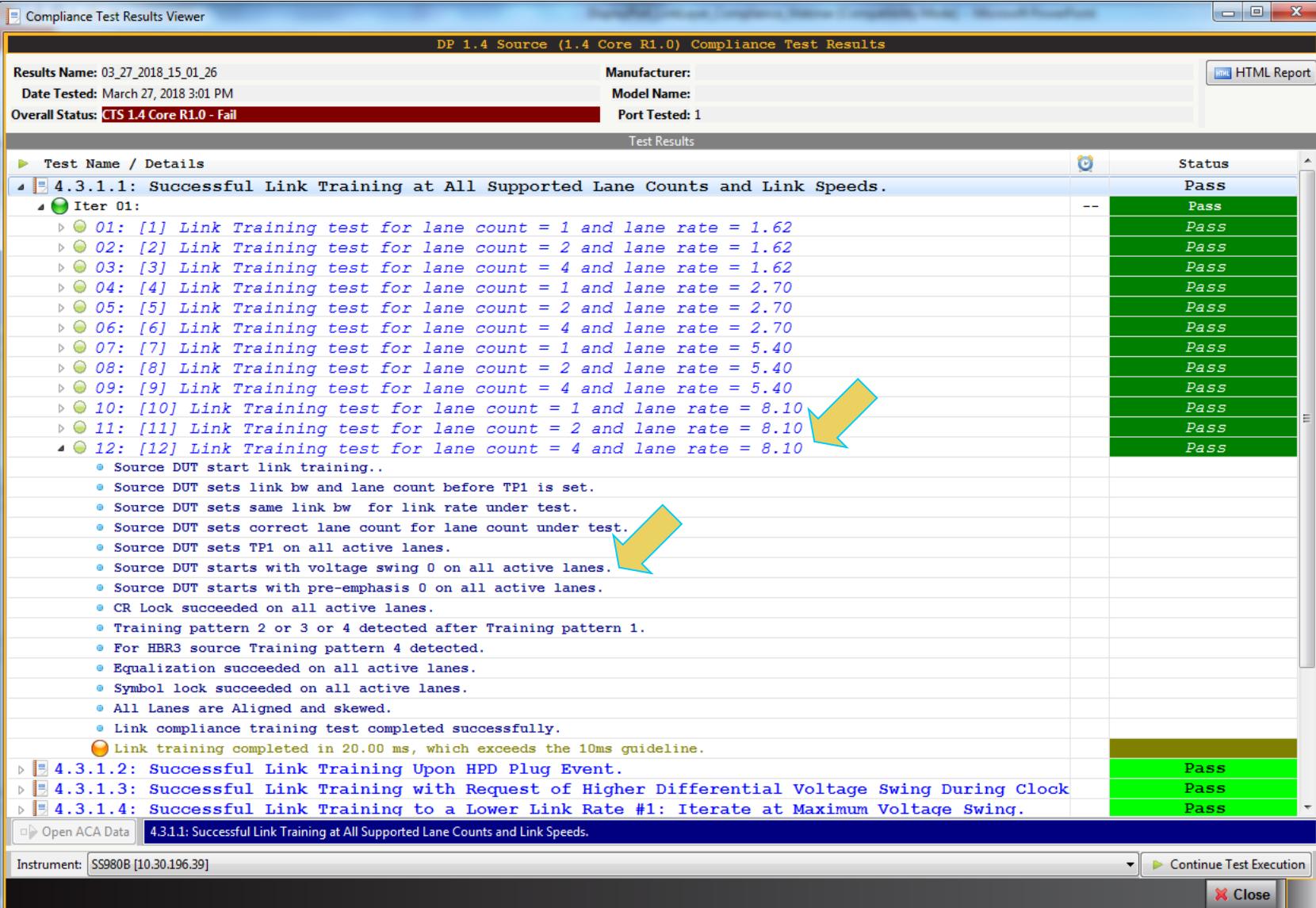
4.3.1.2: Successful Link Training Upon HPD Plug Event.

4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock

4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.

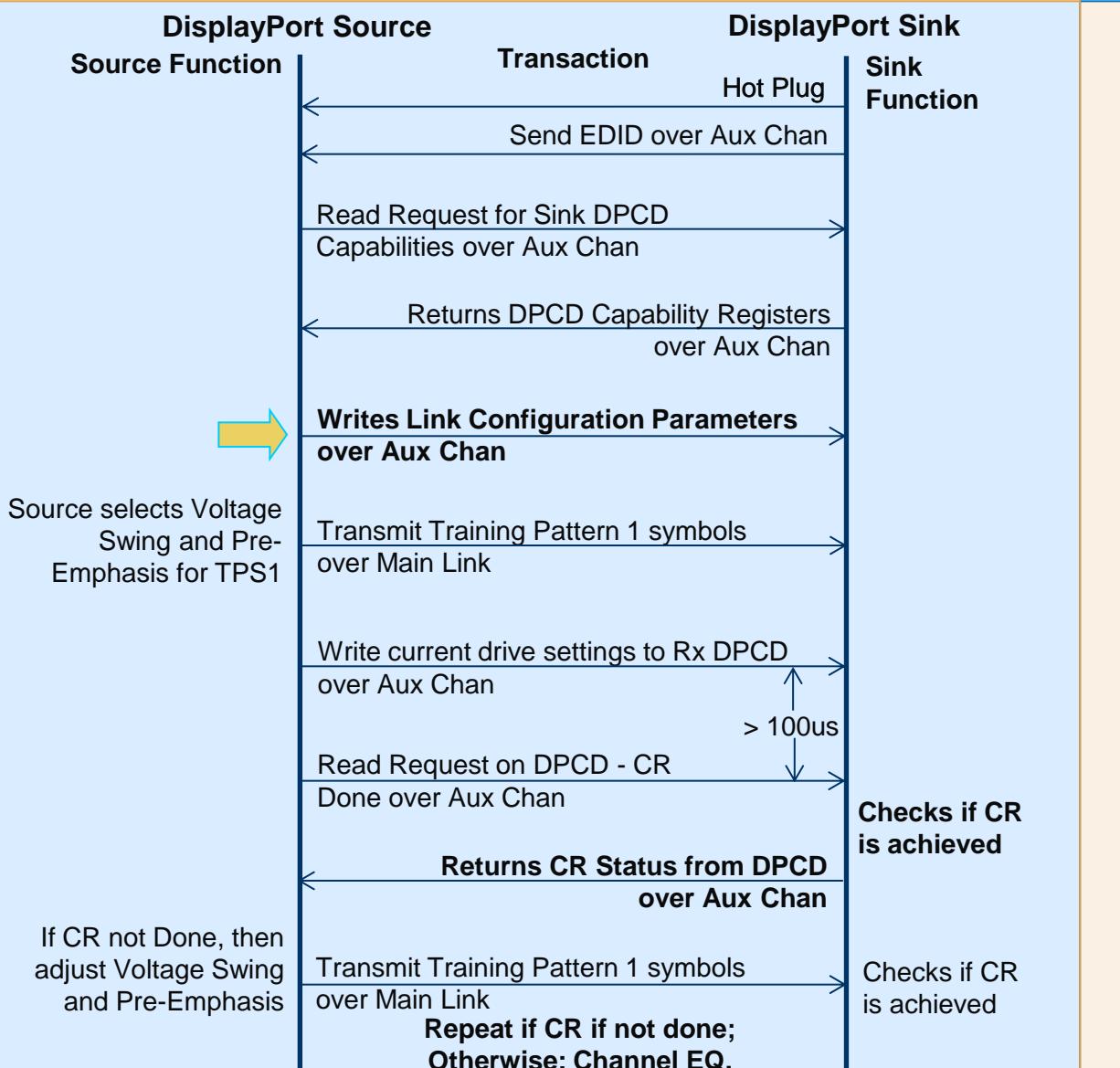
[Open ACA Data](#) 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Instrument: SS980B [10.30.196.39] Continue Test Execution Close



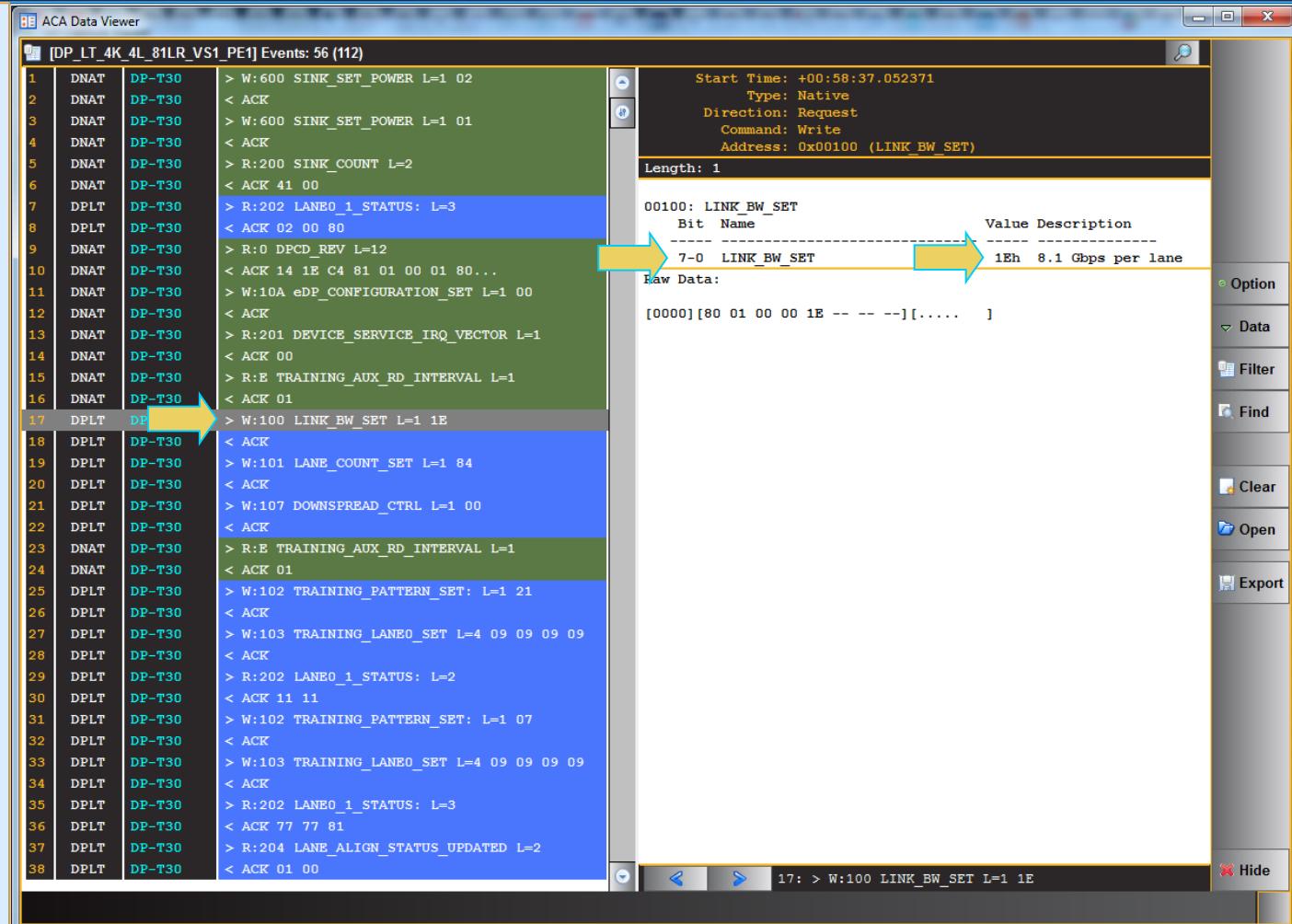
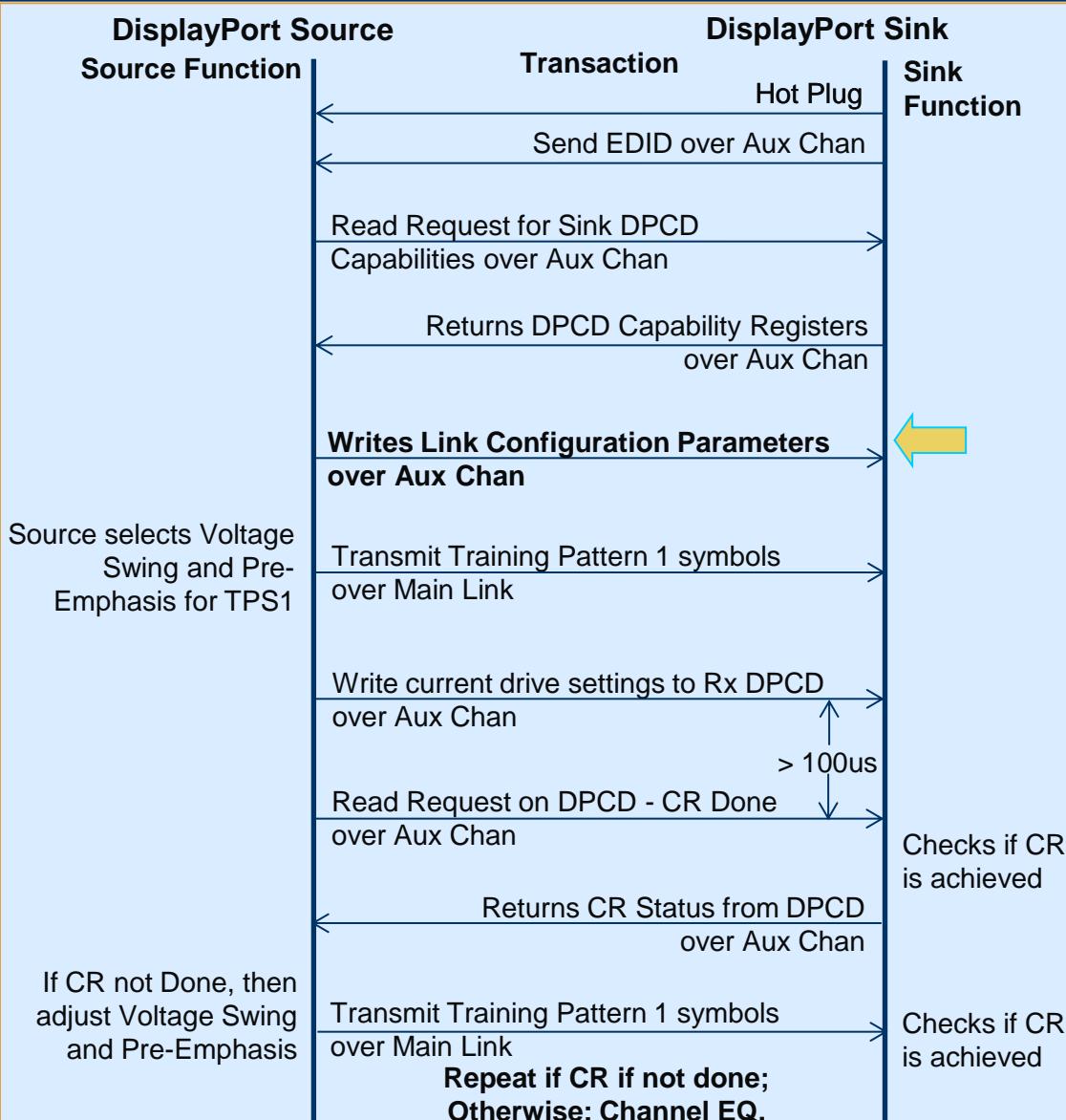
- ◆ Example shows sample test results.
- ◆ Shows details of subtest 12 for link training at 8.1 Gb/s link rate on four (4) lanes.

Connection Sequence – Link Training Clock Recovery Sequence



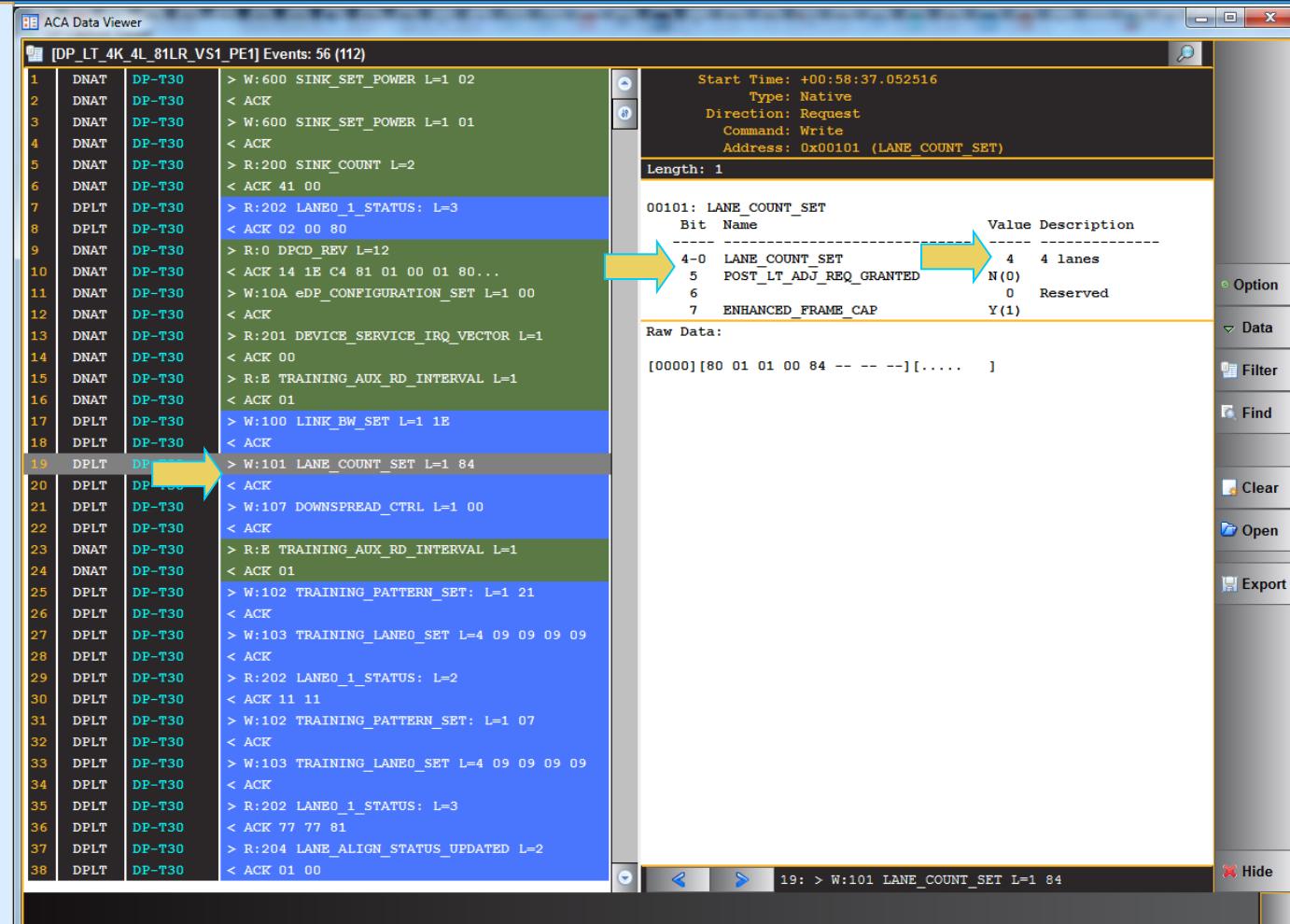
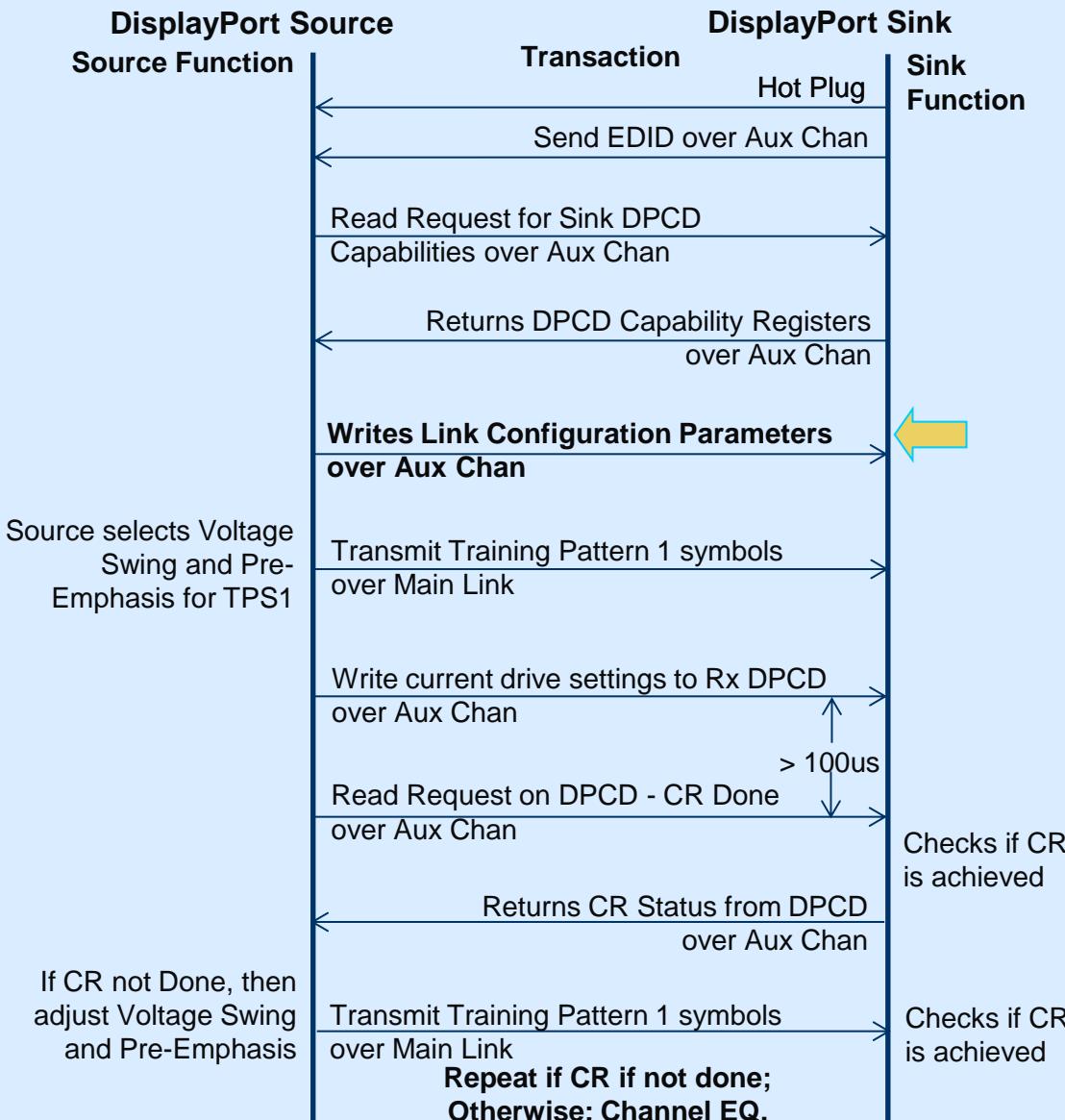
- Clock Recover needed because DisplayPort, like most high speed serial interfaces, **does not have a separate clock channel**—the clock is derived from the bit stream.
- Receiver needs a reference clock of its own at approximately the same frequency.
- Very difficult to have two clocks—one on the transmitter and one on the receiver—that have the same clock frequency.
- Receiver has to align its clock to the edge transitions** of the incoming data stream using a PLL.
- An unscrambled **special sequence of bits** has to be used (“training sequence”) to optimize edge sampling for clock alignment.
- Clock recover begins with the following settings:
 - Lowest drive levels, i.e. voltage swing and pre-emphasis (unless embedded applications).
 - Maximum Link Rate supported, typically HBR2 5.4Gb/s/lane or HBR3 at 8.1Gb/s/lane.
 - Maximum number of lanes supported, typically 2 or 4.

Connection Sequence – Link Training Clock Recovery Sequence



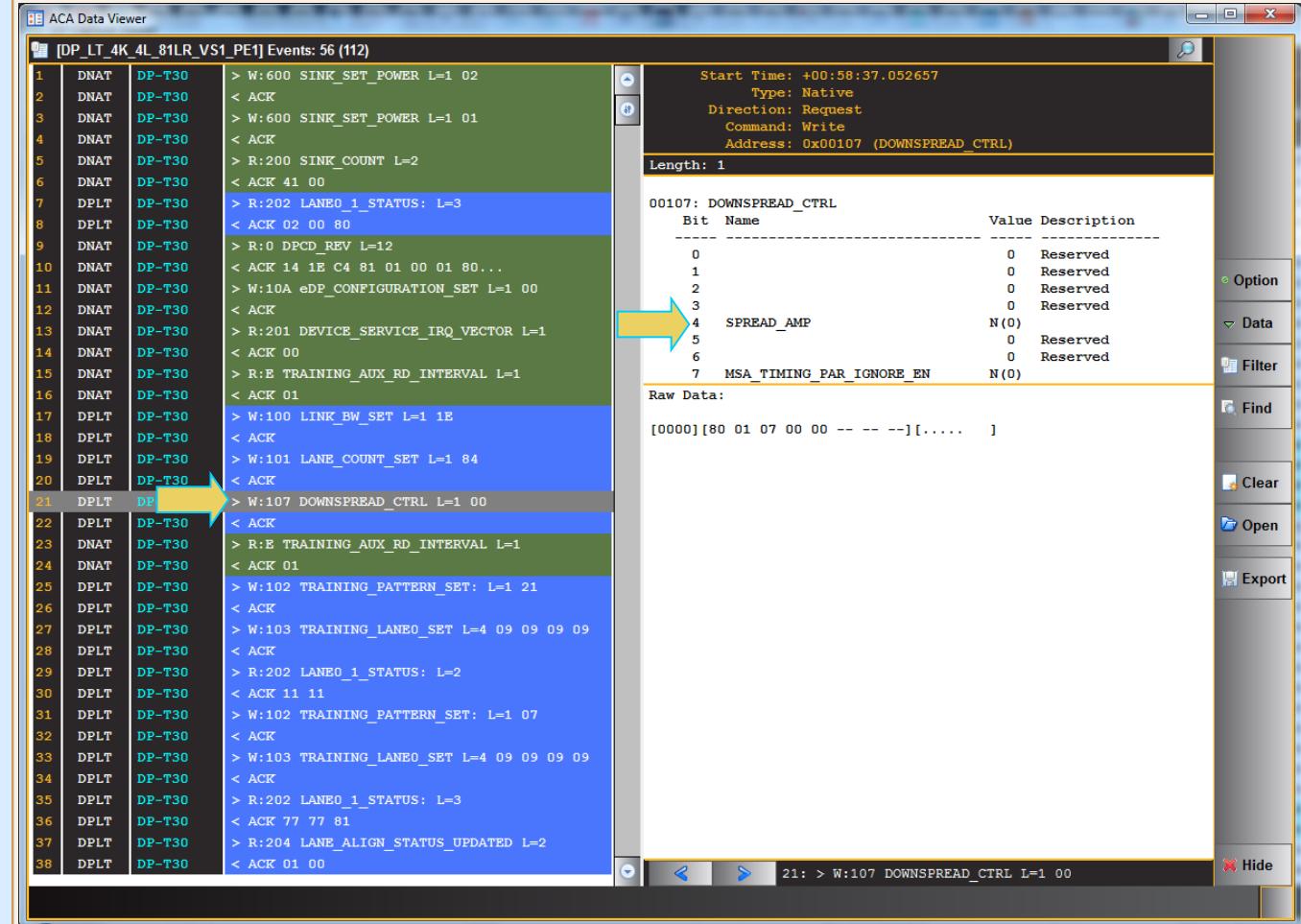
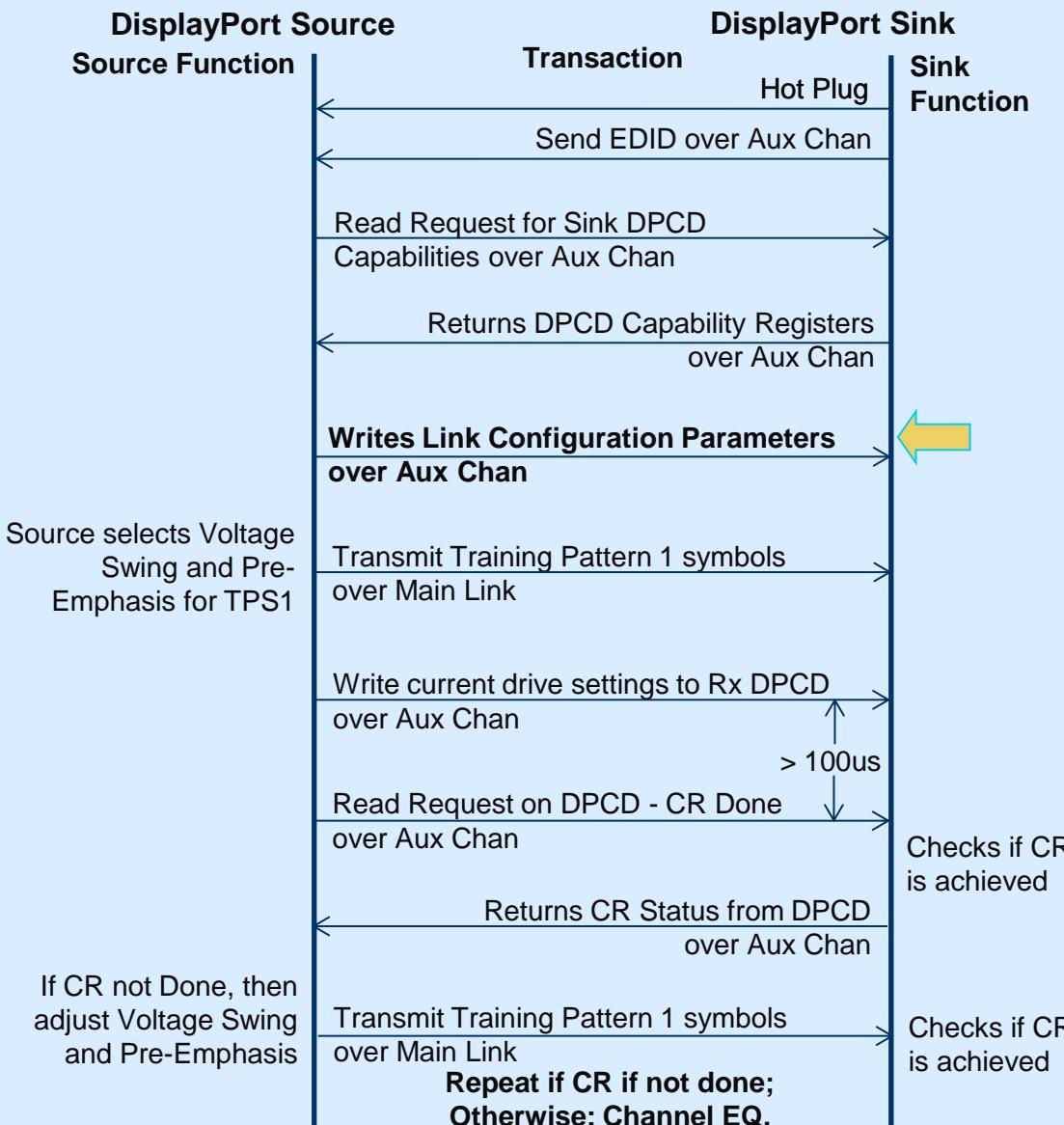
- ◆ Source Writing Link Rate (8.1Gbps) to Sink DPCD Registers to Begin Link Training

Connection Sequence – Link Training Clock Recovery Sequence



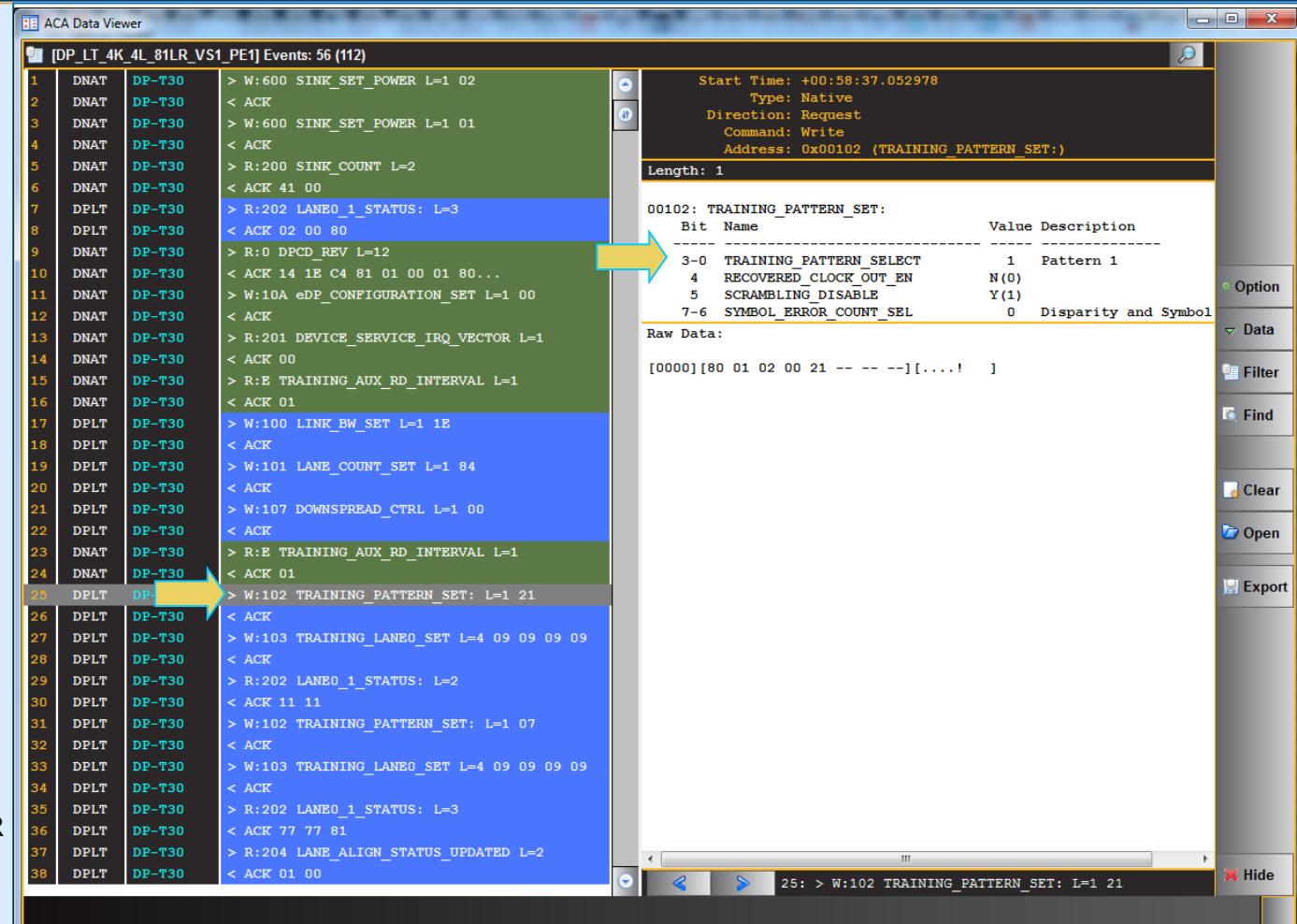
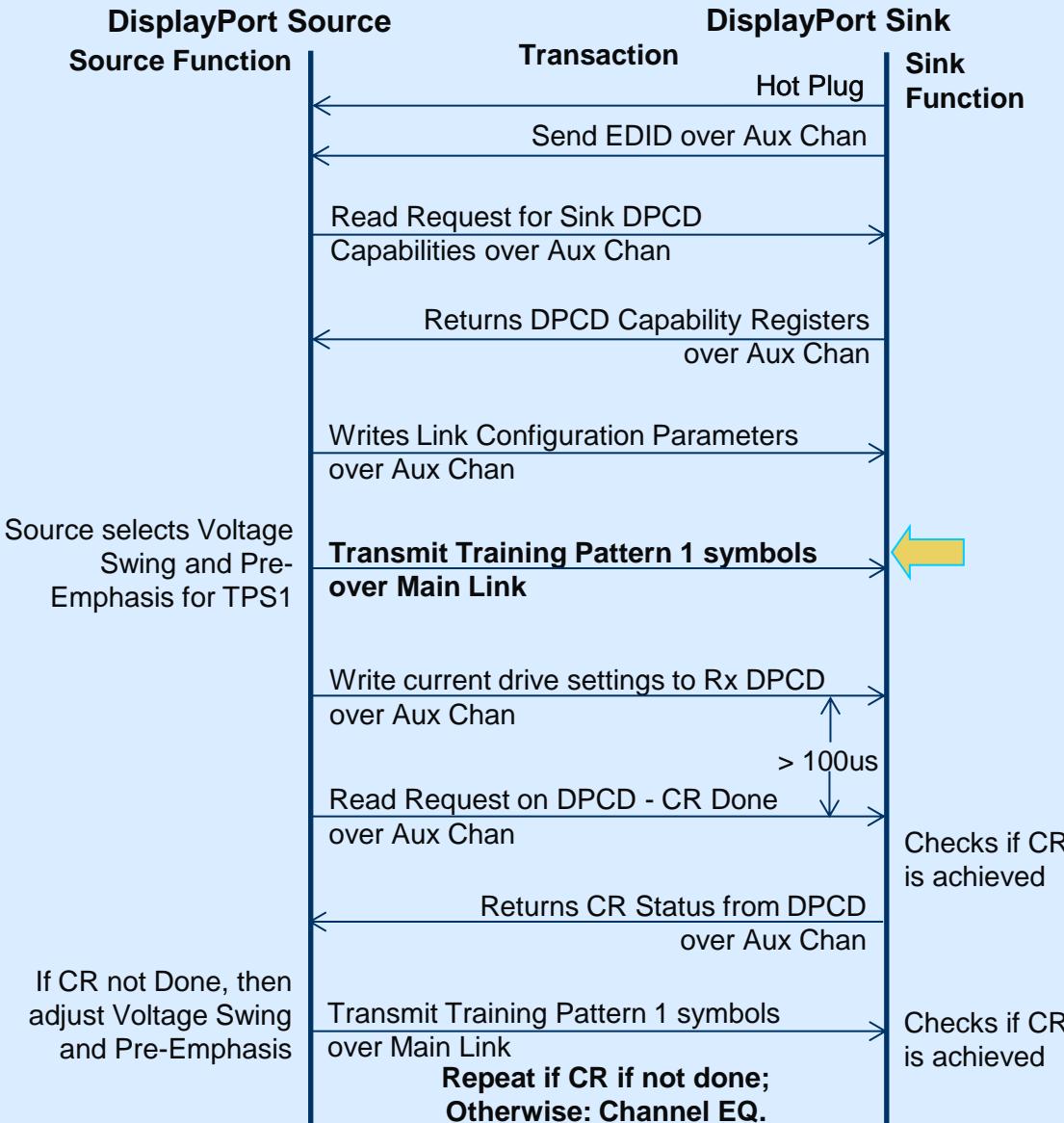
- ◆ Source Writing Lane Count to Sink DPCD Registers to Begin Link Training

Connection Sequence – Link Training Clock Recovery Sequence



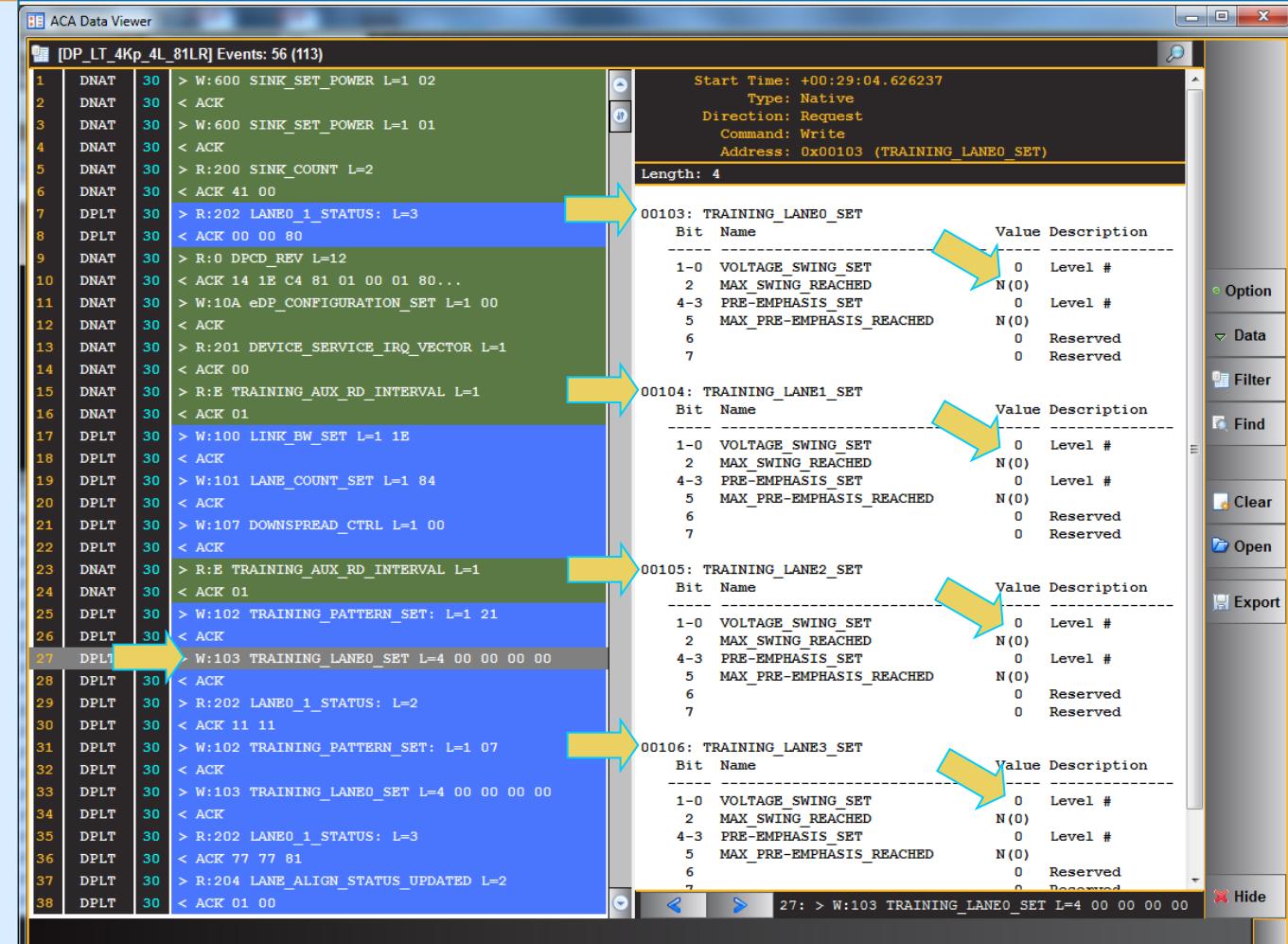
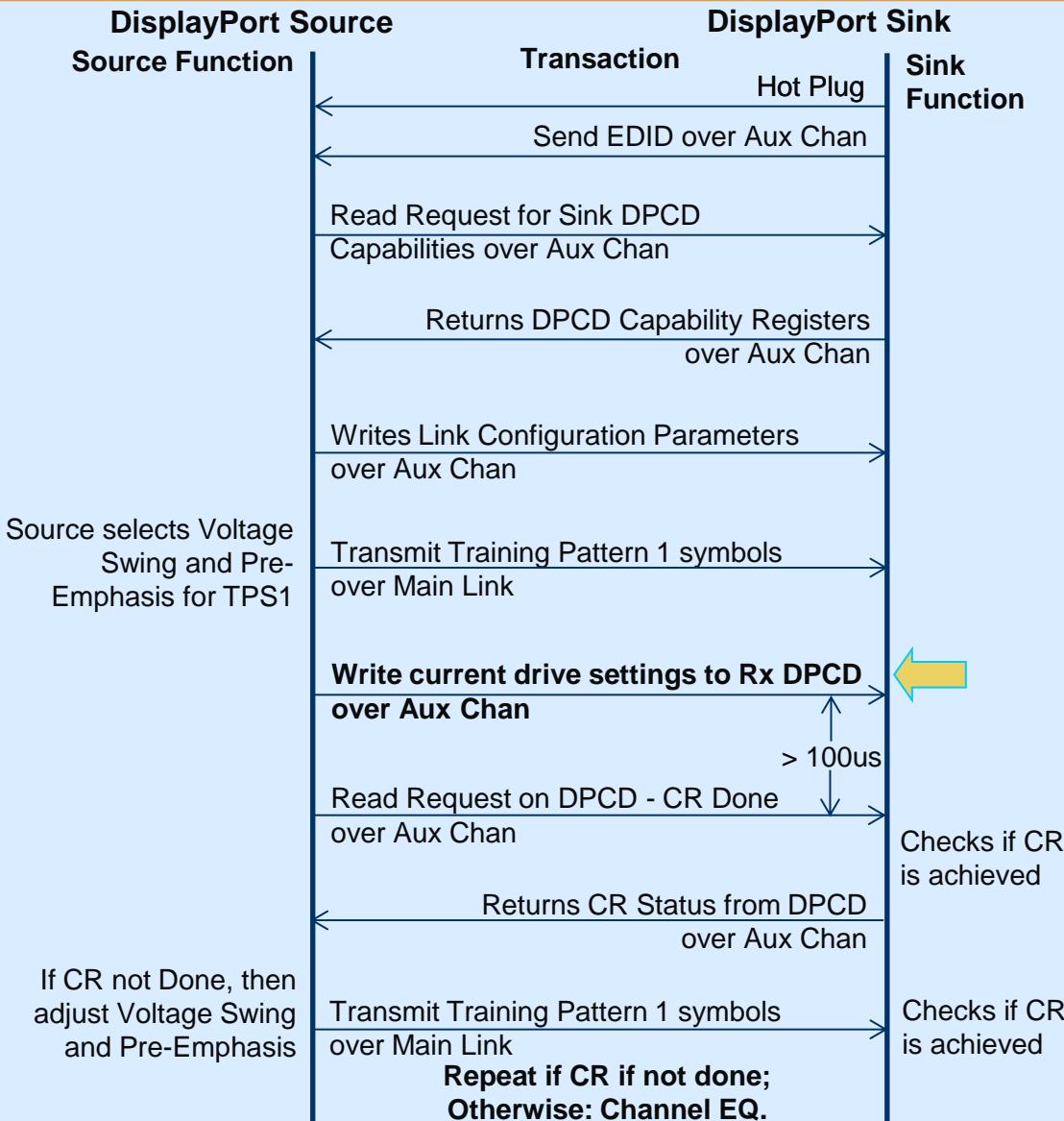
- Source writes Downspread control indication.
- Downspreading or “spread spectrum” is used to **reduce EMI** by reducing the amplitude of a single fundamental frequency and its harmonics across a wider spectrum.

Connection Sequence – Link Training Clock Recovery Sequence



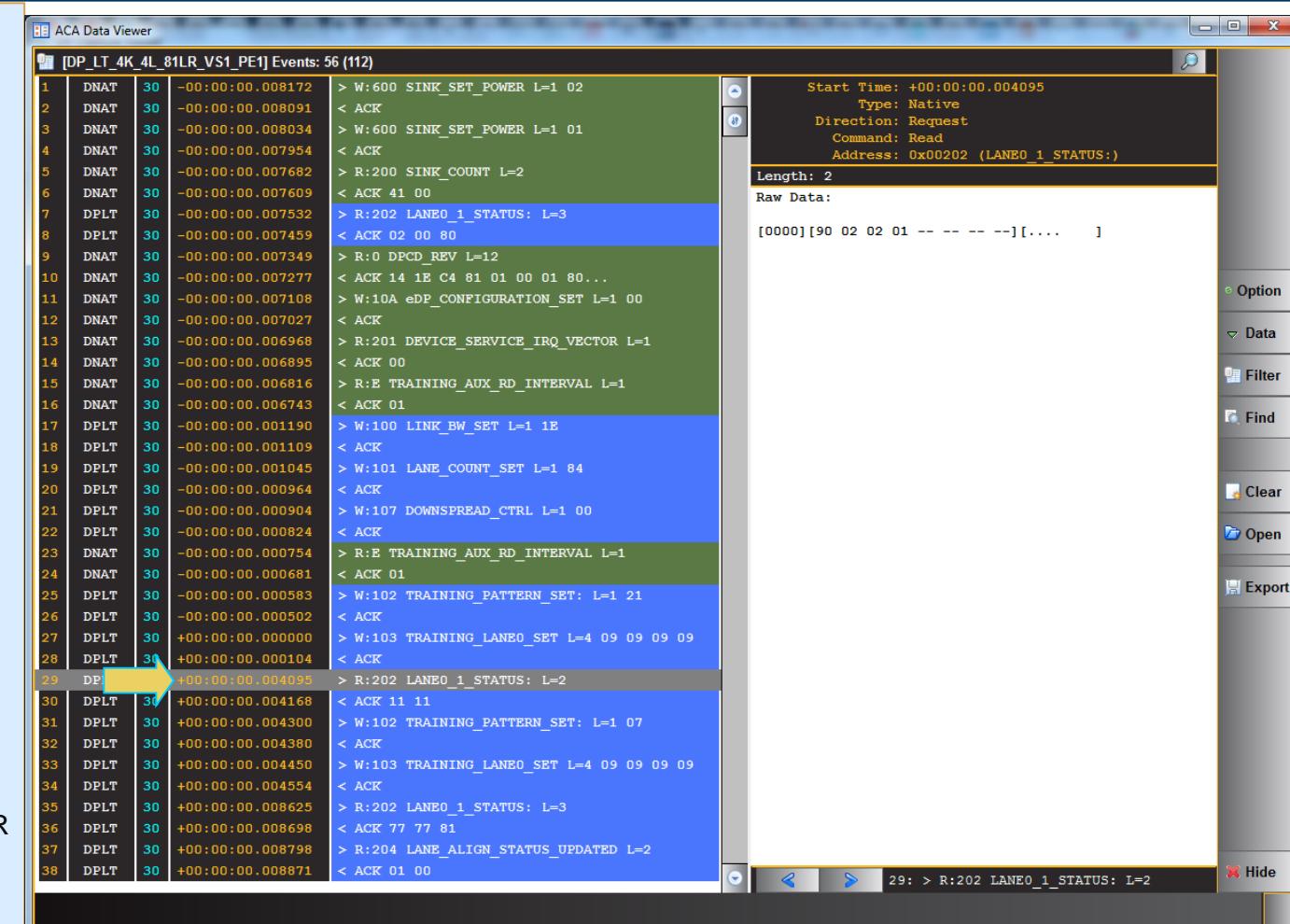
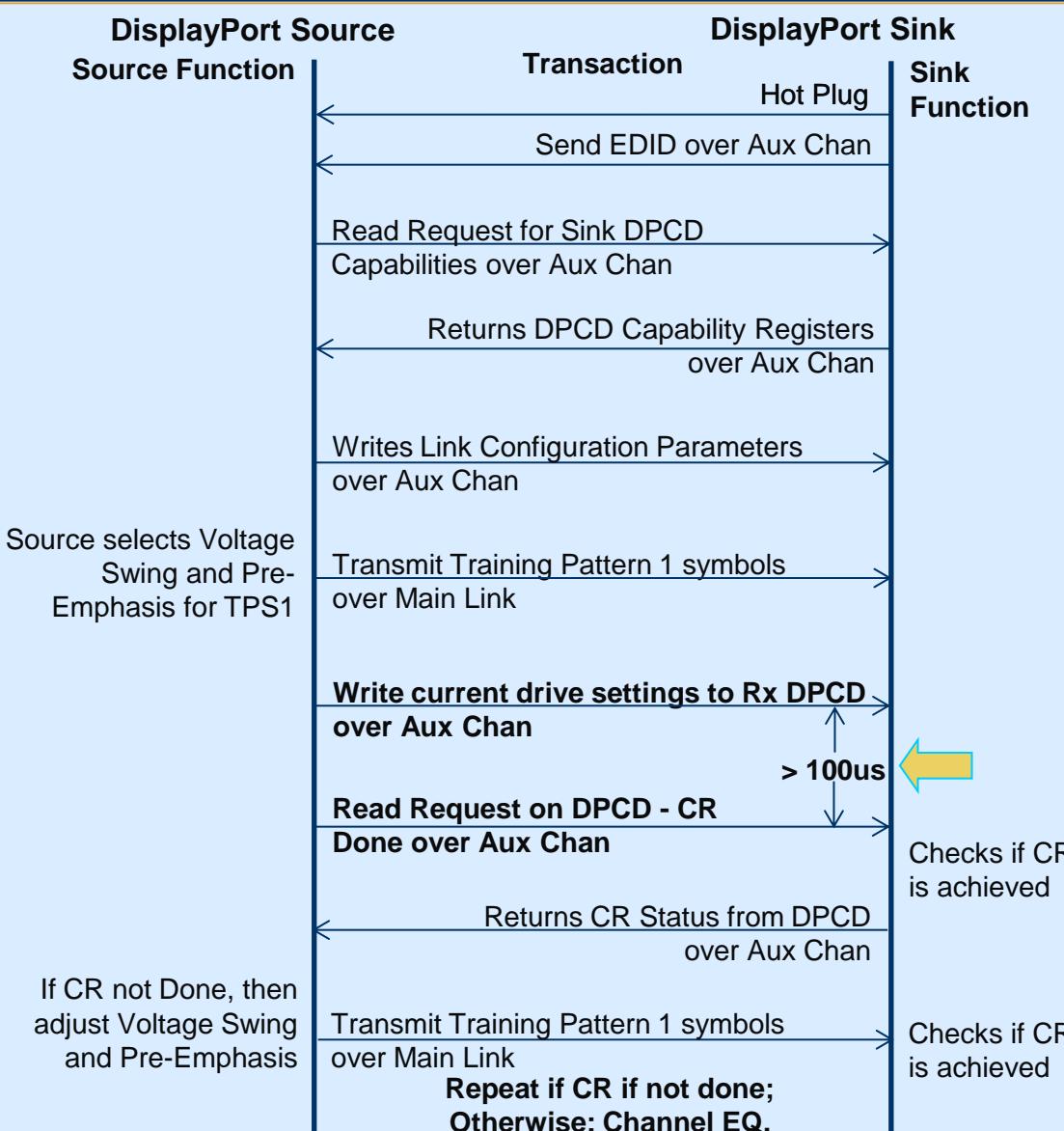
- Source Writing Training Pattern Set 1 (unscrambled) to Sink DPCD Registers.
- Training Pattern 1 is used in Link Training for Clock Recovery.

Connection Sequence – Link Training Clock Recovery Sequence



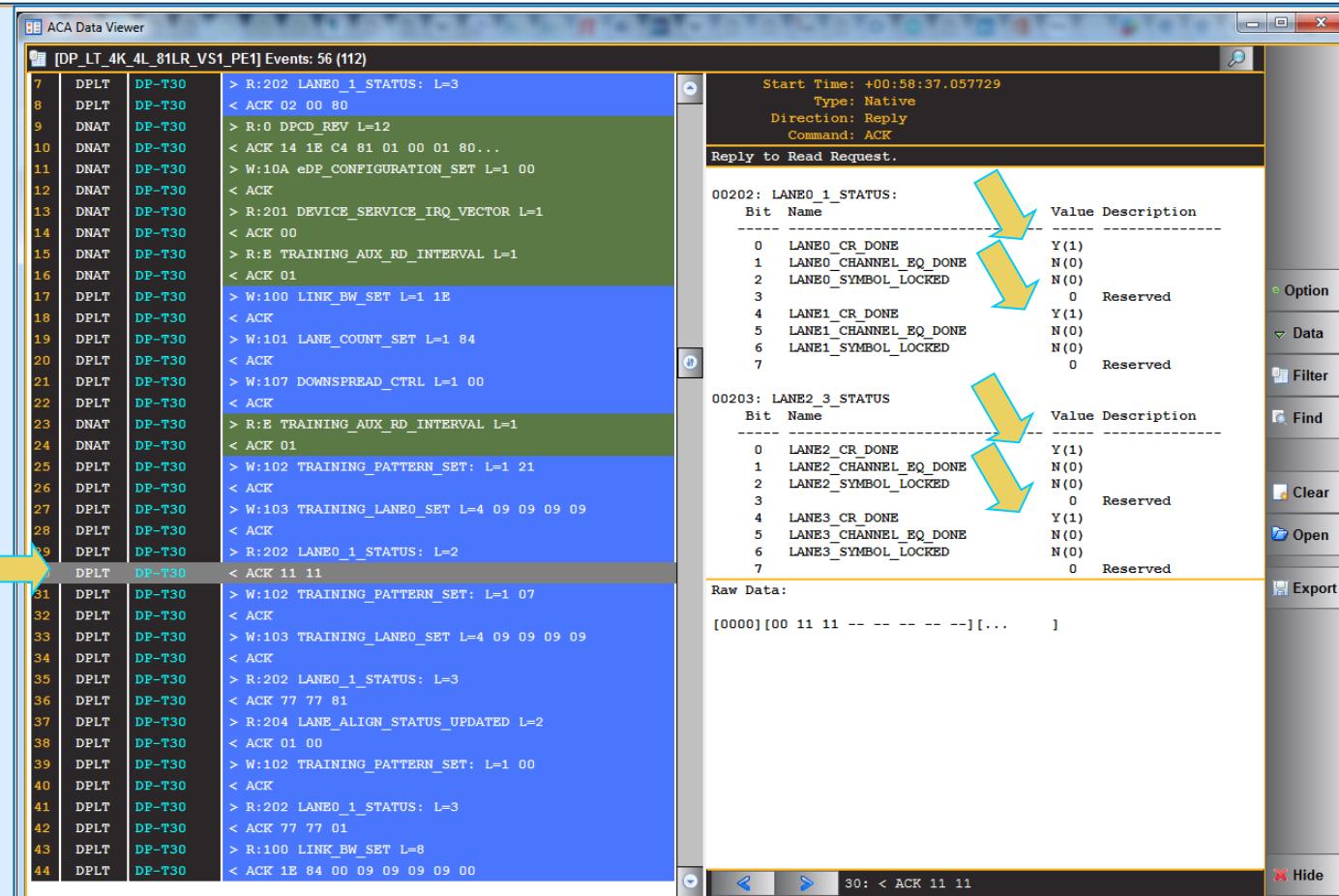
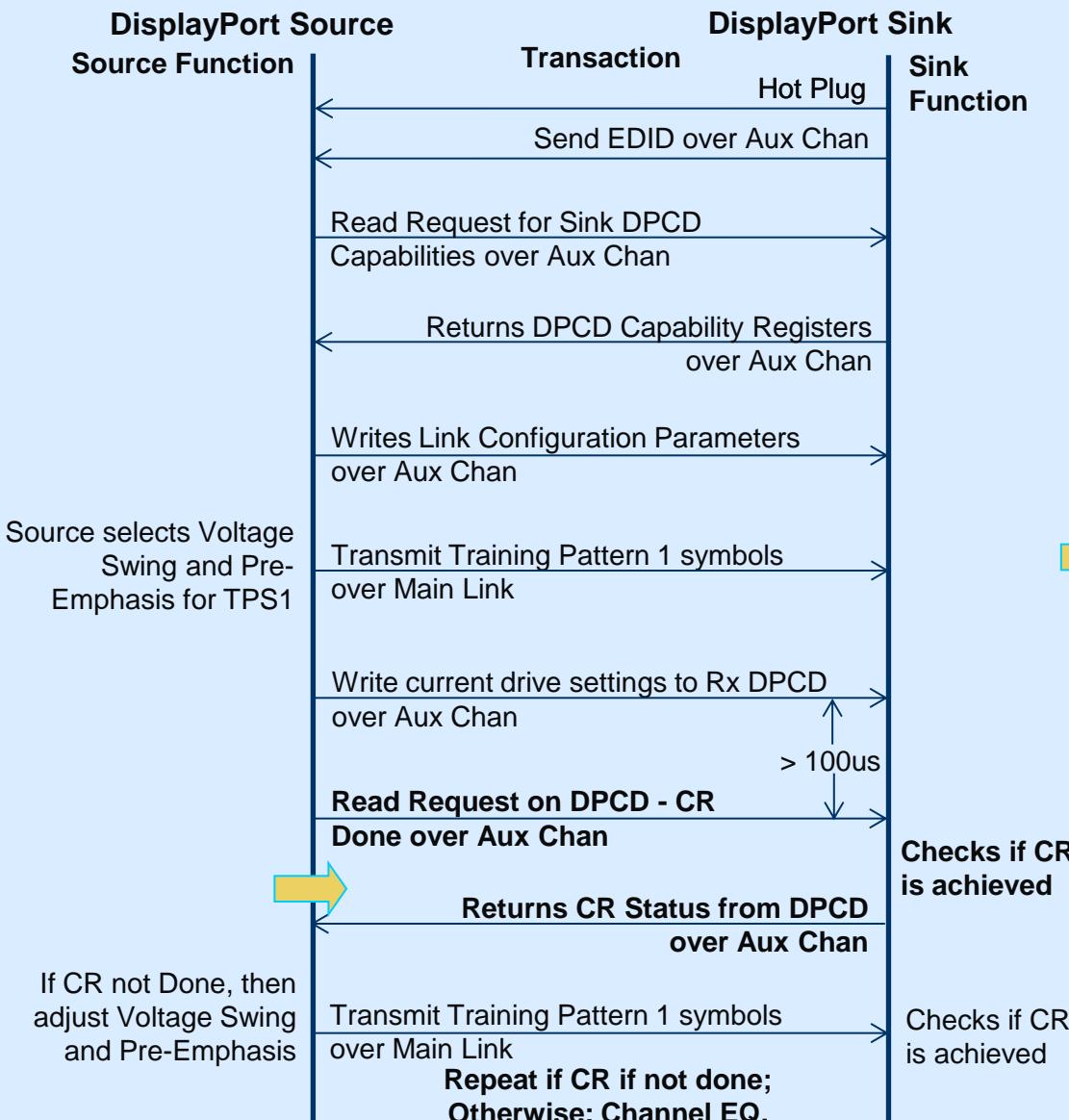
- Source Writing Voltage Swing and Pre-Emphasis Levels for Link Training to Sink DPCD Registers (start with lowest levels).
- Typically drive voltages are the same for all lanes.

Connection Sequence – Link Training Clock Recovery Sequence



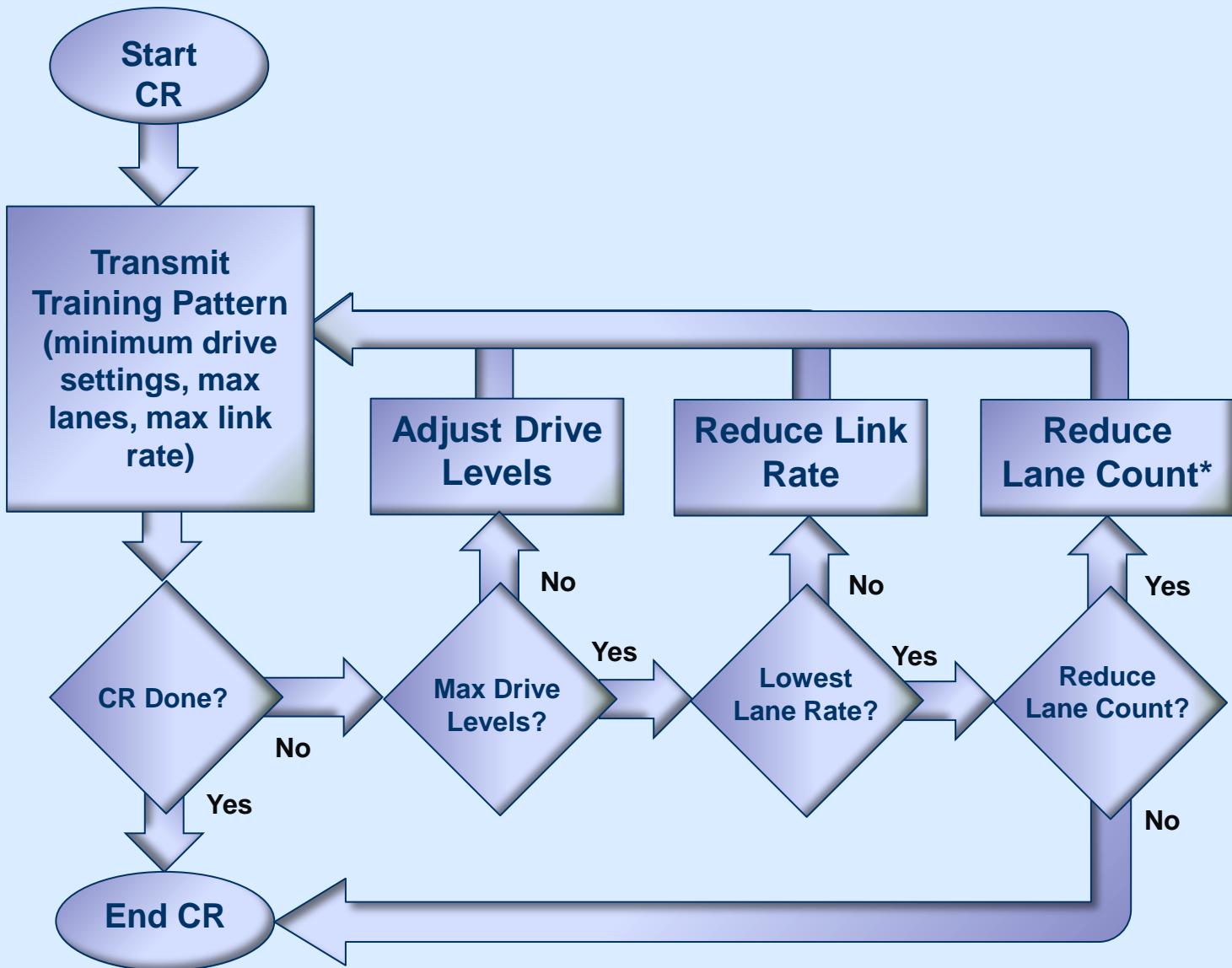
- Verifying Time Duration between Source Writing Voltage Swing and Pre-Emphasis Levels and Reading for CR Done (4.095 msec).

Connection Sequence – Link Training Clock Recovery Sequence



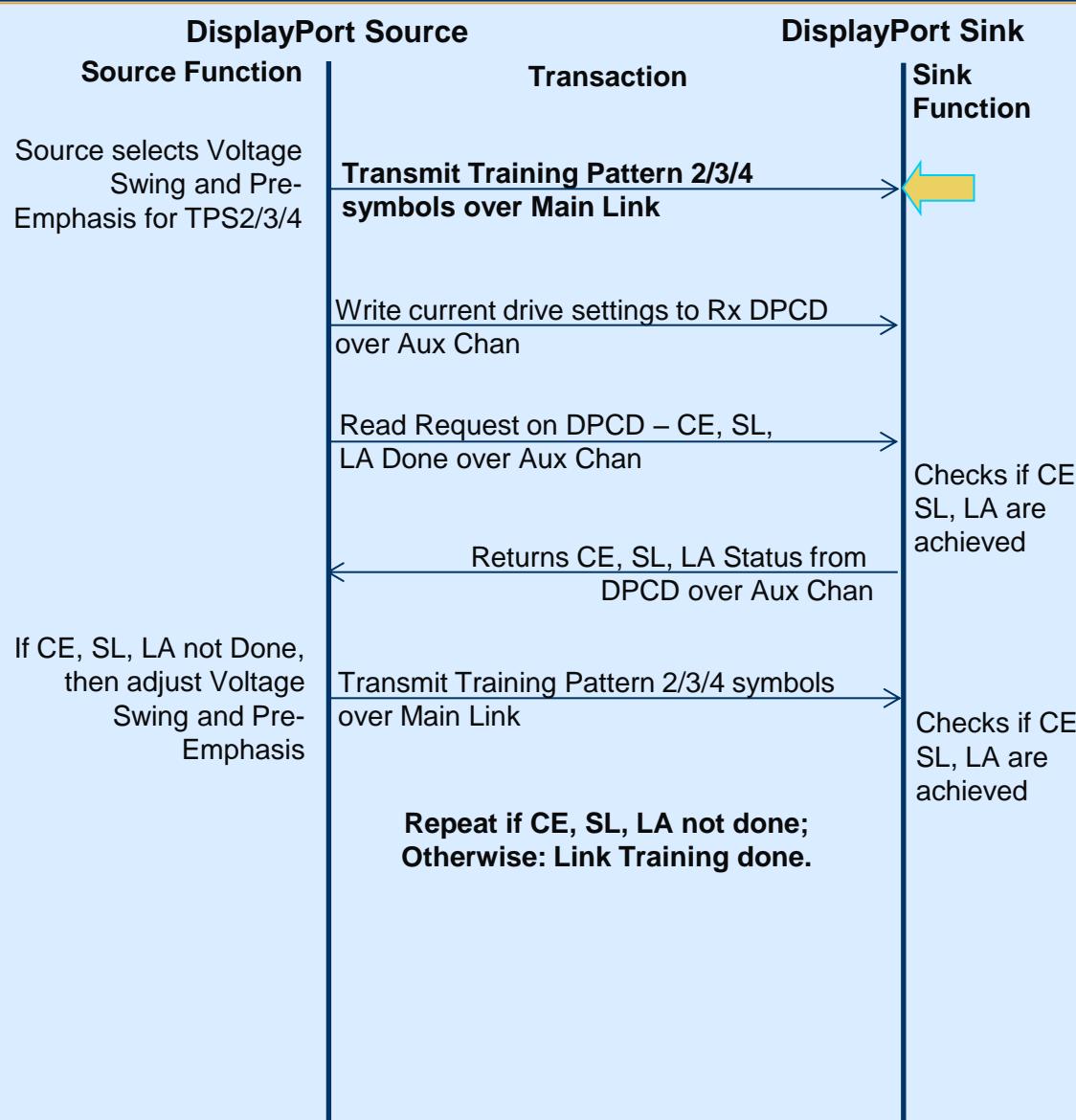
◆ Verifying Clock Recovery Done on all four Lanes.

Connection Sequence – Link Training Clock Recovery

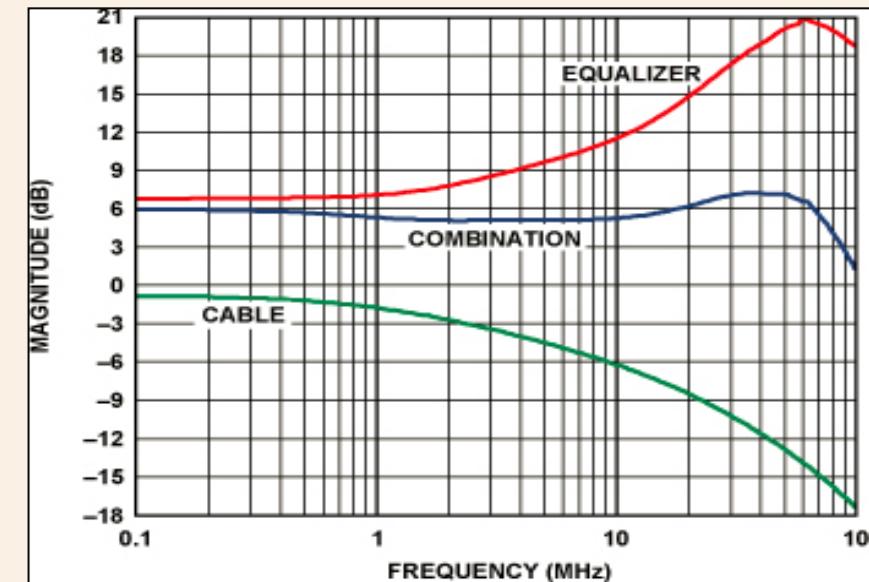


- Link Training Clock Recovery.
- There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
 - Drive levels, i.e. voltage swing and pre-emphasis.
 - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
 - Number of lanes. **Lanes can be reduced if the CR shows that the lower lanes were successfully locked.**

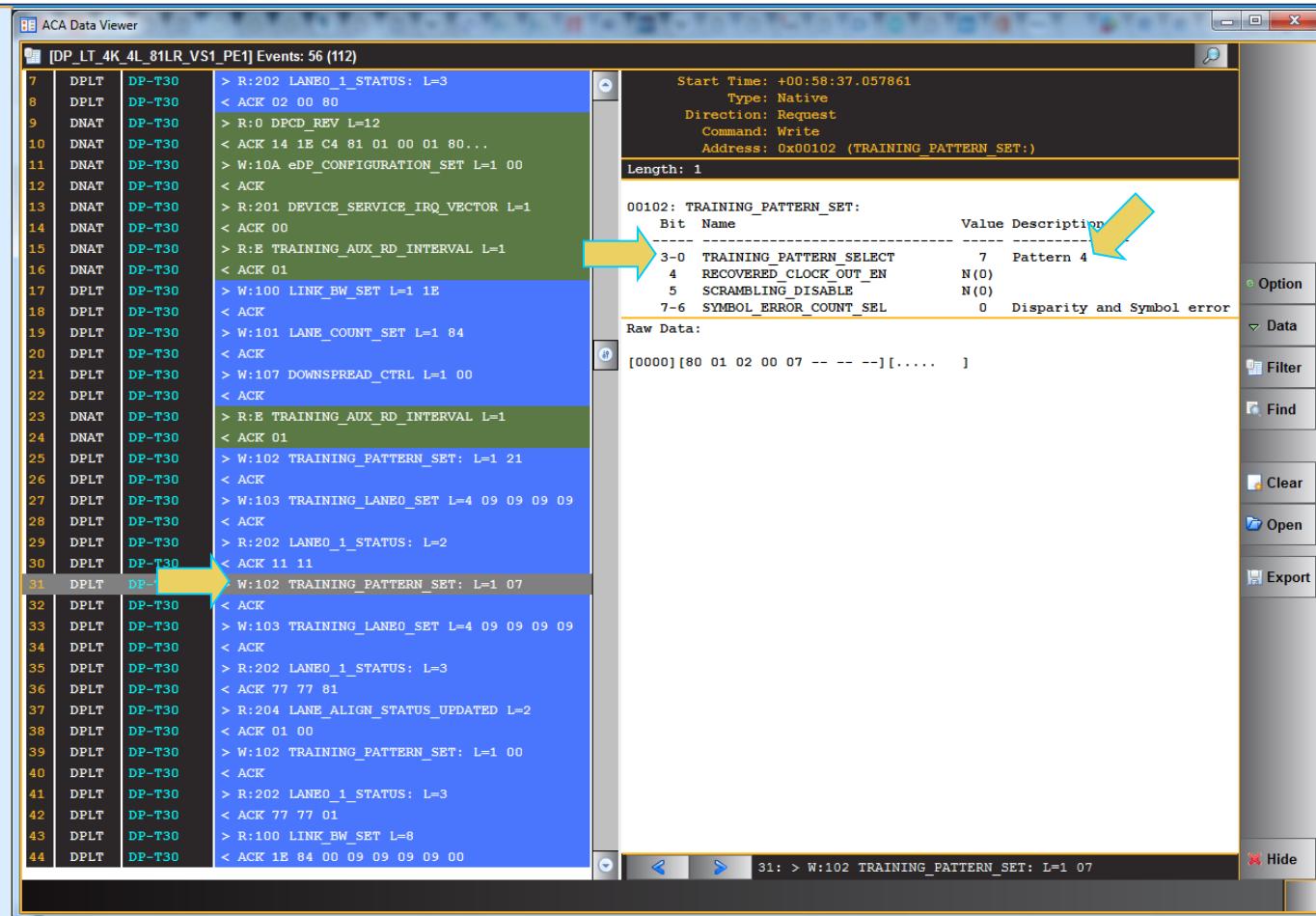
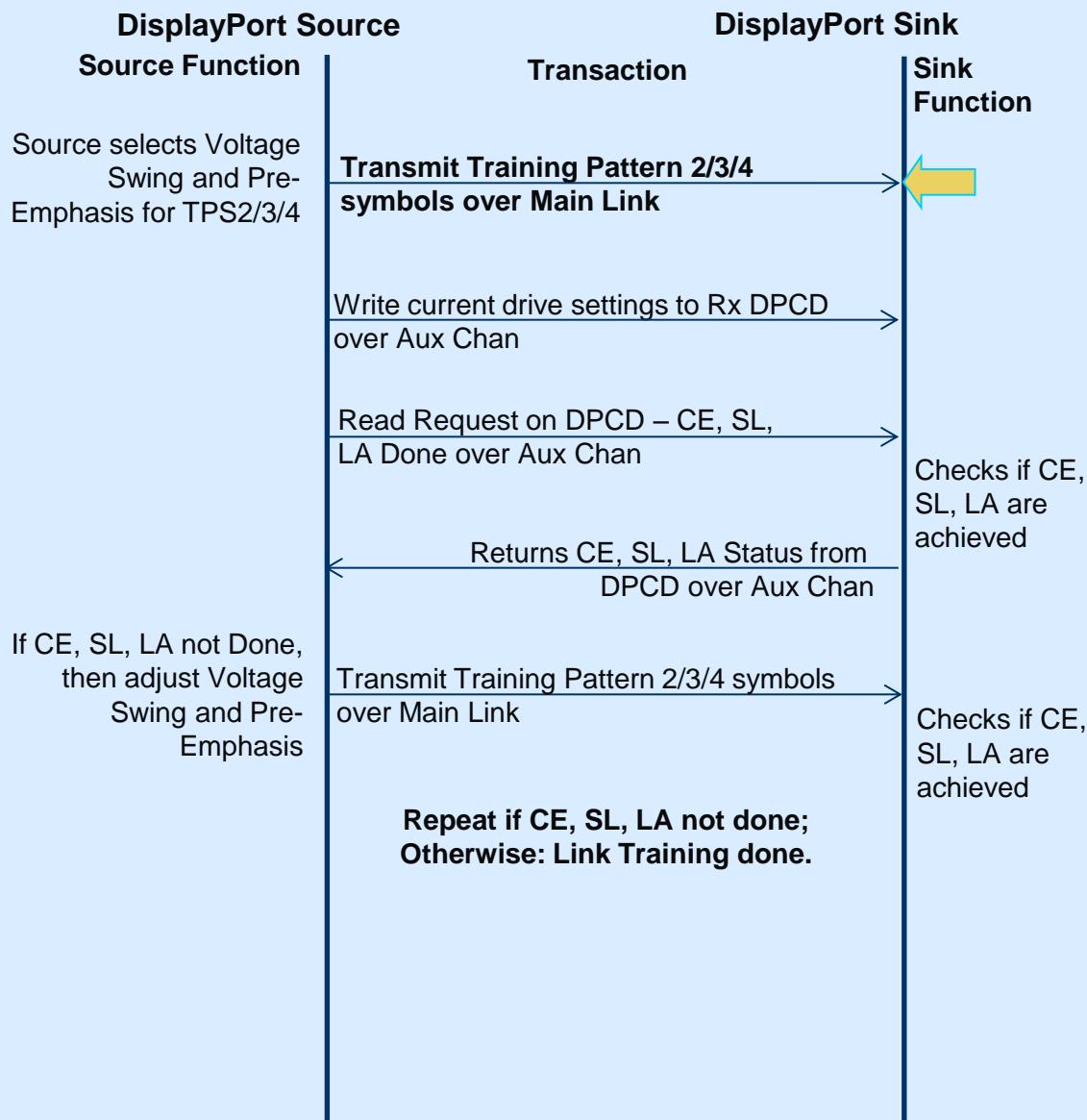
Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment



- **Symbol Lock and Equalization.**
 - Starts with **same link configuration and drive settings** used for Clock Recovery.
 - Symbol Lock is achieved when the receiver has **identified and aligned on the 8b/10b symbol boundaries**.
 - Cable acts like a low pass filter attenuating the harmonics of the fundamental frequency and smearing out the bits resulting in inter-symbol interference.
 - Cable equalization is the process of **altering the frequency response of a video amplifier to compensate for high frequency losses in a cable**.

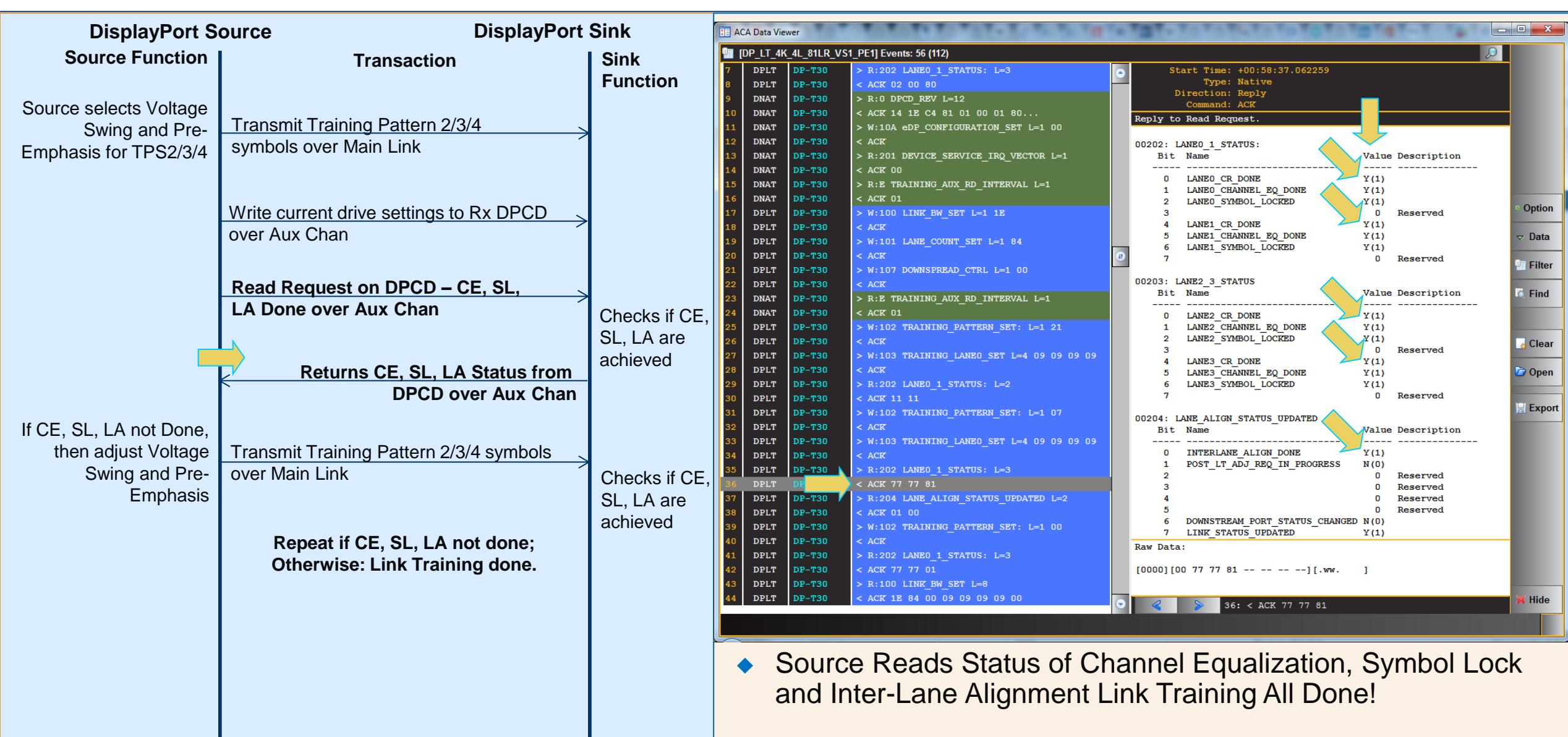


Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment

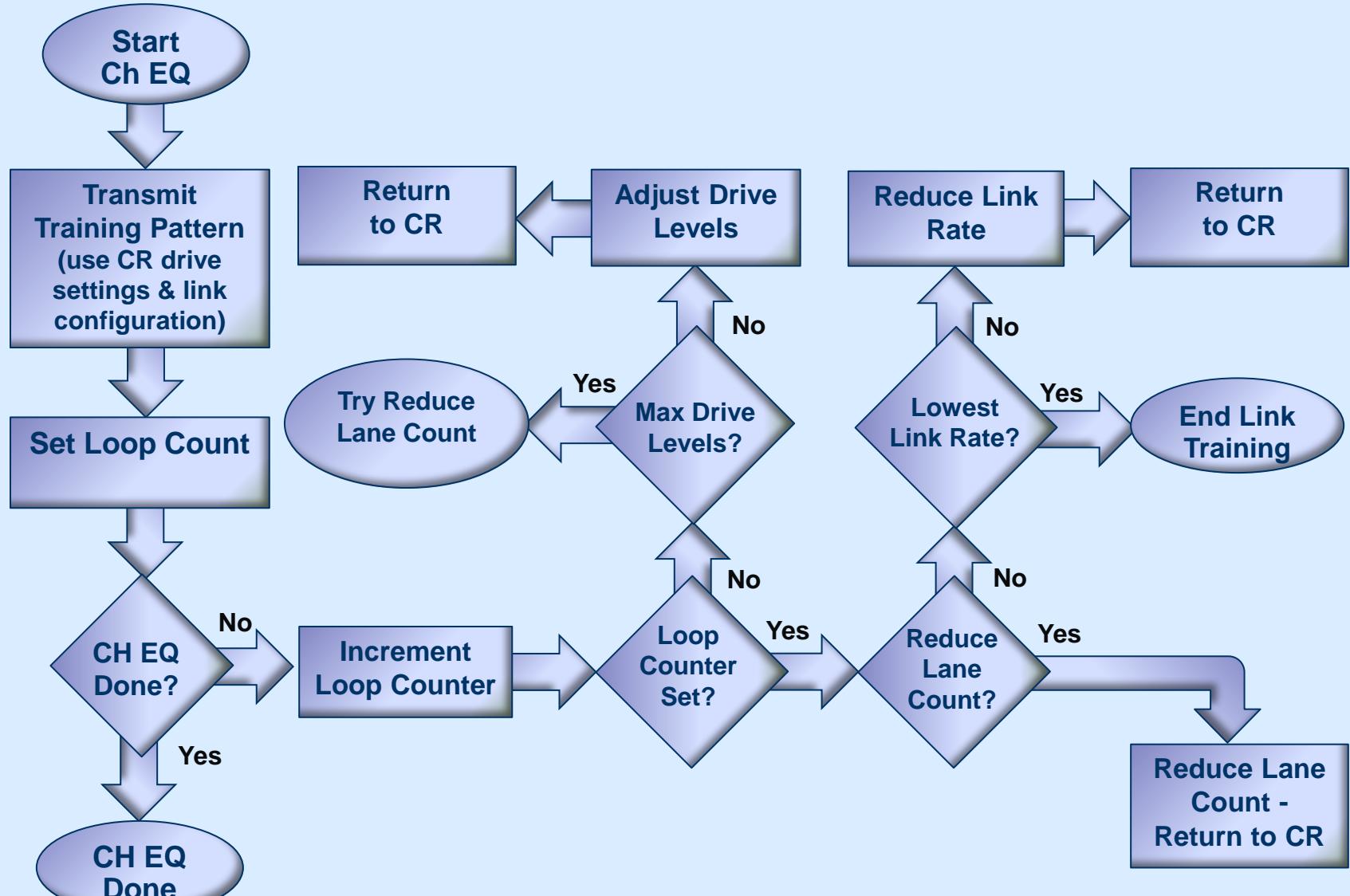


- ◆ Source Writing Training Pattern Set 4 to Sink DPCD Registers.
- ◆ **Training Pattern 4 is always used for 8.1 Gb/s link rate for Channel Equalization, Symbol Lock and Interlane Alignment.**
- ◆ Only training pattern that is sent scrambled.

Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment



Connection Sequence – Channel EQ, Symbol Lock and Interlane Alignment



- There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
 - Drive levels, i.e. voltage swing and pre-emphasis.
 - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
 - Number of lanes. Lanes can be reduced if the CR shows that the lower lanes were successfully locked.

Source Link Layer Compliance – Test 4.3.1.1 Successful Link Training

Compliance Test Results Viewer
DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 03_27_2018_15_01_26 Manufacturer:
Date Tested: March 27, 2018 3:01 PM Model Name:
Overall Status: CTS 1.4 Core R1.0 - Fail Port Tested: 1 [HTML Report](#)

Test Name / Details

4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Iter 01:

- 01: [1] Link Training test for lane count = 1 and lane rate = 1.62
- 02: [2] Link Training test for lane count = 2 and lane rate = 1.62
- 03: [3] Link Training test for lane count = 4 and lane rate = 1.62
- 04: [4] Link Training test for lane count = 1 and lane rate = 2.70
- 05: [5] Link Training test for lane count = 2 and lane rate = 2.70
- 06: [6] Link Training test for lane count = 4 and lane rate = 2.70
- 07: [7] Link Training test for lane count = 1 and lane rate = 5.40
- 08: [8] Link Training test for lane count = 2 and lane rate = 5.40
- 09: [9] Link Training test for lane count = 4 and lane rate = 5.40
- 10: [10] Link Training test for lane count = 1 and lane rate = 8.10
- 11: [11] Link Training test for lane count = 2 and lane rate = 8.10
- 12: [12] Link Training test for lane count = 4 and lane rate = 8.10

Source DUT start link training..
Source DUT sets link bw and lane count before TP1 is set.
Source DUT sets same link bw for link rate under test.
Source DUT sets correct lane count for lane count under test.
Source DUT sets TP1 on all active lanes.
Source DUT starts with voltage swing 0 on all active lanes.
Source DUT starts with pre-emphasis 0 on all active lanes.
CR Lock succeeded on all active lanes.
Training pattern 2 or 3 or 4 detected after Training pattern 1.
For HBR3 source Training pattern 4 detected.
Equalization succeeded on all active lanes.
Symbol lock succeeded on all active lanes.
All Lanes are Aligned and skewed.
Link compliance training test completed successfully.

Link training completed in 20.00 ms, which exceeds the 10ms guideline.

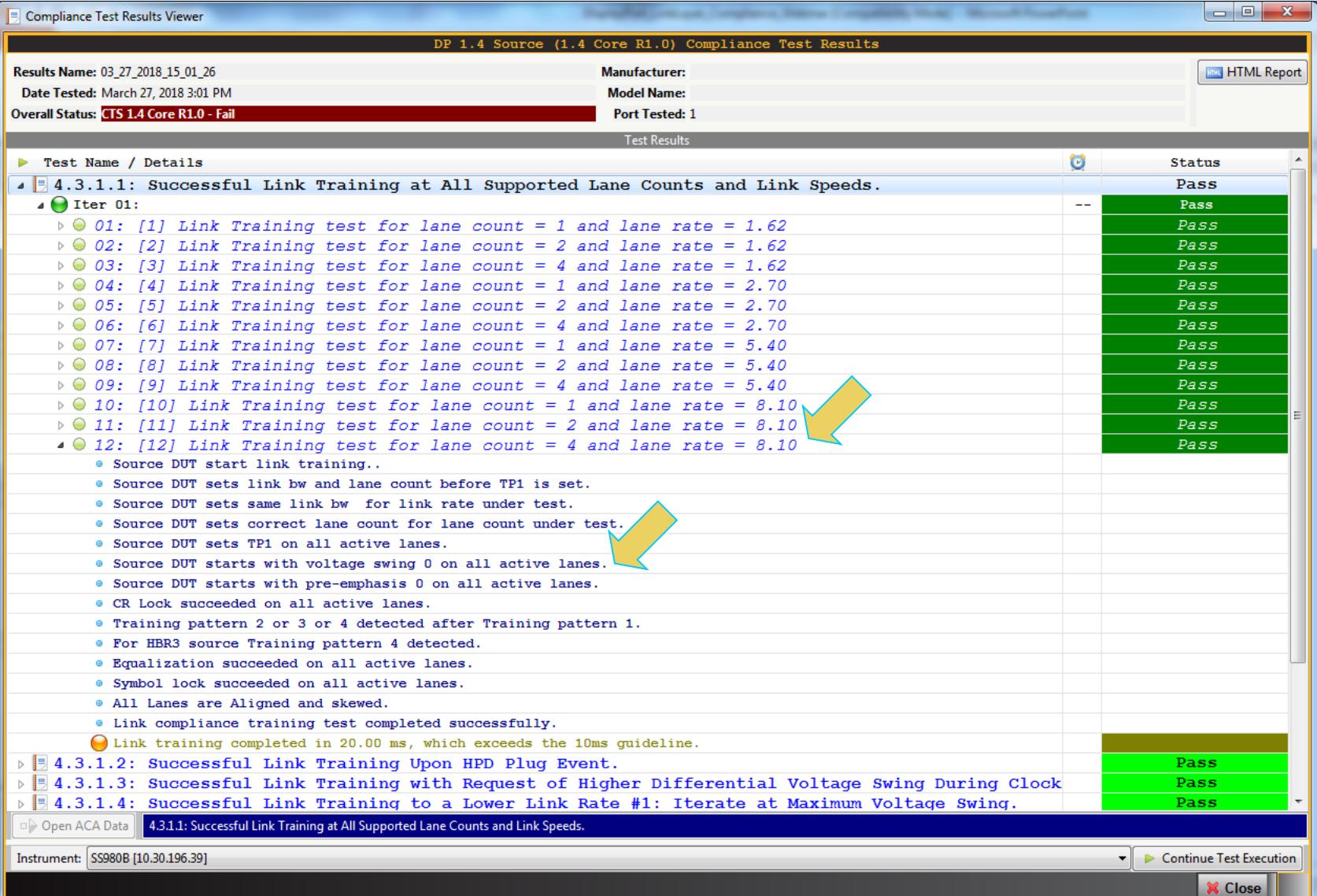
4.3.1.2: Successful Link Training Upon HPD Plug Event.

4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock

4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.

[Open ACA Data](#) 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Instrument: SS980B [10.30.196.39] Continue Test Execution Close



- ◆ Example shows sample test results.
- ◆ Shows details of subtest 12 for link training at 8.1 Gb/s link rate on four (4) lanes.

Source Link Layer Compliance – Test 4.3.1.1 Successful Link Training

Test List	
All	Execute Tests
Instrument: SS980B [10.30.196.39]	Cards...
Category / Test Name	
Link Training	✓
4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.	✓
4.3.1.2: Successful Link Training Upon HPD Plug Event.	✓
4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.	✓
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.	✓
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.	✓
4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence.	✓
4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence.	✓
4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.	✓
4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.	✓
4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).	✓
4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & Channel Equalization	✓
Link Maint.	
4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.	✓
4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.	✓
4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock.	✓
4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.	✓
4.3.2.5: Lane Count Reduction and Increase.	✓
Video	
4.3.3.1: Video Time Stamp Generation	✓
Audio	
4.4.4.3: Audio Time Stamp Generation	✓
Link Training (1.4)	
400.1.1: Source Device HPD Event Pulse Length Test	✓
400.1.2: Source Device IRQ HPD Pulse Length Test	✓
400.1.3: Source Device Inactive HPD / Inactive AUX Test	✓
400.2.1: Source Device Link Training CR Fallback Test	✓
400.2.2: Source Device Link Training EQ Fallback Test	✓

Source Link Layer Compliance – Test 4.3.1.3 Successful Link Training

Compliance Test Results Viewer

DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_25_17
Date Tested: April 23, 2018 11:25 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

HTML Report

Test Name / Details

4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

4.3.1.2: Successful Link Training Upon HPD Plug Event.

4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.

Iter 01:

01: [1] Link Training test for lane count = 4 and lane rate = 8.10

- Source DUT start link training.
- Source DUT sets link bandwidth and lane count before TP1 is set.
- Source DUT sets same link bandwidth for link rate under test.
- Source DUT sets correct lane count for lane count under test.
- Source DUT sets TP1 on all active lanes.
- Source DUT starts with voltage swing 0 on all active lanes.
- Source DUT starts with pre-emphasis 0 on all active lanes.
- Max swing not reached for voltage swing 0 on all active lanes.
- Max swing not reached for voltage swing 1 on all active lanes.
- Voltage swing set to 1 on all active lanes.
- Max swing not reached for voltage swing 2 on all active lanes.
- Voltage swing set to 2 on all active lanes.
- Max swing reached for voltage swing 3 on all active lanes.
- Voltage swing set to 3 on all active lanes.
- CR Lock succeeded on all active lanes.
- Training pattern 2 or 3 or 4 detected after Training pattern 1.
- For HBR3 Source Training pattern 4 detected.
- Equalization succeeded on all active lanes.
- Symbol lock succeeded on all active lanes.
- All Lanes are Aligned and skewed.
- Link compliance training test completed successfully.

Link training completed in 64.46 ms, which exceeds the 10ms guideline.

4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.

4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.

4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence.

4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence.

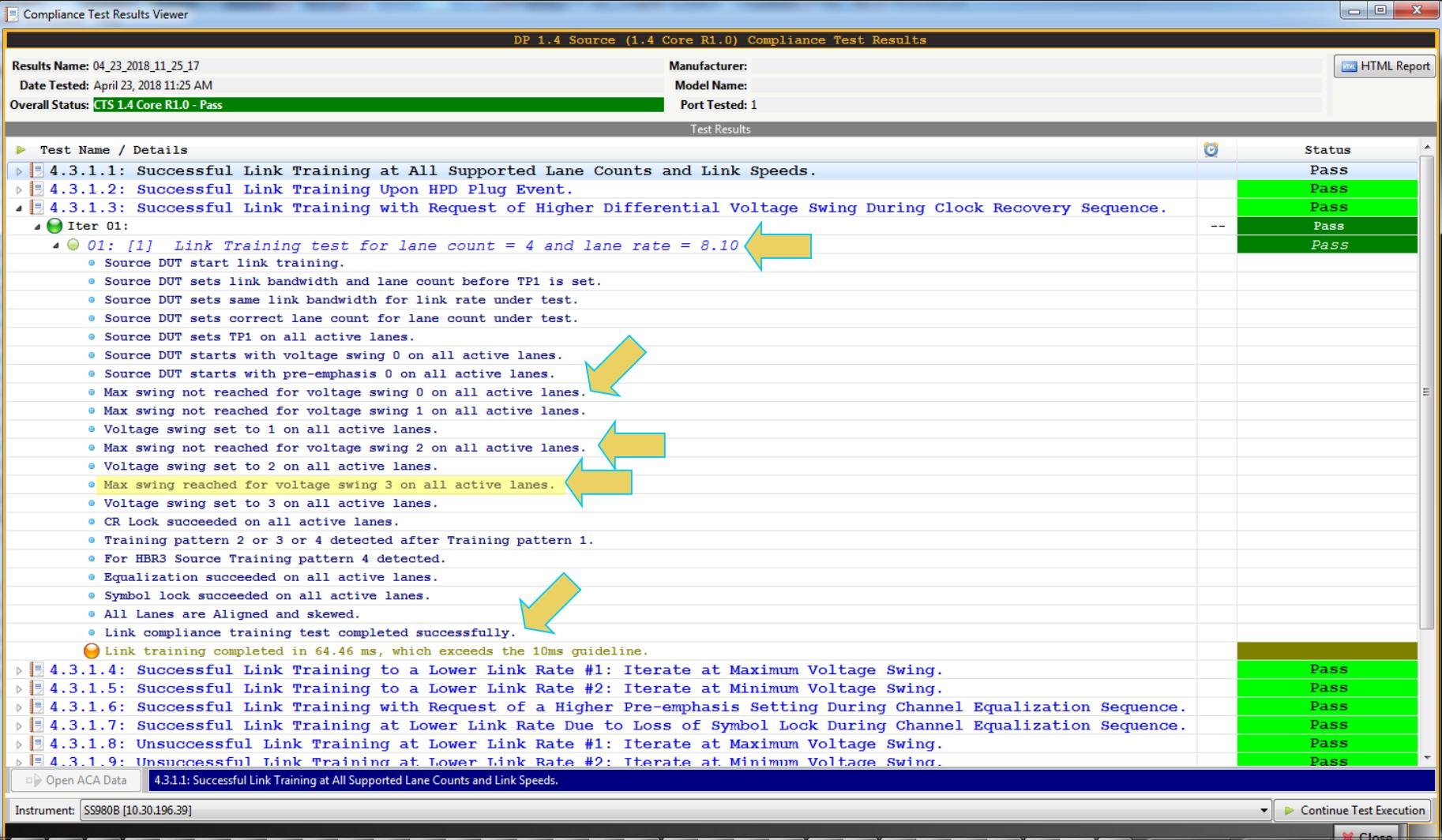
4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.

4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.

Open ACA Data 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Instrument: SS980B [10.30.196.39]

Continue Test Execution Close



- ◆ Example shows sample test results.
- ◆ Uses 4 Lanes with 8.1Gb/s link rate.

Source Link Layer Compliance Tests

DP 1.4 Source CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

All Execute Tests Cards...

Category / Test Name

Link Training

- 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.
- 4.3.1.2: Successful Link Training Upon HPD Plug Event.
- 4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.
- 4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence.
- 4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence.
- 4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).
- 4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & Channel Equalization

Link Maint.

- 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.
- 4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.
- 4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock.
- 4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.
- 4.3.2.5: Lane Count Reduction and Increase.

Video

- 4.3.3.1: Video Time Stamp Generation

Audio

- 4.4.4.3: Audio Time Stamp Generation

Link Training (1.4)

- 400.1.1: Source Device HPD Event Pulse Length Test
- 400.1.2: Source Device IRQ HPD Pulse Length Test
- 400.1.3: Source Device Inactive HPD / Inactive AUX Test
- 400.2.1: Source Device Link Training CR Fallback Test
- 400.2.2: Source Device Link Training EQ Fallback Test

Close

Source Link Layer Compliance – Test 4.3.1.7 Link Training Loss of Symbol Lock

Compliance Test Results Viewer

DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_25_17
Date Tested: April 23, 2018 11:25 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:
Model Name:
Port Tested: 1

HTML Report

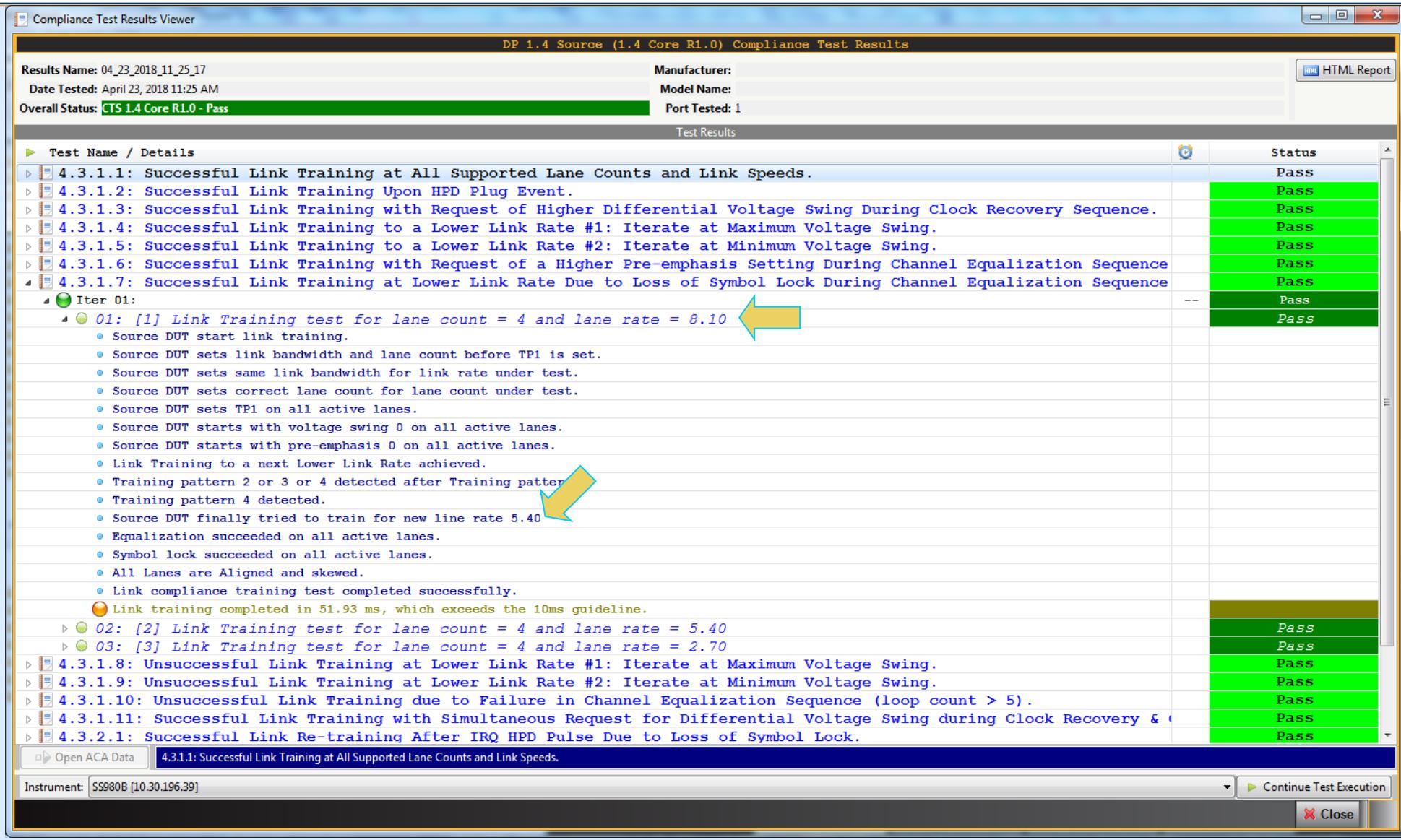
Test Results

Test	Status
4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.	Pass
4.3.1.2: Successful Link Training Upon HPD Plug Event.	Pass
4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.	Pass
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.	Pass
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.	Pass
4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence	Pass
4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence	Pass
Iter 01:	--
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
Source DUT start link training.	
Source DUT sets link bandwidth and lane count before TP1 is set.	
Source DUT sets same link bandwidth for link rate under test.	
Source DUT sets correct lane count for lane count under test.	
Source DUT sets TP1 on all active lanes.	
Source DUT starts with voltage swing 0 on all active lanes.	
Source DUT starts with pre-emphasis 0 on all active lanes.	
Link Training to a next Lower Link Rate achieved.	
Training pattern 2 or 3 or 4 detected after Training patter	
Training pattern 4 detected.	
Source DUT finally tried to train for new line rate 5.40	
Equalization succeeded on all active lanes.	
Symbol lock succeeded on all active lanes.	
All Lanes are Aligned and skewed.	
Link compliance training test completed successfully.	
Link training completed in 51.93 ms, which exceeds the 10ms guideline.	
02: [2] Link Training test for lane count = 4 and lane rate = 5.40	Pass
03: [3] Link Training test for lane count = 4 and lane rate = 2.70	Pass
4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.	Pass
4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.	Pass
4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).	Pass
4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & (Pass
4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.	Pass

Open ACA Data 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Instrument: SS980B [10.30.196.39]

Continue Test Execution Close



- ◆ Example shows results of link training with loss of symbol lock at 8.1Gb/s.

Source Link Layer Compliance – Test 4.3.1.7 Link Training Loss of Symbol Lock

Compliance Test Results Viewer

DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_25_17
Date Tested: April 23, 2018 11:25 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:
Model Name:
Port Tested: 1

HTML Report

Test Name / Details

Test Name	Status
4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.	Pass
4.3.1.2: Successful Link Training Upon HPD Plug Event.	Pass
4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.	Pass
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.	Pass
4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.	Pass
4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence	Pass
4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence	Pass
Iter 01:	--
01: [1] Link Training test for lane count = 4 and lane rate = 8.10	Pass
02: [2] Link Training test for lane count = 4 and lane rate = 5.40	Pass
Source DUT start link training.	
Source DUT sets link bandwidth and lane count before TP1 is set.	
Source DUT sets same link bandwidth for link rate under test.	
Source DUT sets correct lane count for lane count under test.	
Source DUT sets TP1 on all active lanes.	
Source DUT starts with voltage swing 0 on all active lanes.	
Source DUT starts with pre-emphasis 0 on all active lanes.	
Link Training to a next Lower Link Rate achieved.	
Training pattern 2 or 3 or 4 detected after Training pattern 1.	
Training pattern 3 detected.	
Source DUT finally tried to train for new line rate 2.70	Pass
Equalization succeeded on all active lanes.	
Symbol lock succeeded on all active lanes.	
All Lanes are Aligned and skewed.	
Link compliance training test completed successfully.	
Link training completed in 44.84 ms, which exceeds the 10ms guideline.	Pass
03: [3] Link Training test for lane count = 4 and lane rate = 2.70	Pass
4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.	Pass
4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.	Pass
4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).	Pass
4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & C	Pass
4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.	Pass

Open ACA Data 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

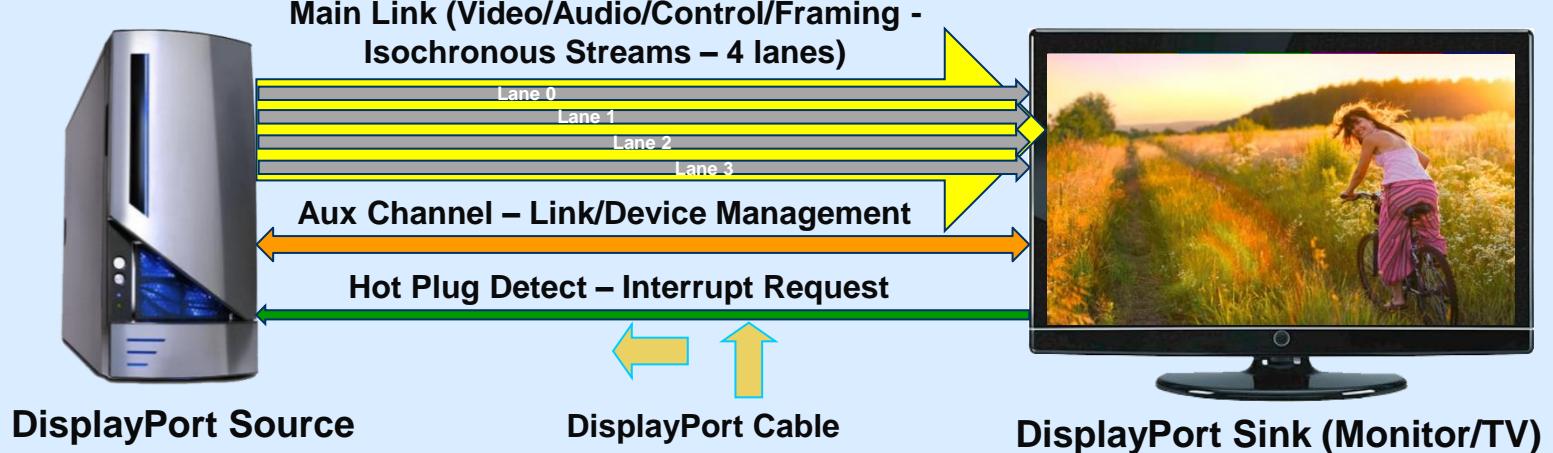
Instrument: SS980B [10.30.196.39]

Continue Test Execution Close

- ◆ Example shows results of link training with loss of symbol lock at 5.4Gb/s.

Source Link Layer Compliance Link Maintenance Test

Link Maintenance



- If Link Training is successful, then Link Maintenance mode.
- Link Training does not guarantee that the link will behave without errors.
- In Link Maintenance mode, the Link Policy function may force a retrain if there is a failure on the link.
- Link **retraining** is necessary when there is a **loss of Clock Lock, loss of Symbol Lock or loss of Inter-Lane Alignment**.
- Failure results in an **IRQ interrupt** using the Hot Plug Detect lead. The interrupt is a low-going pulse.
- Source **re-initiates Link Training**.

DP 1.4 Source Link Layer Compliance

DP 1.4 Source CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

All Execute Tests Cards...

Category / Test Name

Link Training

- 4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.
- 4.3.1.2: Successful Link Training Upon HPD Plug Event.
- 4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence.
- 4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.6: Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence.
- 4.3.1.7: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence.
- 4.3.1.8: Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing.
- 4.3.1.9: Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing.
- 4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).
- 4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery & Channel Equalization

Link Maint.

- 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.
- 4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.
- 4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock.
- 4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.
- 4.3.2.5: Lane Count Reduction and Increase.

Video

- 4.3.3.1: Video Time Stamp Generation

Audio

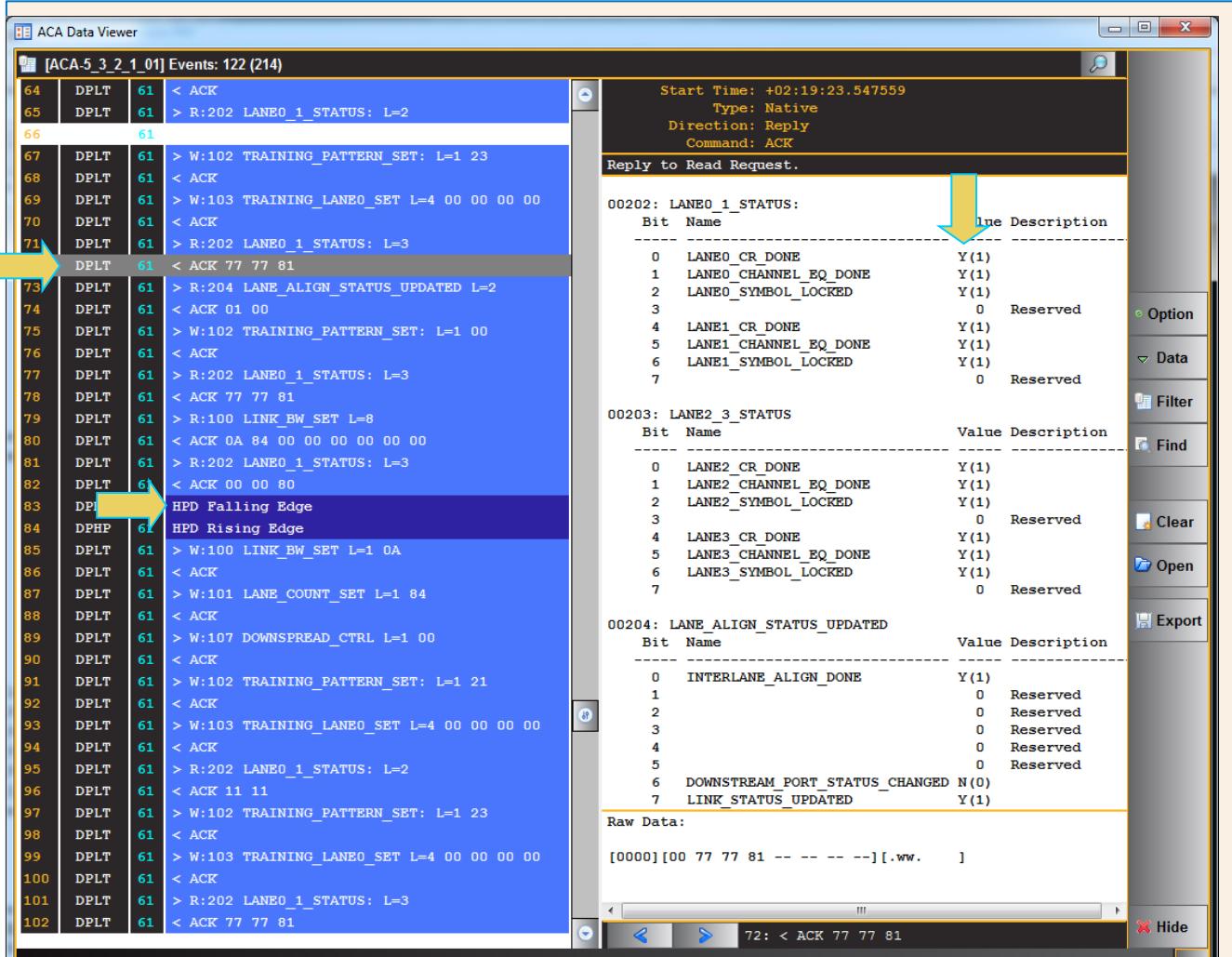
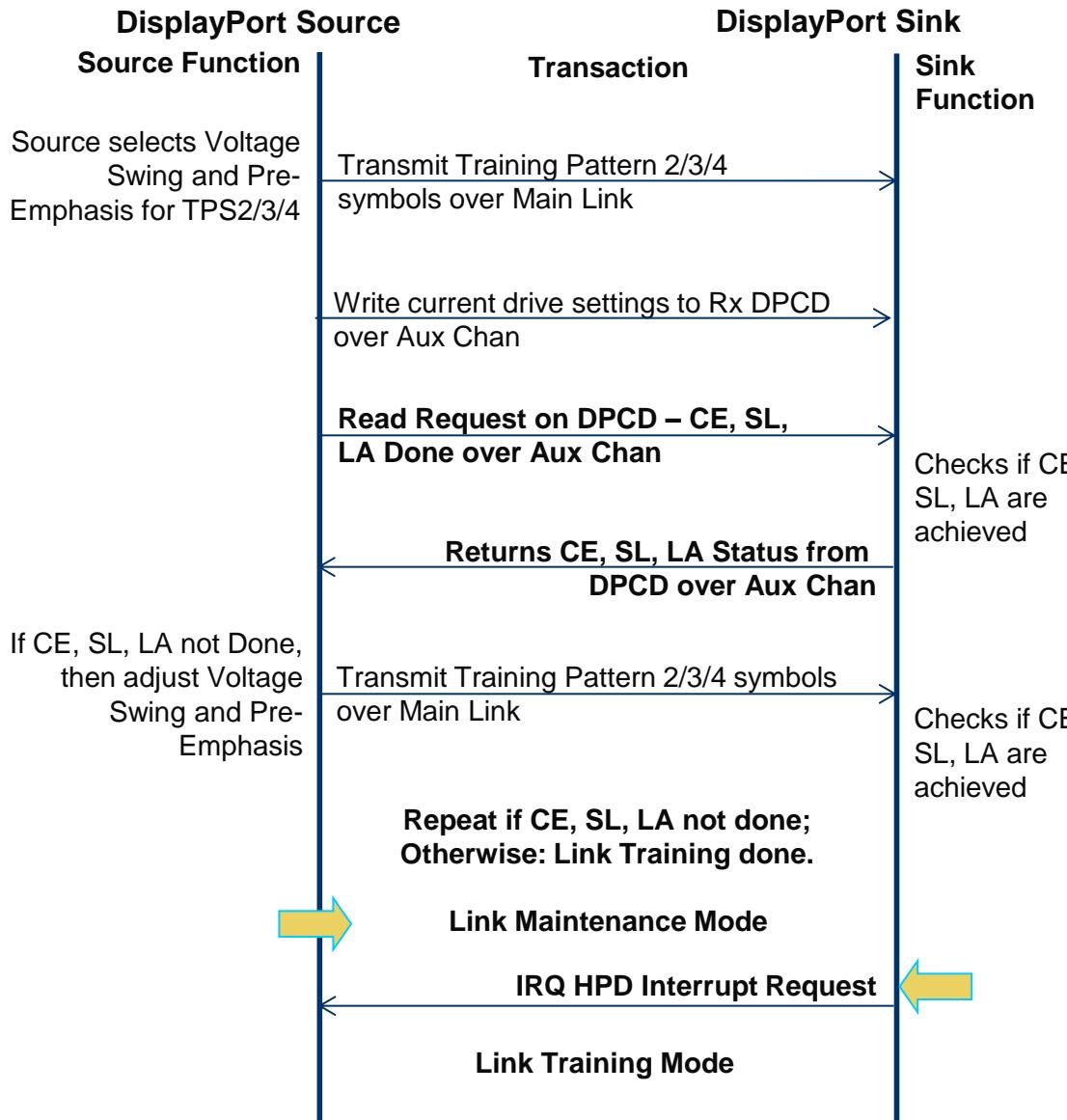
- 4.4.4.3: Audio Time Stamp Generation

Link Training (1.4)

- 400.1.1: Source Device HPD Event Pulse Length Test
- 400.1.2: Source Device IRQ HPD Pulse Length Test
- 400.1.3: Source Device Inactive HPD / Inactive AUX Test
- 400.2.1: Source Device Link Training CR Fallback Test
- 400.2.2: Source Device Link Training EQ Fallback Test

Close

Auxiliary Channel Analyzer (ACA) – Link Maintenance – IRQ Request



Link Training has been completed. Link failure occurs;
Interrupt generated Link Training re-initiated

Source Link Layer Compliance – Test 4.3.2.2 Re-Training After IRQ

Compliance Test Results Viewer

DP 1.4 Source (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_25_17
Date Tested: April 23, 2018 11:25 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

Test Results

	Status
4.3.1.10: Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5).	Pass
4.3.1.11: Successful Link Training with Simultaneous Request for Differential Voltage Swing during Clock Recovery	Pass
4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.	Pass
4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.	Pass
Iter 01:	--
01: [1] Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
• Source DUT start link training.	
• Source DUT sets link bandwidth and lane count before TP1 is set.	
• Source DUT sets same link bandwidth for link rate under test.	
• Source DUT sets correct lane count for lane count under test.	
• Source DUT sets TP1 on all active lanes.	
• Source DUT starts with voltage swing 0 on all active lanes.	
• Source DUT starts with pre-emphasis 0 on all active lanes.	
• CR Lock succeeded on all active lanes.	
• Training pattern 2 or 3 or 4 detected after Training pattern 1.	
• Equalization succeeded on all active lanes.	
• Symbol lock succeeded on all active lanes.	
• All Lanes are Aligned and skewed.	
• Link compliance training test completed successfully.	
● Link training completed in 20.11 ms, which exceeds the 10ms guideline.	
02: [2] After clock lock error on lane 1, Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
• After loss of Clock Lock on lane 1.	
• Link re-training starts after IRQ pulse.	
• Source DUT reads DPCD address 0200-0205h.	
• Source DUT read link status within 100ms.	
• Source DUT start link training.	
• Source DUT sets link bandwidth and lane count before TP1 is set.	
• Source DUT sets TP1 on all active lanes.	
• CR Lock succeeded on all active lanes.	
• Training pattern 2 or 3 or 4 detected after Training pattern 1.	
• Equalization succeeded on all active lanes.	
• Symbol lock succeeded on all active lanes.	
• All Lanes are Aligned and skewed.	
• Link compliance training test completed successfully.	
● Link training completed in 20.61 ms, which exceeds the 10ms guideline.	
03: [3] After clock lock error on lane 2, Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
04: [4] After clock lock error on lane 3, Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
05: [5] After clock lock error on lane 4, Link Maintenance test for lane count = 4 and lane rate = 8.10	Pass
4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock.	Pass
4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set.	Pass
Open ACA Data	4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.
Instrument: SS980B [10.30.196.39]	Continue Test Execution
	X Close

Instrument: SS980B [10.30.196.39]

4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds.

Continue Test Execution

X Close

- ◆ Example shows details of IRQ test at 8.1Gb/s link rate with a loss of clock recover on Lane 1.

Sink Link Layer Compliance Tests



TELEDYNE LECROY
Everywhereyoulook™

Emulating DisplayPort Source to Run Link Layer Sink Compliance Tests

DP 1.4 Reference Source
Example: Teledyne LeCroy
quantumdata 980 Test Platform
with DP 1.4 Video Generator /
Protocol Analyzer

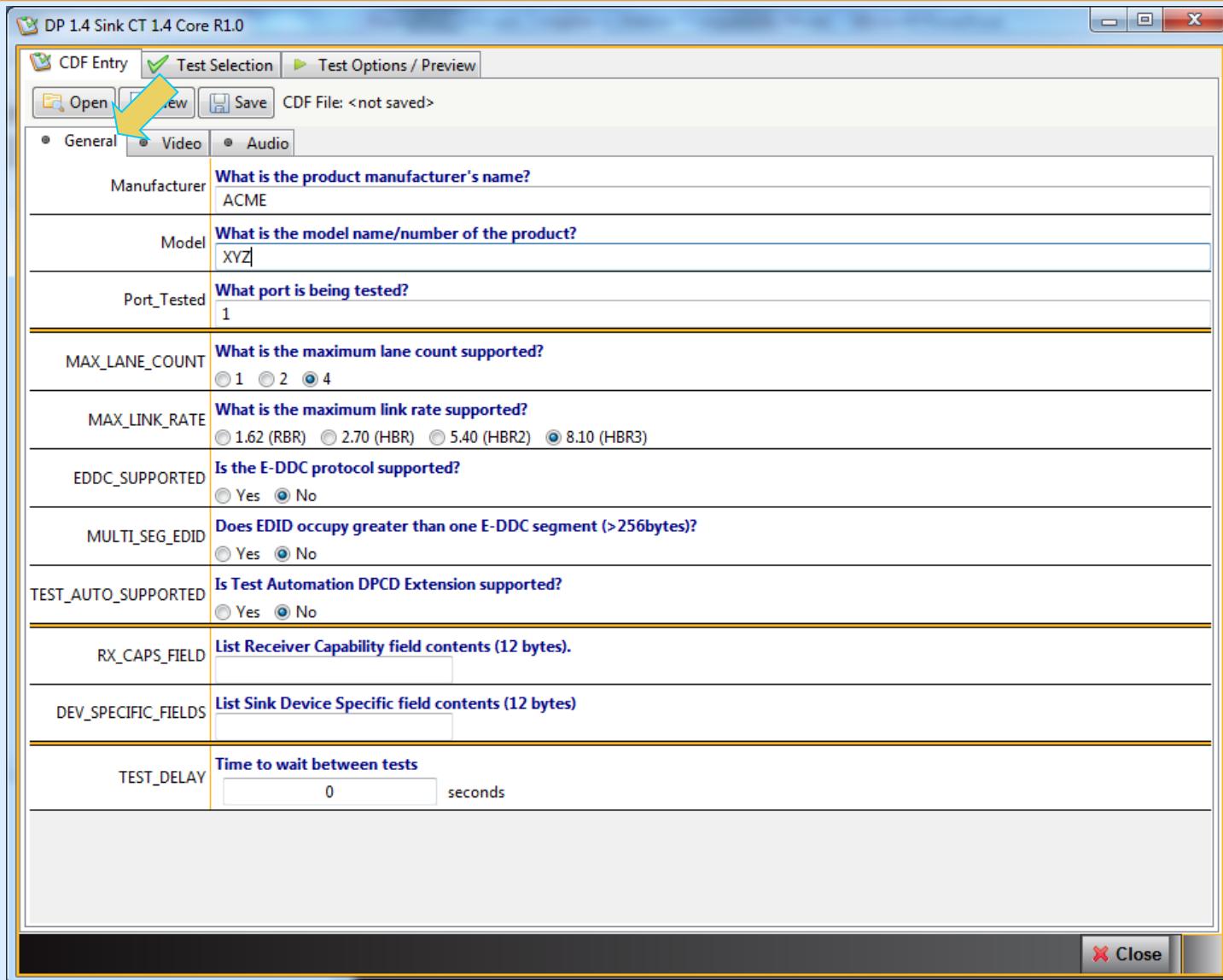


DisplayPort Cable

DisplayPort Sink (Monitor/TV)

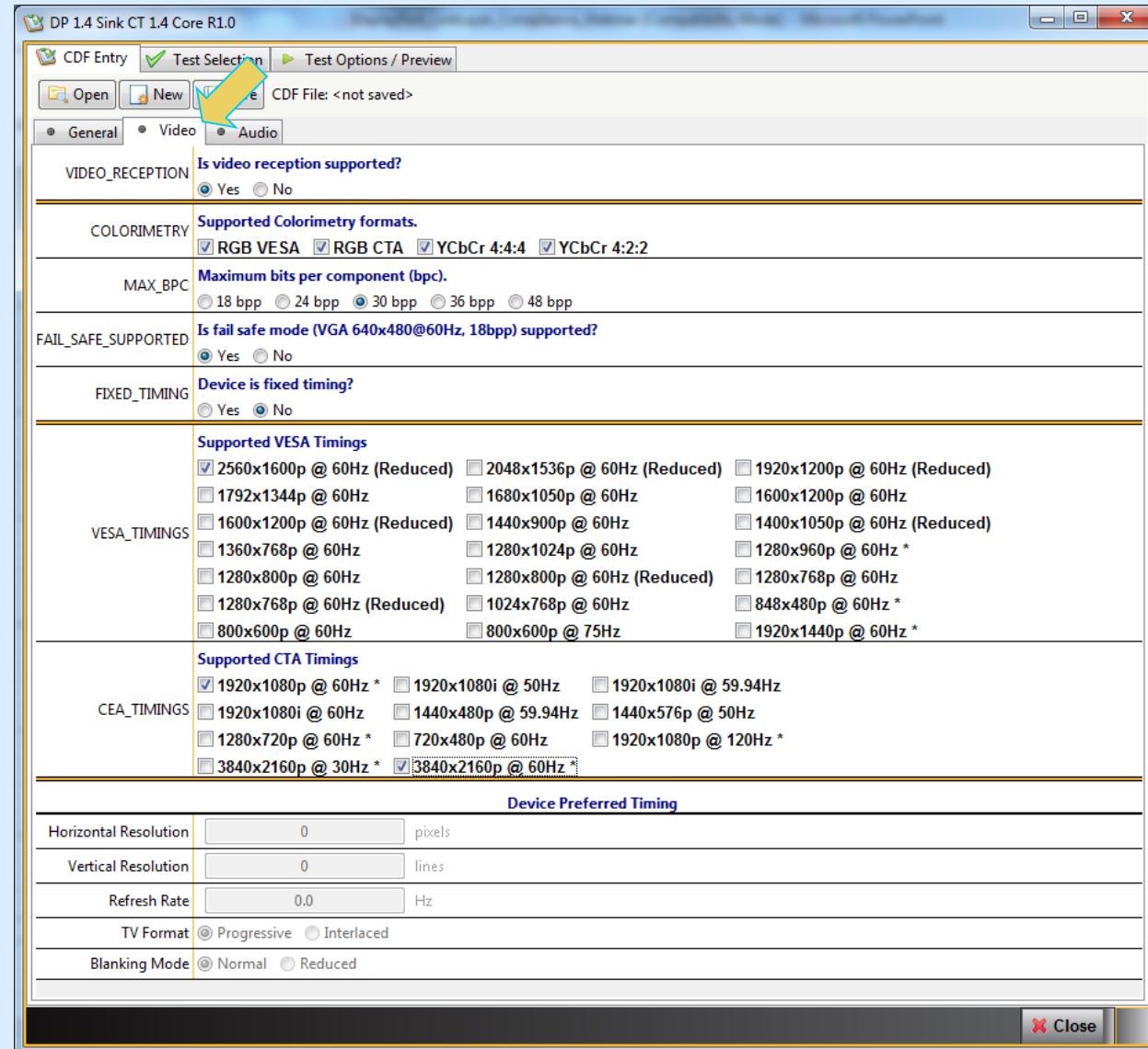


Entering the CDF Information – Sink General Link Layer Capabilities



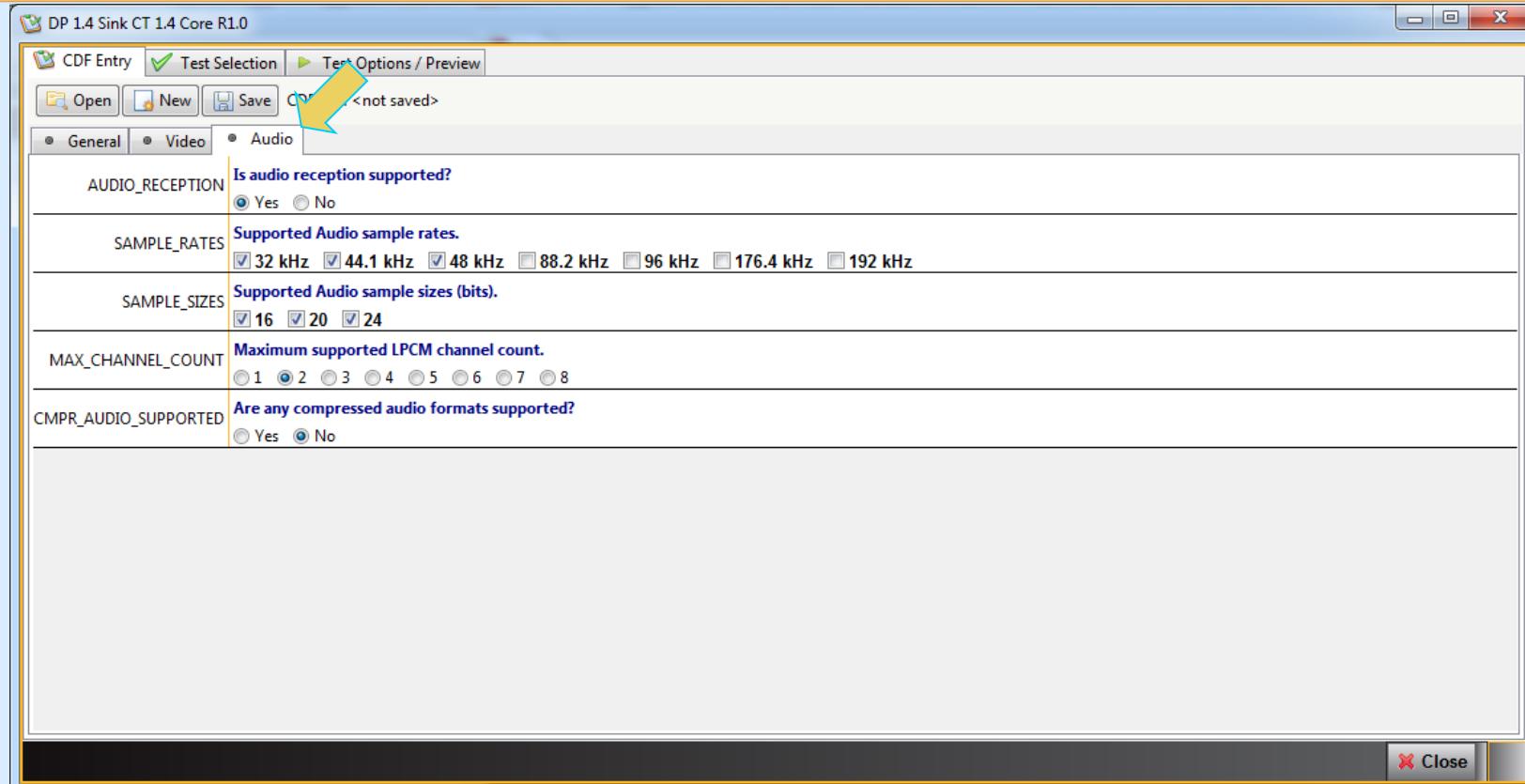
- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF is used by the reference sink to know which Link Layer related sink features to test.
- There are three (3) tabs:
 - General Tab - Describes the link capabilities of the sink device.
 - Video – Described in next slide(s).
 - Audio – Described in next slide(s).

Entering the CDF Information – Sink Video Capabilities



- Video – Described video capabilities of the sink device.

Entering the CDF Information – Sink Audio Capabilities



- **Audio** – Described audio capabilities of the sink device.

Sink Link Layer Compliance

List of Current Tests

Sink Link Layer Compliance – List of Current Sink Tests

DP 1.4 Sink CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

All Category / Test Name

AUX Ch. Proto.

- 5.2.1.1: One byte DPCD Read ✓
- 5.2.1.2: Multi-byte DPCD Read ✓
- 5.2.1.3: One Byte DPCD Write ✓
- 5.2.1.4: Multi-byte DPCD Write ✓
- 5.2.1.5: Write EDID Offset ✓
- 5.2.1.6: Read One EDID Byte ✓
- 5.2.1.7: EDID Read ✓
- 5.2.1.8: Illegal AUX Request Syntax ✓
- 5.2.1.9: Glitch Rejection ✓
- 5.2.1.10: Interleaved EDID and DPCD Read ✓
- 5.2.1.11: Downstream Stop on MOT Reset ✓
- 5.2.1.12: Downstream Stop on Timeout ✓

Link Training

- 5.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds ✓
- 5.3.1.2: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence ✓
- 5.3.1.3: Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure During Clock Recovery Sequence ✓
- 5.3.1.4: Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization ✓
- 5.3.1.5: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence ✓
- 5.3.1.6: Lane Count Reduction ✓
- 5.3.1.7: Lane Count Increase ✓

Link Maint.

- 5.3.2.1: IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock. ✓
- 5.3.2.2: IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock ✓

Main Video

- 5.4.1.1: Pixel Data Reconstruction ✓
- 5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU ✓
- 5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU ✓
- 5.4.2: Main Video Stream Format Change Handling ✓

Power Management

- 5.4.3.1: Entering and Exiting Power Save Mode ✓
- 5.4.3.2: Resumption of Main Link Activity After Extended Idle ✓

Execute Tests Cards...

Close

- ◆ Current list of Sink Tests – Page 1

Sink Link Layer Compliance – List of Current Tests (continued)

DP 1.4 Sink CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

Category / Test Name	Status
5.3.1.5: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence	✓
5.3.1.6: Lane Count Reduction	✓
5.3.1.7: Lane Count Increase	✓
Link Maint.	
5.3.2.1: IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock.	✓
5.3.2.2: IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock	✓
Main Video	
5.4.1.1: Pixel Data Reconstruction	✓
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	✓
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	✓
5.4.2: Main Video Stream Format Change Handling	✓
Power Management	
5.4.3.1: Entering and Exiting Power Save Mode	✓
5.4.3.2: Resumption of Main Link Activity After Extended Idle	✓
Main Audio	
5.4.4.2: Audio Startup and Format Change	✓
5.4.4.4: Audio InfoFrame Packet	✓
5.4.4.5: Audio Clock Recovery	✓
5.4.4.6: Audio Stream Reception	✓
DPCD	
7.2.1.1: Sink Organizationally Unique Identifier (OUI)	✓
7.2.1.2: Sink Count	✓
7.2.1.3: Sink Status	✓
7.2.1.4: Symbol Error Count	✓
7.2.1.5: Device Identifications	✓
7.2.1.6: Number of Receiver Ports	✓
7.2.1.7: Main Link Channel Coding	✓
Other (1.4)	
500.1.1: 2-Lane Link Training CR/EQ Fallback Test	✓
500.1.2: 1-Lane Link Training CR/EQ Fallback Test	✓
500.1.3: Sink Device Error Count	✓
600.1.1: Sink Device DPCD Register Check	✓

Execute Tests Cards... Close

- ◆ Current list of Sink Tests – Page 2

Sink Link Layer Compliance – Test 5.4.1

Main Video Stream Reconstruction Tests

Sink Link Layer Compliance

DP 1.4 Sink CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

All Category / Test Name

AUX Ch. Proto.

- 5.2.1.1: One byte DPCD Read ✓
- 5.2.1.2: Multi-byte DPCD Read ✓
- 5.2.1.3: One Byte DPCD Write ✓
- 5.2.1.4: Multi-byte DPCD Write ✓
- 5.2.1.5: Write EDID Offset ✓
- 5.2.1.6: Read One EDID Byte ✓
- 5.2.1.7: EDID Read ✓
- 5.2.1.8: Illegal AUX Request Syntax ✓
- 5.2.1.9: Glitch Rejection ✓
- 5.2.1.10: Interleaved EDID and DPCD Read ✓
- 5.2.1.11: Downstream Stop on MOT Reset ✓
- 5.2.1.12: Downstream Stop on Timeout ✓

Link Training

- 5.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds ✓
- 5.3.1.2: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence ✓
- 5.3.1.3: Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure During Clock Recovery Sequence ✓
- 5.3.1.4: Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence ✓
- 5.3.1.5: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence ✓
- 5.3.1.6: Lane Count Reduction ✓
- 5.3.1.7: Lane Count Increase ✓

Link Maint.

- 5.3.2.1: IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock. ✓
- 5.3.2.2: IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock ✓

Main Video

- 5.4.1.1: Pixel Data Reconstruction ✓
- 5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU ✓
- 5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU ✓
- 5.4.2: Main Video Stream Format Change Handling ✓

Power Management

- 5.4.3.1: Entering and Exiting Power Save Mode ✓
- 5.4.3.2: Resumption of Main Link Activity After Extended Idle ✓

Main Audio

- 5.4.4.2: Audio Startup and Format Change ✓
- 5.4.4.4: Audio InfoFrame Packet ✓
- 5.4.4.5: Audio Clock Recovery ✓
- 5.4.4.6: Audio Stream Reception ✓

DPCD

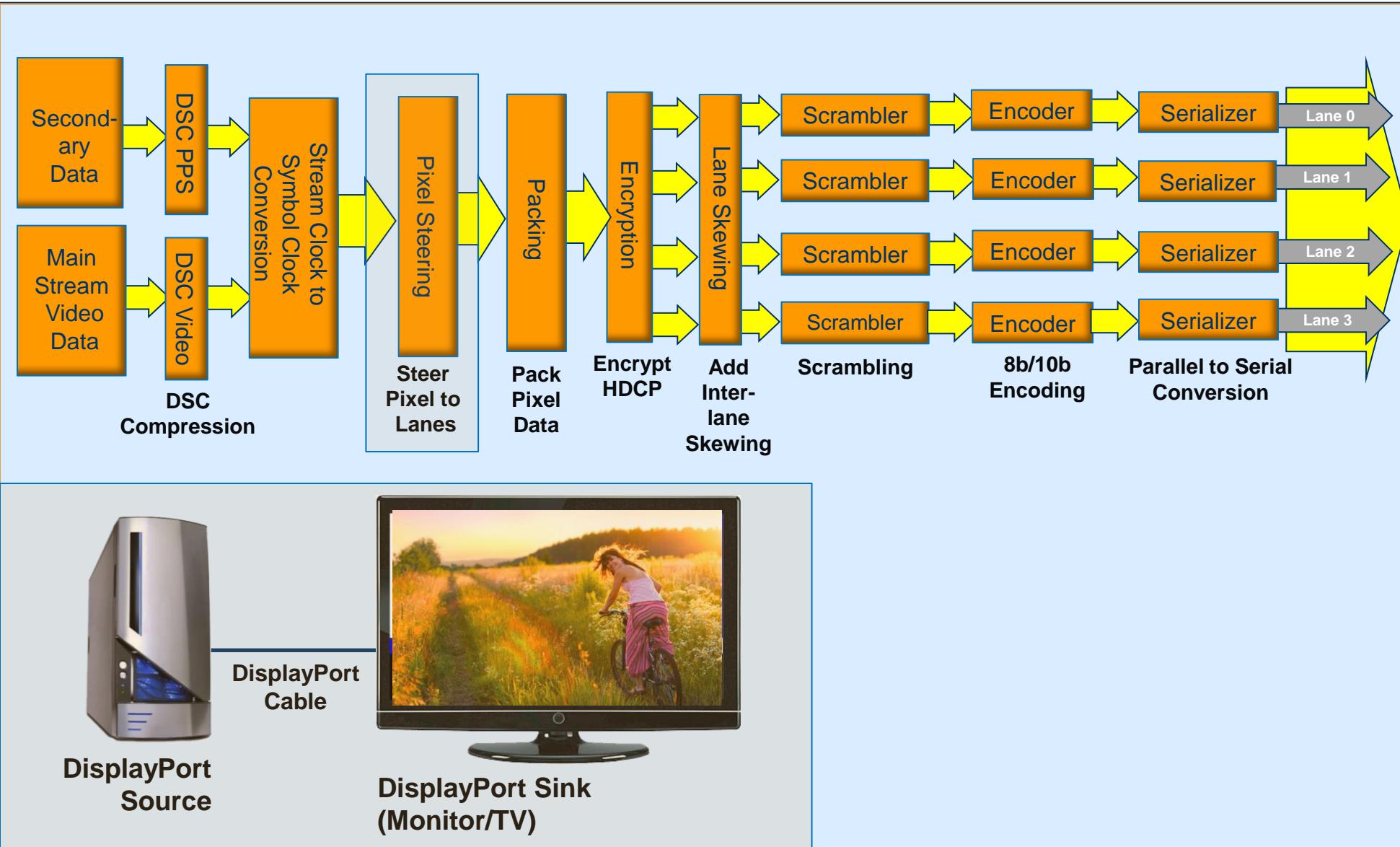
Test List

Execute Tests Cards...

Close

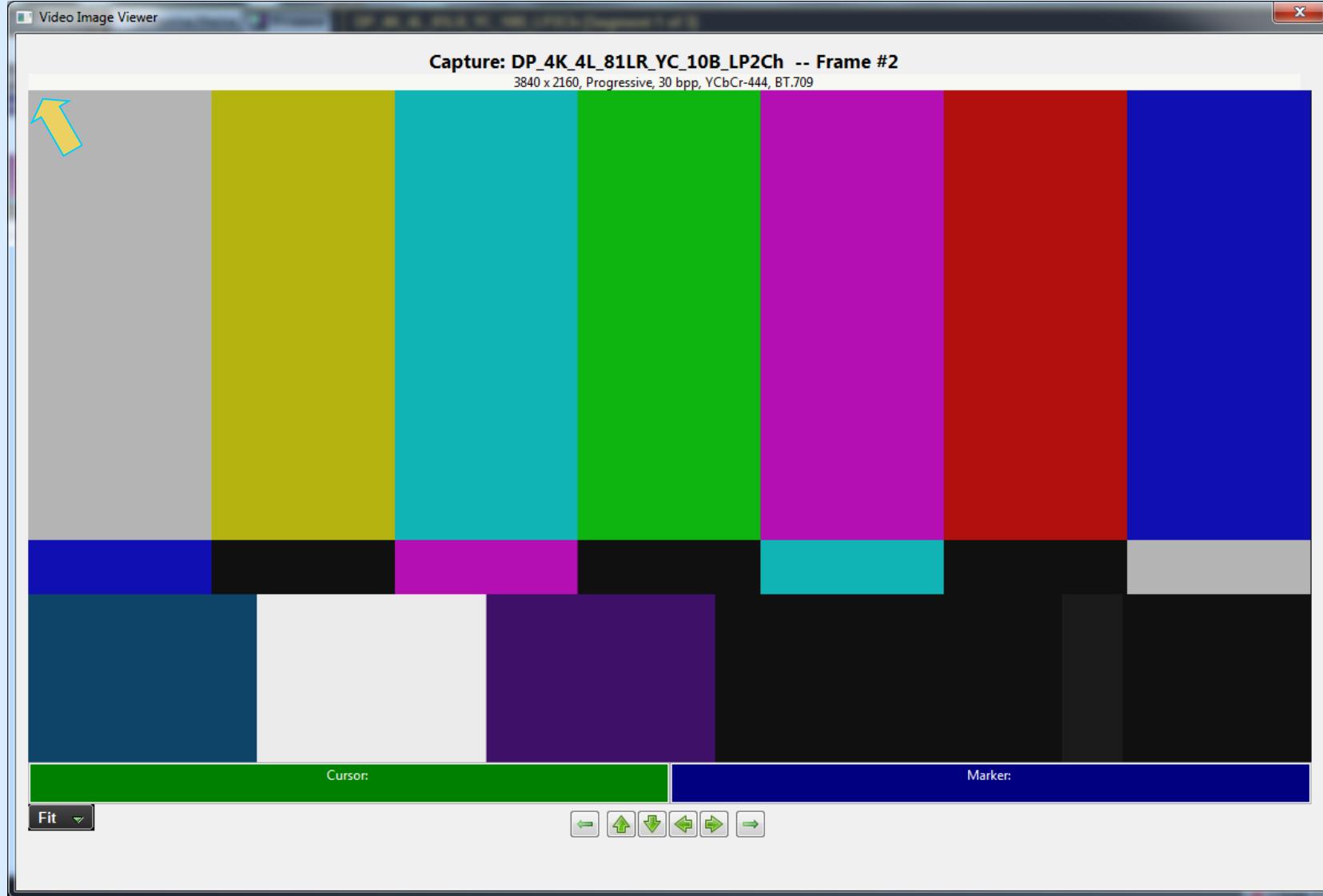
- ◆ Main Video Sink tests.

DisplayPort Main Link Stream Generation – Packing and Stuffing



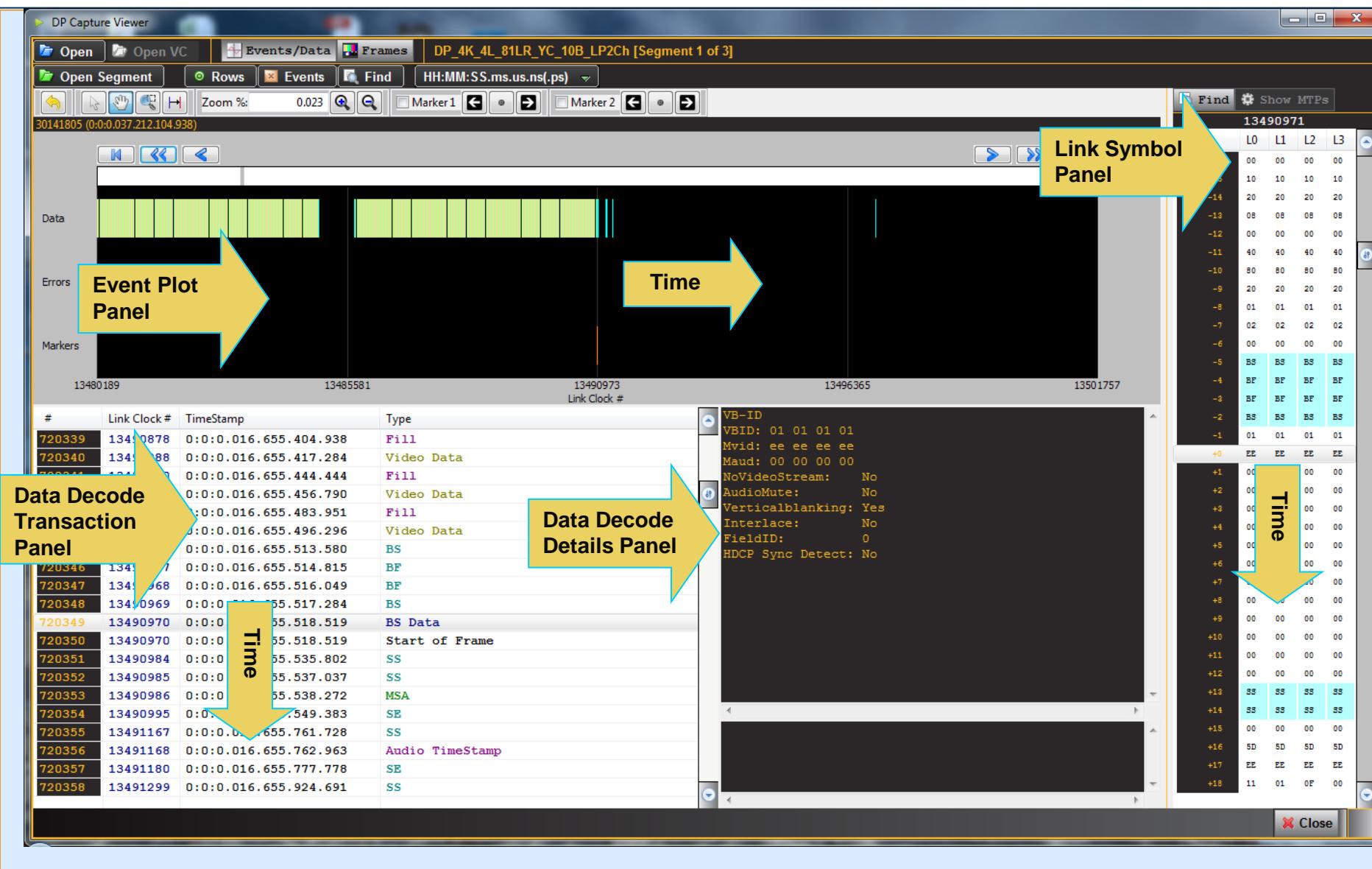
- **Two types of link symbols:**
 - **Data symbols** (e.g. pixel, metadata)
 - **Control symbols** (K-Chars) to frame the data symbols.
- **Pixel Steering** – The process of mapping the pixel data to each of the 2 or 4 lanes.

DisplayPort Main Link Protocol – Pixel Mapping



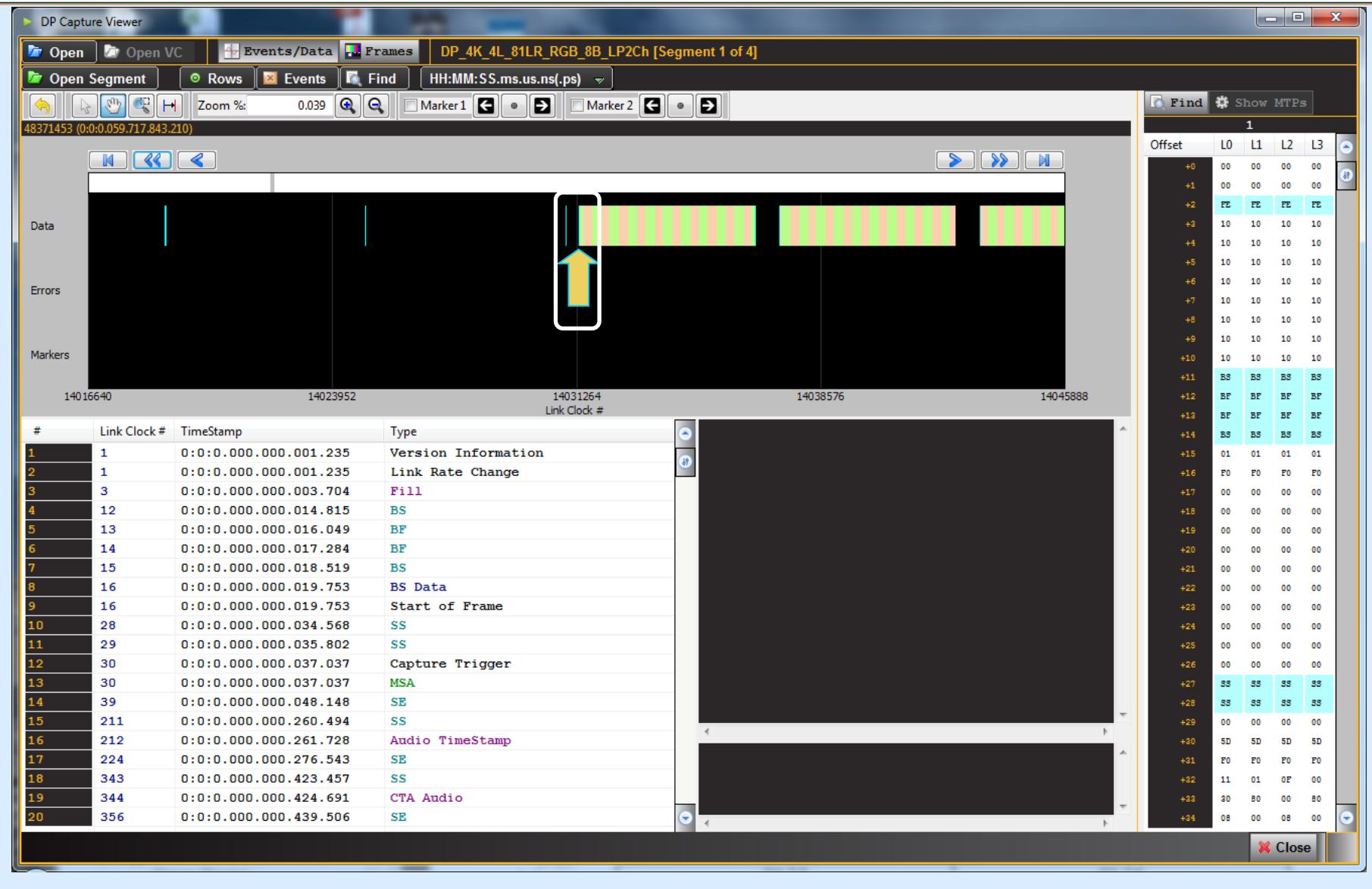
- Pixels data values are mapped “steered” on the lanes that are used.
- The video frame is a test pattern SMPTEbar.

DisplayPort Protocol Analyzer



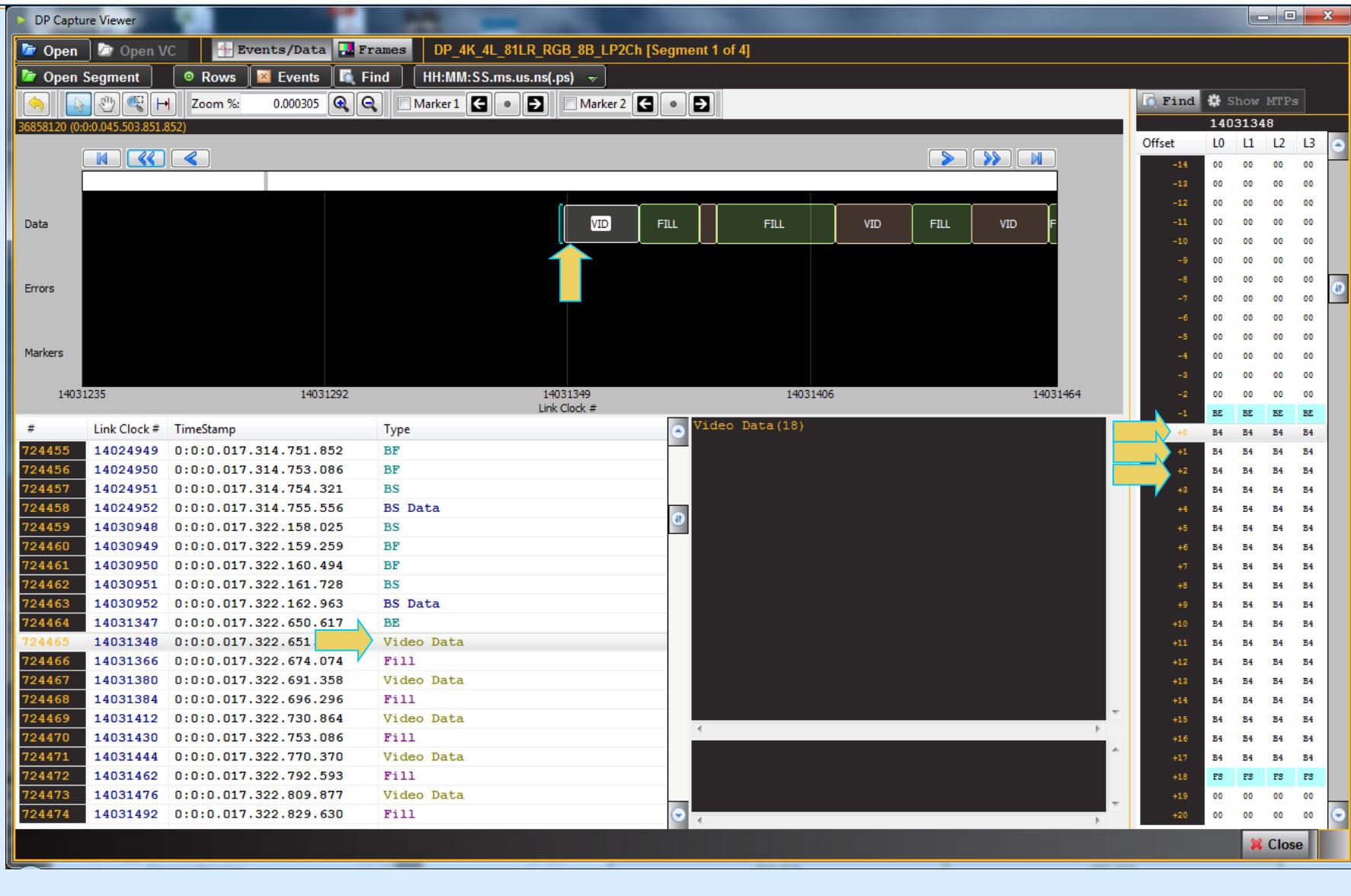
- Showing end of Video Display Frame, beginning of vertical blanking.
- Also showing the horizontal blanking region.

DisplayPort Main Link Protocol – Pixel Mapping, Steering (8 bit)



- Looking at the first pixel of a frame on a 4K video resolution with a link rate of 8.1Gb/s using four lanes using a color depth of 8 bits per component.

DisplayPort Main Link Protocol – Pixel Mapping, Steering (8 bit)



- Looking at the first video transfer unit in a frame.
- Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

Lane0 Lane1 Lane2 Lane3

R0-7:0 R1-7:0 R2-7:0 R3-7:0

G0-7:0 G1-7:0 G2-7:0 G3-7:0

B0-7:0 B1-7:0 B2-7:0 B3-7:0

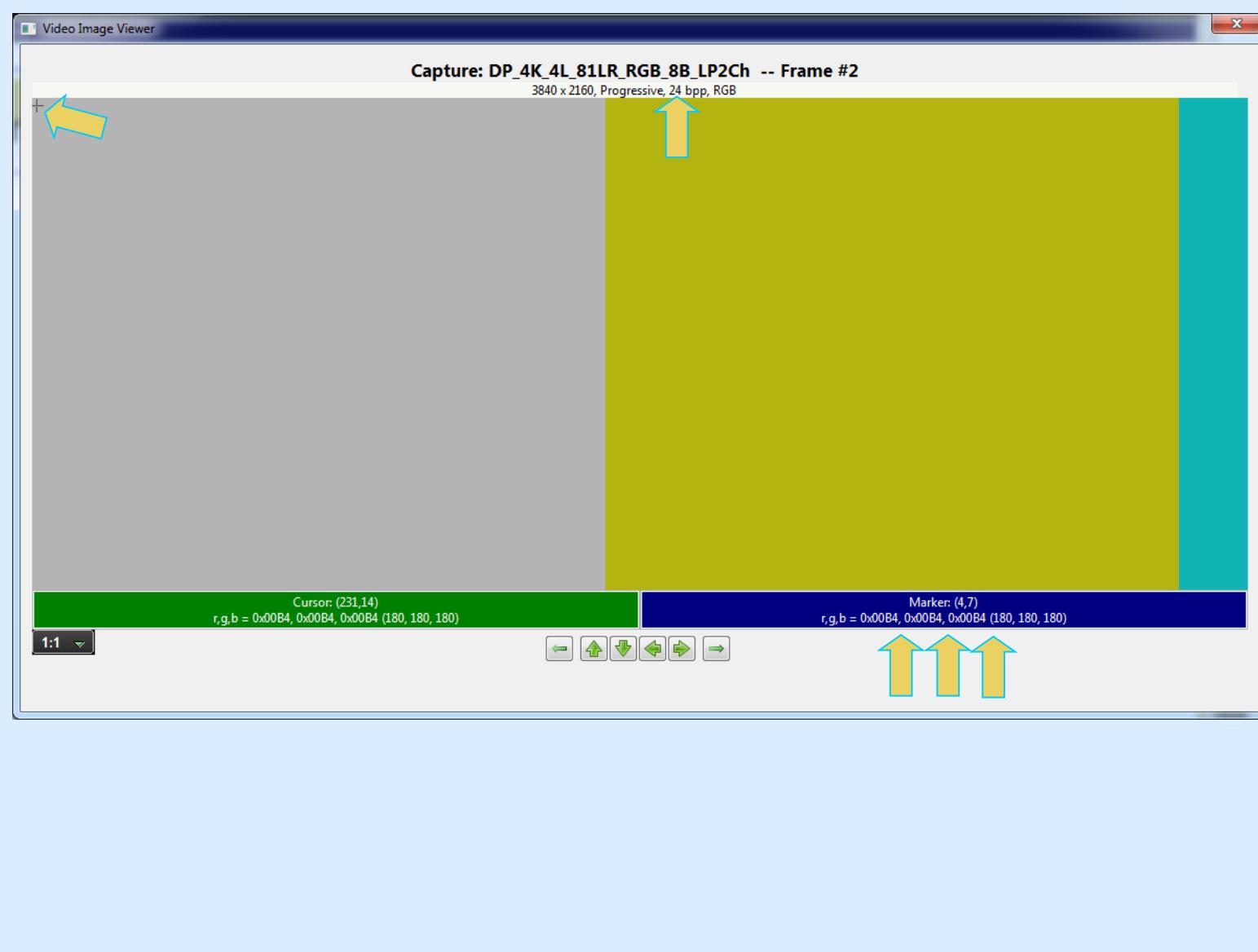
Lane0 Lane1 Lane2 Lane3

R0-B4 R1-B4 R2-B4 R3-B4

G0-B4 G1-B4 G2-B4 G3-B4

B0-B4 B1-B4 B2-B4 B3-B4

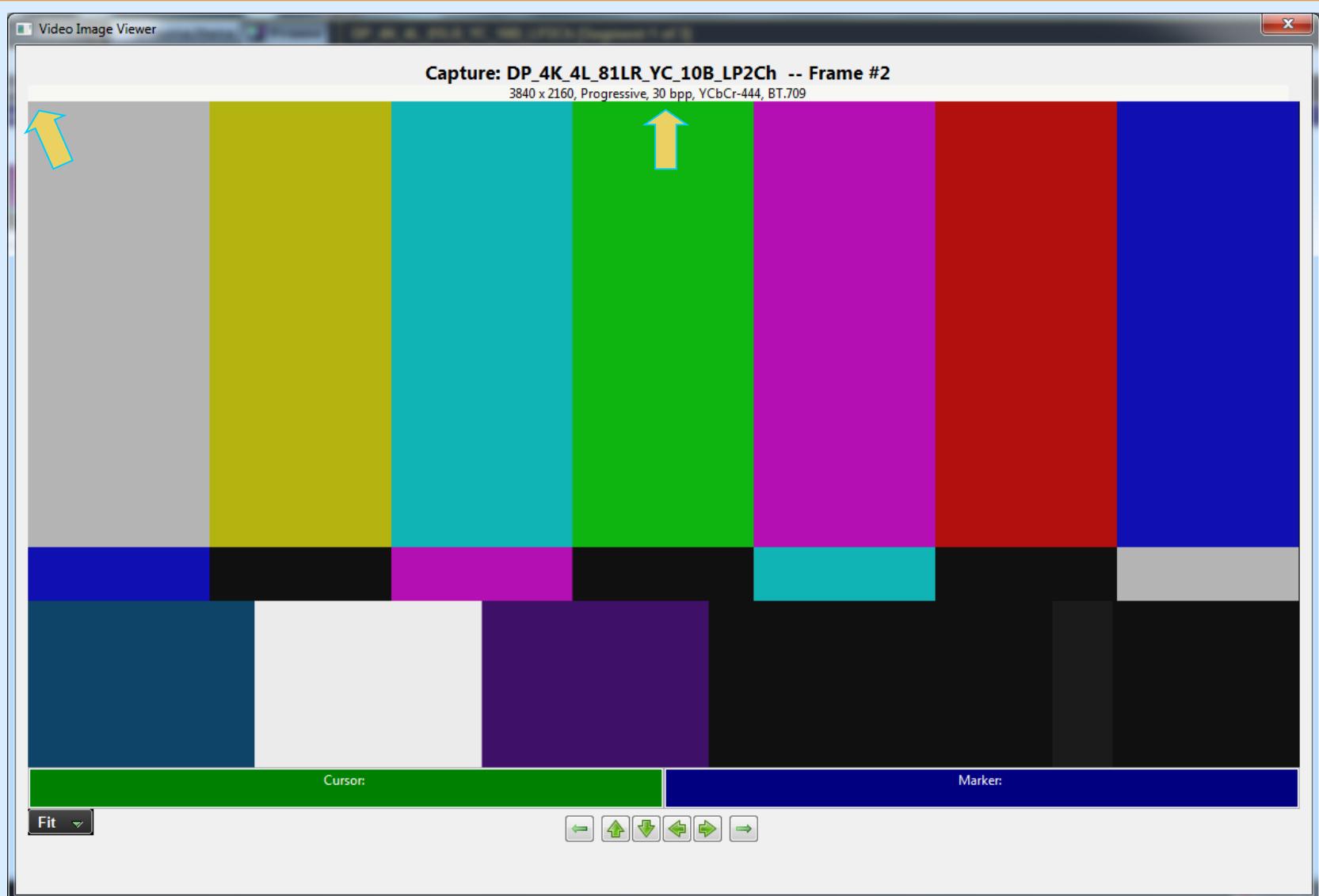
DisplayPort Main Link Protocol – Pixel Mapping Steering (8 bit)



- Looking at the first video transfer unit in a frame.
- Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

Lane0	Lane1	Lane2	Lane3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R0-B4	R1-B4	R2-B4	R3-B4
G0-B4	G1-B4	G2-B4	G3-B4
B0-B4	B1-B4	B2-B4	B3-B4
B 4			
1011 0100	1011 0100	1011 0100	1011 0100
B 4			
1011 0100	1011 0100	1011 0100	1011 0100
B 4			
1011 0100	1011 0100	1011 0100	1011 0100

DisplayPort Main Link Protocol – Pixel Mapping (10bit Color Depth (30bpp))



- Pixels data values are spread out mapped “steered” on the lanes that are used.
- The video frame is a test pattern SMPTEbar.
- Example 30 bits per pixel bit depth.

DisplayPort Main Link Protocol – Pixel Mapping, Steering (10 bit–4 Lanes)

DP_4K_4L_81LR_RGB_10B_LP2Ch [Segment 1 of 4]

HH:MM:SS.ms.us.ns(.ps)

Marker 1 | Marker 2

VID FILL VID FILL VID FILL VID

14031369 Link Clock #

14031426

14031484

Type

- BS Data
- SS
- Audio Stream
- SE
- BS
- BF
- BF
- BS
- BS Data
- BE
- Video Data
- Fill

Video Data(22)

-3	00	00	00	00
-2	00	00	00	00
-1	BE	BE	BE	BE
+0	B4	B4	B4	B4
+1	2D	2D	2D	2D
+2	0B	0B	0B	0B
+3	42	42	42	42
+4	D0	D0	D0	D0
+5	B4	B4	B4	B4

Offset

Offset	L0	L1	L2	L3
-16	00	00	00	00
-15	00	00	00	00
-14	00	00	00	00
-13	00	00	00	00
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
00	00	00	00	00
+1	2D	2D	2D	2D
+2	0B	0B	0B	0B
+3	42	42	42	42
+4	D0	D0	D0	D0
+5	B4	B4	B4	B4
+6	2D	2D	2D	2D
+7	0B	0B	0B	0B
+8	42	42	42	42
+9	D0	D0	D0	D0
+10	B4	B4	B4	B4
+11	2D	2D	2D	2D
+12	0B	0B	0B	0B
+13	42	42	42	42
+14	D0	D0	D0	D0
+15	B4	B4	B4	B4
+16	2D	2D	2D	2D
+17	0B	0B	0B	0B
+18	42	42	42	42

Find Show MTPs

14031368

14031369

14031426

14031484

Cursor: (1065,13) r,g,b = 0x02D0, 0x02D0, 0x0040 (720,720,64)

Marker: (0,0) r,g,b = 0xD2D0, 0xD2D0, 0xD2D0 (720,720,720)

Video Image Viewer

Capture: DP_4K_4L_81LR_RGB_10B_LP2Ch -- Frame #2
3840 x 2160, Progressive, 30 bpp, RGB

Lane 0 Lane 1 Lane 2 Lane 3

R0-9:2 R1-9:2 R2-9:2 R3-9:2

R0-1:0|G0-9:4 R1-1:0|G1-9:4 R2-1:0|G2-9:4 R3-1:0|G3-9:4

G0-3:0|B0-9:6 G1-3:0|B1-9:6 G2-3:0|B2-9:6 G3-3:0|B3-9:6

B0-5:0|R4-9:8 B1-5:0|R5-9:8 B2-5:0|R6-9:8 B3-5:0|R7-9:8

R4-7:0 R5-7:0 R6-7:0 R7-7:0

Lane 0 Lane 1 Lane 2 Lane 3

Pixel → B 4
Values 1011 0100 1011 0100 1011 0100 1011 0100

2D0 → 2 D
0010 1101 0010 1101 0010 1101 0010 1101

2D0 → 0 B
0000 1011 0000 1011 0000 1011 0000 1011

2D0 → 4 2
0100 0010 0100 0010 0100 0010 0100 0010

2D0 → D 0
1101 0000 1100 0000 1100 0000 1100 0000

Sink Link Layer Compliance – Test 5.4.1.1 Pixel Data Reconstruction

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 03_27_2018_16_07_26_sink
Date Tested: March 27, 2018 4:07 PM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:
Model Name:
Port Tested: 1

HTML Report

Test Results

Test Name / Details

5.4.1.1: Pixel Data Reconstruction

Iter 01:

- 01: Link Training at lane count = 1 and low lane rate
- 02: Test validation when lane count = 1 and 6 bpc
- 03: Test validation when lane count = 1 and 8 bpc
- 04: Test validation when lane count = 1 and 10 bpc
- 05: Test validation when lane count = 1 and 12 bpc
- 06: Test validation when lane count = 1 and 16 bpc
- 07: Link Training at lane count = 2 and low lane rate
- 08: Test validation when lane count = 2 and 6 bpc
- 09: Test validation when lane count = 2 and 8 bpc
- 10: Test validation when lane count = 2 and 10 bpc
- 11: Test validation when lane count = 2 and 12 bpc
- 12: Test validation when lane count = 2 and 16 bpc
- 13: Link Training at lane count = 4 and low lane rate
- 14: Test validation when lane count = 4 and 6 bpc
- 15: Test validation when lane count = 4 and 8 bpc
 - TEST_CRC_R_Cr field equals to the Reference Source's internal CRC calculations (0xF58C).
 - TEST_CRC_G_Y field equals to the Reference Source's internal CRC calculations (0xA3D3).
 - TEST_CRC_B_Cb field equals to the Reference Source's internal CRC calculations (0x0720).
- 16: Test validation when lane count = 4 and 10 bpc
- 17: Test validation when lane count = 4 and 12 bpc
- 18: Test validation when lane count = 4 and 16 bpc

5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU

Iter 01:

- 01: Initial Link Training at maximum link rate and lane count success
 - HPD is asserted
 - Reference Source receives AUX_ACK at 1 attempts
 - Reference Source receives AUX ACK from either write request

Open ACA Data 5.4.1.1: Pixel Data Reconstruction

Instrument: SS980B [10.30.196.39]

Continue Test Execution Close



- ◆ Example test results for pixel data reconstruction.
- ◆ CRC check and visual check of received video data.
- ◆ Read CRC values in DPCD registers.
- ◆ Details show subtest with Lane count of 4 with 8 bits per component.

Sink Link Layer Compliance – Test 5.4.1.2 – Main Stream Data Unpacking

DP 1.4 Sink CT 1.4 Core R1.0

CDF Entry Test Selection Test Options / Preview

Instrument: SS980B [10.30.196.39]

Test List

All Execute Tests Cards...

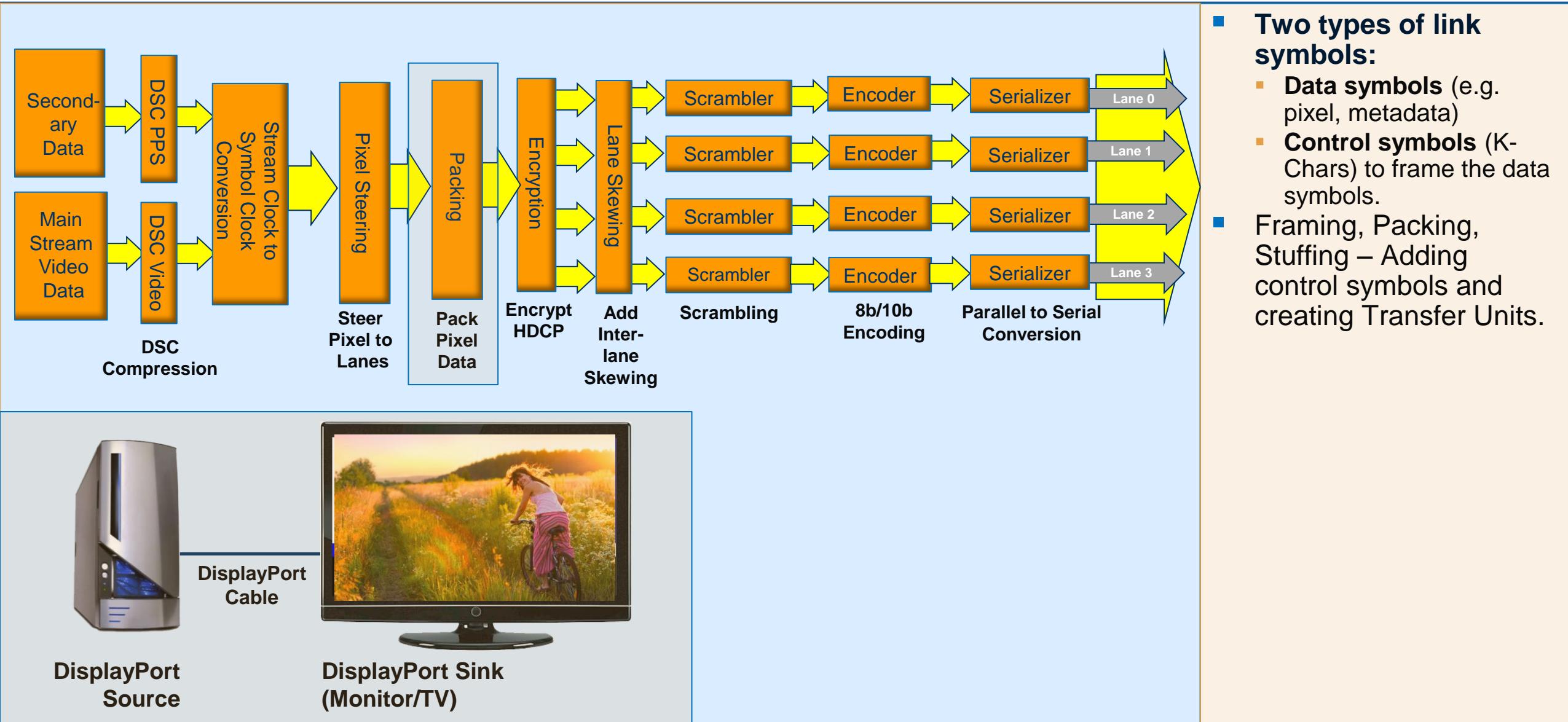
Category / Test Name

- AUX Ch. Proto.
 - 5.2.1.1: One byte DPCD Read ✓
 - 5.2.1.2: Multi-byte DPCD Read ✓
 - 5.2.1.3: One Byte DPCD Write ✓
 - 5.2.1.4: Multi-byte DPCD Write ✓
 - 5.2.1.5: Write EDID Offset ✓
 - 5.2.1.6: Read One EDID Byte ✓
 - 5.2.1.7: EDID Read ✓
 - 5.2.1.8: Illegal AUX Request Syntax ✓
 - 5.2.1.9: Glitch Rejection ✓
 - 5.2.1.10: Interleaved EDID and DPCD Read ✓
 - 5.2.1.11: Downstream Stop on MOT Reset ✓
 - 5.2.1.12: Downstream Stop on Timeout ✓
- Link Training
 - 5.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds ✓
 - 5.3.1.2: Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence ✓
 - 5.3.1.3: Successful Link Training to a Lower Link Rate Due to Clock Recovery Lock Failure During Clock Recovery Sequence ✓
 - 5.3.1.4: Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence ✓
 - 5.3.1.5: Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence ✓
 - 5.3.1.6: Lane Count Reduction ✓
 - 5.3.1.7: Lane Count Increase ✓
- Link Maint.
 - 5.3.2.1: IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock. ✓
 - 5.3.2.2: IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock ✓
- Main Video
 - 5.4.1.1: Pixel Data Reconstruction ✓
 - 5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU ✓
 - 5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU ✓
 - 5.4.2: Main Video Stream Format Change Handling ✓
- Power Management
 - 5.4.3.1: Entering and Exiting Power Save Mode ✓
 - 5.4.3.2: Resumption of Main Link Activity After Extended Idle ✓
- Main Audio
 - 5.4.4.2: Audio Startup and Format Change ✓
 - 5.4.4.4: Audio InfoFrame Packet ✓
 - 5.4.4.5: Audio Clock Recovery ✓
 - 5.4.4.6: Audio Stream Reception ✓
- DPCD

Close

◆ Main Video Test – Main Stream Data Unpacking

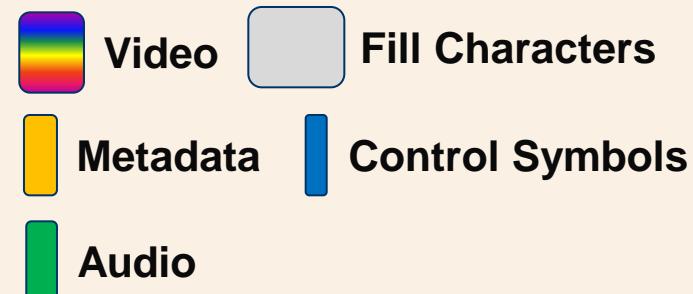
DisplayPort Main Link Stream Generation – Packing and Stuffing



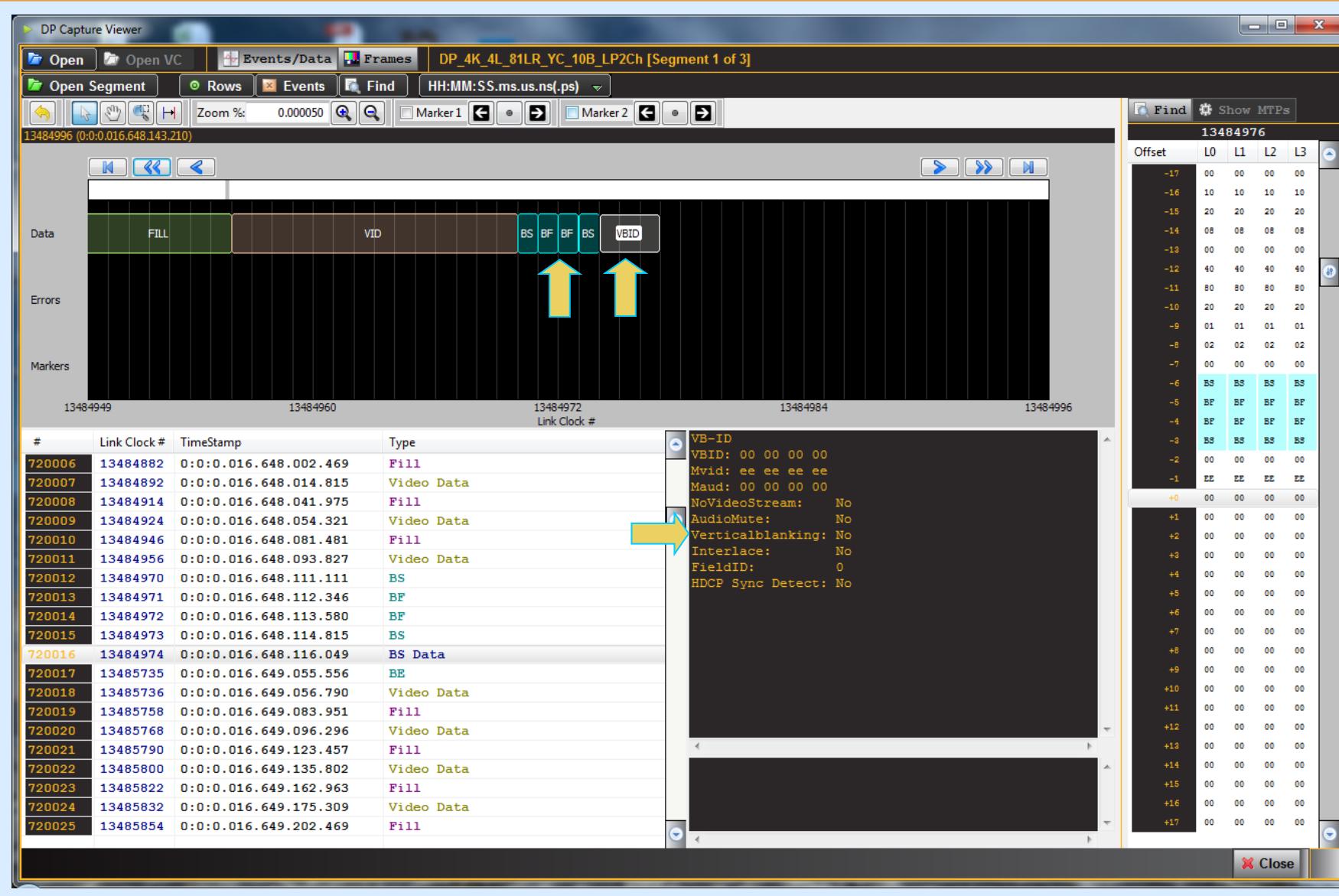
DisplayPort Main Link Protocol – One Video Frame



- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period.
- There is a lot of **over capacity**. **Fill characters** are zeros for filling up (stuffing) the unused link symbols.

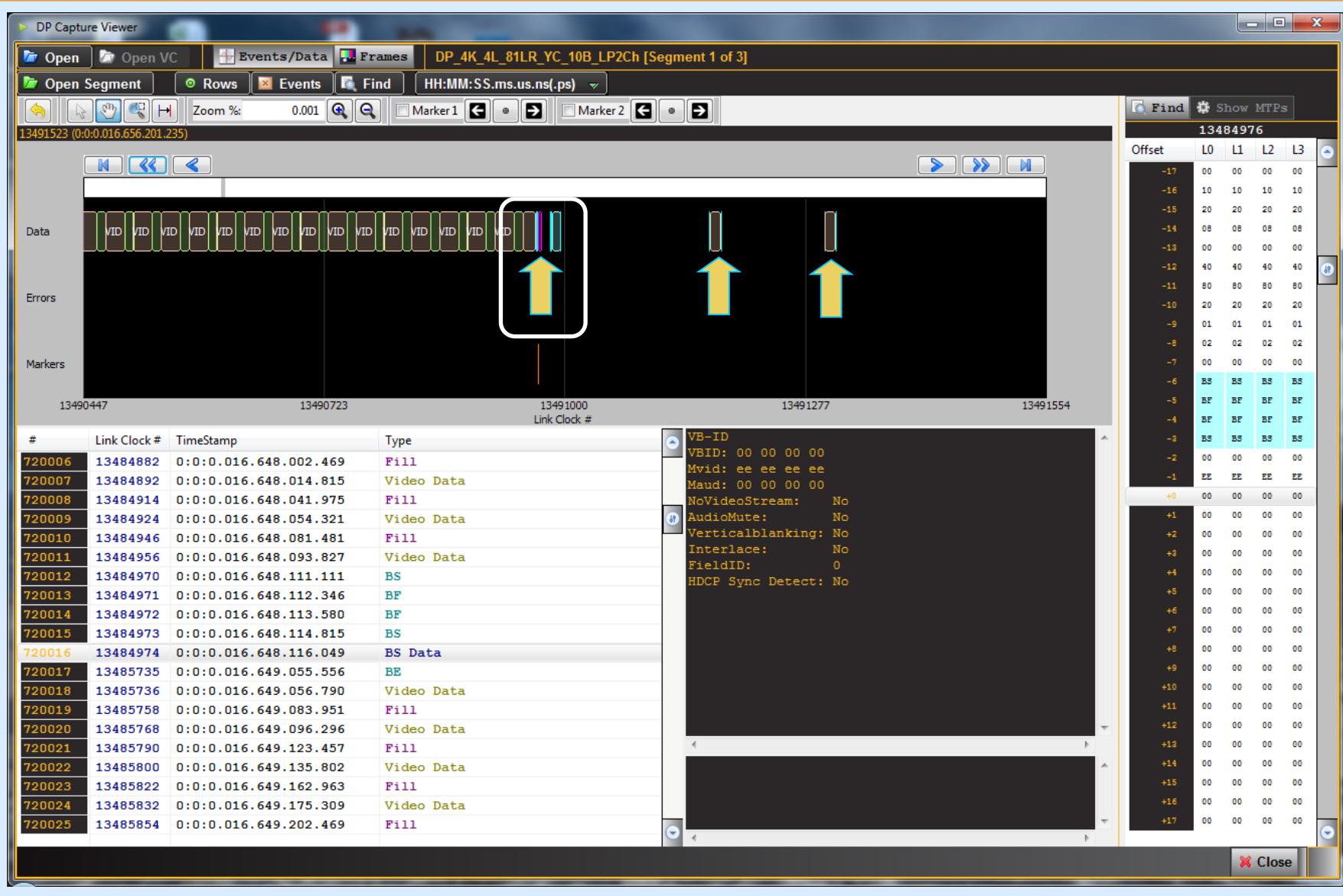


DisplayPort Main Link Protocol – Horizontal Blanking



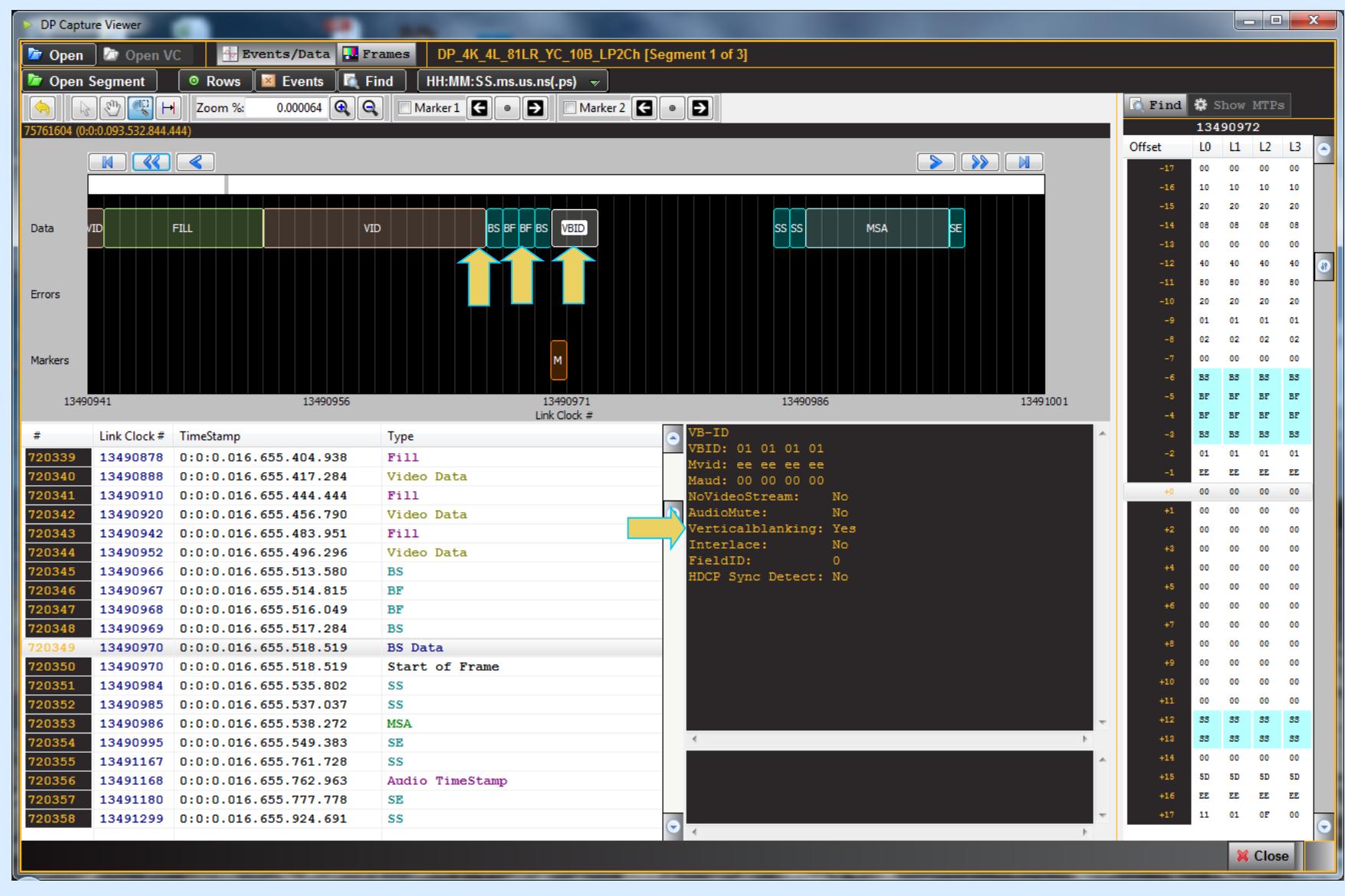
- **Two types of link symbols:**
 - **Data symbols** (e.g. pixel, metadata)
 - **Control symbols** (K-Chars) to frame the data symbols.
- Horizontal blanking is preceded by the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.
- The VBID data indicates that this blanking period is not Vertical Blanking.

DisplayPort Main Link Protocol – Framing Control Symbols



- Showing end of Video Display Frame, beginning of vertical blanking.
- Fill regions are visible as are some of the protocol elements in the vertical blanking region.

DisplayPort Main Link Protocol – Framing Control Symbols



- Showing end of Video Display Frame, beginning of vertical blanking.
- Last video element is preceded by a set of Fill Characters.
- Then the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.
- VBID details shown in Data Decode Details panel indicating Vertical Blanking = Yes.

Sink Link Layer Compliance – Test 5.4.1.2 Stream Unpacking/Unstuffing

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_55_18_sink
Date Tested: April 23, 2018 11:55 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	Pass
Iter 01: <ul style="list-style-type: none">01: Initial Link Training at maximum link rate and lane count success<ul style="list-style-type: none">HPD is assertedReference Source receives AUX_ACK at 1 attemptsReference Source receives AUX ACK from either write requestAUX Read 0x2201 (MAX_LINK_RATE) = 0x1eAUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4Link Training at lane count 4 and link rate 8.1 successful02: CRC check or Visual check<ul style="list-style-type: none">TEST_CRC_R_Cr field equals to the Reference Source's internal CRC calculations (0x731C).TEST_CRC_G_Y field equals to the Reference Source's internal CRC calculations (0x0A08).TEST_CRC_B_Cb field equals to the Reference Source's internal CRC calculations (0x352B).	Pass
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	Pass

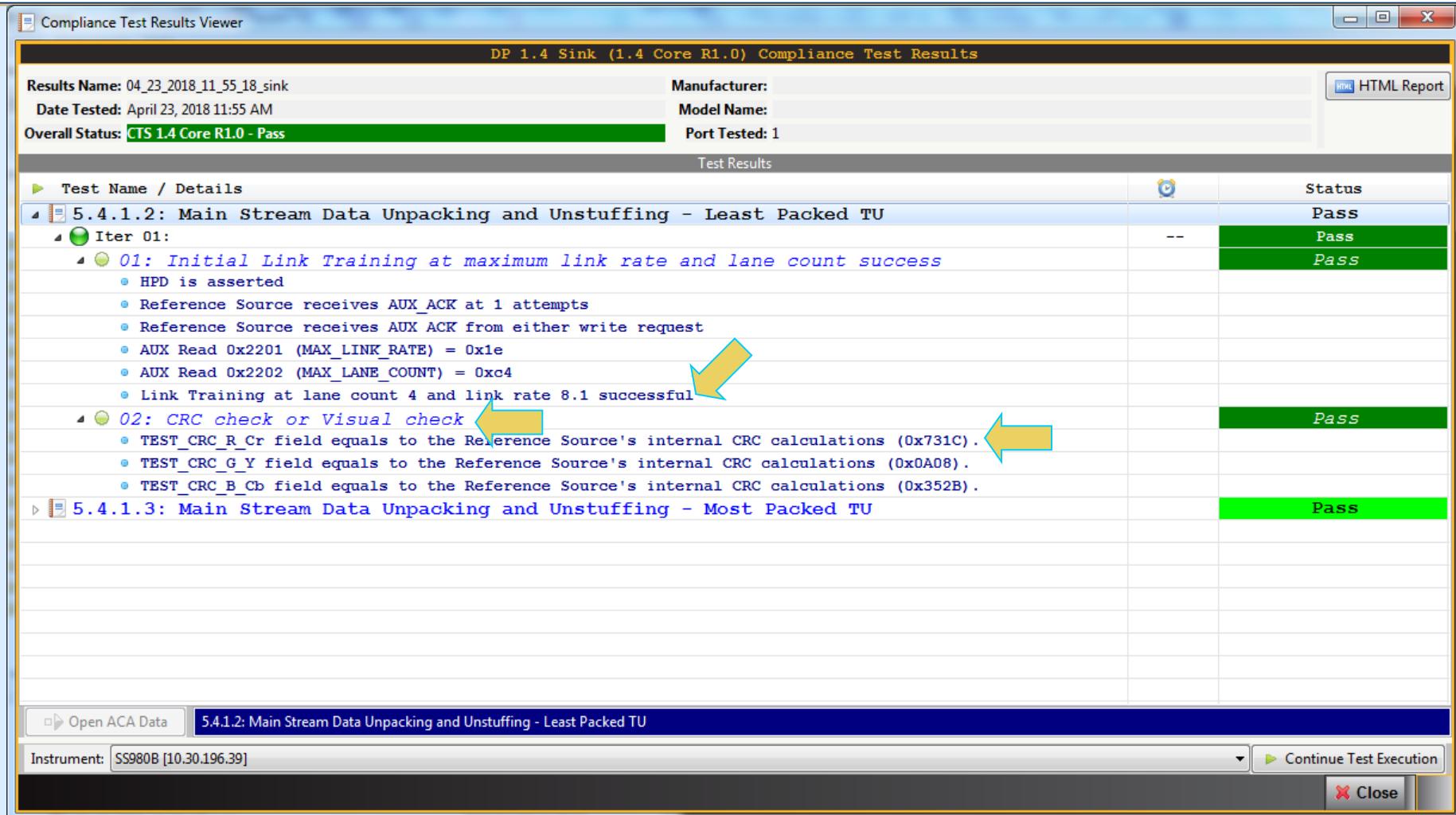
Open ACA Data

5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU

Instrument: SS980B [10.30.196.39]

Continue Test Execution

Close



- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Least Packed** means less video than fill characters per transfer unit.
- ◆ Uses 480p on 4 Lanes at 8.1Gb/s.

Sink Link Layer Compliance – Test 5.4.1.3 Stream Unpacking/Unstuffing

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 04_23_2018_11_55_18_sink
Date Tested: April 23, 2018 11:55 AM
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:
Model Name:
Port Tested: 1

HTML Report

Test Results

	Status
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	Pass
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	Pass
	Pass
Iter 01:	Pass
01: Link Training at lane count = 1 and low lane rate	Pass
HPD is asserted	Pass
Reference Source receives AUX_ACK at 1 attempts	Pass
Reference Source receives AUX ACK from either write request	Pass
AUX Read 0x2201 (MAX_LINK_RATE) = 0x1	Pass
AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4	Pass
Link Training at lane count 1 and link rate 1.62 successful	Pass
02: Test validation when lane count = 1	Pass
03: Link Training at lane count = 2 and low lane rate	Pass
04: Test validation when lane count = 2	Pass
05: Link Training at lane count = 4 and low lane rate	Pass
HPD is asserted	Pass
Reference Source receives AUX_ACK at 1 attempts	Pass
Reference Source receives AUX ACK from either write request	Pass
AUX Read 0x2201 (MAX_LINK_RATE) = 0x1	Pass
AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4	Pass
Link Training at lane count 4 and link rate 1.62 successful	Pass
06: Test validation when lane count = 4	Not Judged

Open ACA Data

5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU

Instrument: SS980B [10.30.196.39]

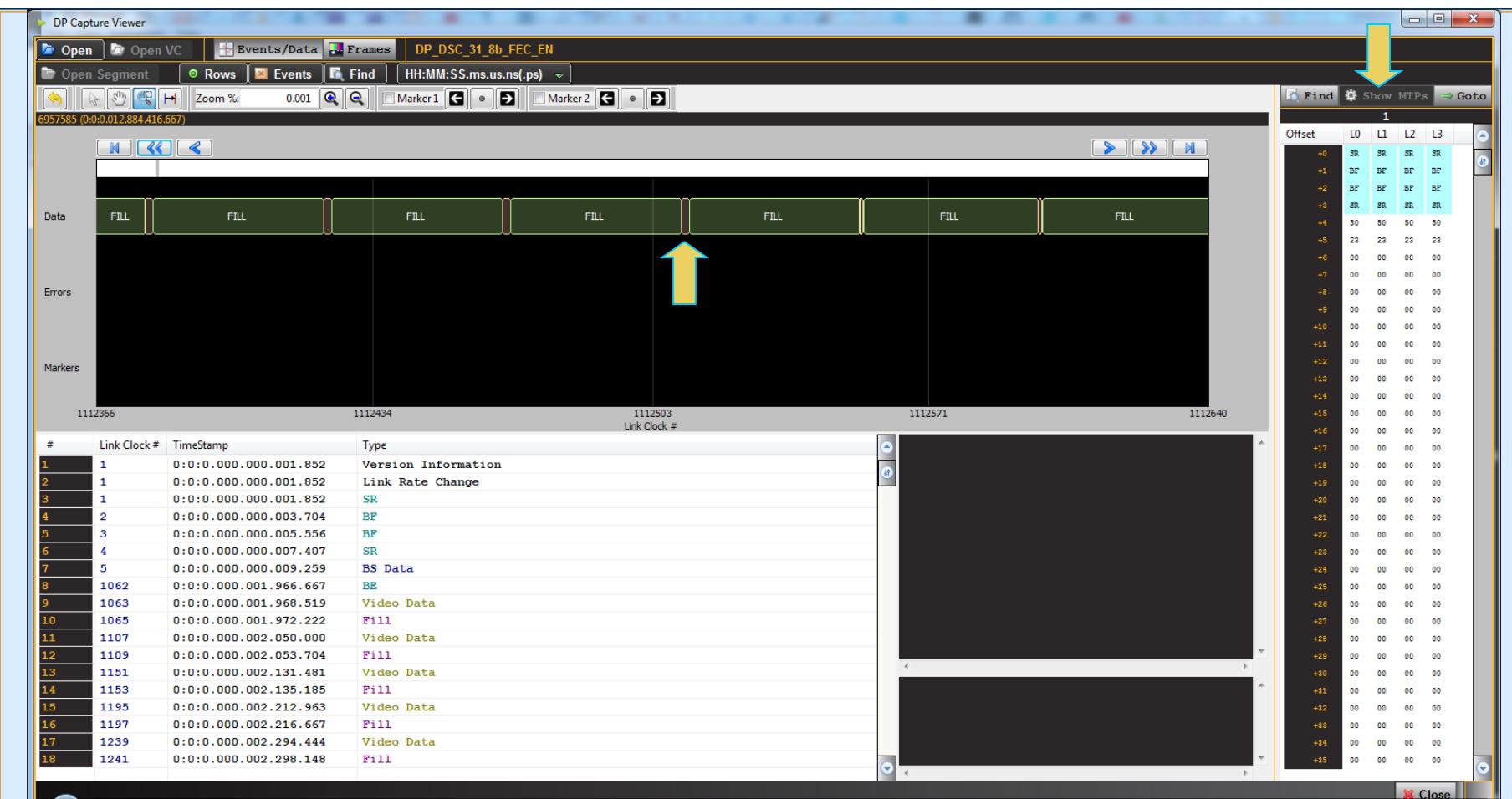
Continue Test Execution

Close



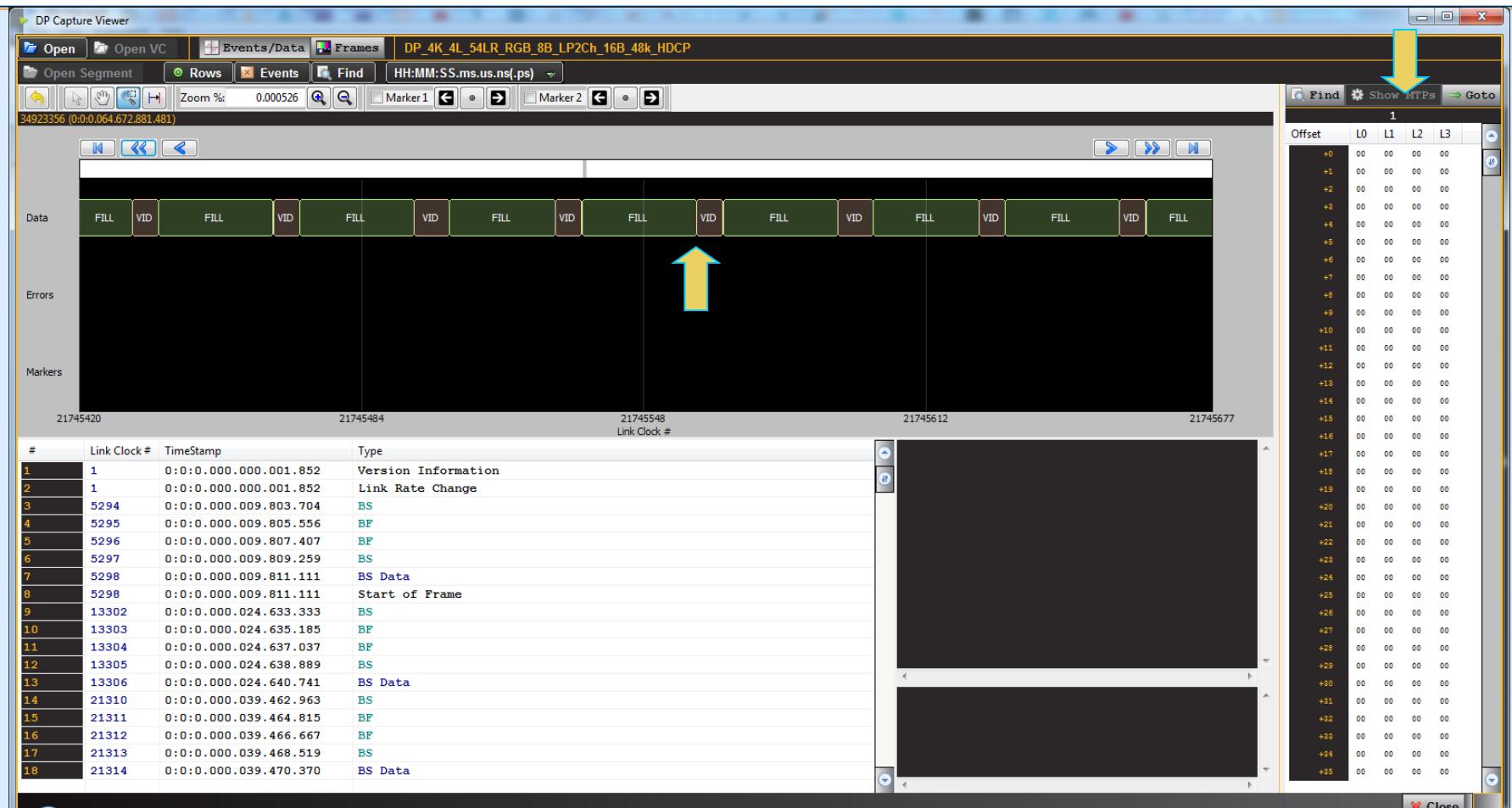
- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Most Packed** means more video than fill characters per transfer unit.
- ◆ Test uses high resolution format on 4 lanes at 1.62Gb/s link rate.

DisplayPort Main Link Protocol – Transfer Unit (Least Packed)



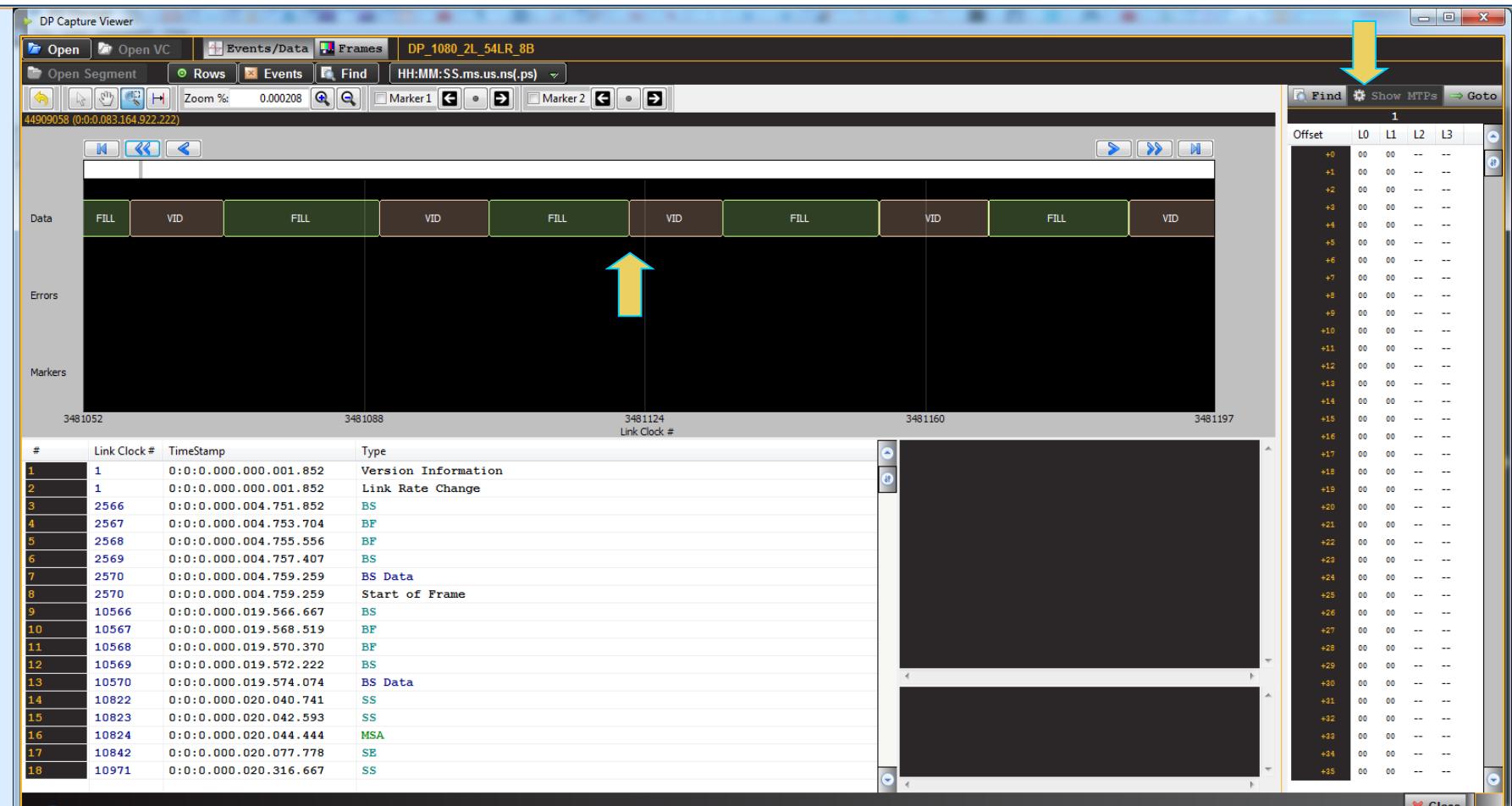
- Example shows 4 lane example at 8.1Gb/s link rate with a 480p format at 8 bit color depth.
- Transfer units are composed of almost entirely fill characters.

DisplayPort Main Link Protocol – Transfer Unit (More Packed)



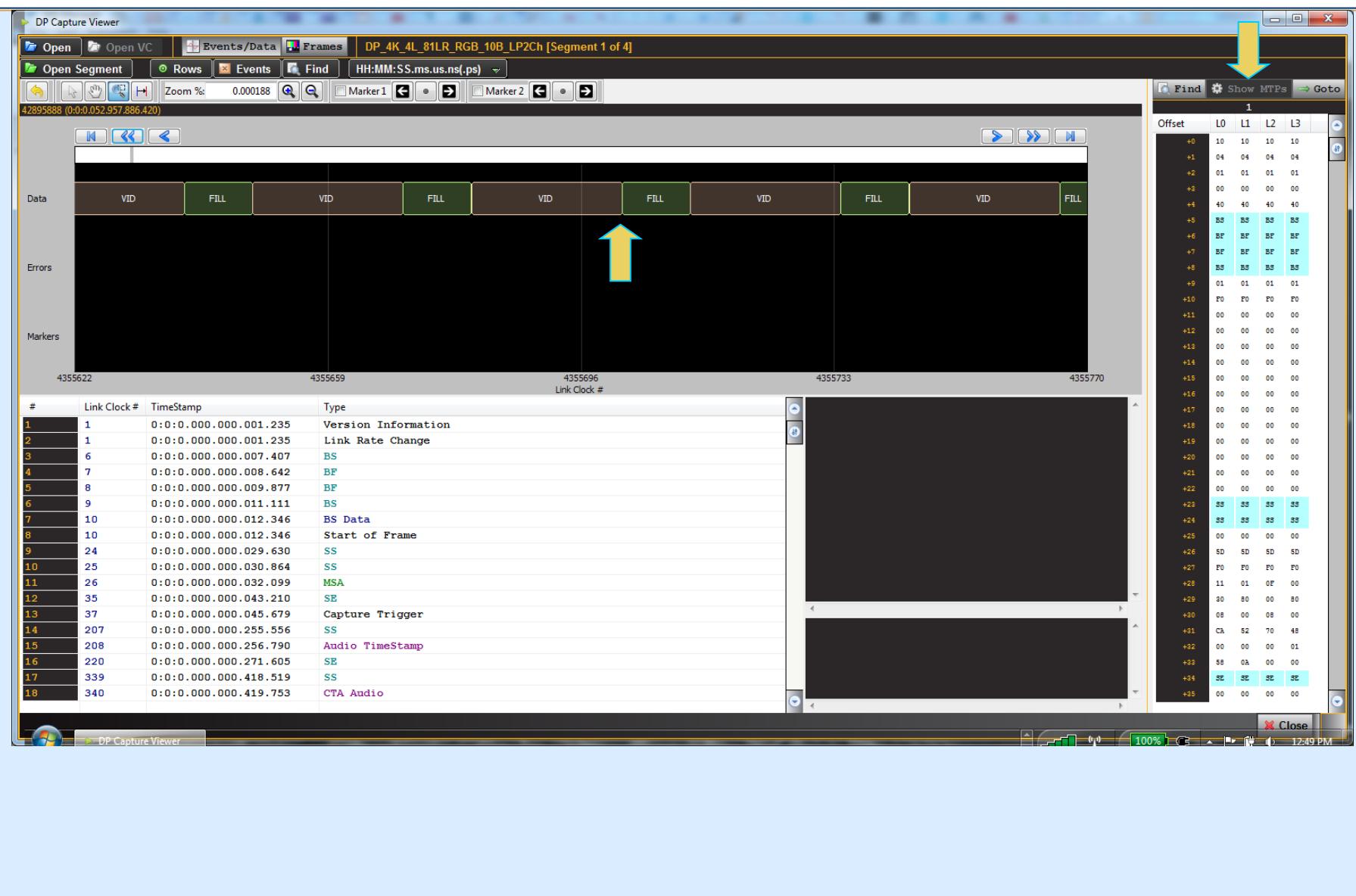
- Example shows 4 lane example at 5.4Gb/s link rate with a 4K format at 8 bit color depth.
- Transfer units are predominantly fill characters for stuffing.

DisplayPort Main Link Protocol – Transfer Unit (More Packed)



- Example shows **2 lane** example at 5.4Gb/s link rate with a 1080p format with 8 bit color depth.
- Transfer units are nearly equal amounts of video and fill characters.

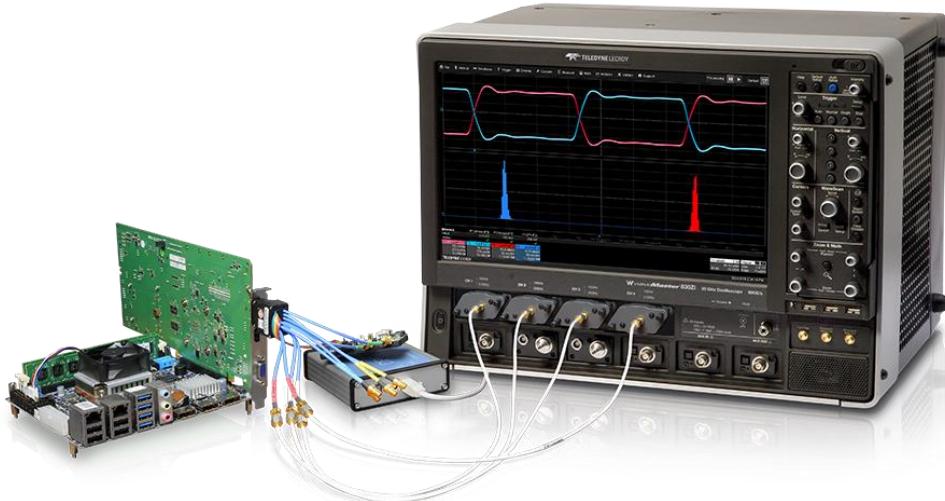
DisplayPort Main Link Protocol – Transfer Unit (Most Packed)



- Example shows 4 lane example at 8.1Gb/s link rate with a 4K format with 10 bit color depth.
- Transfer units are mostly video.

Teledyne LeCroy – DisplayPort Phy & Protocol Testing

DisplayPort Phy
Compliance Testing
at 8.1Gbps Link Rate



WaveMaster

DisplayPort Protocol
Testing at
8.1Gbps Link Rate



980B Test Platform

Thank you for attending
Questions?

Please contact me, Neal Kendall at:
neal.kendall@teledyne.com
If you have any questions.

Please Check out our DisplayPort “Essentials of” Webinars:

- ◆ [Essentials of DisplayPort Protocols](#)
- ◆ [Essentials of HDCP 2.2 Protocols](#)
- ◆ [Essentials of DisplayPort Display Stream \(DSC\) Protocols](#)