HD49343NP/HNP

CDS/PGA & 12-bit A/D Converter

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Rev.2.00
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Description

The HD49343NP/HNP is a CMOS IC that provides CDS-PGA analog processing (CDS/PGA) suitable for CCD camera digital signal processing systems together with a 12-bit A/D converter in a single chip.

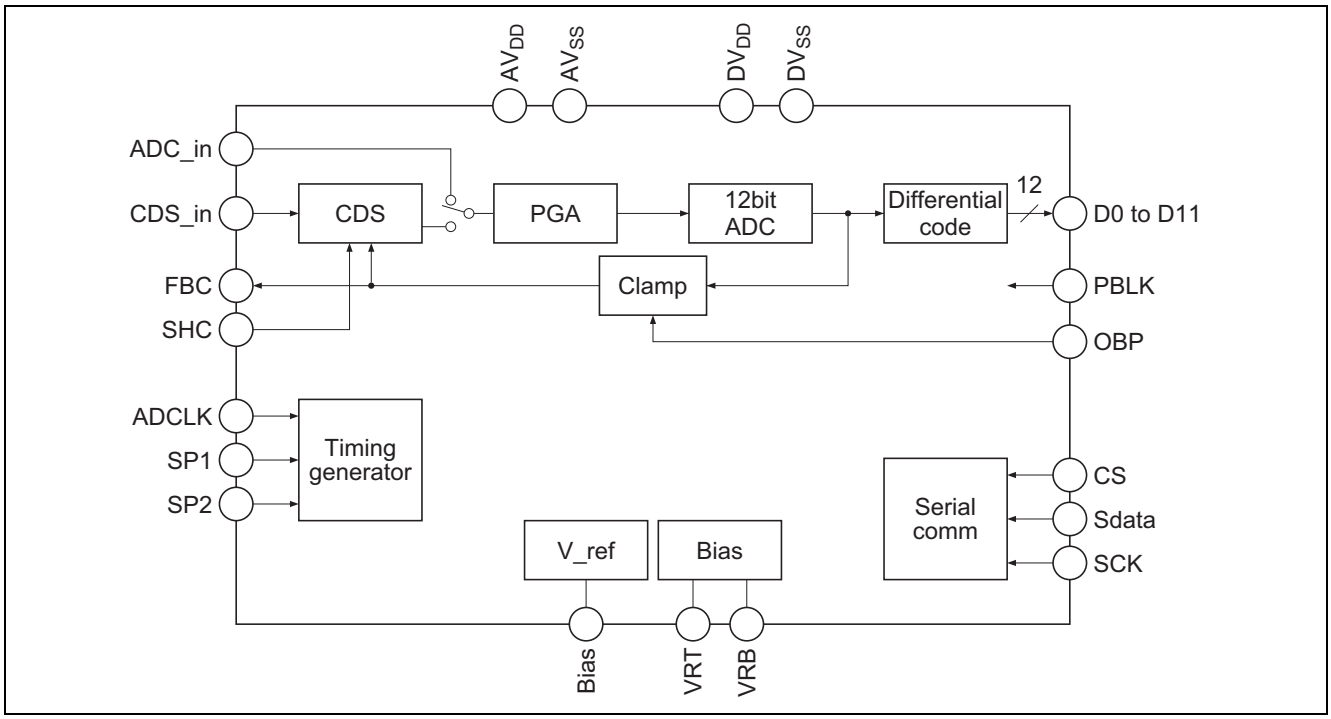
Functions

- Correlated double sampling
- PGA
- Serial interface control
- 12-bit ADC
- Operates using only the 3 V, ADC output
- Corresponds to switching mode of power dissipation and operating frequency
  HD49343HNP : 200 mW, f_max: 36 MHz
  HD49343NP : 120 mW, f_max: 25 MHz
- QFN 36-pin package

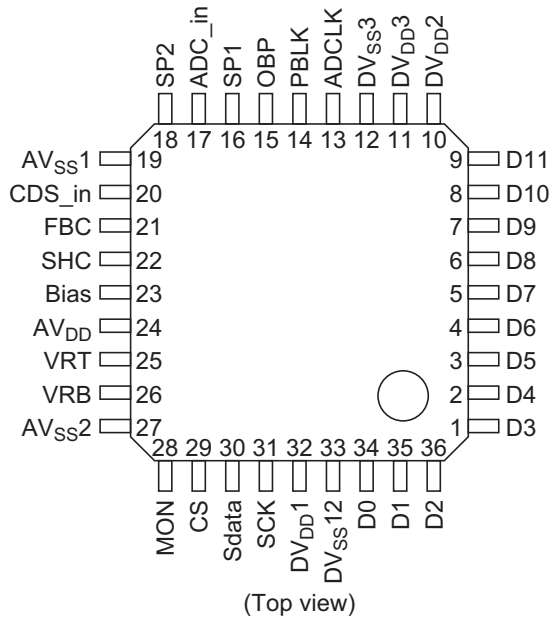
Features

- Suppresses the CCD reset noise by the correlated double sampling.
- High sensitivity can be achieved by 10 bit gray scale provided by PGA which can be set to –6 to 34 dB.
- PGA gain, S/H frequency response, pulse timing, etc., is achieved via a serial interface.
- High precision is provided by a 12-bit resolution A/D converter.
- Difference encoded gray code can be selected as an A/D output code. It is effective in suppression of solarization (wave pattern). It is patented by Renesas.

Block Diagram



Pin Arrangement

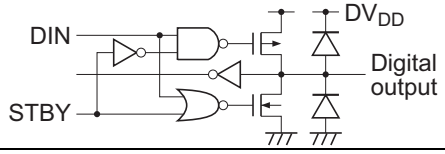
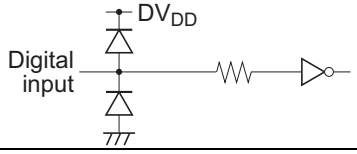
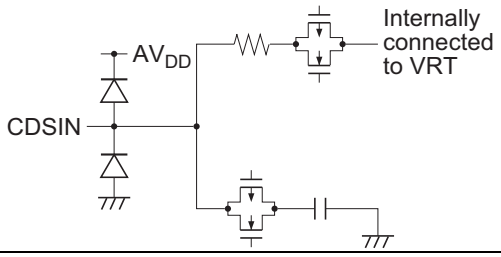
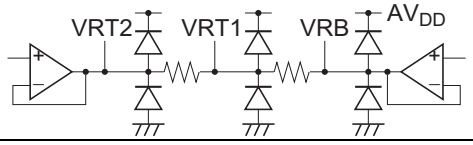


(Top view)

Pin Description

Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)	Remarks
1 to 9 34 to 36	D0 to D11	ADC digital output (D0: LSB, D11: MSB)	O	D	2 mA/10 pF
10	$DV_{DD}2$	Digital power supply of ADC output part (3 V)	—	D	
11	$DV_{DD}3$	Digital power supply of timing generator part (3 V)	—	D	
12	$DV_{SS}3$	Digital ground of timing generator part (0 V)	—	D	
13	ADCLK	ADCLK input	I	D	
14	PBLK	Preblanking pulse input	I	D	
15	OBP	OBP input	I	D	
16	SP1	SP1 input	I	D	
17	ADC_in	ADC input	I	D	
18	SP2	SP2 input	I	D	
19	AV_{SS}	Analog ground of CDS, PGA part (0 V)	—	A	
20	CDS_in	CDS input pin (0.1 μF)	I	A	
21	FBC	Capacitor pin for Feed Back clamp (0.22 μF for SHC)	O	A	
22	SHC	47 Ω + 1000 pF to ground	—	A	
23	Bias	Bias current settings pin (33 kΩ to ground)	O	A	
24	$AV_{DD}2$	Analog power supply of ADC part (3 V)	—	A	
25	VRT	ADC bias voltage of top side (0.1 μF to ground)	O	A	
26	VRB	ADC bias voltage of bottom side (0.1 μF to ground)	O	A	
27	$AV_{SS}2$	Analog ground of ADC part (0 V)	—	A	
28	MON	Cp-sw, cpdm output	O	D	2 mA/10 pF
29	CS	Serial communication pulse CS input	I	D	
30	Sdata	Serial communication pulse Sdata input	I	D	
31	SCK	Serial communication pulse SCK input	I	D	
32	$DV_{DD}1$	Analog power supply of serial communication part (3 V)	—	D	
33	$DV_{SS}12$	Ground of ADC output part of serial communication part (0 V)	—	D	

Input/Output Equivalent Circuit

Pin Name		Equivalent Circuit
Digital output	D0 to D11, MON	
Digital input	PBLK, OBP, ADCLK, CS, SCK, Sdata	
Analog	CDS_in	
	VRT, VRB	

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	V_{DD}(max)	4.1	V
Power dissipation	Pt(max)	400	mW
Operating voltage	Vopr	2.7 to 3.45	V
Analog input voltage	V_{IN}(max)	–0.3 to AV_{DD} +0.3	V
Digital input voltage	V_I(max)	–0.3 to DV_{DD} +0.3	V
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Note: AV_{DD} 1, 2, AV_{SS}1, 2 are analog power source series of CDS, PGA, ADC.
DV_{DD}1, DV_{SS}1 are digital power source series of serial communication.
DV_{DD}2, DV_{SS}2 are digital power source series of ADC output timing.
DV_{DD}3, DV_{SS}3 are digital power source series of timing generator.

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V)

- CDS_in, ADC_in Mode Common Items

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	V_{DD}	2.70	3.00	3.45	V	Select VRT = 2.0 V	
	V_{DD2}	3.10	3.30	3.45	V	Select VRT = 2.4 V	
Conversion frequency	f_{CLK}_hi	25	—	36	MHz		HD49343HNP
	f_{CLK}_low	5.5	—	25	MHz		HD49343NP
Digital input voltage	V_{IH2}	$2.2 \times \frac{DV_{DD}}{3.0}$	—	DV_{DD}	V		All of digital input pins
	V_{IL2}	0	—	$0.6 \times \frac{DV_{DD}}{3.0}$	V		
Digital output voltage	V_{OH}	DV_{DD} –0.5	—	—	V	I_{OH} = –1 mA	Digital output pins
	V_{OL}	—	—	0.5	V	I_{OL} = +1 mA	
Digital input current	I_{IH}	—	—	50	µA	$V_{IH} = V_{DD}$	
	I_{IL}	–50	—	—	µA	V_{IL} = 0 V	
ADC resolution	RES	—	12	—	bit		
ADC integral linearity	INL	—	(8)	—	LSB	f_{CLK} = 20 MHz	
ADC differential linearity	DNL	—	(0.6)	—	LSB	f_{CLK} = 20 MHz	*1
Sleep current	I_{SLP}	–100	—	100	µA	Digital input pin is set to 0 V, output pin is open	
Standby current	I_{STBY}	—	3	5	mA	Digital I/O pin is set to 0 V	

Notes: 1. Differential linearity is the calculated difference in linearity errors between adjacent codes.
2. Values within parentheses ( ) are for reference.

Electrical Characteristics (cont.)

(Unless otherwise specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V)

- Items for CDS_in Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current	I_{DD1}	—	(40)	—	mA	f_{CLK} = 36 MHz	HD49343HNP
	I_{DD2}	—	(25)	—	mA	f_{CLK} = 25 MHz	HD49343NP
CCD offset tolerance range	V_{CCD}	(–150)	—	(150)	mV		
Sampling timing specifications	t_{CDS1}	—	(1.5)	—	ns		Refer to table 4
	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
	t_{CDS3}	—	(1.5)	—	ns		
	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.0	ns		
	t_{CDS6}	—	(5)	—	ns		
	t_{CDS7}	11	—	—	ns		
	t_{CDS8}	11	—	—	ns		
	t_{CDS9}	—	(7)	—	ns		
	t_{CDS10}	—	(16)	—	ns		
Clamp level	CLP(00)	—	(56)	—	LSB		Clamp level = settings value × 8 + 56
	CLP(09)	—	(128)	—	LSB		
	CLP(31)	—	(304)	—	LSB		
PGA gain at CDS_in	PGA(0)	–8	–6	–4	dB		At 1.0 V input, when PGA output is 1V, it is defined as 0dB
	PGA(256)	2	4	6	dB		
	PGA(512)	12	14	16	dB		
	PGA(768)	22	24	26	dB		
	PGA(1023)	32	34	36	dB		

Note: Values within parentheses ( ) are for reference.

- Items for ADC_in Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current	I_{DD3}	—	(30)	—	mA	f_{CLK} = 36 MHz	
	I_{DD4}	—	(20)	—	mA	f_{CLK} = 25 MHz	
Timing specifications	t_{ADC1}	—	(6)	—	ns		
	t_{ADC2}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
	t_{ADC3}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
	t_{ADC4}	—	(14.5)	—	ns		
	t_{ADC5}	—	(23.5)	—	ns		
Input current at ADC input	IIN_{CIN}	–110	—	110	µA	V_{IN} = 1.0 V to 2.0 V	
Clamp level at ADC input	OF2	1848	2048	2248	LSB		
PGA gain at ADC_in	GSL(0)	–8	–6	–4	dB		At 1.0 V input, when PGA output is 1V, it is defined as 0dB
	GSL(128)	–3	–1	1	dB		
	GSL(256)	2	4	6	dB		
	GSL(384)	7	9	11	dB		
	GSL(511)	12	14	16	dB		

Note: Values within parentheses ( ) are for reference.

Internal Functions

Functional Description

- CDS input
  - CCD low-frequency noise is suppressed by CDS (correlated double sampling).
  - The signal level is clamped at 56 LSB to 304 LSB by resister during the OB period. *[1]
  - Gain can be adjusted using 10 bits of register within the range from –6 to 34 dB.
- Automatic offset calibration of PGA and ADC
- DC offset compensation feedback for CCD and CDS
- Pre-blanking
  - Digital output is fixed at clamp level.

Note: 1. It is not covered by warranty when 56 LSB settings.

Operating Description

Figure 1 shows function block of this LSI.

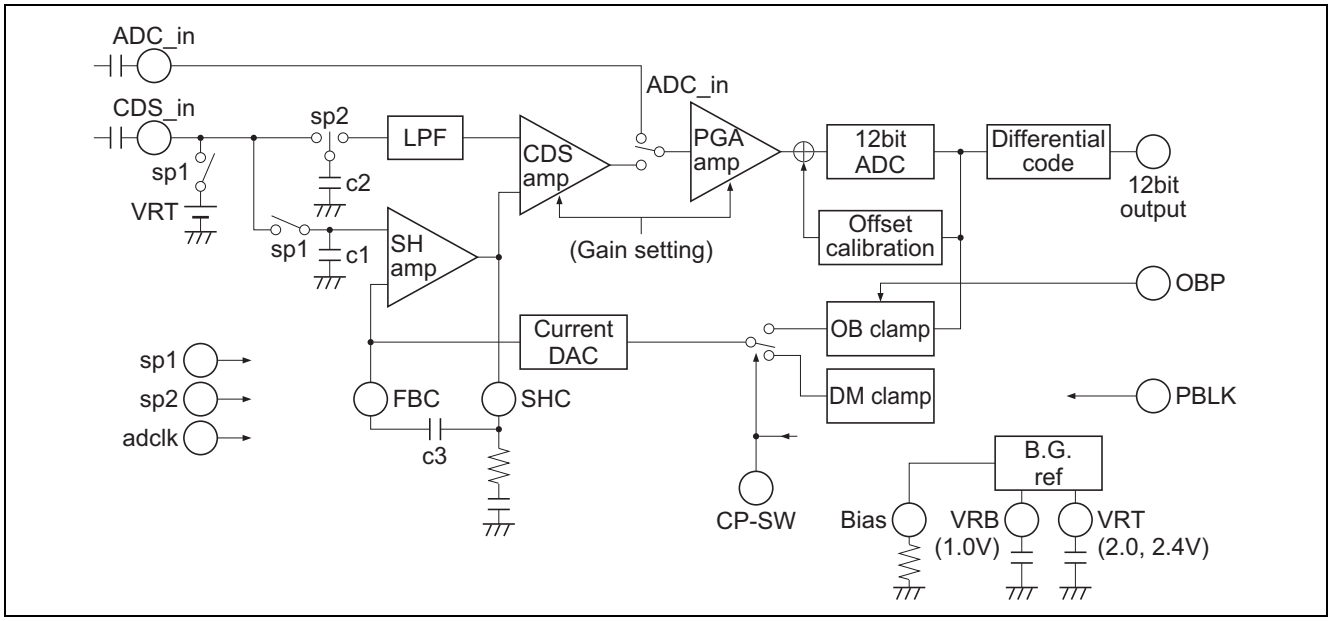
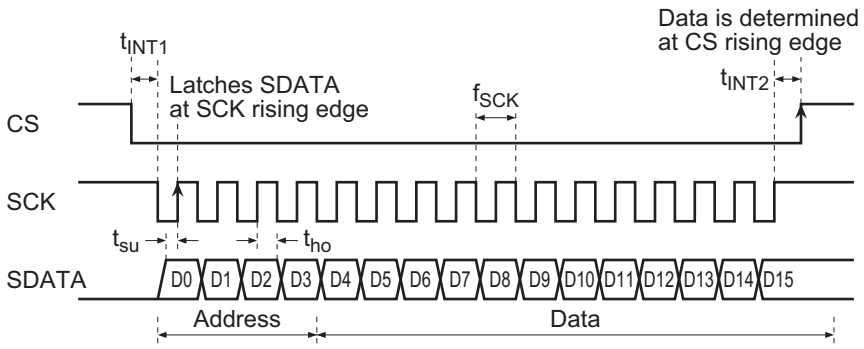


Figure 1 Functional Block Diagram of CDS/PGA Part

1. CDS (Correlated Double Sampling) Circuit
   The CDS circuit extracts the voltage differential between the black level and a signal level. The black level is directly sampled at C1 by using the SP2 pulse, buffered by the SHAMP, then provided to the CDSAMP.
   The difference between these two signal levels is extracted by the CDSAMP, which also operates as a programmable gain amplifier at the previous stage.
   The CDS input is biased with VRT (2.0 V or 2.4 V)
   During the PBLK period, the above sampling and bias operation are paused.
2. PGA Circuit
   The PGAMP is the programmable gain amplifier for the latter stage. The PGAMP and the CDSAMP set the gain using 10 bits of register.
   The equation below shows how the gain changes when register value N is from 0 to 1023.
   $\text{Gain} = -6\ \text{dB} + 0.04\ \text{dB} \times N$ (Log linear)
3. OB Clamp
   Feedback is done to set the black signal level input during the OB period to the DC standard, and all offsets (including the CCD offset and the CDSAMP offset) are compensated for.
   The offset from the ADC output is calculated during the OB period, and SHAMP feedback capacitor C3 is charged by the current DAC.

Serial Interface Specifications

Serial Interface Specifications



	Min	Max
f_{SCK}	—	5 MHz
$t_{INT1,2}$	50 ns	—
t_{su}	50 ns	—
t_{ho}	50 ns	—

Notes: 1. Communication is 2 byte continuation communications.
2. Input 16 clocks of SCK while CS is low.
3. Data is invalid if data transmission is aborted during transmission.

Figure 2 Serial Interface Timing Specifications

Table 1 Serial Data Function List

Address	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Remarks
0	PGA gain				PGA gain										Bias_sel		PGA gain: –6 to 34dB (0.04dB/step) D4: LSB, D13: MSB D15, D14: Bias_sel:
	0	0	0	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	When 0: Biasing regularly, When 1cpdm: biasing
	Default value				0	0	0	0	0	0	0	0	0	0	0	0	After 2,3obp: 8clk biasing
1	Filter				LPF_sel				shsw_sel				sha_fsel		slp	stby	LPF_sel: LPF selection of 5 to 56MHz
	1	0	0	0	D4	D5	D6		D8	D9	D10	D11	D12	D13	D14	D15	shsw_fsel, sha_fsel; Sampling filter of sp1 part
	Default value				1	1	0		0	0	0	1	0	1	0	0	slp, stby: Normally 0 settings
2	Clamp Polar selection Reset				clamp					obp_W	Polar selection				calb	Reset	clamp: Setting value × 8+56 obp_W: 8clk detection at 0, 4clk detection at 1 Polar selection; 0 = Negative, 1 = Positive
												obp inv	pblk inv	Lo-pwr			Lo-pwr: Guarantee 36MHz at 0, Guarantee 25MHz at 1
	0	1	0	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	calb: 1 Offset calibration execution
	Default value				1	0	0	1	0	0	0	0	0	1	0	1	Reset: Software reset at 0, Normally 1 settings
3	Dummy clamp others				Dummy clamp						Others						cpdm_th/i: Dummy clamp settings VRT_sel: 2.0/2.4V switching Vref_off: Bias off of VRT, VRB ADC_in: ADC input mode at 1
					cpdm_th			cpdm_i			VRT sel	Vref off	DLL off			ADC_in	
	1	1	0	0	D4	D5	D6	D7	D8		D10	D11	D12	D13	D14	D15	
	Default value				0	0	0	0	0		0	0	0			0	
4	Differential code				Differential code							Output fixation					Gray Standard phase: Move between 0 to 3clk adclk phase: Positive/Negative edge selection 10/12: Bit number of gray conversion Gry, difference: On/Off of differential coded gray code Gry_ref: 0 = 2 Pixel standard, 1 = 1 Pixel standard
					Standard phase	adclk phase	Gry	difference	10/12	Gry ref	test 0	MINV	LINV				
	0	0	1	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13			Output fixation: test0, MINV, LINV (Refer to HD49330 for details)
	Default value				0	0	0	0	0	0	0	0	0	0			
5					MON												MON: cp-sw at 0, cpdm at 1
	1	0	1	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value				1	1	0	0	0	0	0	1	0	1	0	0	

Table 1 Serial Data Function List (cont.)

Address	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Remarks
6	new func					cpad sel	winck sel			wide obp	pblk act	wob_ vth1	clp_Hsel		wob_ i	clp_ l	cpad sel: pad test. Normally 0 settings winck sel: High clamp compensation window width 0: ×32, 1: ×64, 2: ×128, 3: ×16 wide_obp: Correspond to wide OB pblk act: OBP in a PBLK period is valid wob_vth1: Switching 200μA current of for wide OB 0: 63cnt, 1: 200cnt clp_Hsel: Continuing H number after high speed lead-in 0: 1H, 1: 2H, 2: 4H, 3: 8H wob_i: Twice as current for wide OB clp_l: D15 = 1 1/2 Half of normal clamp current
	0	1	1	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value					0	0	0		0	0	0	0	0	0	0	
7	test1																Test bit is bit for testing at the time of shipment in our company. Usually, please set up an all 0 or do not transmit. D10: 1 Pulse output regardless of the cpdm function.
	1	1	1	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value				0	0	0	0	0	0	0	0	0	0	0	0	
8																	
	0	0	0	1	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value																
9																	
	1	0	0	1	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value																
10											wob_ vth1		wob_ vth2		wob_ vth3		wob_vth1: Switching 200μA current of for wide OB wob_vth2: Switching 20μA current of for wide OB wob_vth3: Switching 2μA current of for wide OB
	0	1	0	1	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value										0	0	0	0	0	0	
11	cpdm_dl				cpdm_dl												cpdm_dl: Select 0 to 1016clk (Every 4clk) (Default value = 0, Pulse stopping at all 1) Pulse phase = Data × 4 (clk)
	1	1	0	1	D4	D5	D6	D7	D8	D9	D10	D11		D13	D14		
	Default value				0	0	0	0	0	0	0	0					
12	test2																
	0	0	1	1	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value				0	0	0	0	0	0	0	0	0	0	0	0	
13	test3																
	1	0	1	1	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value				0	0	0	0	0	0	0	0	0	0	0	0	
14	test4																
	1	1	1	0	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	
	Default value				0	0	0	0	0	0	0	0	0	0	0	0	

Note: Address 15 is not in use.

• Control of wide OB

	Current Value wob_i		The Number of Counts wob_th1, 2, 3				Remarks
	0	1	0	1	2	3	
Iclp_th1	200μA	400μA	15	63	200	Infinity	Only when an address 11 is 0, the setting value of an address 6 reflects the number of counts.
Iclp_th2	20μA	40μA	127	255	511	Infinity	
Iclp_th3	2μA	4μA	511	1023	Infinity	Infinity	

Explanation of Serial Data

- PGA Gain (D4 to D13 of address 0)
  Refer to the P.4 block diagram for details. A gain shifts 3 dB by voltage setup (D12 of address 4) of VRT.
  PGA gain: –6dB + 0.04 dB × N (Log linear)

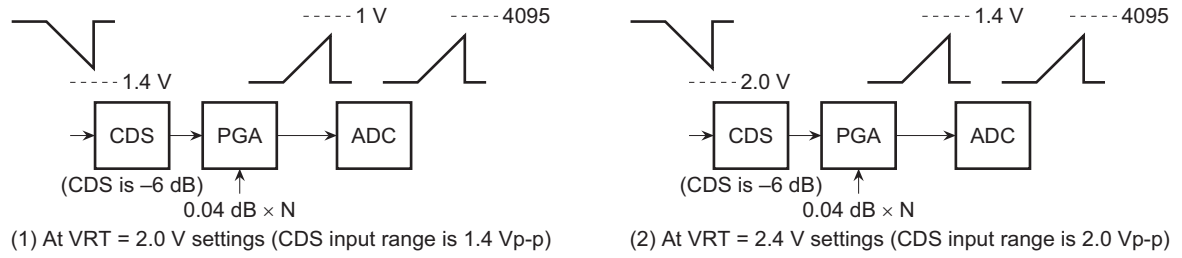


Figure 3 Level Dia of PGA

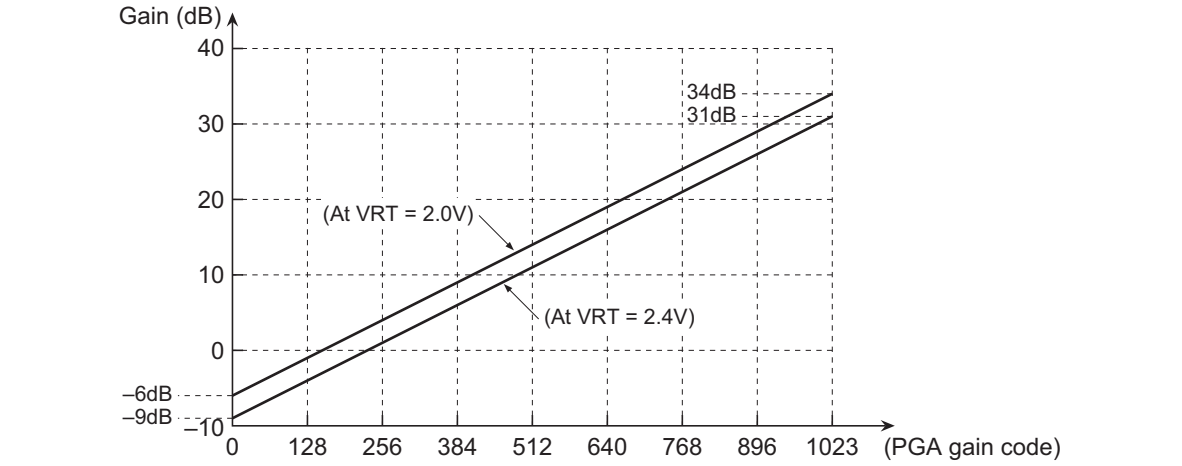


Figure 4 PGA Gain Characteristics

- LPF_sel (D4 to D6 of address 1)
  Frequency band restrictions of a CDS input part are chosen.

LPF_sel	Sensor Frequency
0	6 MHz
1	12 MHz
2	18 MHz
3	25 MHz
4	30 MHz
5	35 MHz
6	40 MHz
7	50 MHz

Although S/N will rise if a frequency band is lowered, but opposite side amplifier operation becomes slow and which problem with line crawl and insufficient gain occurs. Please choose a high point from the actually used frequency.

About LFP_sel, followings are only testing guaranteed.

(1) At Low Power mode: Data = 3
(2) At Normal Power mode: Data = 6

- SHSW_fsel, SHA_fsel (D8 to D13 of address 1)
  Filtering processing is performed to the precharge part sampled by SP1. The cutoff frequency at this time can be chosen.

Table 1 SHSW Time Constant Setting

SHSW_fsel Data	Cutoff Frequency (MHz)
0	72
1	69
2	63
3	60
4	54
5	51
6	45
7	42
8	36
9	33
10	27
11	24
12	18
13	15
14	9
15	6

Table 2 SHAMP Frequency Characteristics Setting

SHA_fsel Data	Cutoff Frequency (MHz)
0	116
1	75
2	56
3	32

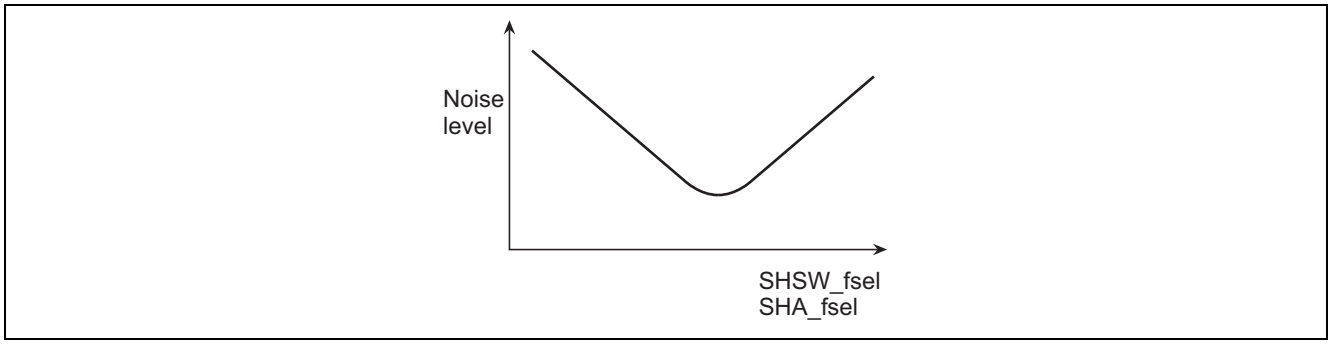


Figure 5 The Effect by SHSW_fsel, SHA_fsel

Note: S/N changes with data selections of SHSW_fsel, SHA_fsel, as shown in figure 5. Please find the optimal value with evaluating a picture.

- SLP and STBY (D14, D15 of address 1)
  SLP: Stop the all of circuit. Consumption current should below 10 μA at CDS section.
  When returning is necessary, please start up from an offset calibration {(3) of figure 6}.
  STBY: Operates with only a standard voltage generating circuit. Consumption current is about 3 mA
  Please expect about 20 H as time to stabilize a feedback clamp by return.

- Clamp level (D4 to D8 of address 2)
  Clamp level = Setting data × 8 + 56
  D4: LSB, D8: MSB
  Default value is set to 9 × 8 + 56 = 128

- Clamp high-speed lead-in (D6, D7, D12, D13 of address 6)
  If a PGA gain is changed, it will shift to high-speed lead-in operation automatically, and a feedback loop gain will be controlled by the magnification which set by D6 and D7. During end of the high speed lead-in to returning normal loop gain, high-speed lead-in mode is continuing until H count number which set by D12, D13. (High-speed lead-in operation is continuing during offset error is more than 32 LSB, and it returns to normal loop gain in the H counter number which set by D12, D13 is countered.)
  In the usual clamp operation, the open loop differentiation gain (ΔGain/ΔH) of per 1 H is given by the lower formula. (1 H is 1 cycle of OBP)
  $\Delta Gain/\Delta H = 0.01/(fclk \times C3)$ (fclk: ADCLK frequency, C3: External capacity of FBC)
  Ex): fclk = 20 MHz, C3 = 0.1 μF → ΔGain/ΔH = 0.005
  DC offset compensation amount per 1 H (LSB) = 0.005 × Offset error amount (LSB) *
  Note: There is a maximum value in the above-mentioned amount of offset errors.

  On the other hand, in high-speed lead-in operation, speed changes as follows.
  Ex): fclk = 20 MHz, C3 = 0.1 μF → 32 × ΔGain/ΔH = 0.16
  DC offset compensation amount per 1 H (LSB) = 0.16 × Offset error amount (LSB)

  When the error of about 500 LSB arises by high-speed lead-in operation, it can lead in a target clamp level by about 20 H.

- Wide_obp (D9 of address 6)
  When D9 = 1, it corresponds to wide OBP. When the width of OBP is 63 ± 1 or more clks, it recognizes automatically that it is wide and detection & compensation is performed every clk. In using this function, please contact to our company sales.

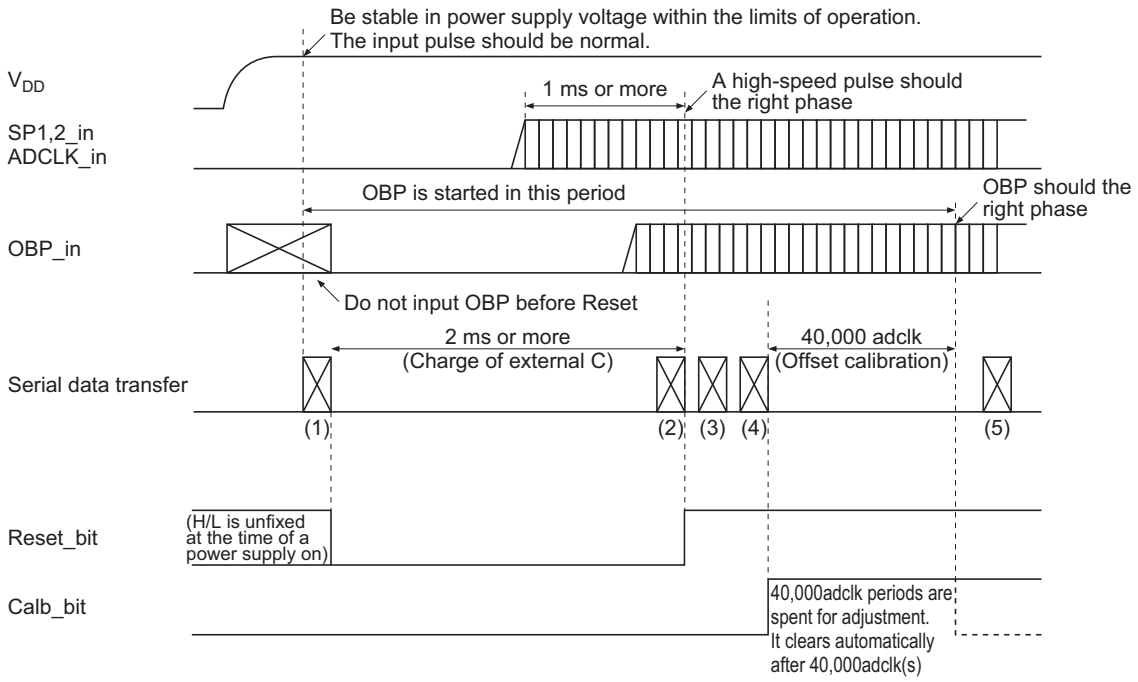
- OBP_W (D9 of address 2)
  Clamp detection is changed to 4 pixels at the time of 8 pixels and D9 = 1 at the time of D9 = 0.

- Each polar selection (D10 to D12 of address 2)

Data	Name	Contents
D11	OBP_inv	Polar selection of OBP. Input the negative pulse at 0. Input the positive pulse at 1.
D12	PBLK_inv	Polar selection of PBLK Input the negative pulse at 0. Input the positive pulse at 1. PBLK_inv is conjunction with SP_inv.

- Low_pwr (D13 of address 2)
  It guarantees to sensor clk = 36 MHz at the time of D13 = 0. (HD49343HNP)
  It guarantees to sensor clk = 25 MHz at the time of D13 = 1. (HD49343NP)

- Calibration and Reset (D14, D15 of address 2)
  By performing Software Reset and a calibration only once at the time of a power supply, a bias gap of an internal circuit is canceled automatically. (Offset calibration) Please be sure to perform by this LSI.
  An automatic offset calibration adjusts DC voltage of DAC added to the output of PGA amplifier.
  The clamp data (56 LSB to 304 LSB) based on a register setup is added to the data which cancels output offset of PGA amplifier and input offset of ADC, and it is given to this DAC.
  Automatic offset calibration starts automatically after the Reset mode release by register setup, and it ends after 40000 (adclk). (In case of fclk = 20 MHz: 2.0 ms, In case of fclk = 10 MHz: 4.0 ms)



The contents of the above-mentioned serial data transmission are shown below.
Refer to the serial data specification table for the details of a register setup.

(1) Reset = 0, Calb = 0	: Reset bit = Transfer 0 It stands by 2 ms or more as charge time of an external capacitor.
(2) Reset = 1, Calb = 0	: Reset bit = Transfer 1 → All registers are initialized.
(3) All data transfer	: Transfer the resister which needs data changes.
(4) Calb = 1	: Automatic offset calibration is start. Standby time is 40,000 or more adclks.
(5) Transfer the changed data	: Data, such as a PGA gain, to change is transmitted. An address 2 is necessary to send after a calibration finishes, please set as Reset = 1 and Calb = 1.

∗ Since it is necessary to decide SP1, SP2, and an ADCLK phase before transmitting Calb bit = 1, please perform this work with input pulse is stabilized.
∗ When offset calibration is needed, please avoid the V.BLK period.

Figure 6 Operation Sequence of at Power ON

- Dummy clamp (D4 to D8 of address 3)

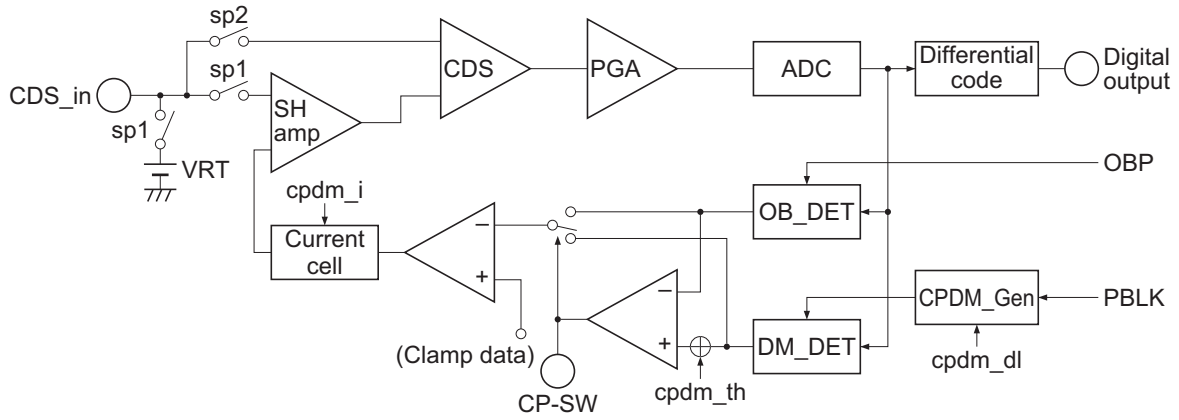
  When a intense highlight like a solar is photoed, light leaks also to the OB part of a sensor and a clamp mistake is occurred. In order to prevent this incorrect operation, when the level difference of the OB part and a dummy part is supervised and it becomes the conditions of OB part > dummy part + cpdm_th, it changes to the clamp in a dummy level automatically. It becomes the amount of current which also set up simultaneously the feedback current at the time of Dummy on by cpdm_i.

  The cpdm pulse for performing a dummy clamp is generated by the following formulas from delay of PBLK.

  Cpdm phase = PBLK phase + (address 11)

  If a cpdm phase is set as the portion of Shutter noise, it may incorrect-operate. When incorrect operation cannot be prevented, please turn off a function as cpdm_th = 0.

  Moreover, since clamp mistake voltage is also changed by the PGA gain, please control cpdm_th for a gain to be interlocked with.



cpdm_i	Contents
0	1/4 of current at normal time
1	1/8 of current at normal time
2	1/16 of current at normal time
3	1/32 of current at normal time

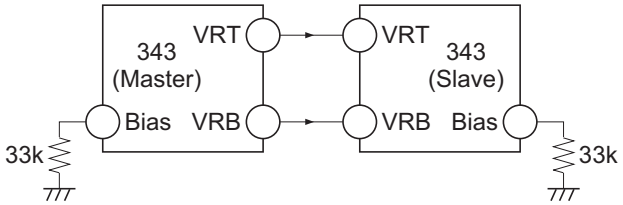
cpdm_th	Contents
0	Function off
1	+128
2	+256
3	+384
4	+512
5	+640
6	+768
7	+896

Figure 7 Composition of Dummy Clamp Circuit

- VRT_sel (D10 of address 3)
  When D10 = 0, VRT is 2.0 V,
  when D10 = 1, VRT is 2.4 V are chosen.
  However, when set to as D10 = 1, more than in 3.1 V AV_{DD} voltage as conditions.

VRT_sel	VRT Voltage	CDS Input Range	ADC Dynamic Range	AV_{DD} Condition
0	2.0 V	1.4 Vp-p	1.0 Vp-p	Min = 2.7 V
1	2.4 V	2.0 Vp-p	1.4 Vp-p	Min = 3.1 V

- Vref_off (D11 of address 3)
  At the time of D11 = 1, VRB and VRT intercept the supply from the inside of LSI, and the voltage supply from the outside becomes available.
  When making parallel connection, gain variation etc. can be suppressed by setting up as a master/a slave, as shown in the following figure.
  When external supply mode is chosen, please perform an offset calibration in the state of the voltage.



- ADC_in (D15 of address 3)
  When D15 = 0, Normal CDS operation mode,
  or when D15 = 1, ADC_in mode for testing (bias is about 1.0 V at this time) are chosen.

- MON (D4 of address 5)

Data	MON Pin
0	cp-sw
1	cpdm

- Gray code (D4 to D10 of address 4)
  ADC output code can be changed by differential coded gray SW (D7, D8) as followings.
  D7: 0 Binary code :1 Gray code
  D8: 0 Normal :1 Differential code
  When switching the several of ADC out put at the same time, ripple (pseudo outline caused by miss quantization) occurs to the image. Differential code and gray code are recommended for this countermeasure. Figure 8 indicates circuit block. When luminance signal changes are smoothly, the number of bit of switching digital output bit can be reduced and easily to reduce the ripple using this function.
  This function is especially effective for longer the settings of sensor more than clk = 30 MHz, and ADC output.
  In using this code, a complex circuit is needed by the DSP side. Figure 10 indicates the example.

Standard Phase (D4)	Standard Phase (D5)	Standard Data Output Timing at Differential Code Selected
0	0	Third and fourth (Third)
1	0	Fourth and fifth (Fourth)
0	1	Fifth and sixth (Fifth)
1	1	Sixth and seventh (Sixth)

Note: Color filter is different from odd/even pixel, so considers 2 pixels of a head as a standard. When the inside of ( ) makes a standard 1 pixel.

- adclk phase (D6): ADCLK polarity to OBP
  When 0: select positive edge
  When 1: select negative edge
- 10/12 (D9): Binary→Gray convert bit number
  When 0: select 12 bit
  When 1: select 10 bit
- Gry_ref (D10): The number of standard pixel
  When 0: select 2 pixel
  When 1: select 1 pixel

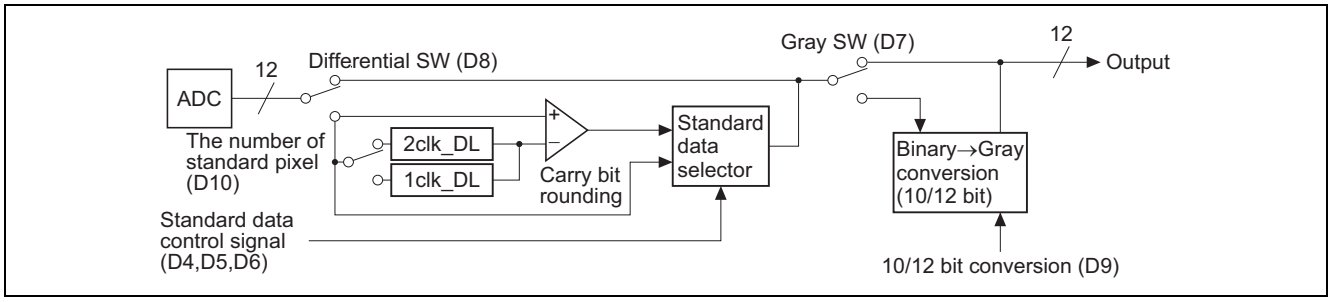


Figure 8 Differential code, Gray code Circuit

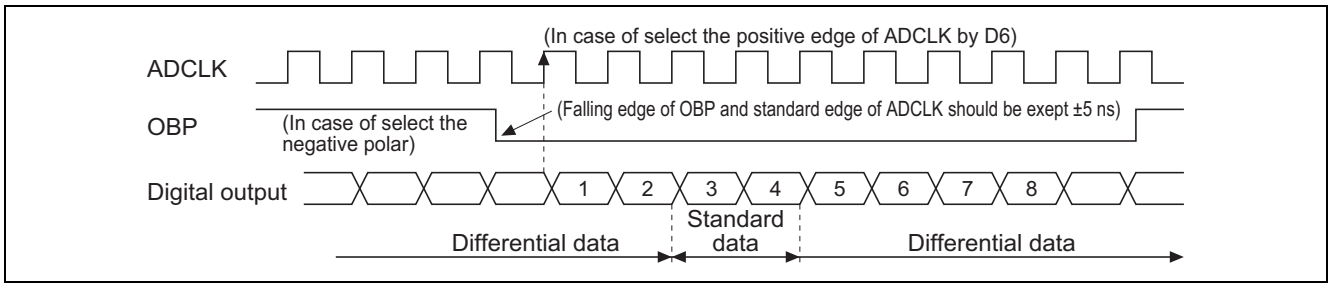


Figure 9 Timing Specification of Differential code

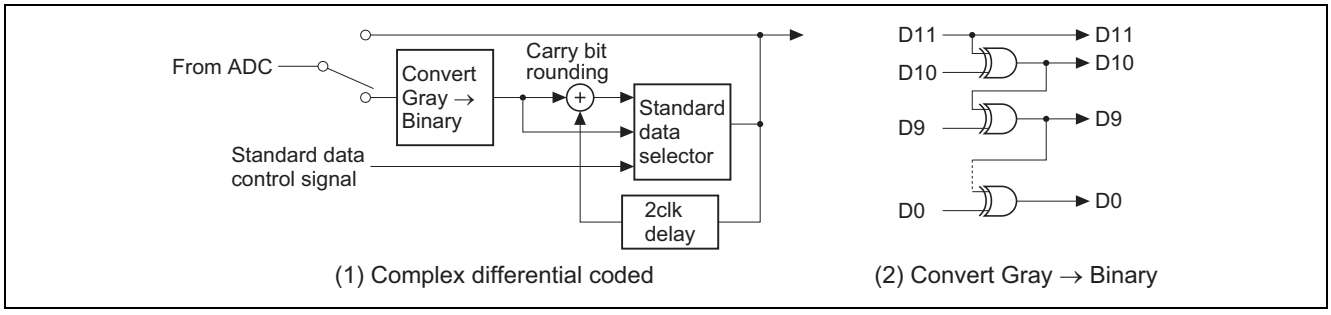
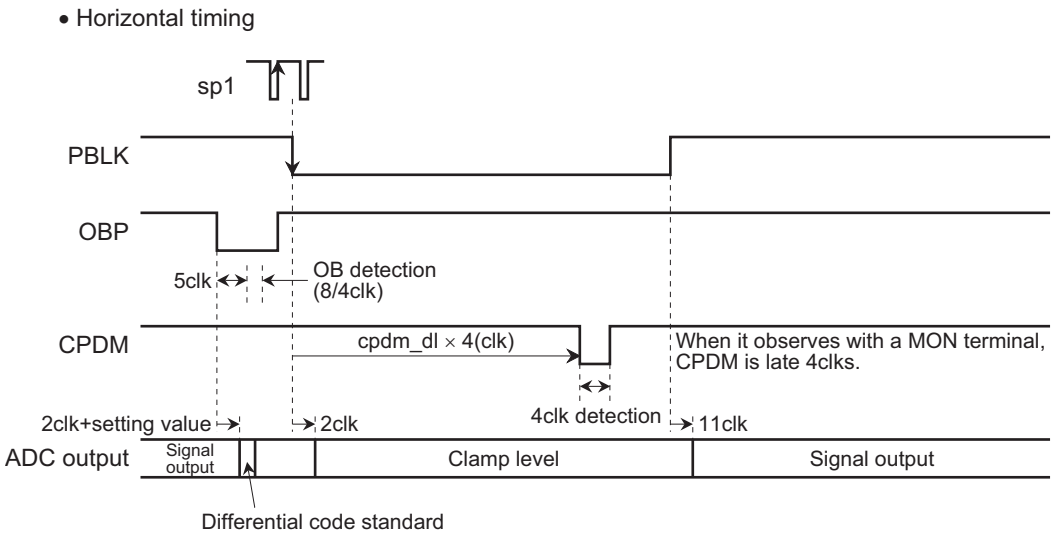


Figure 10 Complex Circuit Example at the DSP Side



Notes: 1. Duty of CLK_in should be less than 50 ± 15%.
2. The rising edge of sp1 and the edge of PBLK should not overlap.
(Should not be within ±5ns.)
3. Each pulse is indicated on the basis of negative polarity.
4. CPDM cannot be made from a set without PBLK.

Figure 11 The Timing of H.BLK Period

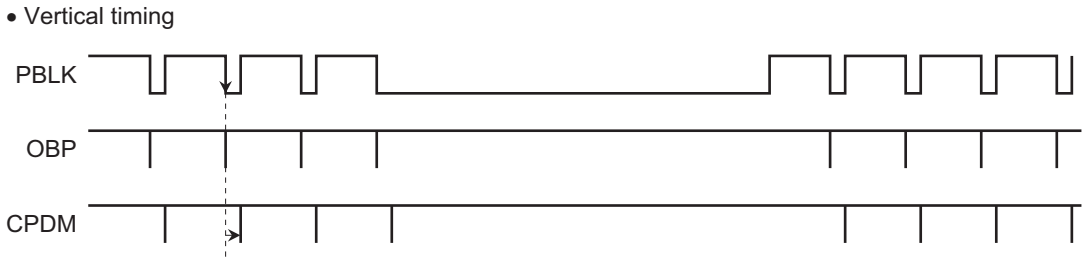


Figure 12 The Timing of V.BLK Period

Pipeline Delay

The output timing figure at the time of using each input terminal of CDS_in and ADC_in for figure 13 is shown.

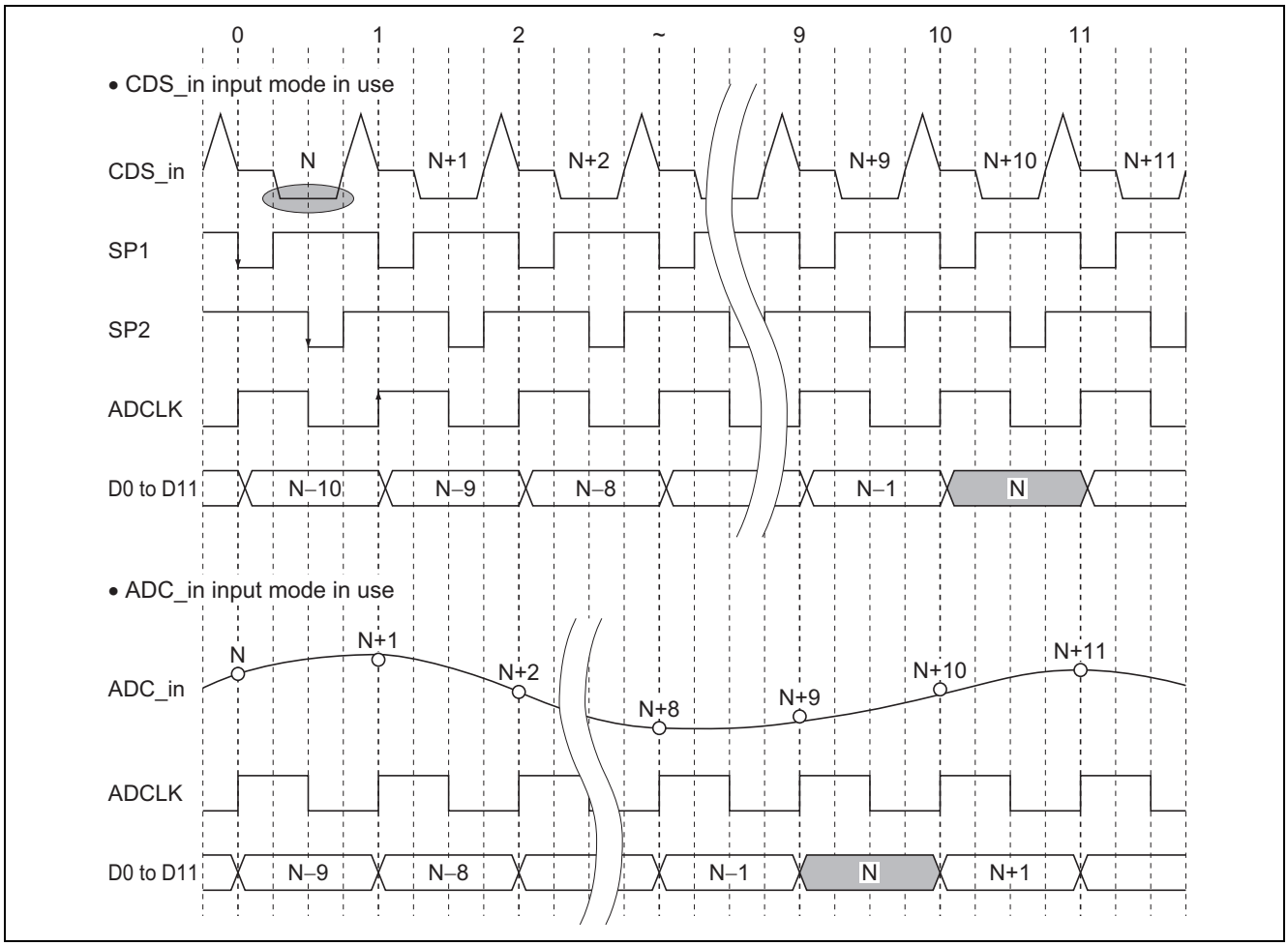


Figure 13 Output Timing Figure at the Time of Using Each Input Terminal of CDS_in and ADC_in

- As for an ADC output (D0 to D11), both input mode is outputted by the rising edge of ADCLK.
- The pipeline delay at the time of CDSIN in use is 10 clocks and ADC_in in use is 9 clocks.
- The input signal sampling at the time of ADC_in input mode is performed by the rising edge of ADCLK.
- The pipeline delay increases 1 more clock when using the differential code.

Detailed Timing Specifications

Detailed Timing Specifications when CDS_in Mode is Used

Figure 14 shows the detailed timing specifications when the CDS_in input mode is used, and table 4 shows each timing specification.

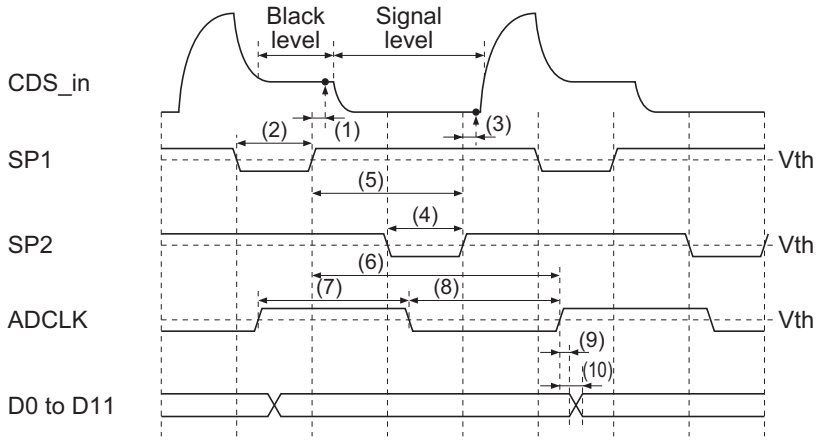


Figure 14 Detailed Timing Chart when CDS_in Input Mode is Used

Table 4 Timing Specifications when the CDS_in Input Mode is Used

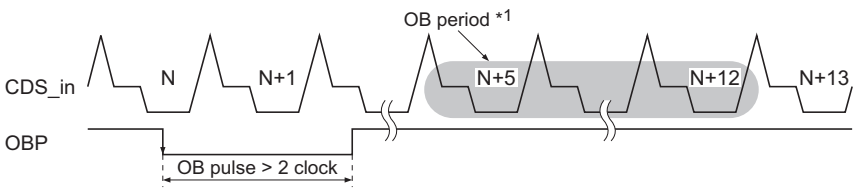
No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Black-level signal fetch time	t_{CDS1}	—	(1.5)	—	ns
(2)	SP1 low period	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(3)	Signal-level fetch time	t_{CDS3}	—	(1.5)	—	ns
(4)	SP2 low period	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(5)	SP1 rising to SP2 rising time	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.00	ns
(6)	SP1 rising to ADCLK rising inhibition time	t_{CDS6}	—	(5)	—	ns
(7), (8)	ADCLK t_{WH} min./t_{WL} min.	$t_{CDS7, 8}$	11	—	—	ns
(9)	ADCLK rising to digital output hold time	t_{CHLD9}	—	(7)	—	ns
(10)	ADCLK rising to digital output delay time	t_{COD10}	—	(16)	—	ns

Notes: 1. The value specified on frequency of operation is the case where "t_{CDS5}" is being protected. Even if the frequency used is in specification, when this time is short, it becomes equivalent to the operation of high frequency. Moreover, please set up max of t_{CDS5} as $1/2f_{CLK}$.
2. SP1 at the time of single sampling mode needs to set it as the phase shifted 180° to SP2.

OBP Detailed Timing Specifications

Figure 15 shows the OBP detailed timing specifications.

The OB period is from the fifth to the twelfth clock cycle after the OB pulse is input. The average of the black signal level is taken for eight input cycles during the OB period and becomes the clamp level (DC standard).



Note: 1. Shifts ±1 clock cycle depending on the OBP input timing.

Figure 15 OBP Detailed Timing Specifications

Detailed Timing Specifications at Pre-Blanking

Figure 16 shows the pre-blanking detailed timing specifications.

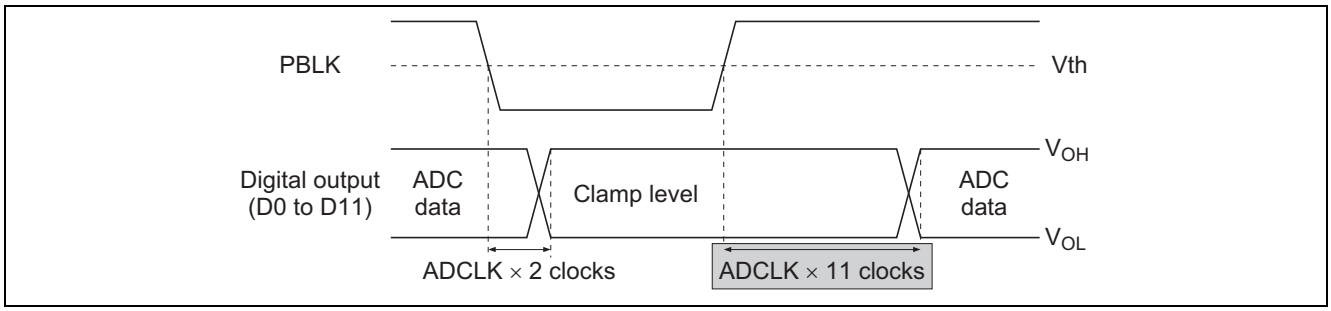


Figure 16 Detailed Timing Specifications at Pre-Blanking

Detailed Timing Specifications when ADC_in Input Mode is Used

Figure 17 shows the detailed timing chart when ADC_in input mode is used, and table 5 shows each timing specification.

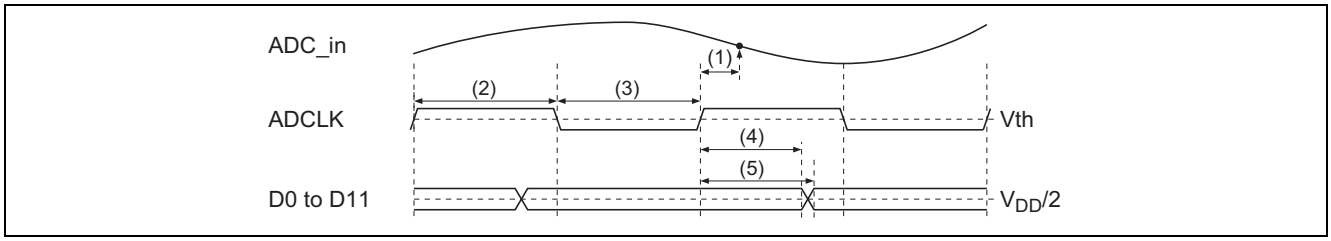
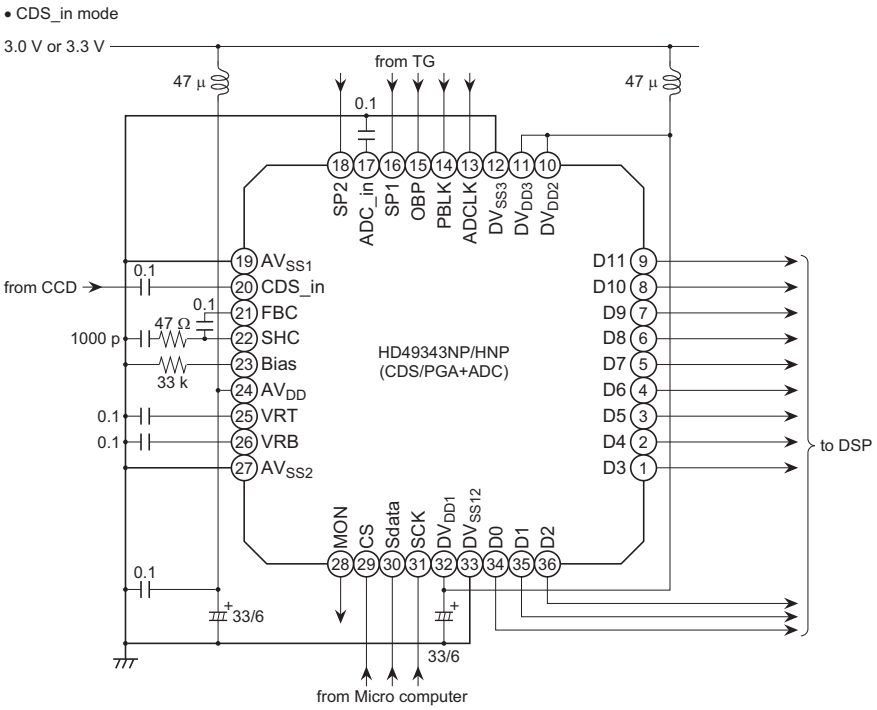


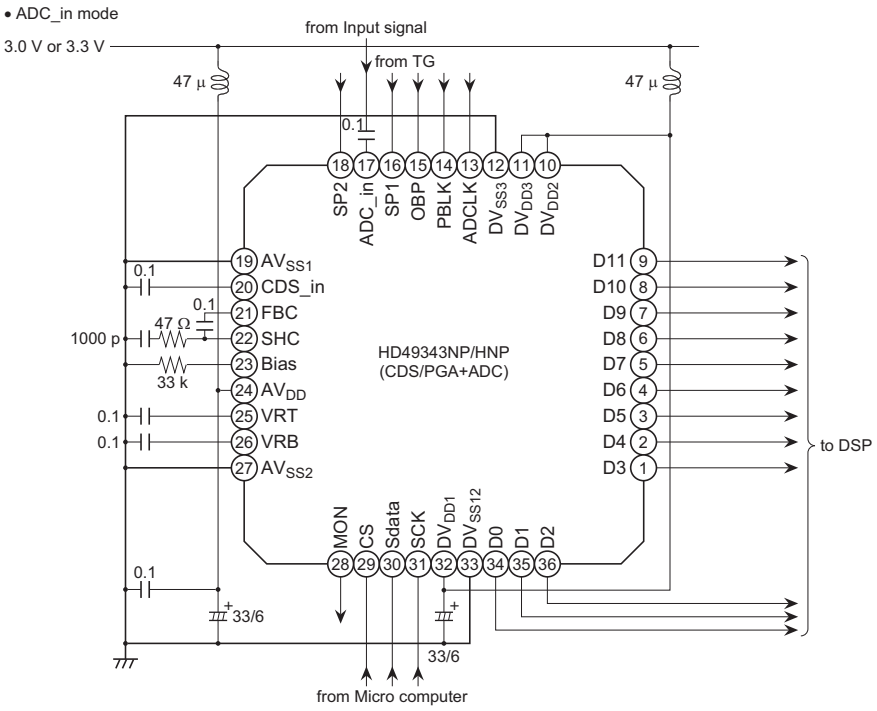
Figure 17 Detailed Timing Chart when ADC_in Input Mode is Used

Table 5 Timing Specifications when ADC_in Input Mode is Used

No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Signal fetch time	t_{ADC1}	—	(6)	—	ns
(2), (3)	ADCLK t_{WH} min./t_{WL} min.	$t_{ADC2, 3}$	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns
(4)	ADCLK rising to digital output hold time	t_{AHLD4}	—	(14.5)	—	ns
(5)	ADCLK rising to digital output delay time	t_{AOD5}	—	(23.5)	—	ns

Example of External Circuit





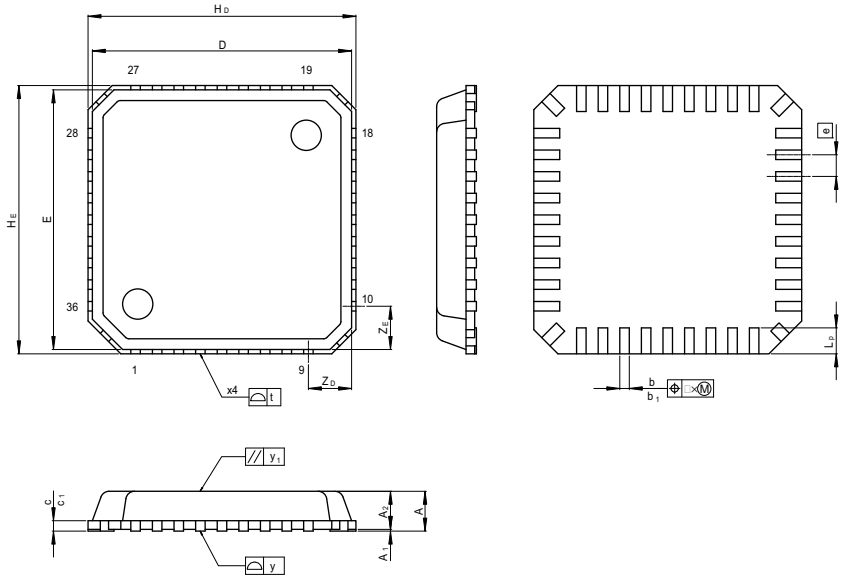
Check Item

Please check following items for use.

No.	Item	Contents	Judgment
1	Input pulse polarity	Are the polarity of OBP and PBLK and the polarity set as D11-D12 of an address 2 match?	
2	Input pulse timing	Do SP1 and SP2 keep the relation of Figure 14 and Table 4? Note: Since especially tCDS5 becomes equivalent to frequency of operation. Moreover, as for SP1 and SP2, a Low period should not overlap.	
		Is the ADCLK rising set up near SP1 falling edge? (Figure 14, Table 4)	
		Are an ADCLK rising and OBP falling edge separated ±5 ns or more? (Figure 9)	
		Is the margin for ±5 ns or more in the edge of the ADCLK rising to PBLK? Is it satisfactory to an OBP phase and a CPDM phase? (Figure 11 and 12)	
3	Output timing	Is a margin in the latch phase of an ADC output and DSP?	
		When using differential code, does not a standard signal phase have a problem? (Figure 9 and 11)	
4	Power supply voltage	When VRT voltage = 2.4 V are chosen, more than Vdd = 3.1 V is required.	
5	Offset calibration	Is the offset calibration of Figure 6 performed at the time of a power on?	
6	S/N improvement	Adjustment of SP1 and SP2 phase. Adjustment of an ADCLK phase. When adjustment finishes, re-check about item 2.	
		Filter adjustment of LPF_sel, SHSW_fsel, and SHA_fsel.	
7	Clamp operation	The capacitor of FBC becomes the relation of a trade-off of high-speed lead in of a horizontal line noise and a clamp. Please check both characteristics and determine the optimal value.	
		A clamp mistake is made to induce and data and pulse timing of a dummy clamp are set up. Please see a margin with the time of alumnus clamp.	
8	The notes about hardware	Take large Gnd as much as possible.	
		Please separate an analog power supply and a digital power supply by L etc.	
		Please arrange an input pulse, a serial communication line, etc. not to jump in to an analog part.	
		An ADC output is extended for a long time, or 30 MHz or more in carrying out high-speed operation, it becomes easy to generate a ripple. In such a case, feed in about 100 Ω into 12 ADC output pins as dumping resistance in series, or please try reduction using differential code.	

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VQFN36-6x6-0.50	PVQN0036KA-A	TNP-36/TNP-36V	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
A_2	—	0.89	—
A	—	—	0.95
A_1	0.005	0.02	0.04
b	0.17	0.22	0.27
b_1	—	0.20	—
e	—	0.5	—
L_p	0.50	0.60	0.70
x	—	—	0.05
y	—	—	0.05
y_1	—	—	0.20
t	—	—	0.20
H_D	—	6.2	—
H_E	—	6.2	—
Z_D	—	1.0	—
Z_E	—	1.0	—
c	0.17	0.22	0.25
c_1	—	0.20	—

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