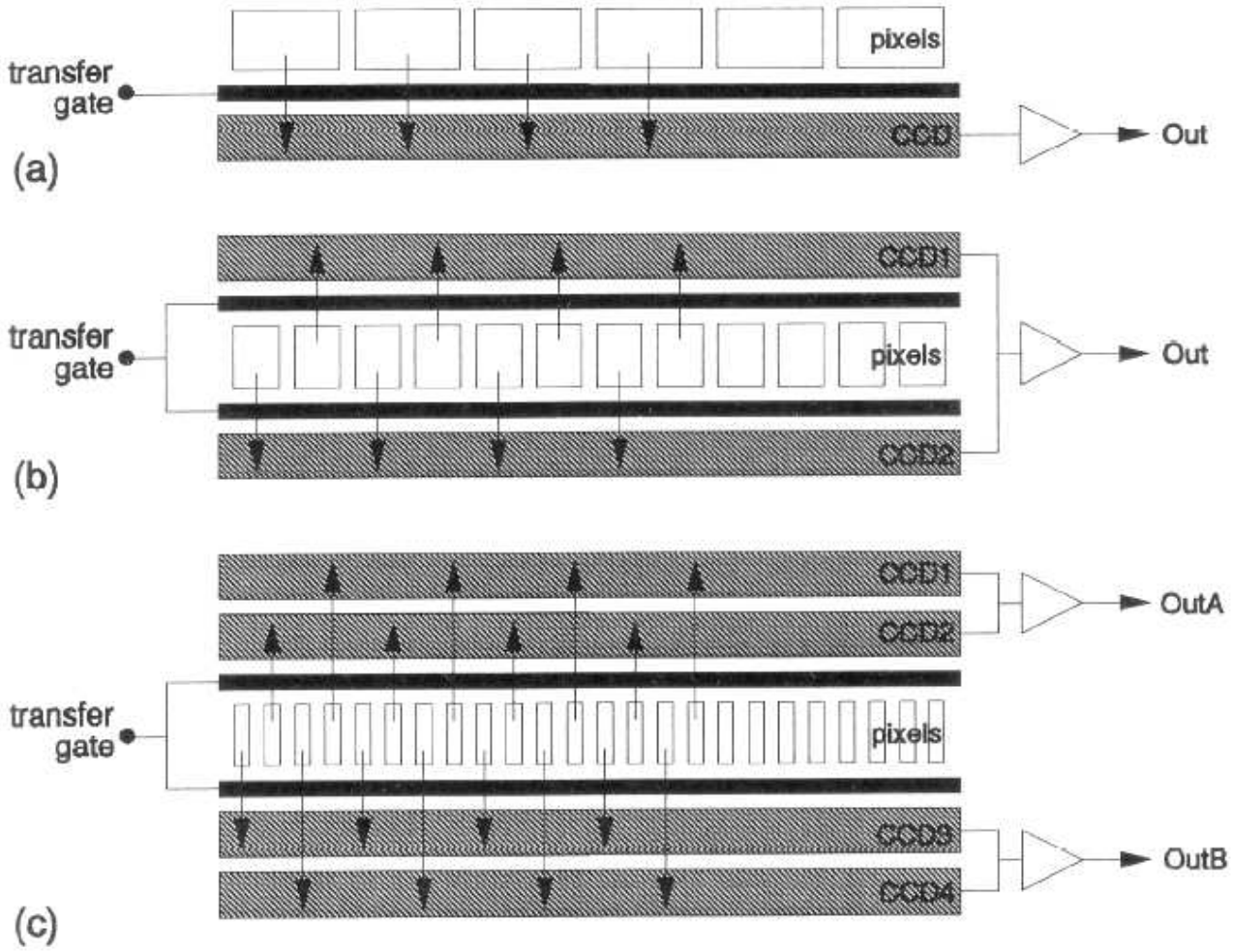
Lecture Notes 3
Charge-Coupled Devices (CCDs) – Part II

- CCD array architectures and pixel layout
  - One-dimensional CCD array
  - Two-dimensional CCD array
- Smear
- Readout circuits
- Anti-blooming, electronic shuttering, charge reset operation
- Window of interest, pixel binning
- Pinned photodiode

One-Dimensional (Linear) CCD Operation



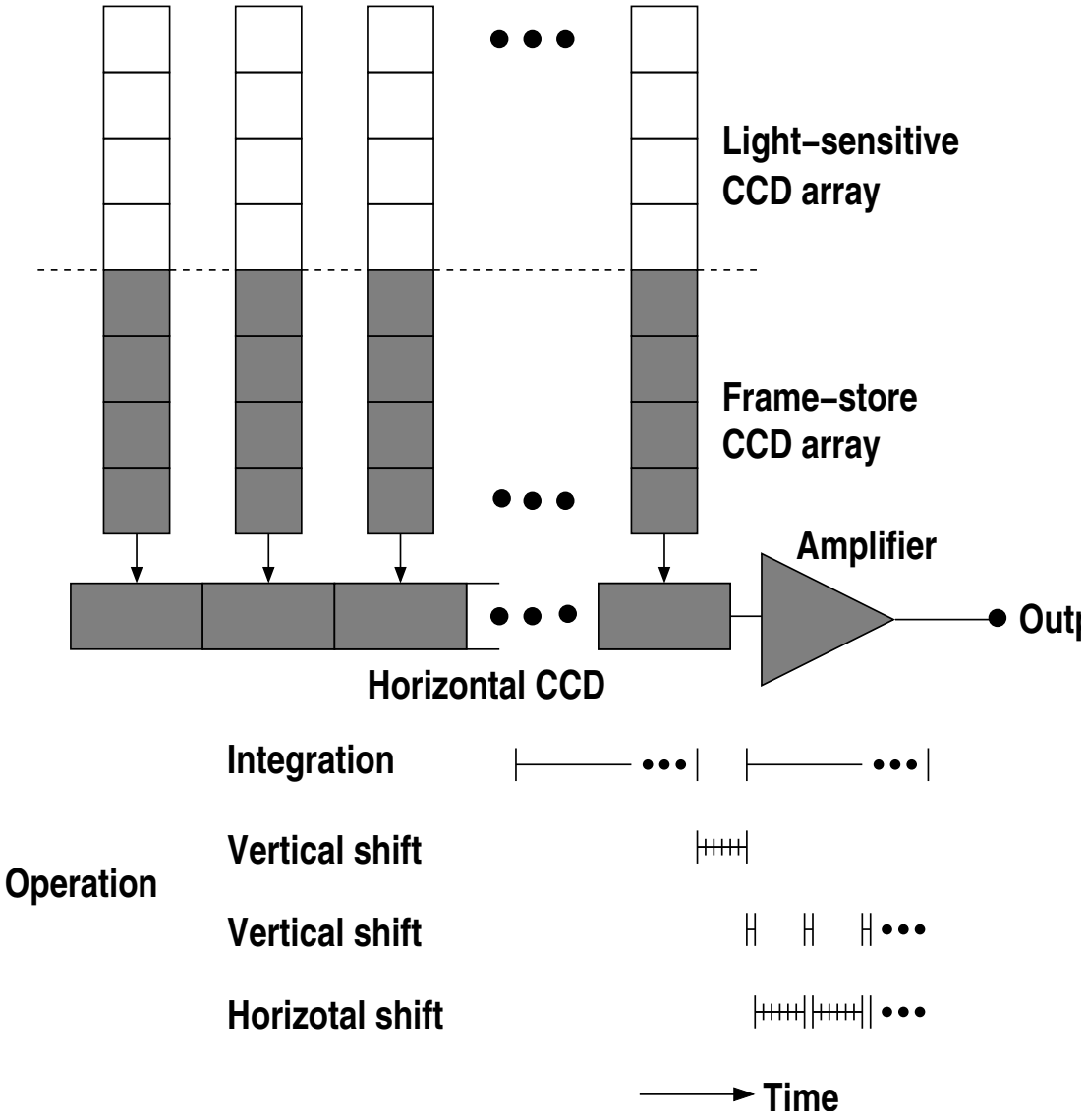
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

- A line of photodiodes or photogates is used for photodetection
- After integration, charge from the entire row is transferred in parallel to the horizontal CCD (HCCD) through transfer gates
- New integration period begins while charge packets are transferred through the HCCD (serial transfer) to the output readout circuit (to be discussed later)
- The scene can be mechanically scanned at a speed commensurate with the pixel size in the vertical direction to obtain 2D imaging
- Applications: scanners, scan-and-print photocopiers, fax machines, barcode readers, silver halide film digitization, DNA sequencing
- Advantages: low cost (small chip size)

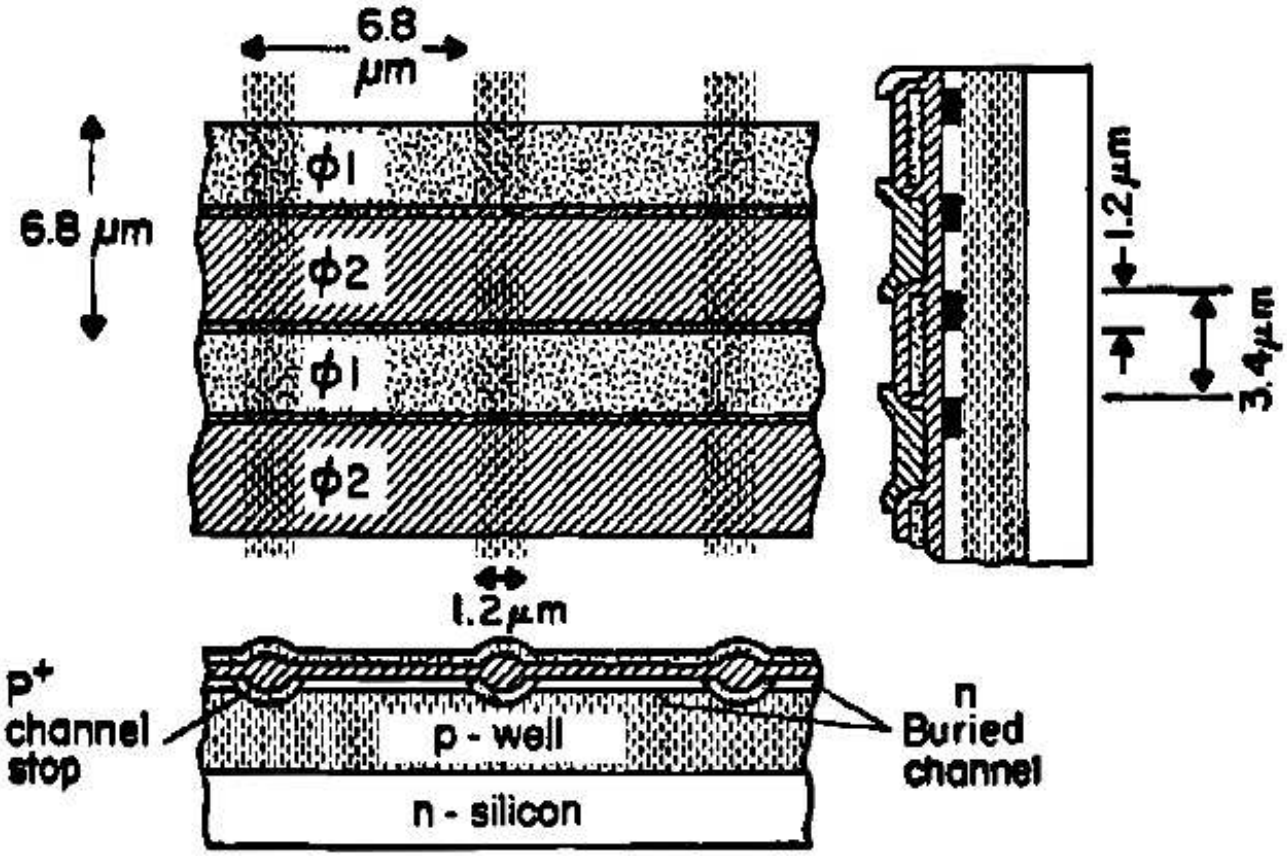
Two-Dimensional (Area) CCD

- Frame transfer CCD (FT-CCD)
  - Full frame CCD
- Interline transfer CCD (IL-CCD)
- Frame-interline transfer CCD (FIT-CCD)
- Time-delay-and-integration CCD (TDI-CCD)

Frame Transfer CCD

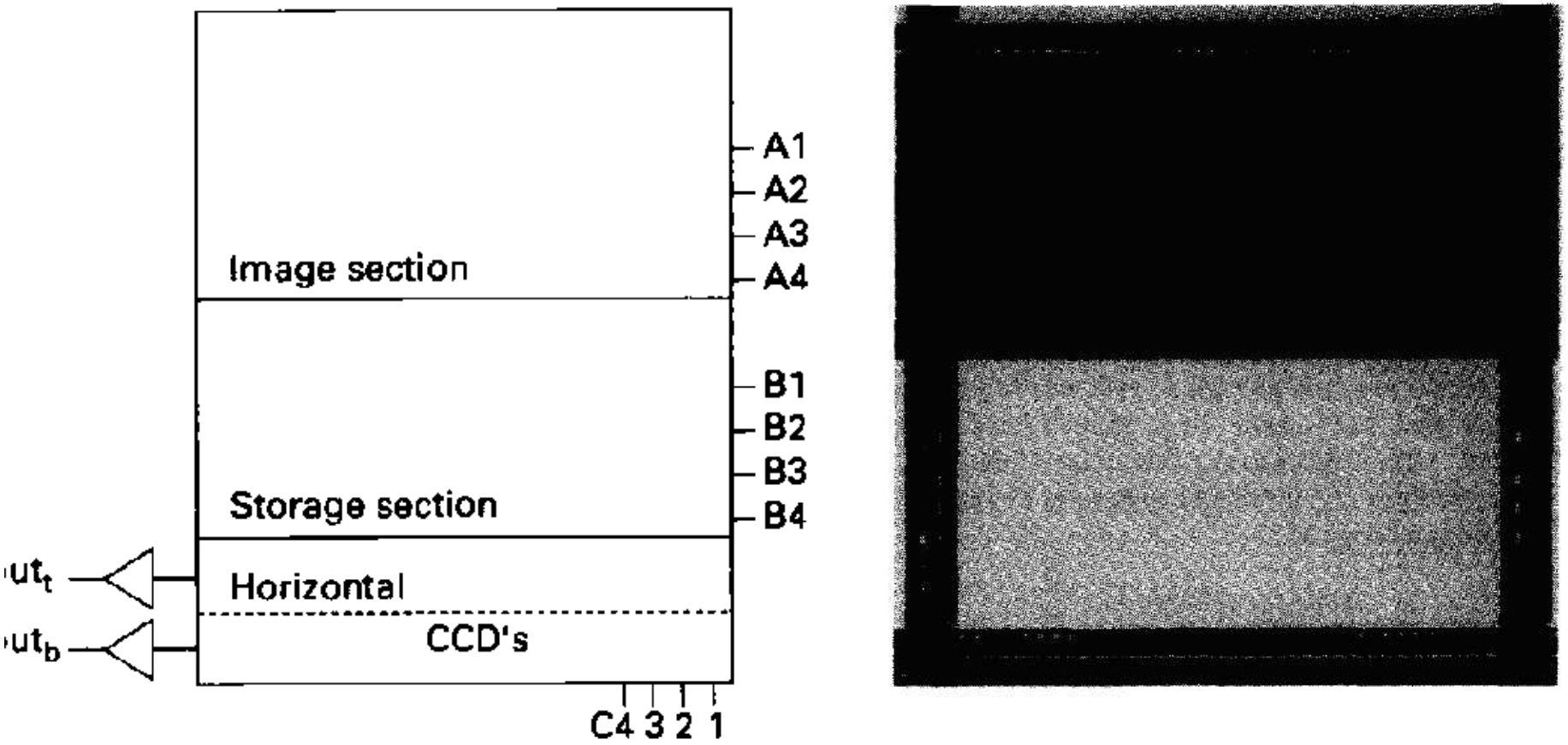


Pixel Layout – FT-CCD



D. N. Nichols, W. Chang, B. C. Burkey, E. G. Stevens, E. A. Trabka, D. L. Losee, T. J. Tredwell, C. V. Stancampiano, T. M. Kelly, R. P. Khosla, and T. H. Lee, "A 1.4 million element, full frame CCD image sensor with vertical overflow drain for anti-blooming and low color crosstalk," IEDM Tech. Dig., pp. 120 - 123, December 1987

2.2 Mpixel FT-CCD Example



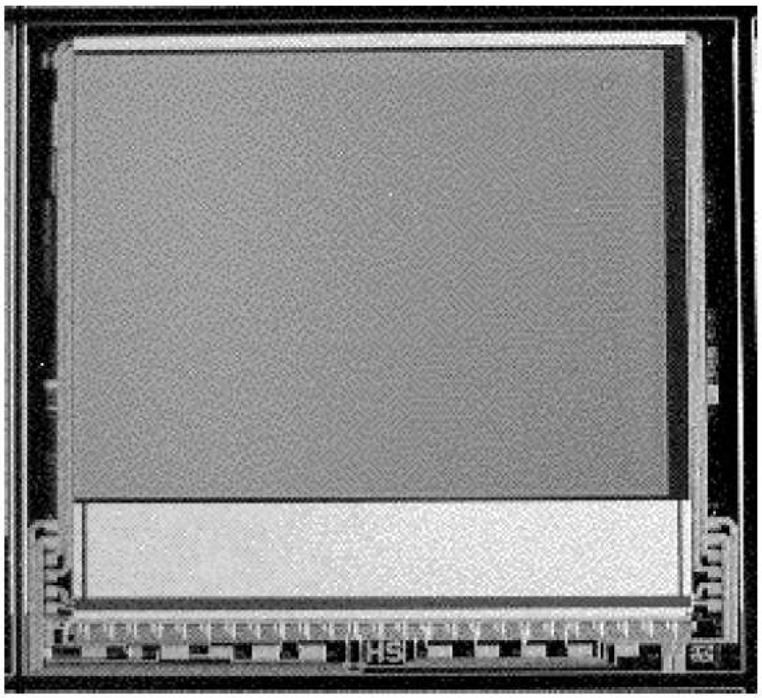
A. J. P. Theuwissen, H. L. Peek, M. J. H. van de Steeg, R. M. G. Boesten, P. B. Hartog, A. L. Kokshoorn, E. A. De Koning, J. M. A. M. Oppers, F. F. Vledder, P. G. M. Centen, H. Blom, and W. Haar, "A 2.2 M pixel FT-CCD imager according to the Eureka HDTV standard," IEEE Trans. Electron Devices, Vol. 40, pp. 1621 - 1629, September 1993

2.2 Mpixel FT-CCD Characteristics

- Image section (H x V) : 13.92 mm x 7.83 mm
- Number of active lines (V) : 1152
- Number of active pixels per line (H): 1920
- Pixel dimensions (H x V): 7.25 μm x 13.6 μm
- Chip dimensions (H x V): 15.37 mm x 15.57 mm
- Number of output registers: 2
- Pixel output rate: 72 MHz
- Horizontal clocks: 36 MHz, 5V
- Vertical clocks: 1.125 MHz, 8 V
- Conversion gain: 6.5 μV/e
- Full well capacity: 10^5 electrons

A. J. P. Theuwissen, H. L. Peek, M. J. H. van de Steeg, R. M. G. Boesten, P. B. Hartog, A. L. Kokshoorn, E. A. De Koning, J. M. A. M. Oppers, F. F. Vledder, P. G. M. Centen, H. Blom, and W. Haar, "A 2.2 M pixel FT-CCD imager according to the Eureka HDTV standard," IEEE Trans. Electron Devices, Vol. 40, pp. 1621 - 1629, September 1993

3 Mpixel FT-CCD Example



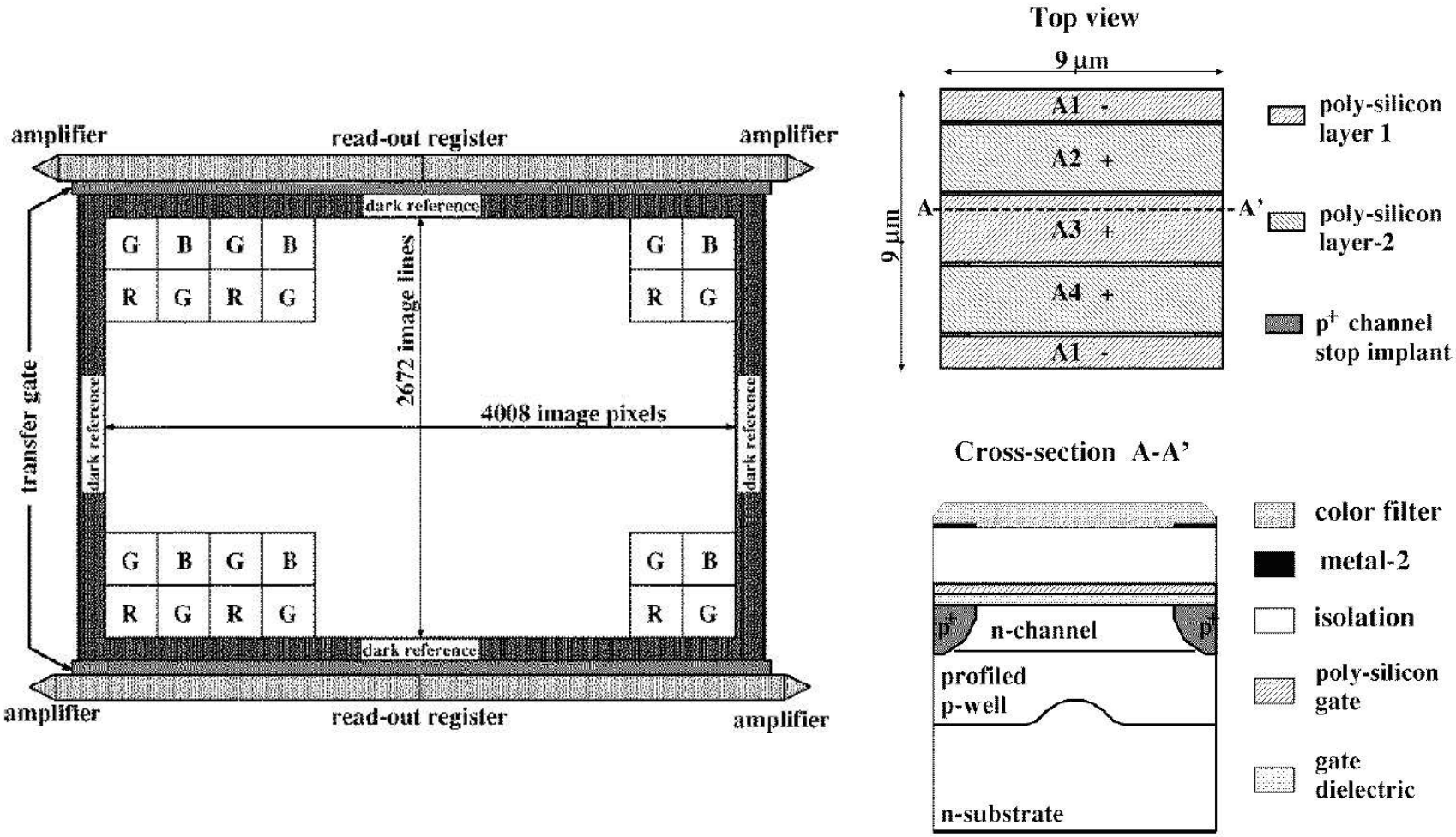
- 1500(V)×2000(H) pixels
- 68.4 mm^2
- 3.6 μm x 3.6 μm pixel
- Vertical clocks: 1.56 MHz, 12V
- Horizontal clocks: 25 MHz, 3.3V
- Well capacity: 28,000 e−

L. Le Cam, J. Bosiers, A. Kleimann, H. van Kuijk, J. Maas, M. Beenhakkers, H. Peek, P. de Rijt, and A. Theuwissen, "A 1/1.8" 3M pixel FT-CCD with on-chip horizontal sub-sampling for DSC Applications," IEEE International Solid-State Circuits Conference, vol. XLV, pp. 34 - 35, February 2002.

Full Frame CCD

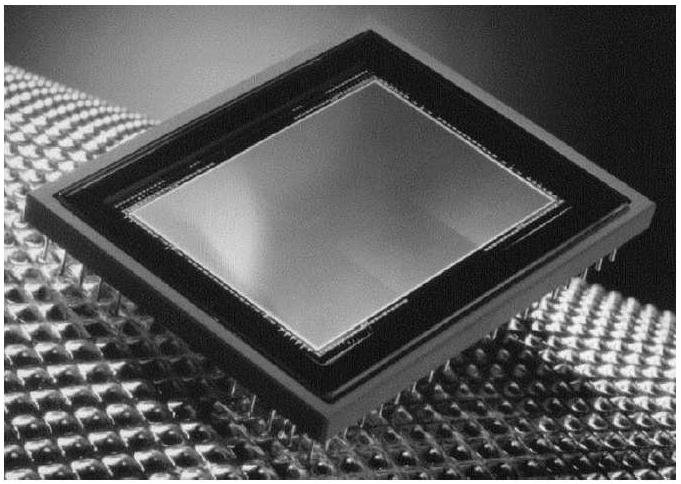
- Frame transfer CCD without the frame store
  - Charge shifted in parallel to HCCD directly one row at a time
- Needs a mechanical shutter
- Used in large-format still cameras that require very high quality
  - No smear
  - No lag

Full Frame CCD Example



J. T. Bosiers, B. G. M. Dillen, C. Draijer, A. C. Kleimann, F. J. Polderdijk, M. A. R. C. de Wolf, W. Klaassens, A. J. P. Theuwissen, H. L. Peek, and H. O. Folkerts, "A 35-mm format 11 M pixel full-frame CCD for professional digital still imaging," IEEE Trans. Electron Devices, Vol. 50, pp. 254 - 265, January 2003

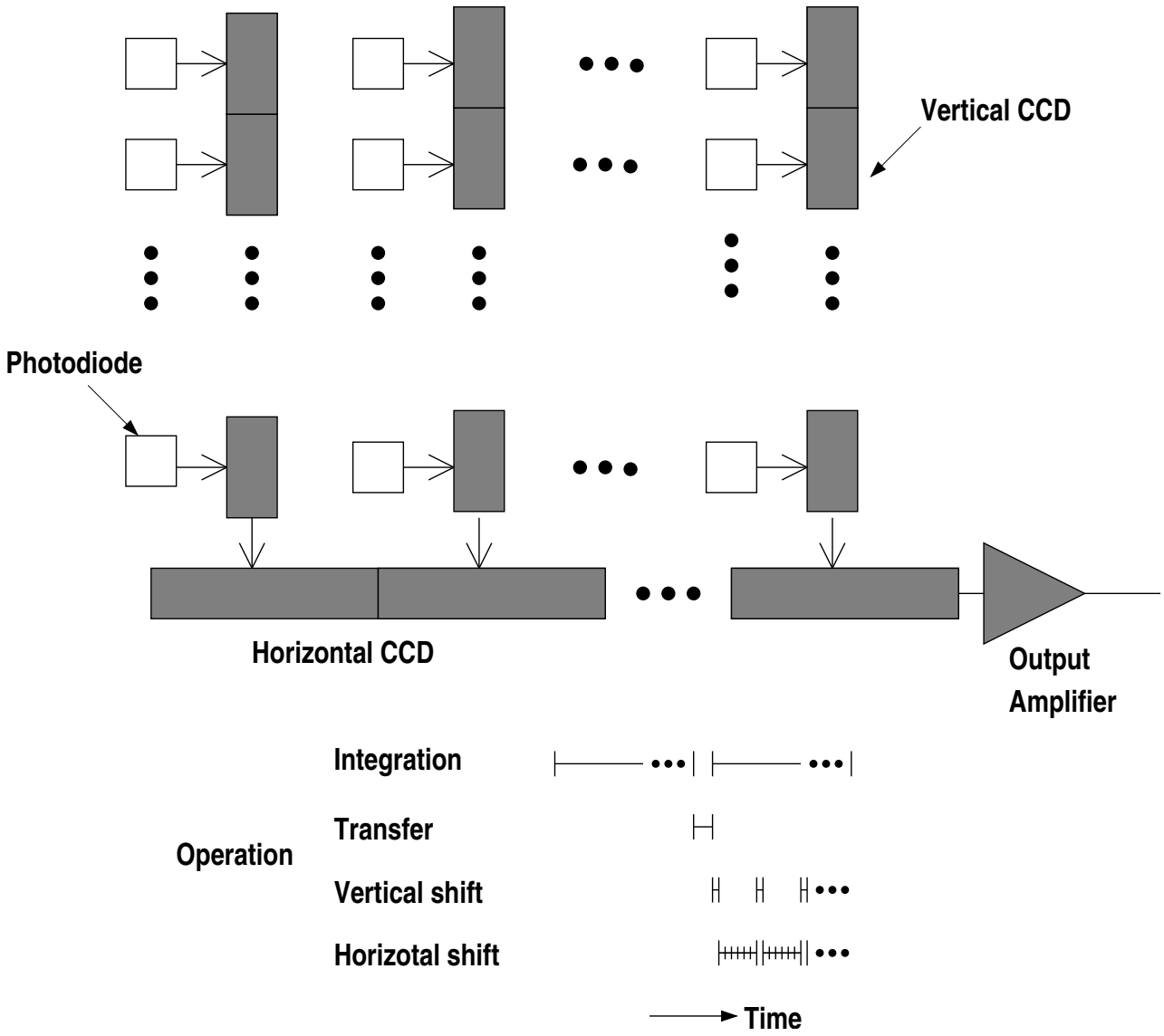
Full Frame CCD Example (contd.)



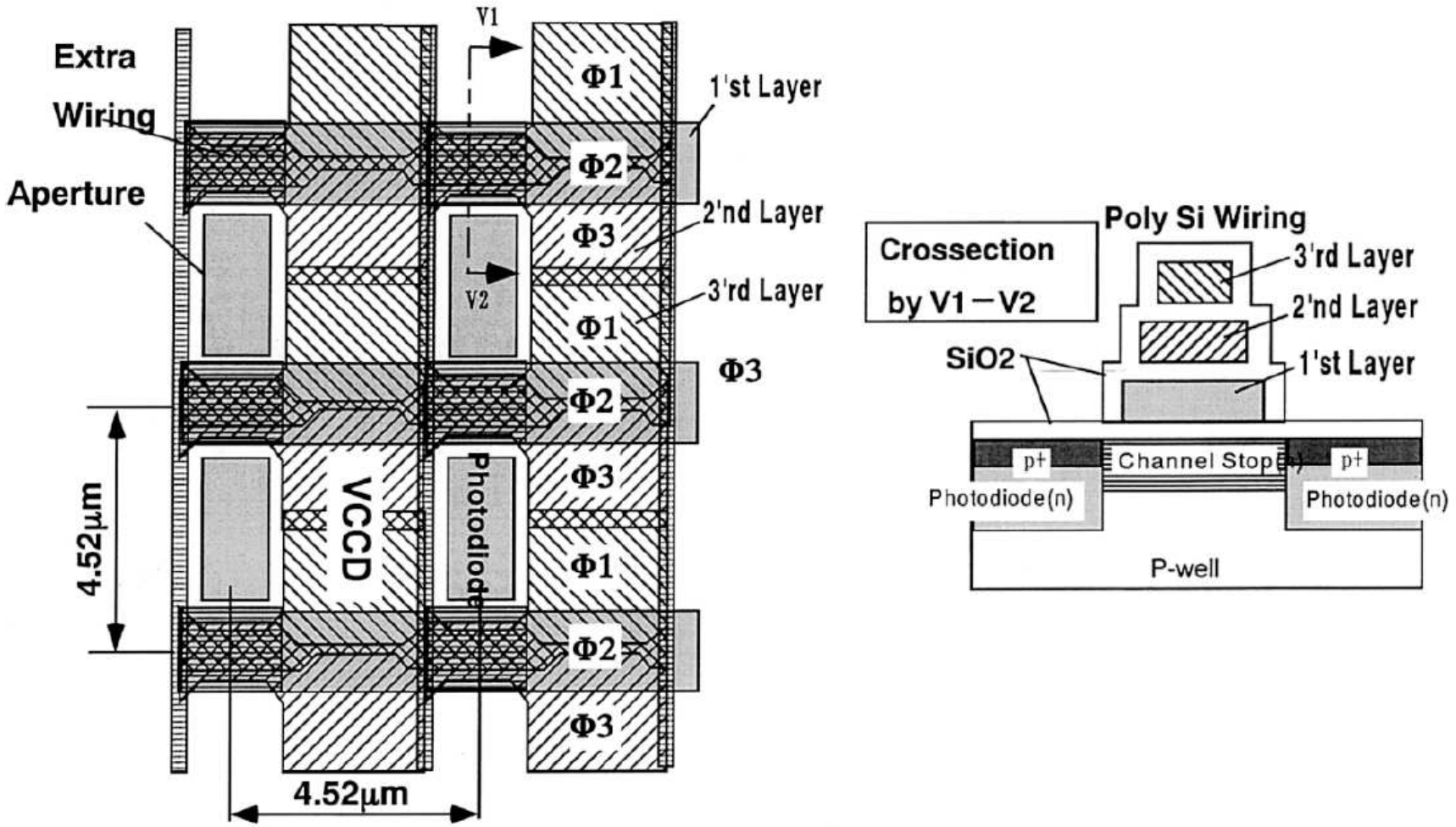
- 0.5 μm, 3 layer polySi, 1 (+1) metal
- 36.072 mm $\times$ 24.048 mm
- 4008×2672 pixels ($\approx$ 11Mpixels)
- 9 μm x 9 μm pixel

J. T. Bosiers, B. G. M. Dillen, C. Draijer, A. C. Kleimann, F. J. Polderdijk, M. A. R. C. de Wolf, W. Klaassens, A. J. P. Theuwissen, H. L. Peek, and H. O. Folkerts, "A 35-mm format 11 M pixel full-frame CCD for professional digital still imaging," IEEE Trans. Electron Devices, Vol. 50, pp. 254 - 265, January 2003

Interline Transfer CCD (IT-CCD)

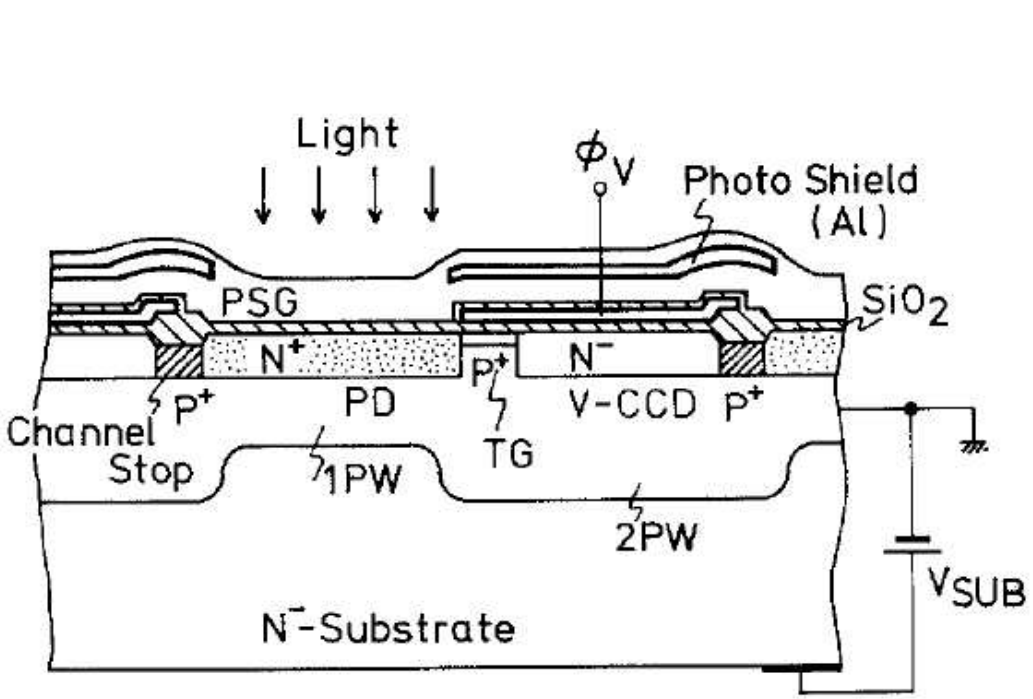


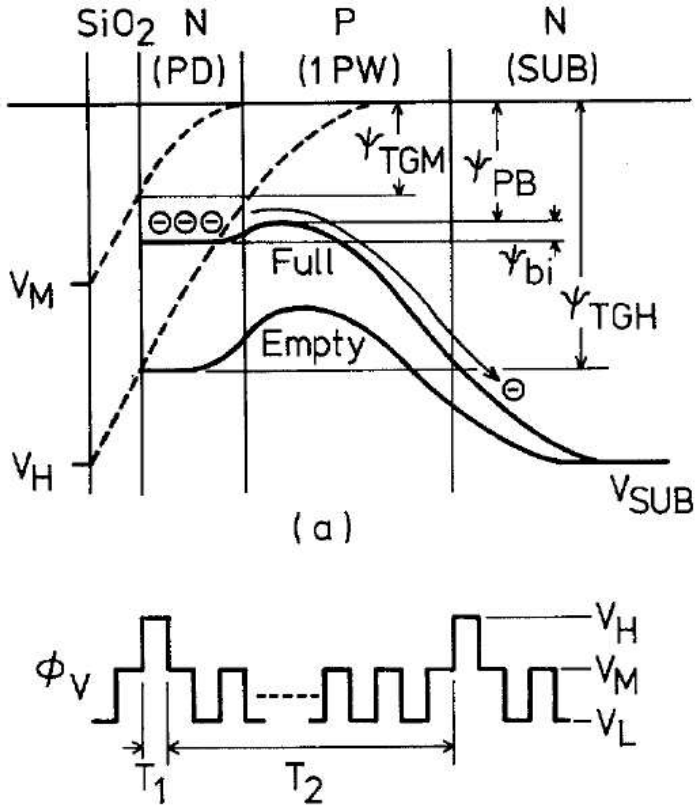
Pixel Layout – IT-CCD



T. Yamada, K. Ikeda, Y. Kim, H. Wakoh, T. Toma, T. Sakamoto, K. Ogawa, E. Okamoto, K. Masukane, K. Oda, and M. Inuiya, "A progressive scan CCD image sensor for DSC applications," IEEE Journal of Solid-State Circuits, vol. 35, pp. 2044 - 2054, December 2000

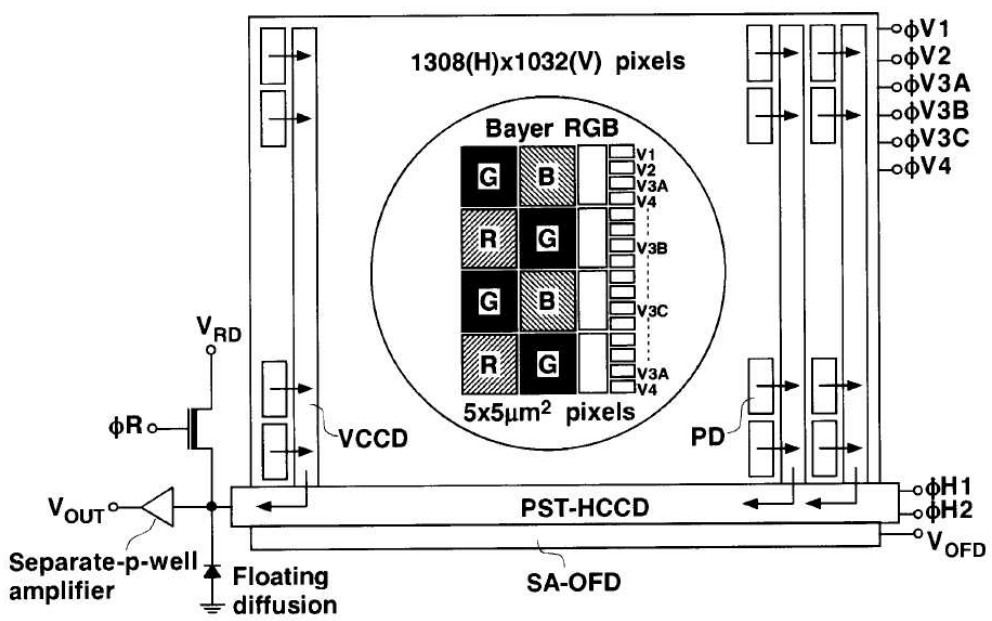
Pixel Cross-Section – IT-CCD

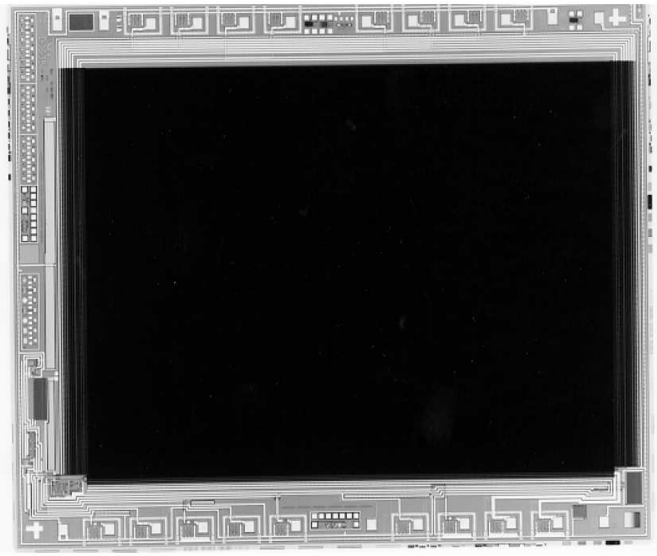




Y. Ishihara, E. Oda, H. Tanigawa, N. Teranishi, E. Takeuchi, I. Akiyama, K. Arai, M. Nishimura, and T. Kamata, "Interline CCD image sensor with an anti blooming structure," IEEE International Solid-State Circuits Conference, vol. XXV, pp. 168 - 169, February 1982

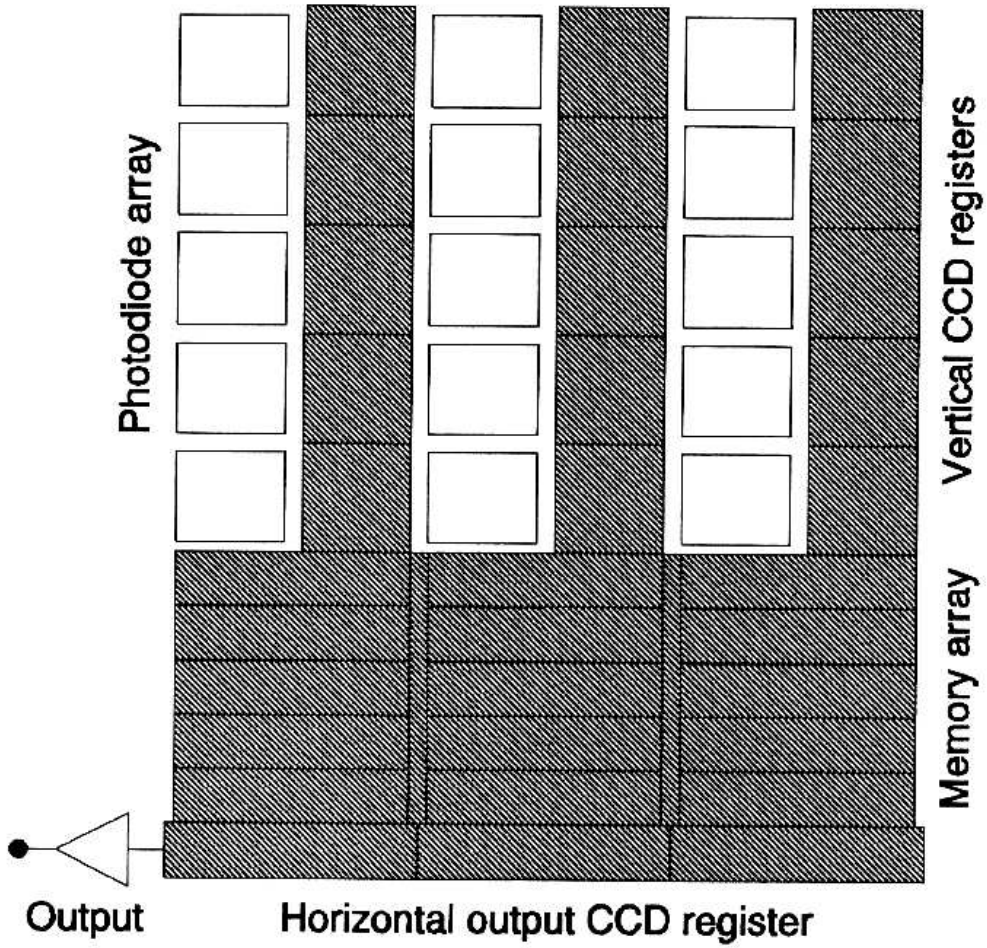
IT-CCD Chip





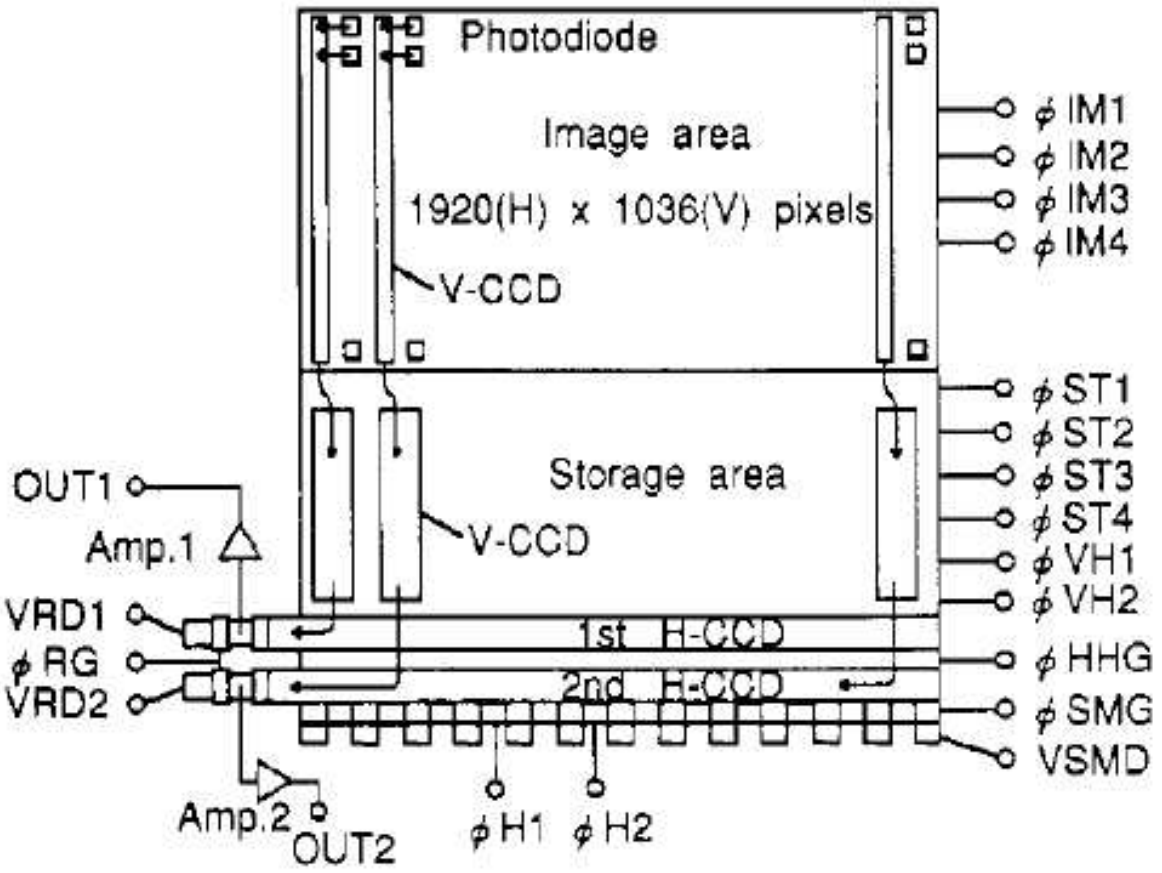
T. Yamada, K. Hatano, M. Morimoto, Y. Nakashiba, S. Uchiya, A. Tanabe, Y. Kawakami, T. Nakano, S. Kawai, S. Suwazono, H. Utsumi, S. Katoh, D. Syohji, Y. Taniji, N. Mutoh, K. Orihara, N. Teranishi, and Y. Hokari, "A 1/2 inch 1.3M-pixel progressive-scan IT-CCD for still and motion picture applications," IEEE International Solid-State Circuits Conference, vol. XLI, pp. 178 - 179, February 1998

Frame-Interline Transfer CCD (FIT-CCD)



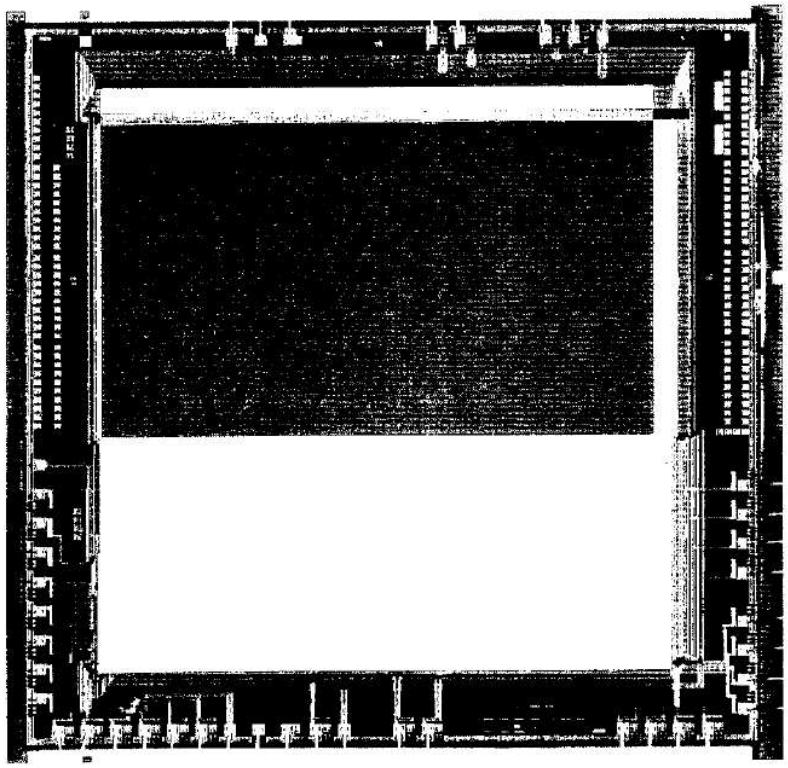
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

FIT-CCD Example



K. Harada, M. Negishi, T. Ohgishi, S. Kubota, T. Oda, and M. Yamagishi, "A 2/3-inch 2M pixel FIT-CCD HDTV image sensor," IEEE International Solid-State Circuits Conference, vol. XXXV, pp. 170 - 171, February 1992

FIT-CCD Example (contd.)

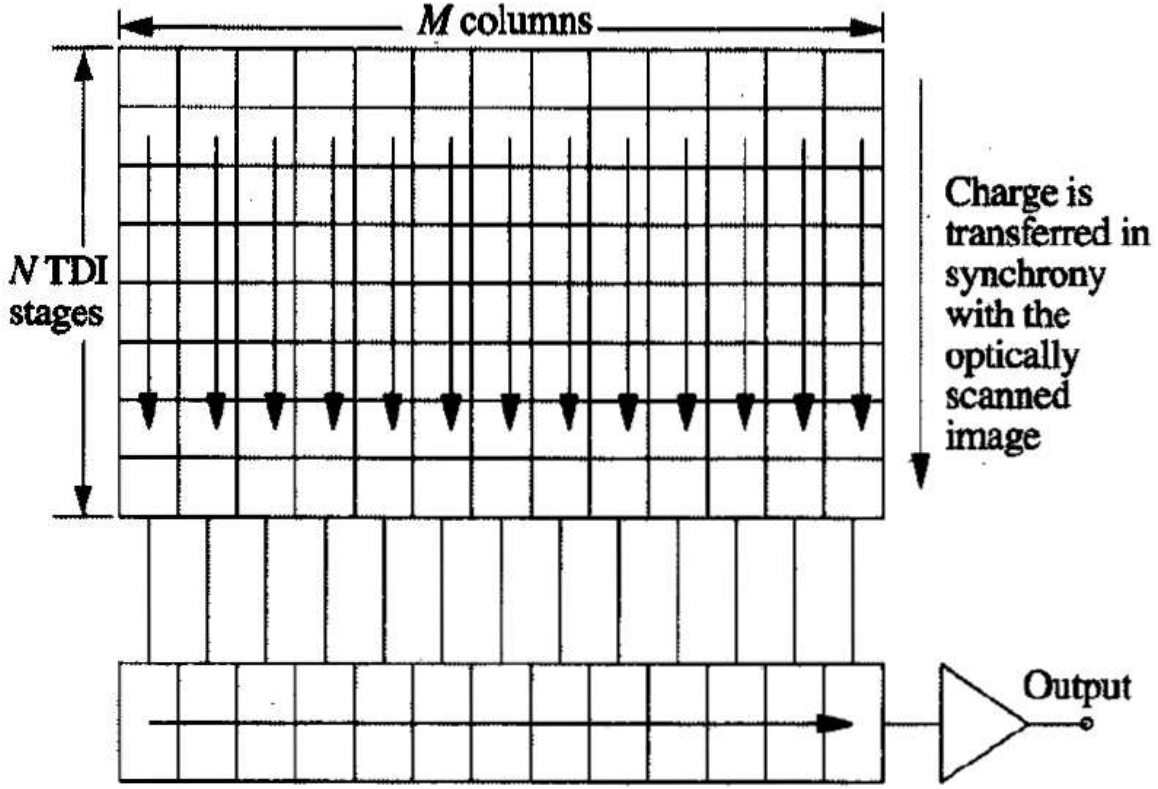


- 2/3 inch optical format
- 9.6mm (H)$\times$5.4mm (V)
- 1920(H)$\times$1036(V) pixels
- 5.0μm(H)$\times$5.2μm(V) image area
- Transfer efficiency: 99.997
- Conversion gain: 14 μV/e
- Sensitivity: 30 nA/lx (at 2856K)
- Smear reduction ratio: - 90 dB

K. Harada, M. Negishi, T. Ohgishi, S. Kubota, T. Oda, and M. Yamagishi, "A 2/3-inch 2M pixel FIT-CCD HDTV image sensor," IEEE International Solid-State Circuits Conference, vol. XXXV, pp. 170 - 171, February 1992

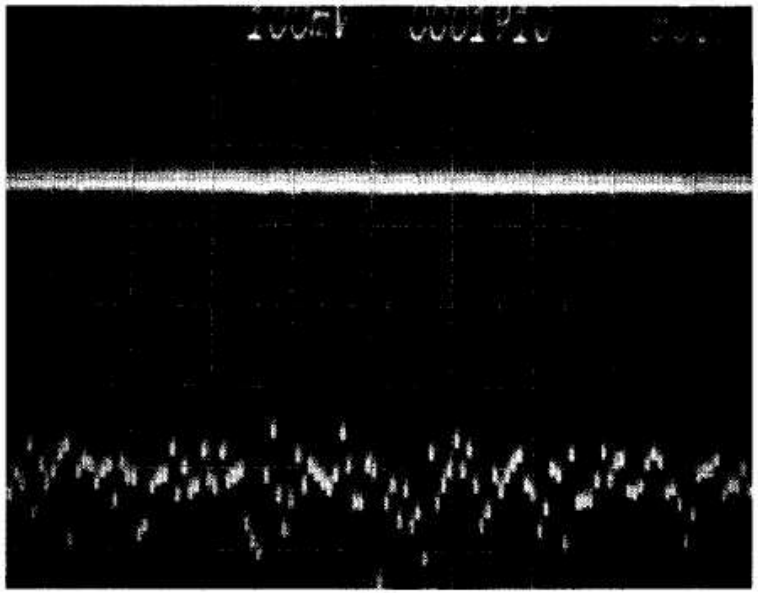
Time-Delay-and-Integration CCD (TDI-CCD)

- Essentially a full frame CCD with m>>n coupled with mechanical motion

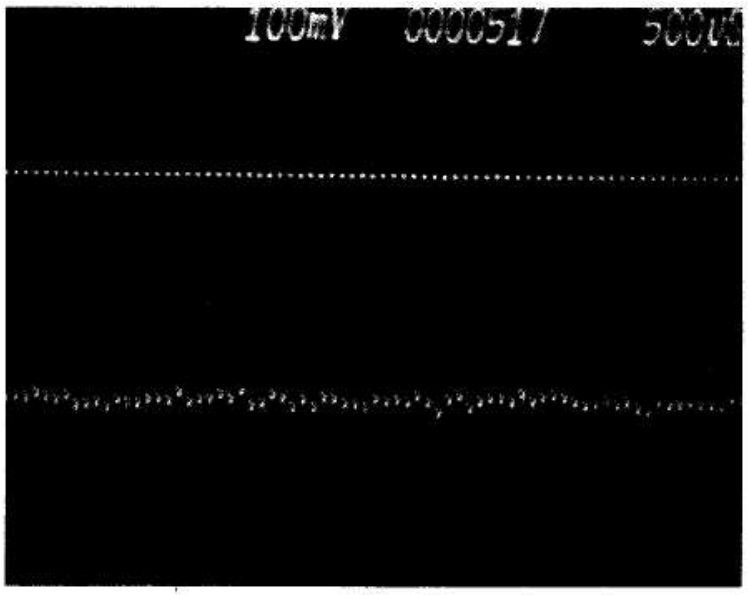


H.-S. P. Wong, Y.L. Yao, E.S. Schlig, "TDI Charge-Coupled Devices - Design and Applications," IBM J. Research & Development, Vol. 36, p. 38, 1992

- Integration provides
  - Dark current averaging
  - Low-light sensitivity
- Employed for high-quality (low-light) imaging
  - Silver halide film digitization
  - Art object imaging
- TDI-CCD dark current averaging:

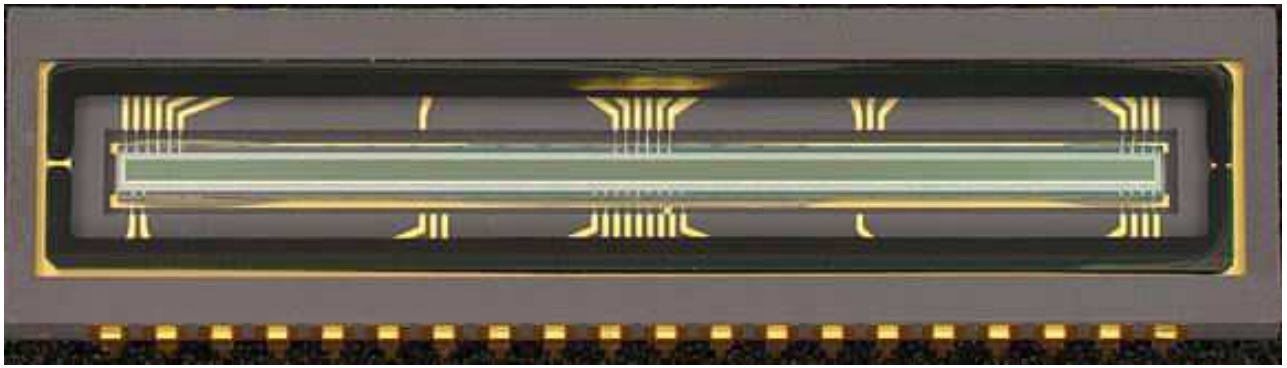


Dark current – full frame mode clocking (no averaging)



Dark current – TDI mode clocking (32 line averaging)

TDI-CCD Example



Imager designation	*Architecture*	*Features and applications*
TDI-2S	512 × 32-stage, one output port, 20-MHz pixel rate	10–15 s/page, office ambient illumination, for optical character recognition
TDI-2	2048 × 32-stage, one output port, 20-MHz pixel rate	0.8–1.5 s/page, flatbed scanner, 240 pels/in. for A4 document
TDI-3	1024 × 32-stage, eight output ports, 96-MHz pixel rate, electronic exposure control of 1× and 32× sensitivity	350 document-in./s (40 Federal Reserve Bank checks per second) at 250 W, *f*/2.8, 240 pels/in.
TDI-4	3072 × 32-stage, two output ports, 24-MHz pixel rate	1–2 page/s, camera-type scanner for museum art object and high-resolution scanning
TDI-5	3072 × 64-stage, two output ports, 24-MHz pixel rate	1–2 page/s, camera-type scanner for museum art object and high-resolution scanning

H.-S. P. Wong, Y.L. Yao, E.S. Schlig, "TDI Charge-Coupled Devices - Design and Applications," IBM J. Research & Development, Vol. 36, p. 38, 1992

Pros and Cons of CCD Architectures

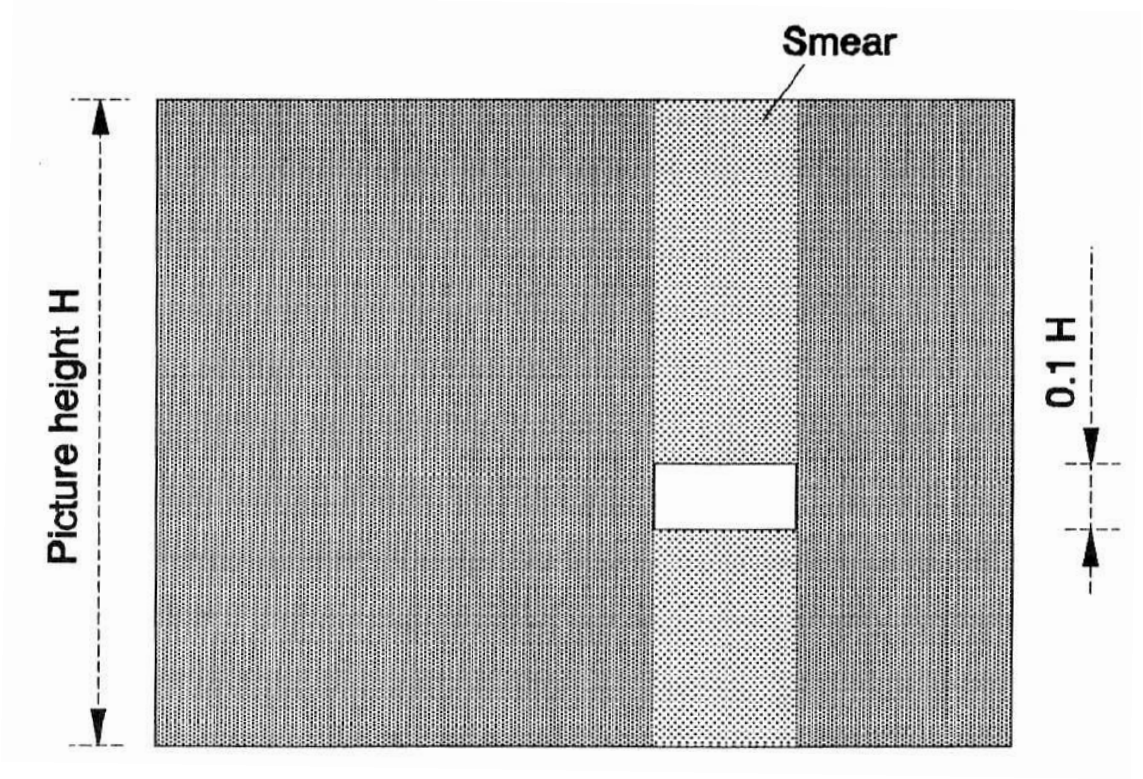
Device	Pros	Cons
FT-CCD	Large light sensitive area Electronic shutter Flexible binning, subsampling	Large chip size High smear level Poorer blue sensitivity
IT-CCD	Small chip size	Small light sensitive area High smear level More complex device fabrication
FIT-CCD	Low smear level	Large chip size Small light sensitive area
Linear CCD	Low cost	Mechanical motion required
TDI-CCD	Low-light sensitivity Dark current averaging	Accurate mechanical motion required

CCD Clocking

- Many clocks with multiple voltage levels are required
- E.g., 4-phase IT-CCD:
  - 4 clocks for VCCD (image section)
  - 4 clocks for VCCD (storage section)
  - 2 clocks for transfer to HCCD
  - 2 clocks for HCCD (fastest clock)
  - 1 clocks to direct transfer to two HCCDs
  - 1 clock to control the smear drain (SMG)
  - 1 clock to reset floating diffusion output node

Smear in FT-CCD

- Smear in FT-CCD is generated when the charge packets are transferred from the imaging section to the storage section
- If the imager is not shielded from incoming light (e.g., by a mechanical shutter) during this transfer, photo-carrier generation continues and spurious signals are added to the charge packets during the transport

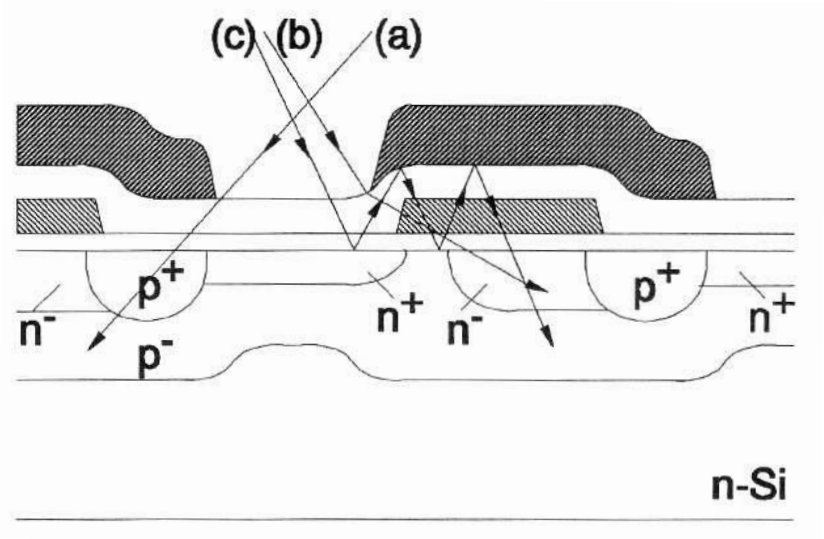


- Smear is usually measured for 10% vertical height illumination (i.e., ΔH=0.1H) as $\Delta H \cdot (t_{transport}/t_{int}) \times 100$
- To reduce smear, fast transport is needed
- But transport is limited by RC delay in the long gate electrodes of the CCD

A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

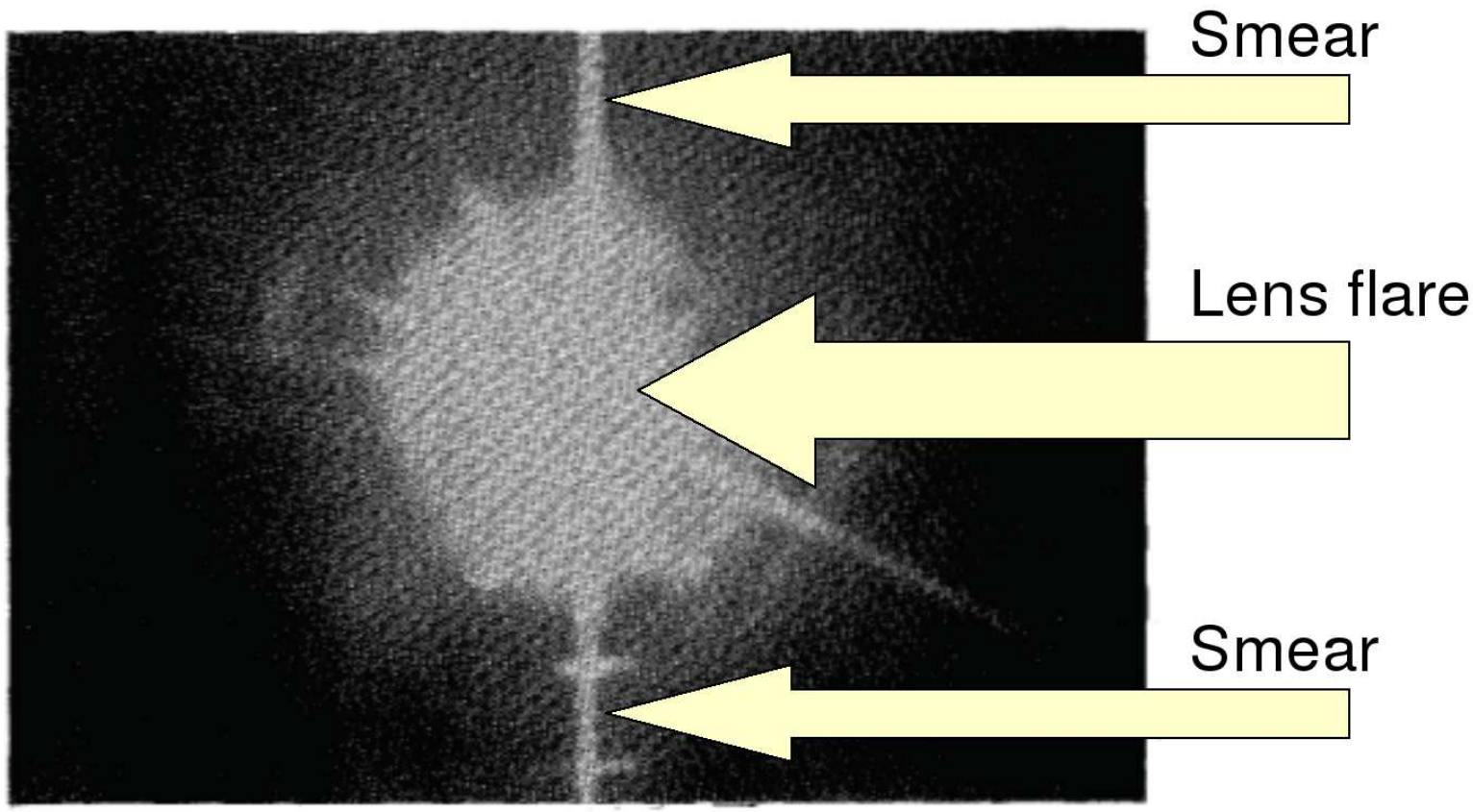
Smear in IT-CCD

- Smear in IT-CCD is due to the presence of the VCCD and happens during the VCCD charge transfer
- It is caused by
  - Stray electrons generated underneath the photodiode area and diffused into the vertical CCD shift registers
  - Stray photons that arrive at the vertical CCD via light pipes (multiple reflections at the Si/SiO2 interface and at the lower surface of the light shield) and generate e-h pairs at that location



- It is composed of two temporal components:
  - Before the start of the integration, and during the last clocking cycles of the frame shift of the previous field
  - After the end of the integration, during the frame shift of the existing field
- Smear manifests itself as vertical stripes (see live demo in class)
- Typical smear is in the 0.01% range for consumer imagers, and much smaller for professional applications (e.g., broadcast)

Smear in IT-CCD – Example



N. Teranishi and Y. Ishihara, "Smear reduction in the interline CCD image sensor," IEEE Trans. Electron Devices, Vol. 34, pp. 1052 - 1056, May 1987

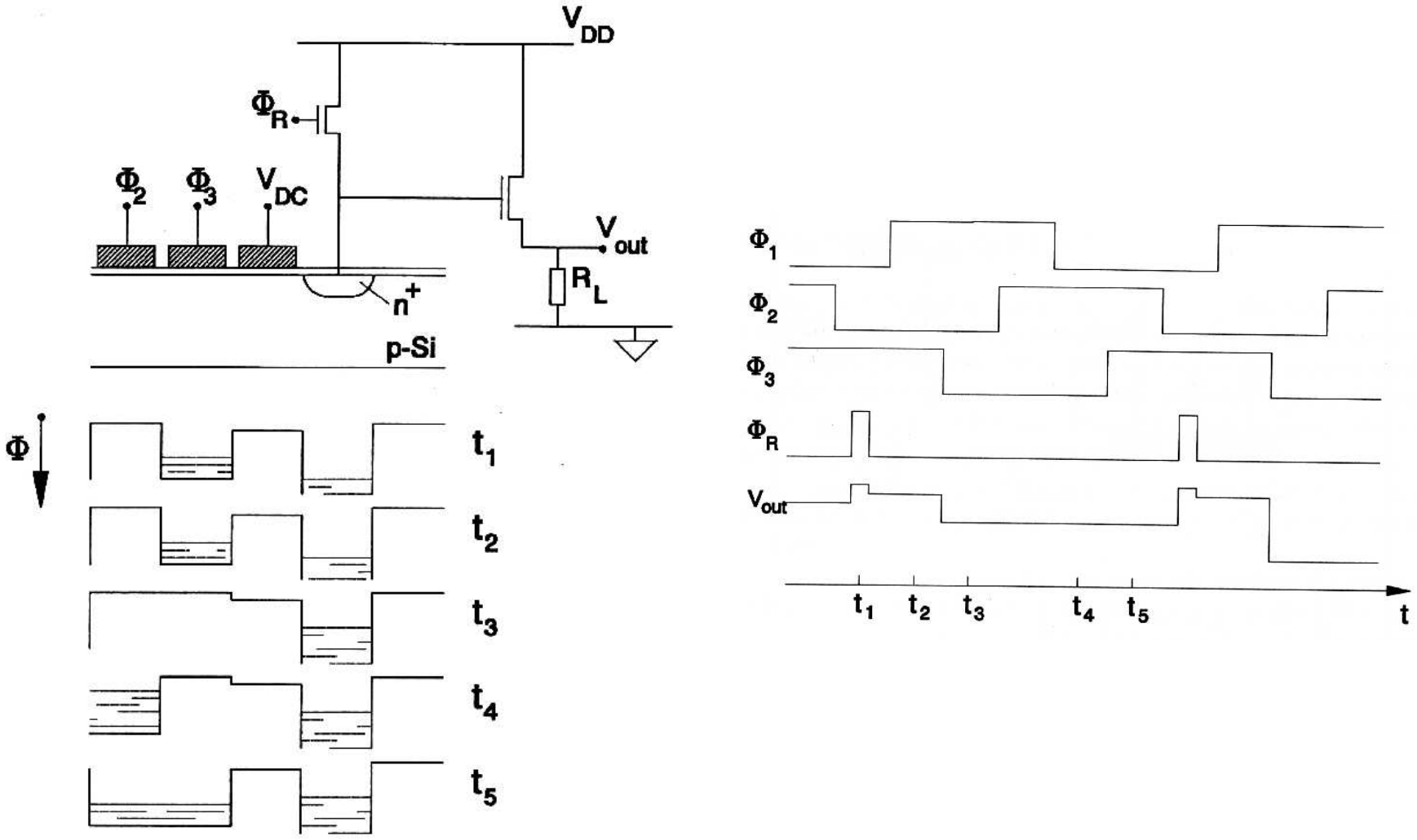
Smear Reduction Techniques

- Add an extra p+ diffusion barrier under the buried channel VCCD that prevents electron in-diffusion from regions deeper in the substrate
- Reduce light piping by optimizing the light shield and locating it as close as possible to the silicon surface
- Reduce the time during which smear electrons can be generated and added to the charge packets (shorten the time charge packets are in the VCCD)
    - Frame-Interline Transfer CCD (FIT-CCD)

Readout Circuit

- So far, we have learned how to
  - Convert photons into electrons (signal charge)
  - Organize the photodetectors (pixels) into arrays to form an image
  - Move the signal charge (electrons) around to an output node
- Now, we discuss how to read out the photo-electrons
- Typically, the signal charge are read out as a voltage
  - Current mode readout also possible (see later discussion on CMOS image sensors)

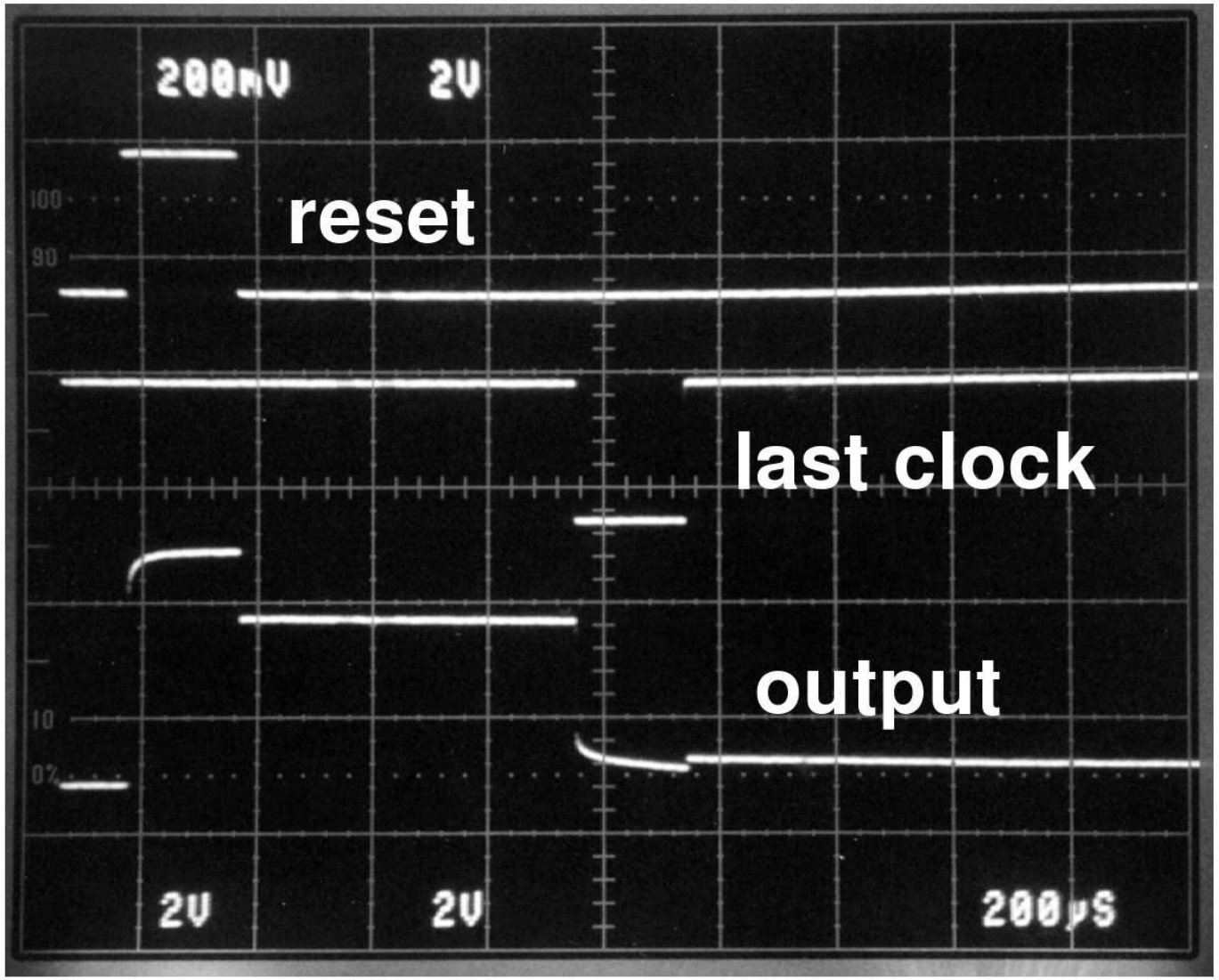
Floating Diffusion With Reset



A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

- The signal charge packet is transferred to a floating diffusion node (a pn-junction capacitor)
- Timing sequence:
  - Floating diffusion node is reset to a high voltage (higher than CCD channel potential at zero charge)
  - Signal charge is pushed (transferred) through a DC biased transfer gate to the floating diffusion node
  - Voltage on the floating diffusion node is read out
  - Repeat step 1 to receive the charge packet for the next pixel
- The DC biased transfer gate is required to prevent charge from flowing back to the CCD from the floating diffusion node

Floating Diffusion Clocking Example



Conversion Gain of Floating Diffusion Output

- Note that

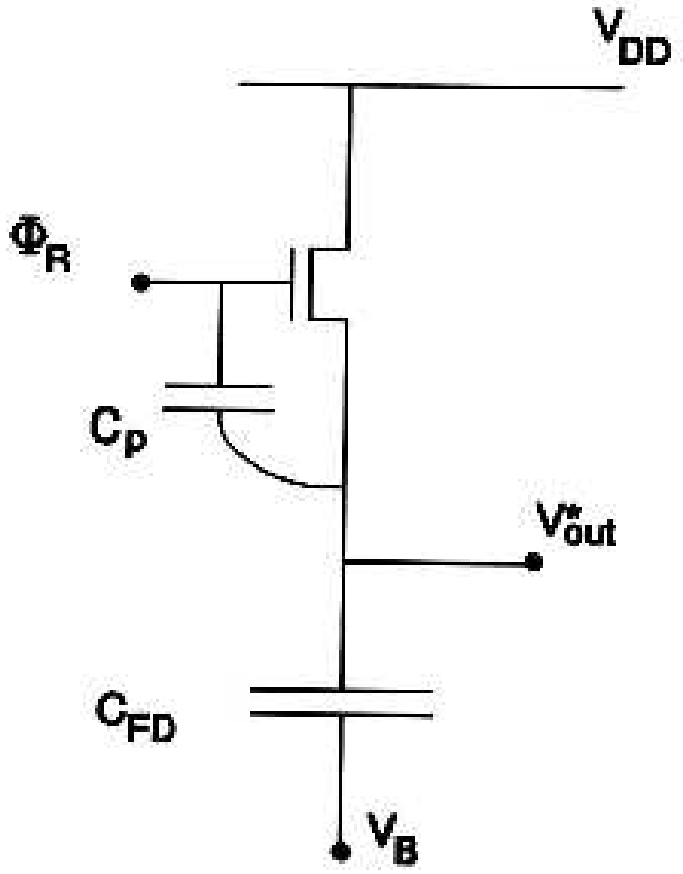
$$\Delta v^*_{out} = \frac{-qQ_{sig}}{C_{FD}+C_p}$$

$$\Delta v_{out} = \frac{-qQ_{sig}}{C_{FD}+C_p}A_{SF},$$

  where A_{SF} is source follower gain

- Conversion Gain (in $V/e-$) is

$$\Delta v_{out}/Q_{sig} = \frac{-q}{C_{FD}+C_p}A_{SF}$$

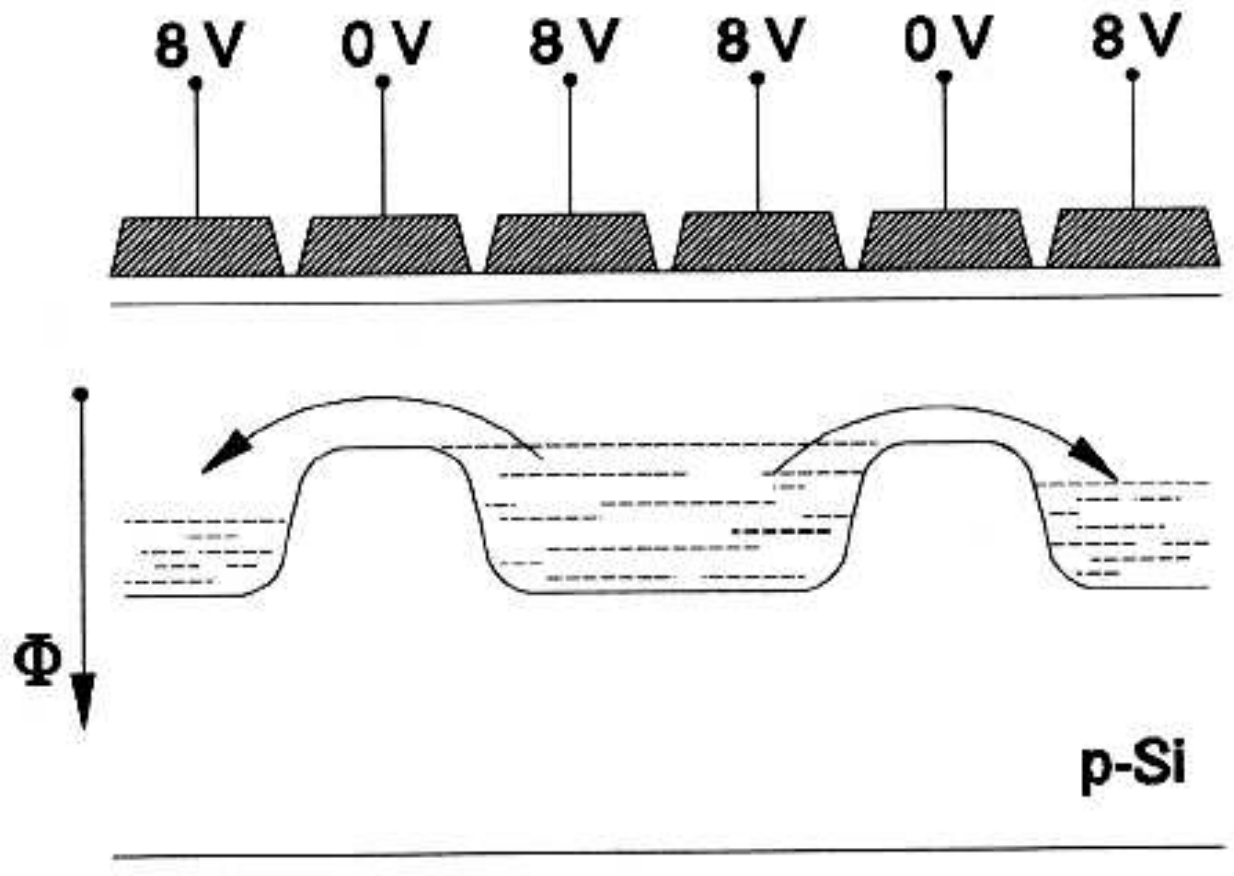


A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

Blooming and Anti-Blooming

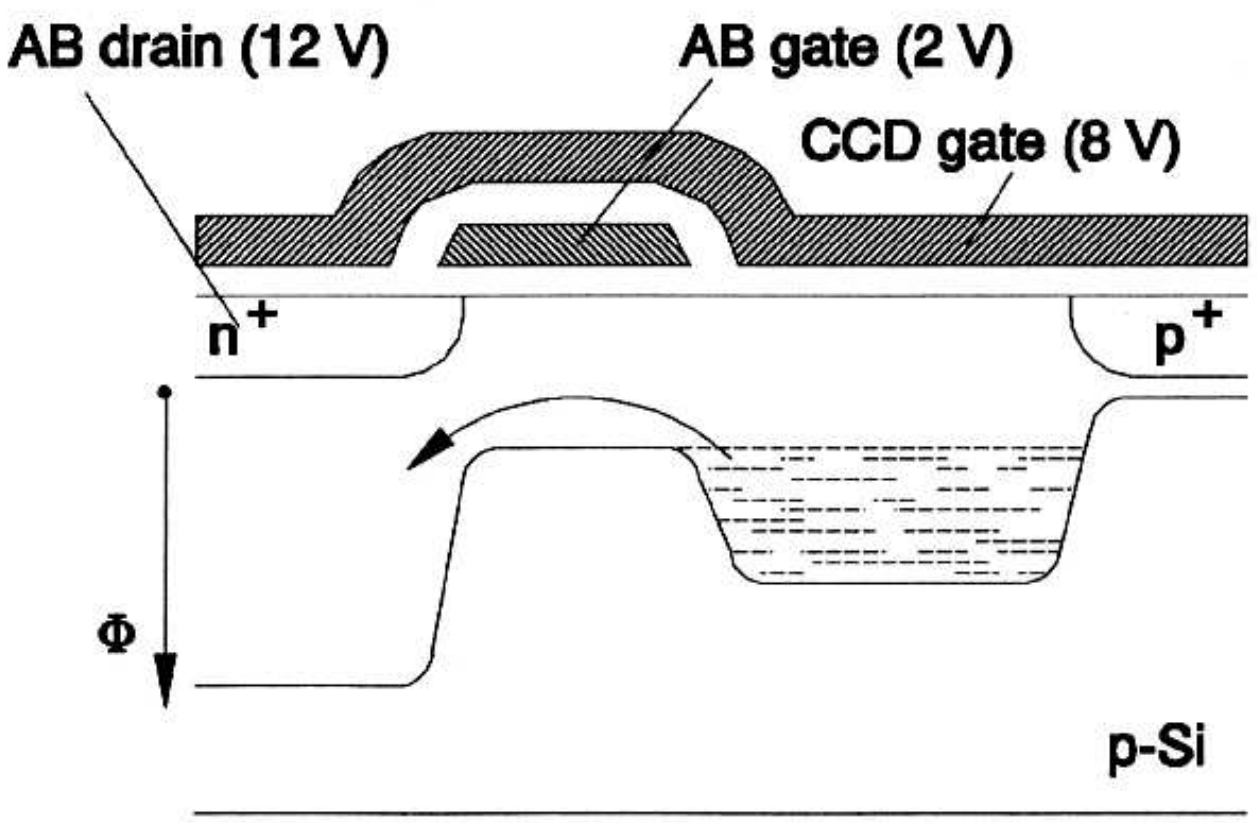
- Scene with highlight (excessive light) can cause an image artifact called "blooming"
- Blooming occurs with the amount of photo-carriers is so large that it spills over to the neighboring potential wells
- Captured image shows artifacts in the scene as column or line defects around the areas with high light intensity
- There are two anti-blooming methods
  - Lateral overflow drain (LOD)
  - Vertical overflow drain (VOD)
- Both methods work for CCD as well as CMOS image sensors
- Vertical overflow drain works differently for FT-CCD and IT-CCD

Blooming – Charge Well Illustration



A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

Lateral Overflow Drain (LOD) Structure



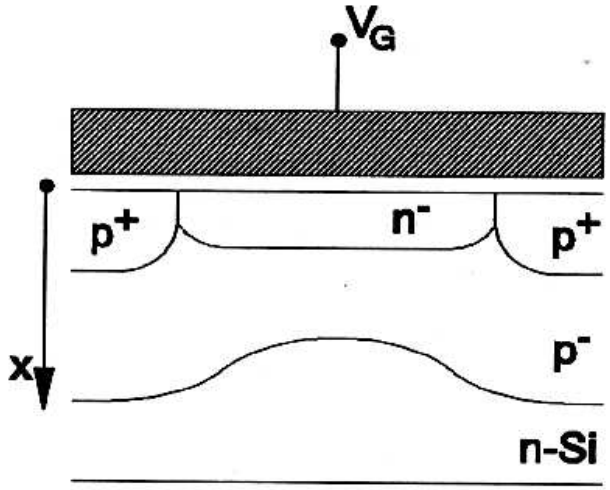
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

LOD Pros and Cons

- Can be implemented in
  - CCD or CMOS image sensors
  - Photodiode or photogate photodetectors
- Pros
  - Very simple to design and fabricate, only needs an extra biased gate
  - Can adjust blooming overflow level by blooming gate biasing
  - Some dynamic range extension schemes are based on this
- Cons
  - Reduces pixel light sensitive area (i.e., reduces fill factor)

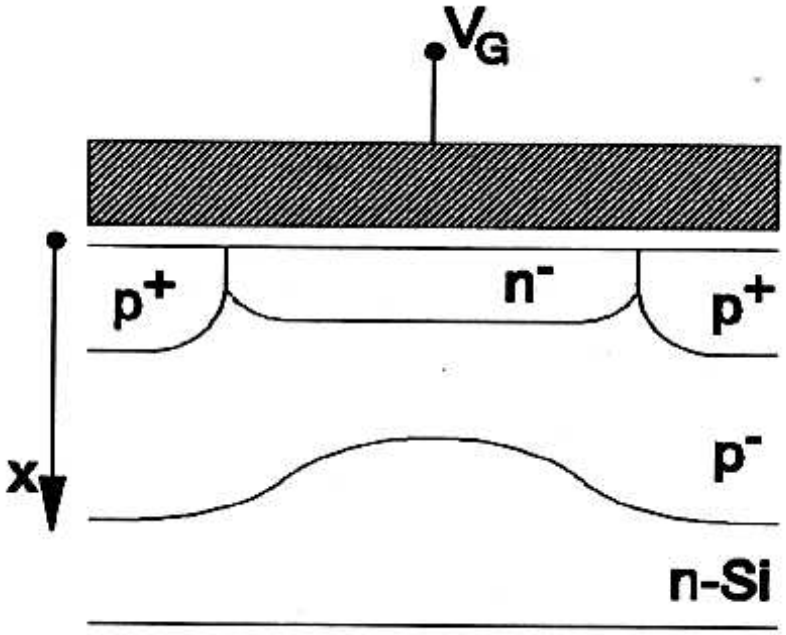
FT-CCD VOD Design and Operation

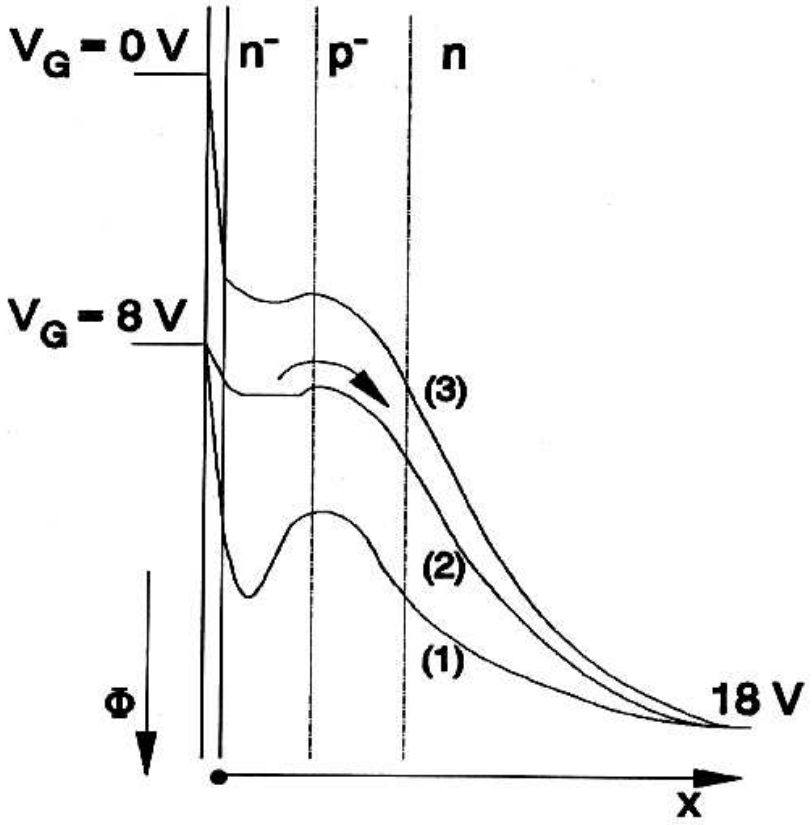
- The VOD structure is underneath the CCD gate; an n-substrate is inserted beneath the p-well of the BCCD



- Apply a large (+ve for n-substrate) bias to the substrate to drain out any excess charge carriers
- Design buried channel potential (ϕ_{min}) such that when charge well is filled up, carriers flow to n-substrate instead of neighboring barrier gates
- The channel potential of the barrier gate must be lower than the (higher energy barrier) potential seen by the electrons flowing into the substrate

FT-CCD VOD Structure and Potential Diagram





(1) Empty well
(2) Full well (saturation)
(3) Barrier gate

A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

FT-CCD with VOD Anti-Blooming

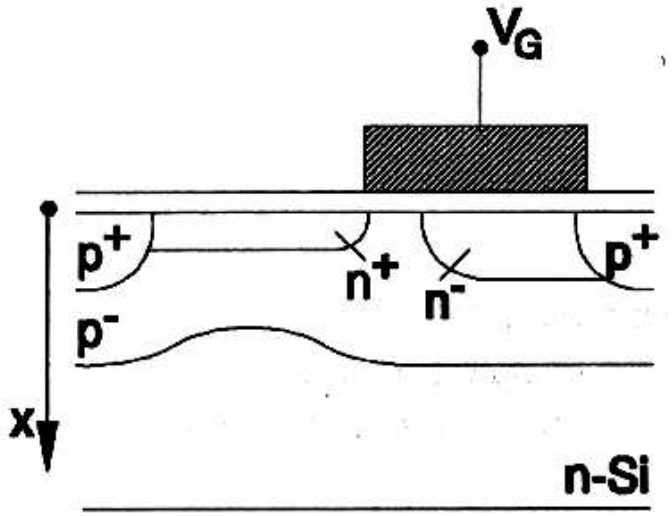
Without VOD

With VOD

D. N. Nichols, W. Chang, B. C. Burkey, E. G. Stevens, E. A. Trabka, D. L. Losee, T. J. Tredwell, C. V. Stancampiano, T. M. Kelly, R. P. Khosla, and T. H. Lee, "A 1.4 million element, full frame CCD image sensor with vertical overflow drain for anti-blooming and low color crosstalk," IEDM Tech. Dig., pp. 120 - 123, December 1987

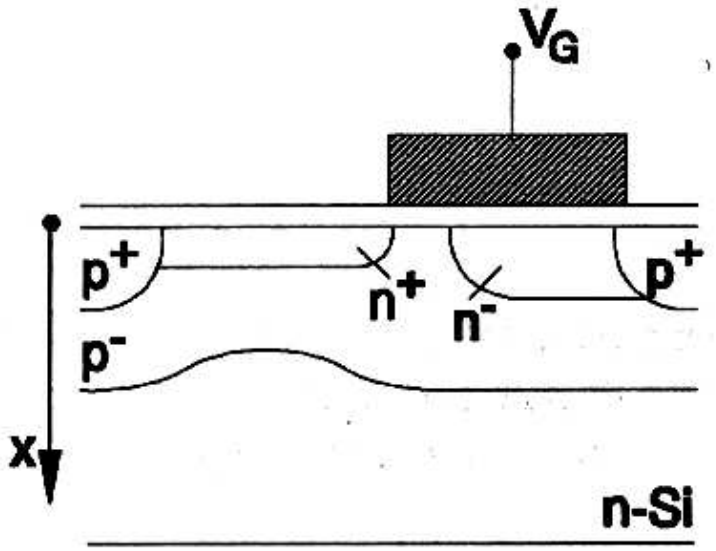
IT-CCD VOD Design and Operation

- VOD structure is located underneath the photodiode
- Insert an n-substrate under the n+/p photodiode

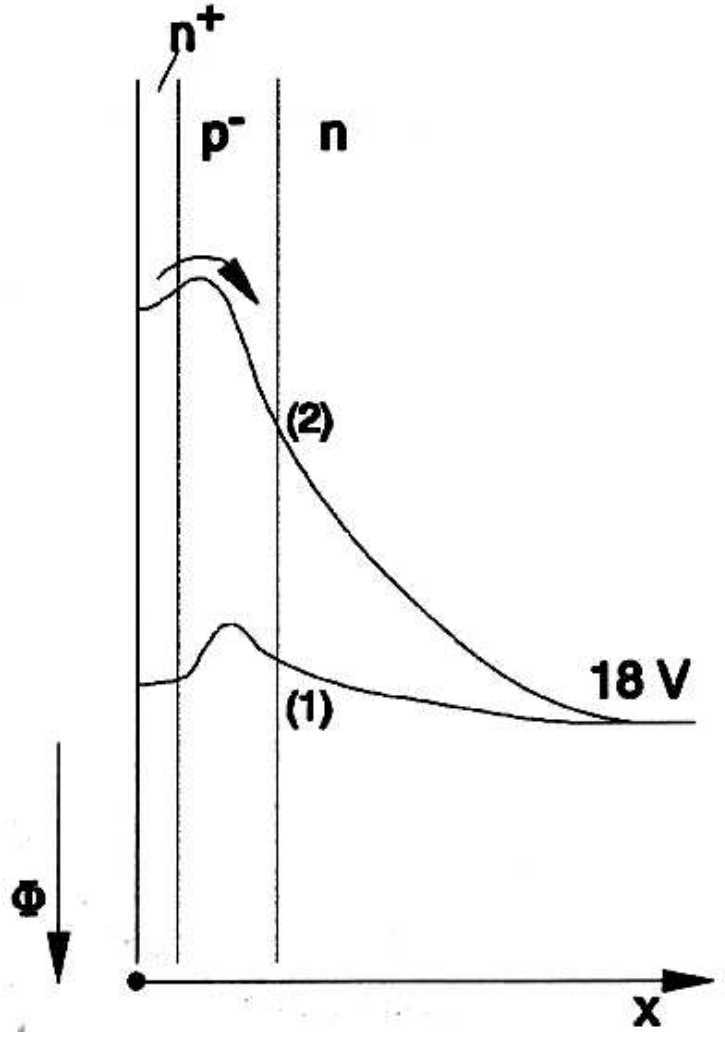


- Apply a large (+ve bias for n-substrate) to the substrate to drain out the excess carriers (electrons)
- When charge well is filled up, excess carriers will spill over the energy barrier of the p-region into the n-substrate.

IT-CCD VOD Structure and Potential Diagram

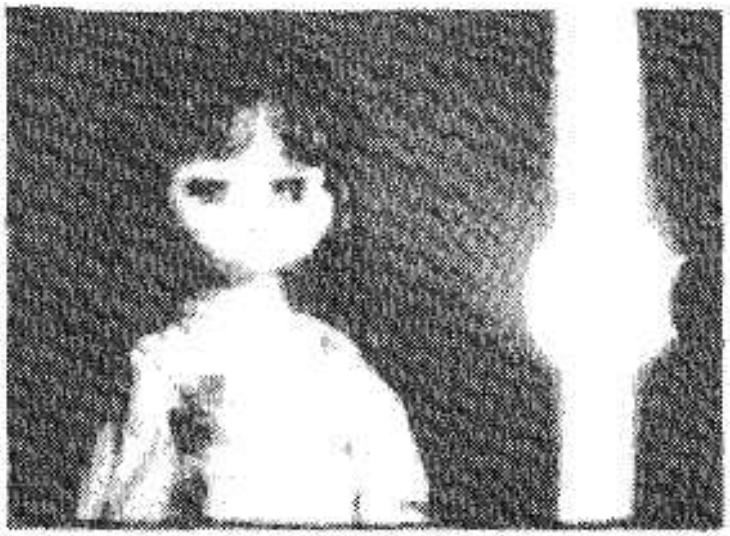


(1) Empty well
(2) Full well (saturation)

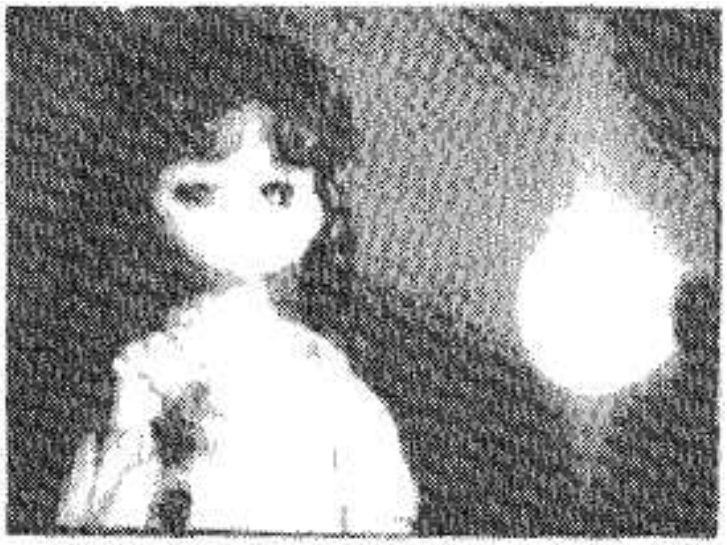


A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

IT-CCD with VOD Anti-Blooming



$V_{sub} = 4V$

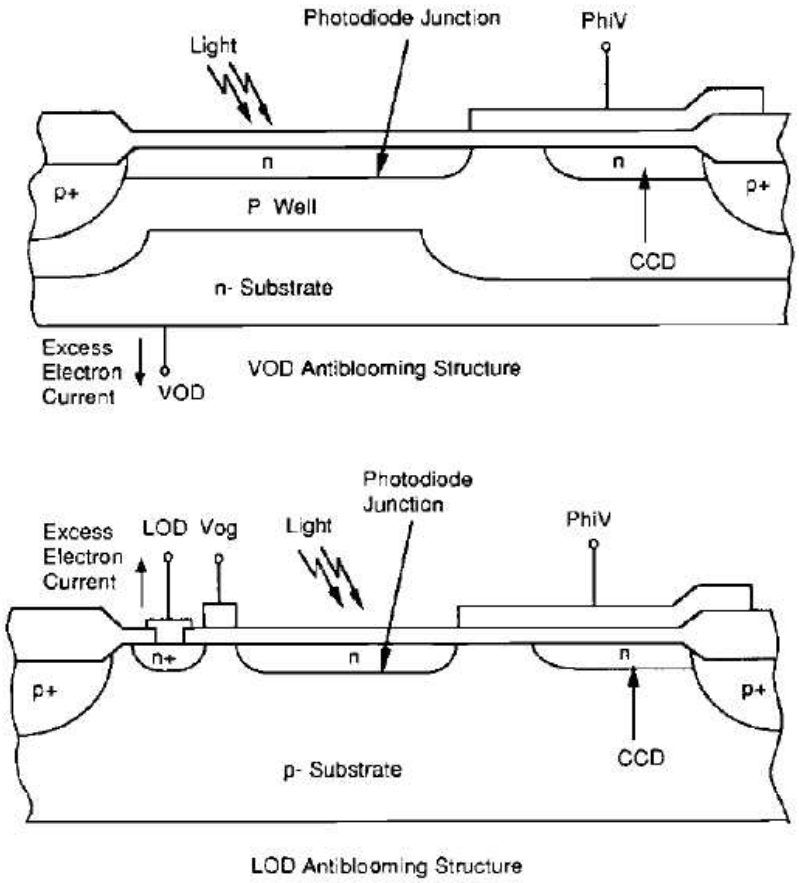


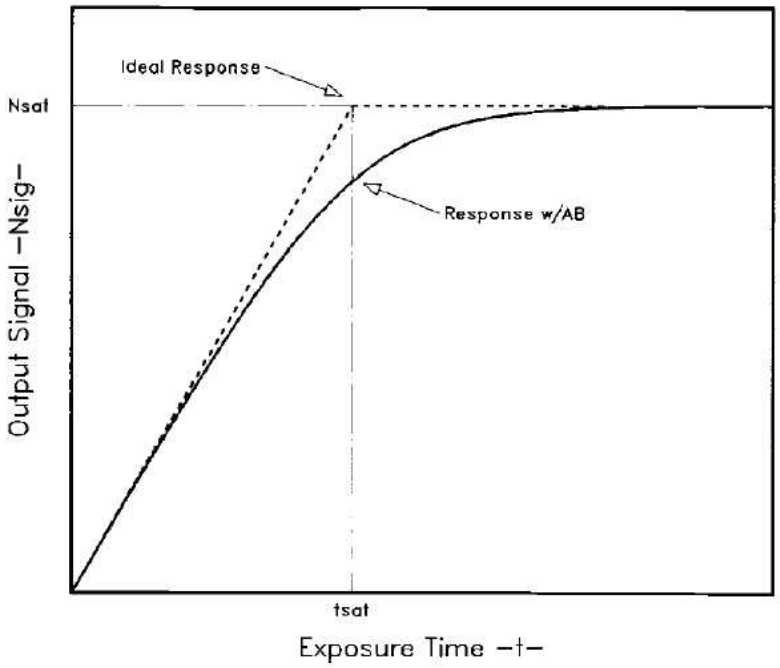
$V_{sub} = 10V$

Y. Ishihara, E. Oda, H. Tanigawa, A. Kohno, N. Teranishi, E. Takeuchi, I. Akiyama, T. Kamata, "Interline CCD Image Sensor with an Antiblooming Structure," IEEE Trans. Electron Devices, pp. 83 - 88, 1984

Photoresponse Non-Linearity of LOD and VOD

- Caused by subthreshold conduction





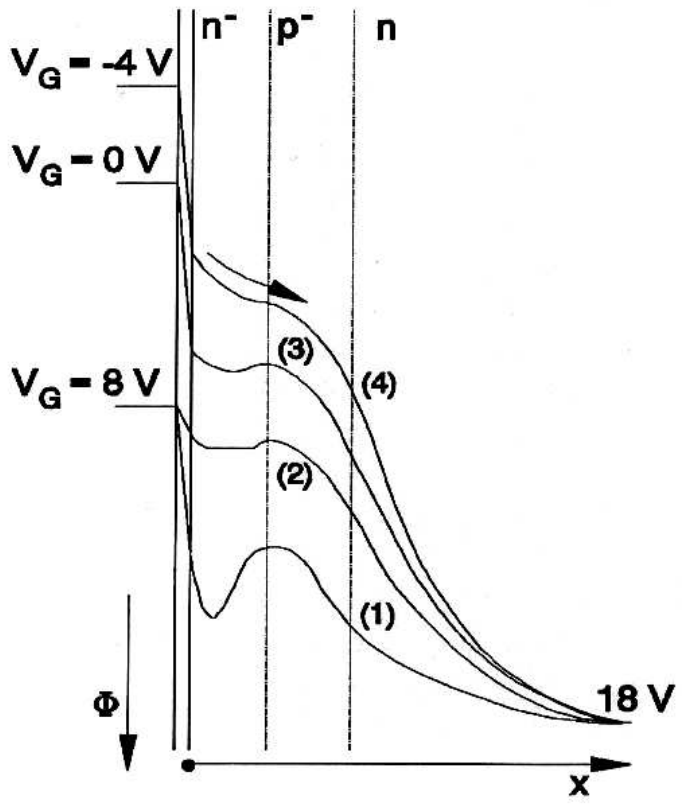
E. Stevens, "Photoresponse Nonlinearity of Solid-state Image Sensors with Antiblooming Protection," IEEE Trans. Electron Devices, pp. 299 - 302, 1991.

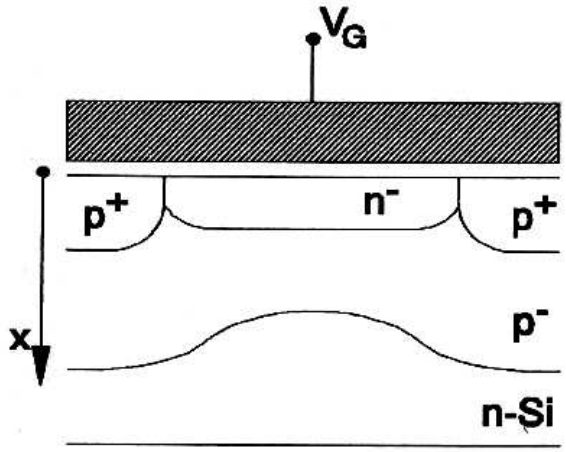
Electronic Shuttering

- Electronic shuttering is needed to
  - Capture fast moving scene (e.g., athlete running, diver jumping from a springboard). The charge integration time must be short compared to the motion
  - Clean out any extra charge prior to the actual integration of photocharge, i.e., act as an electronic iris
    - Electronic iris does not affect the depth of focus (changing the f-stop changes the depth of focus)
- Integration time can be shorter than the field time (e.g., 20msec)
  - This is done by splitting the field time into two parts: (a) charge integrated in the first part is dumped away, then (b) the actual image acquisition begins using the desired integration time (e.g., 10msec)

Charge Reset

- For FT-CCD:
  - Excess charge can be dumped to the substrate by the vertical overflow drain by biasing the CCD gates to negative (raise the bottom of the well above the low voltage level of the CCD clock)





(1) Empty well

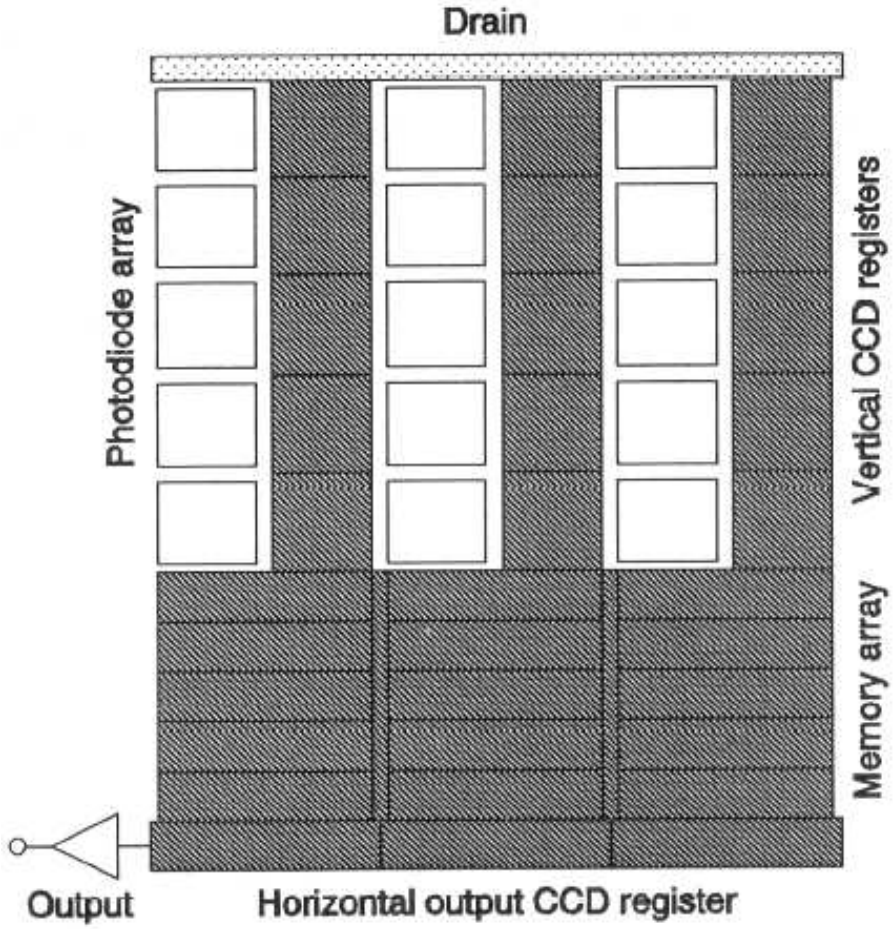
(2) Full well (saturation)

(3) Barrier gate

(4) Charge reset

- For (F)IT-CCD, two methods are used:
  1. Transfer the charge from the photodiode into the vertical CCD and then shift the charge to a drain node at the top of the VCCD (i.e., shift VCCD charge in the opposite direction)
     - Limited to the on set of the vertical blanking period in an IT-CCD because VCCD is not empty of charge during the integration period (charge from the previous frame is still being shifted down to the HCCD)
     - No such limitation for FIT-CCD as the VCCD in the imaging section of an FIT-CCD is always empty of charge
  2. Use a p+ surface pinned diode in conjunction with a large charge resetting substrate bias

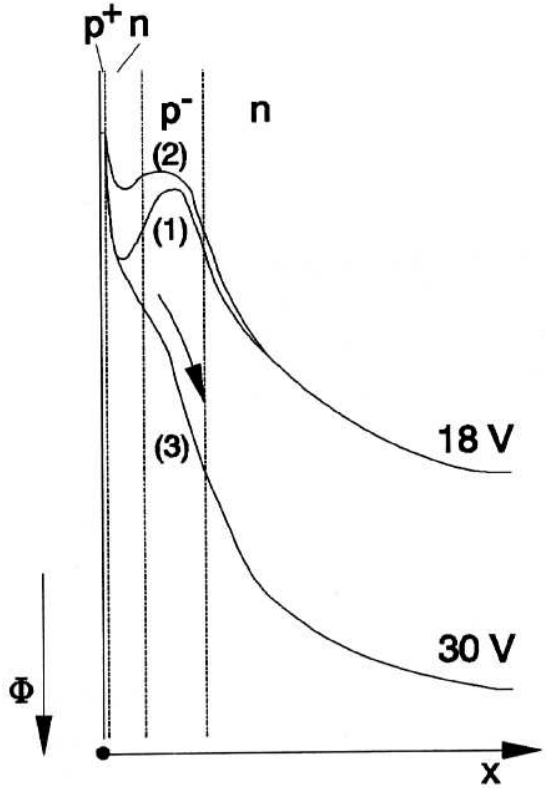
(F)IT-CCD Charge Reset By Charge Shifting

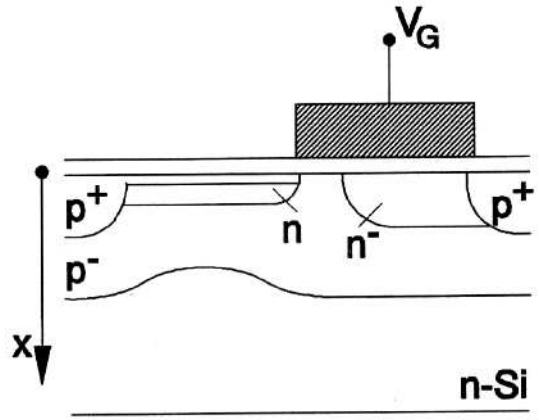


A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

(F)IT-CCD Charge Reset by Surface Pinned Diode

- Insert a p+ layer at the surface of the n/p-well photodiode.
- Bias it (e.g., through p+ layers in channel stop implant) to ensure that it is not depleted, thereby pinning the surface potential to external bias
- A large voltage (30-40V) is applied to the n-substrate to pull potential well so that there is no barrier for electrons to flow to substrate





(1) Empty well

(2) Full well (saturation)

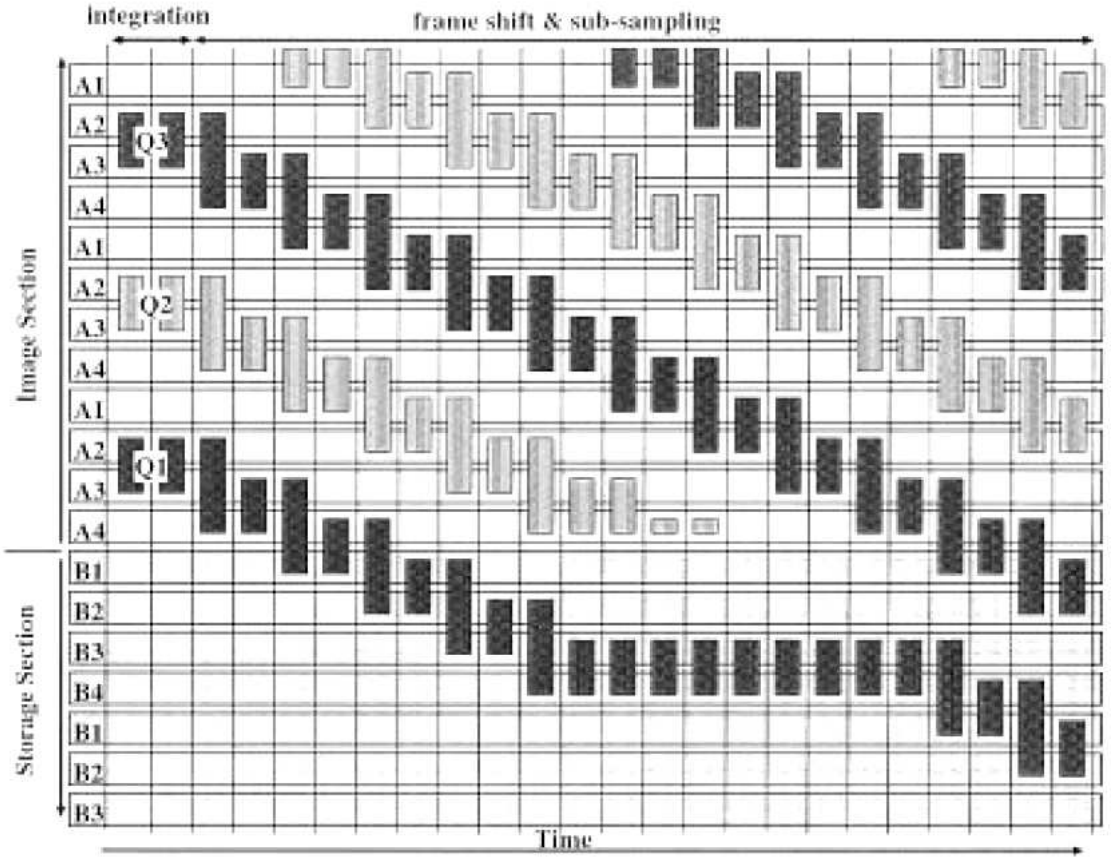
(3) Charge reset

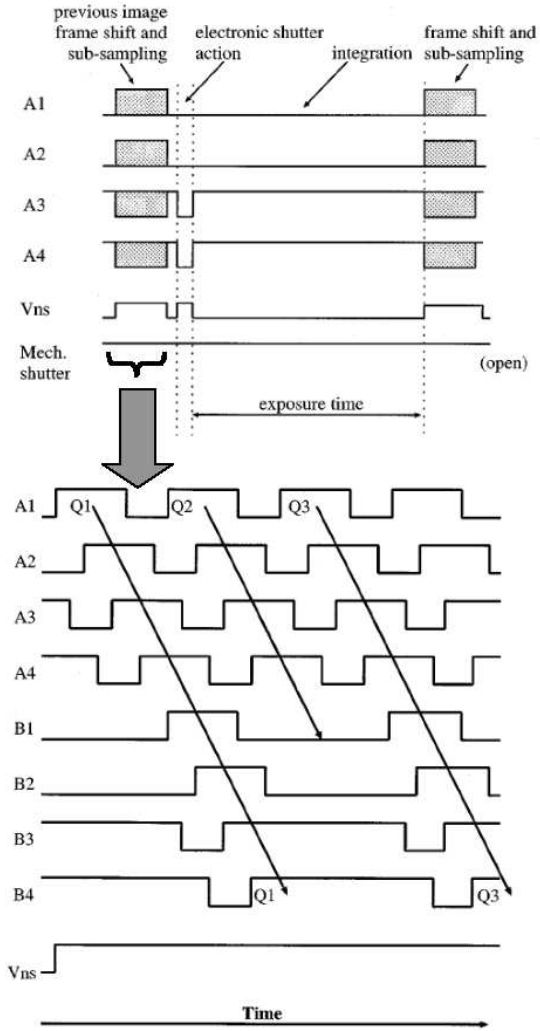
Window of Interest, Binning, Sub-Sampling

- Sub-sampling and window-of-interest
  - "Monitor mode" in a digital still camera
  - Generate scene information for autofocus, autoexposure, electronic field finder
- Binning
  - Allow capture of low-light images during fixed (limited) frame time
  - Trade-off with reduced resolution
- Works differently for FT-CCD and IT-CCD
  - Here, we give some examples, but once the concept is understood, there can be many variations on the theme

FT-CCD Sub-Sampling

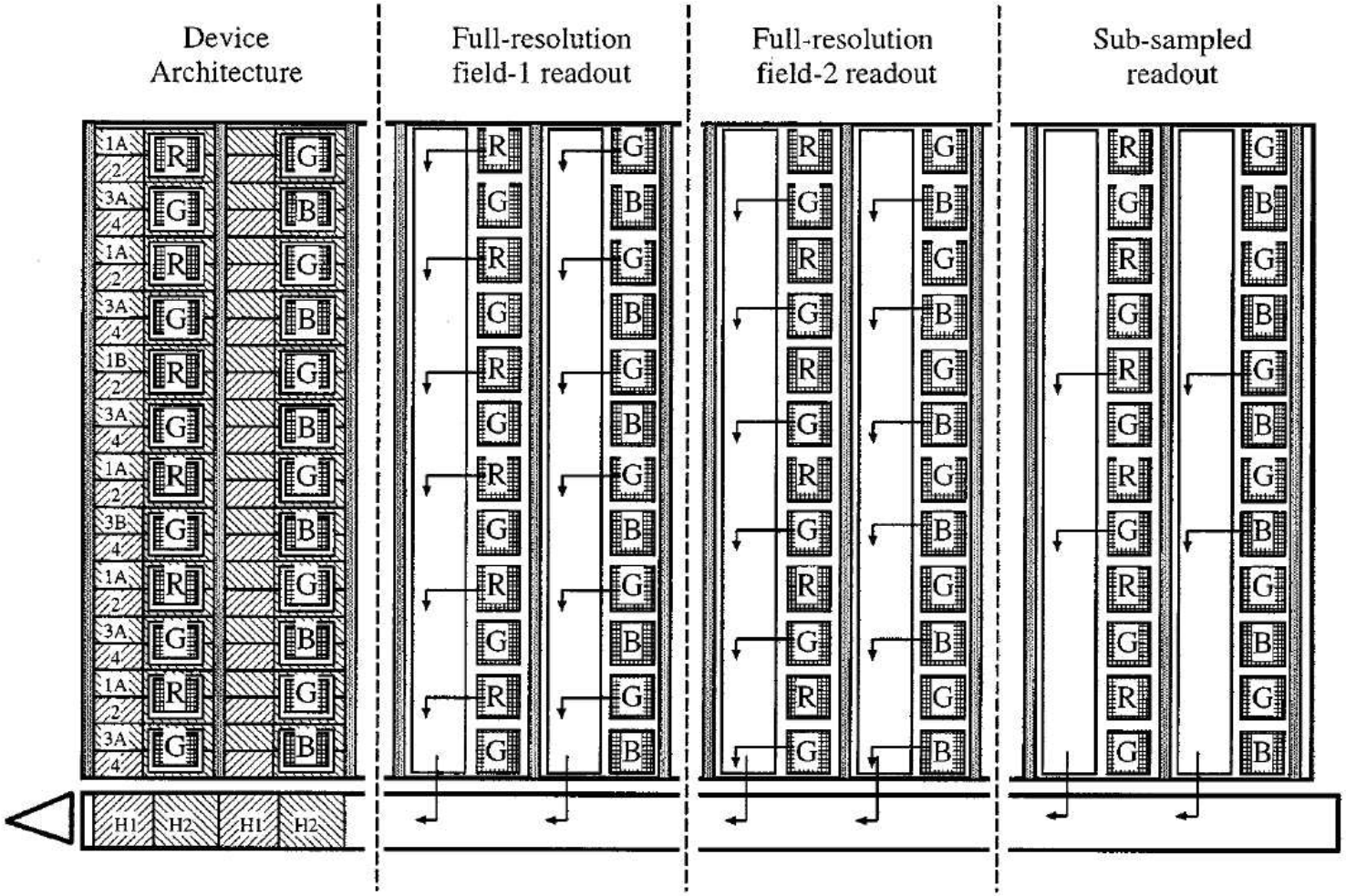
- Dump unwanted charge into VOD





J. T. Bosiers, A. C. Kleimann, H. C. van Kuijk, L. Le Cam, H. L. Peek, J. P. Maas, and A. J. P. Theuwissen, "Frame transfer CCDs for digital still cameras: Concept, design, and evaluation," IEEE Trans. Electron Devices, Vol. 49, pp. 377 - 386, March 2002

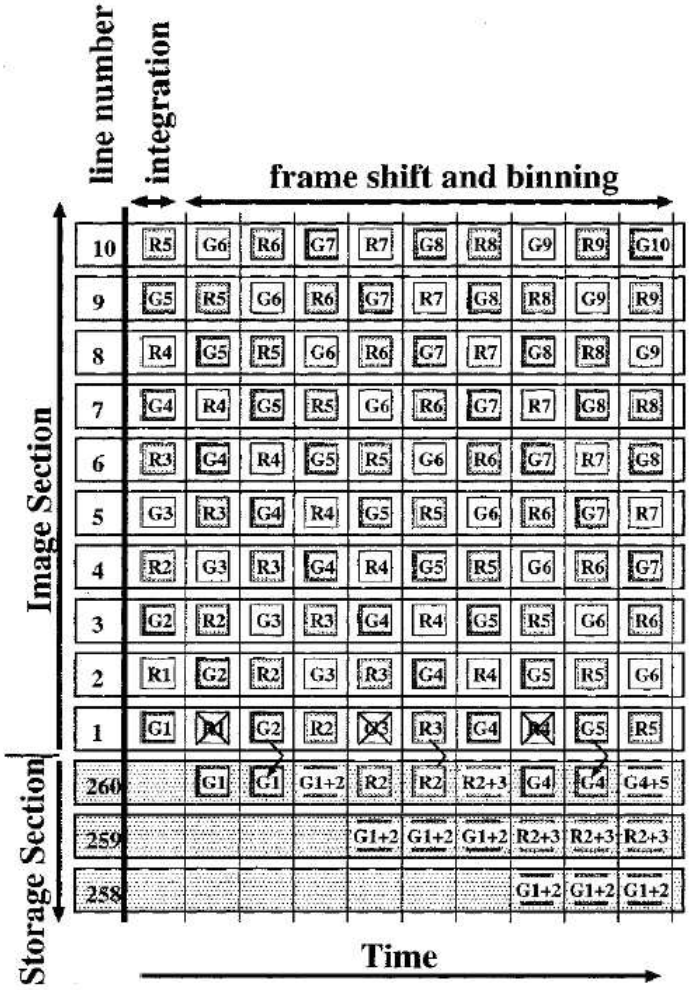
IT-CCD Sub-Sampling



J. T. Bosiers, A. C. Kleimann, H. C. van Kuijk, L. Le Cam, H. L. Peek, J. P. Maas, and A. J. P. Theuwissen, "Frame transfer CCDs for digital still cameras: Concept, design, and evaluation," IEEE Trans. Electron Devices, Vol. 49, pp. 377 - 386, March 2002

FT-CCD Charge Binning

- Combine charge from two CCD stages by clocking

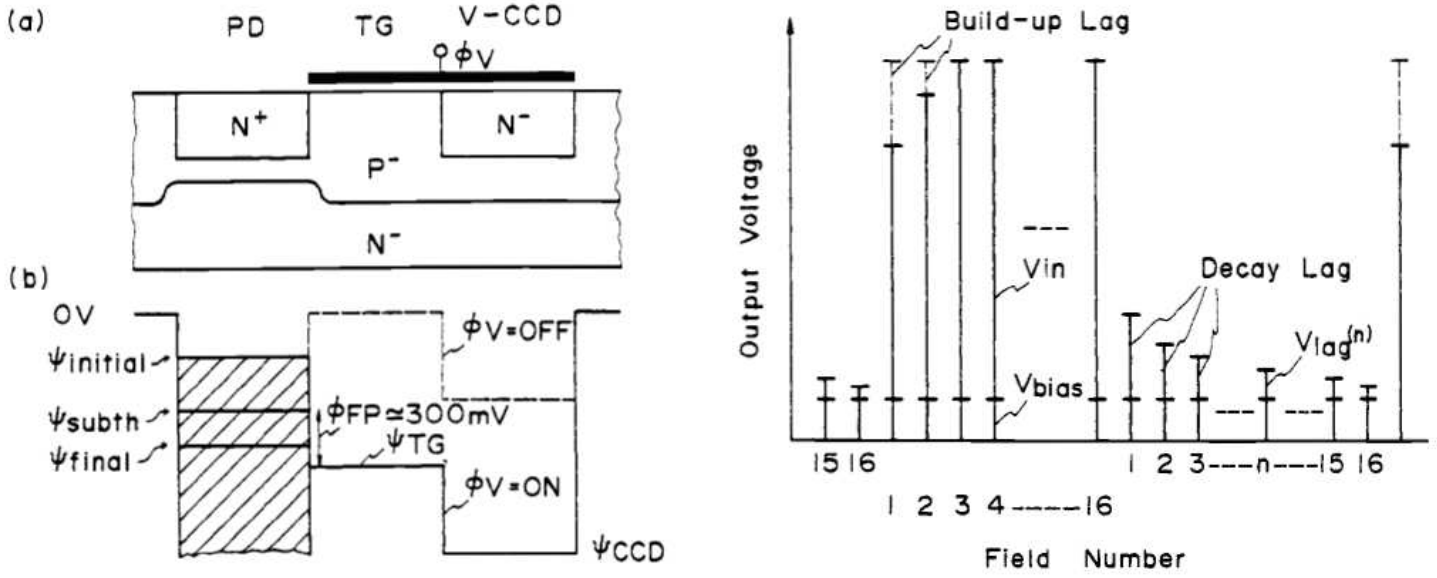


Pinned Photodiode

- Invented (N. Teranishi, IEDM 1982) to solve image lag problem in IT-CCD
- Concept applied to CMOS image sensor (R. Guidash, IEDM 1997)
- Recent advances (I. Inoue, IEDM 1999, T-ED 2003) reduced operating voltage to 3.3V
- Advantages of the pinned photodiode:
  - Improved blue light response
  - No image lag due to complete charge transfer
  - Lower dark current due to accumulated surface
  - Improved charge handling capacity of the photodiode due to the added p+ pinning layer

Image Lag

- Highlights of the present image field show up at subsequent fields
- Caused by incomplete charge transfer from the photodiode to the VCCD or the readout node – charge in photodiode shows up in subsequent fields
- Physical process can be described by subthreshold conduction under the transfer gate

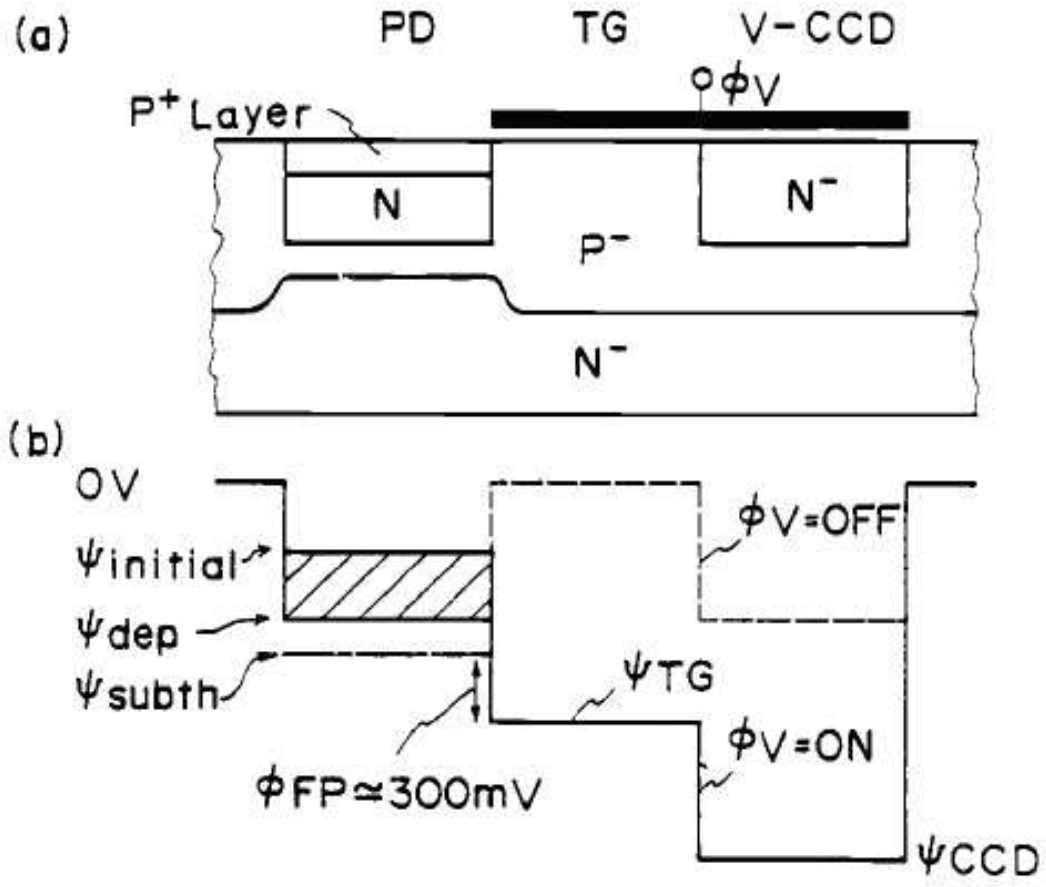


N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, K. Arai, International Electron Devices Meeting (IEDM), pp. 324 - 326, 1982

Pinned Photodiode Design

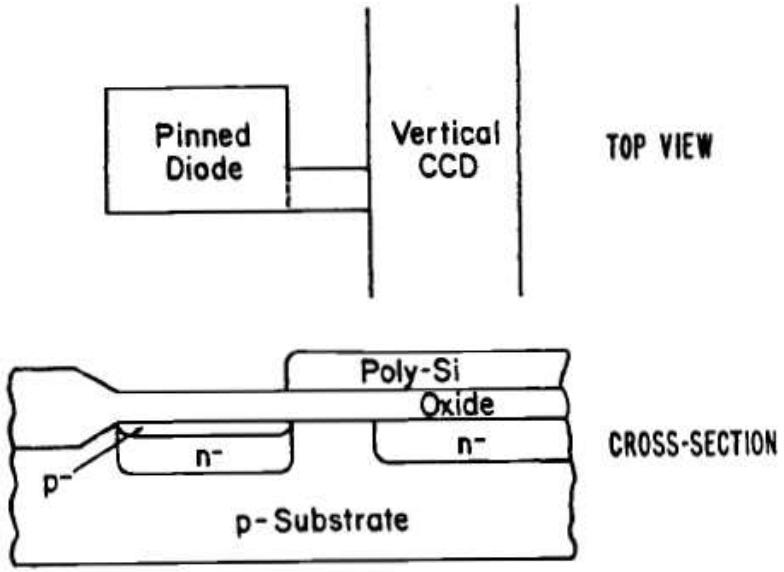
- Insert p+ pinning layer on the surface of the n on p-substrate diode
- The p+ layer is connected to p+ channel stop regions (or other suitable p-type regions) and biased outside of the pixel array
- The doping of the n-layer of the photodiode is reduced (from usual n/p photodiode case) to ensure that the potential of the n-layer at full depletion is lower than the subthreshold Fermi potential (surface potential under the transfer gate minus 300 mV) – this ensures complete charge transfer, i.e. there is no mobile carrier in the n-region after the charge transfer

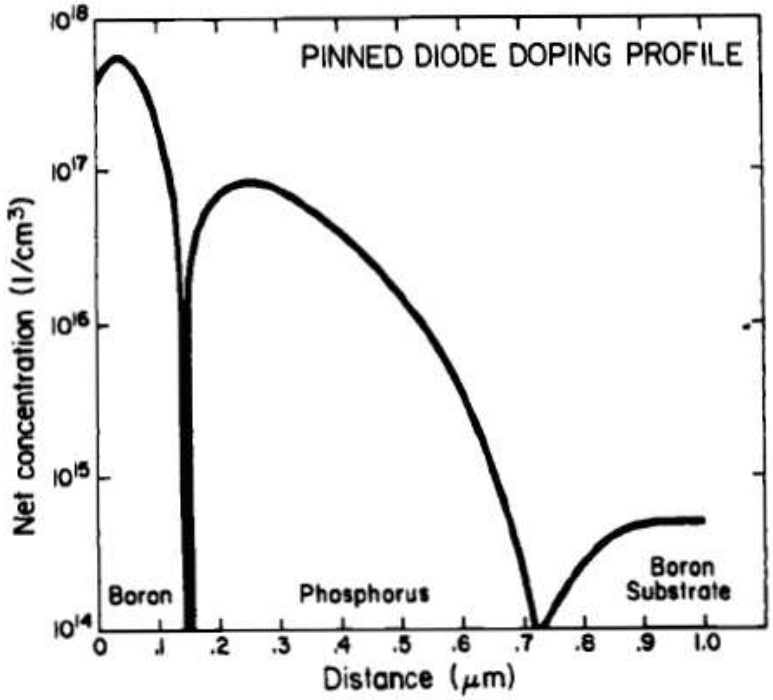
Pinned Photodiode for IT-CCD



N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, K. Arai, International Electron Devices Meeting (IEDM), pp. 324 - 326, 1982

Pinned Photodiode Doping Profile

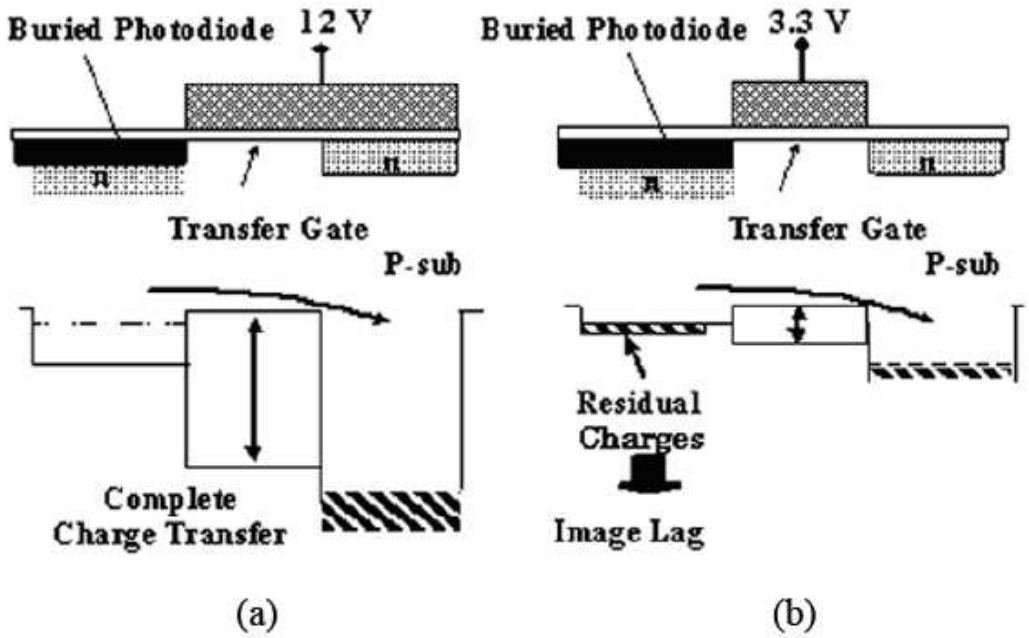




B.C. Burkey, W.C. Chang, J. Littlehale, T.H. Lee, T.J. Tredwell, J.P. Lavine, E.A. Trabka,International Electron Devices Meeting (IEDM), pp. 28 - 31, 1984

Pinned Photodiode for CMOS Image Sensors

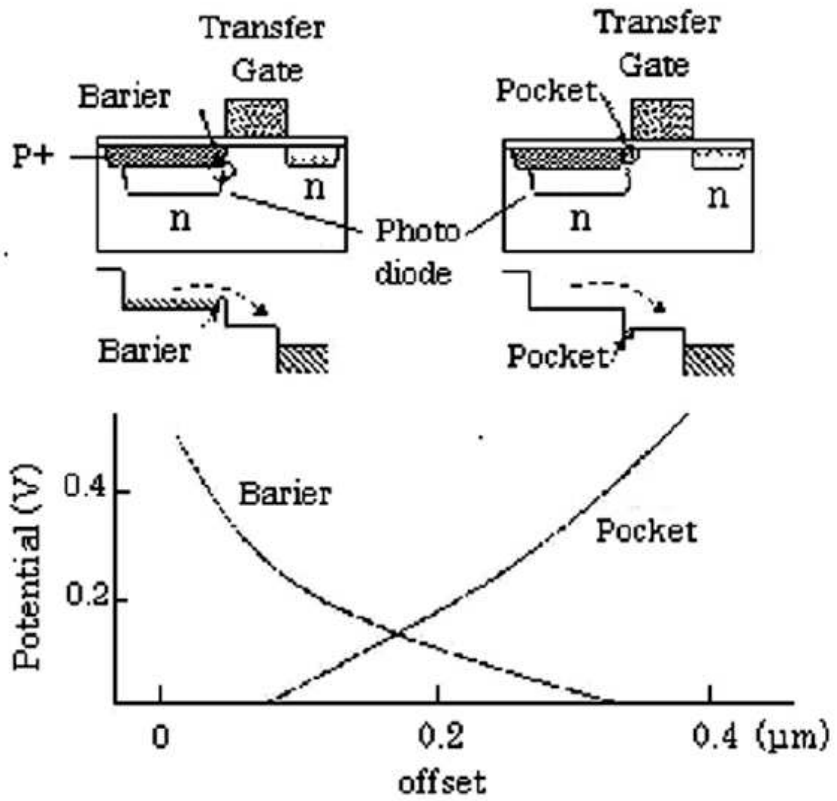
- Additional requirements
  - Low transfer gate voltage (compatible with CMOS voltage)
  - Potential barrier and potential pocket cannot be eliminated by high transfer gate voltages (as in CCD)



I. Inoue, N. Tanaka. H. Yamashita. T. Yamaguchi, H. Ishiwata, H. Ihara, "Low-Leakage-Current and Low-Operating-Voltage Buried Photodiode for a CMOS Imager," IEEE Trans. Electron Devices, Vol. 50, pp. 43-47, January 2003.

Design Issues of Pinned Photodiode for CMOS

- Energy barrier: p+ extending too much beyond n-layer
- Energy pocket: n-layer extending too much beyond p+



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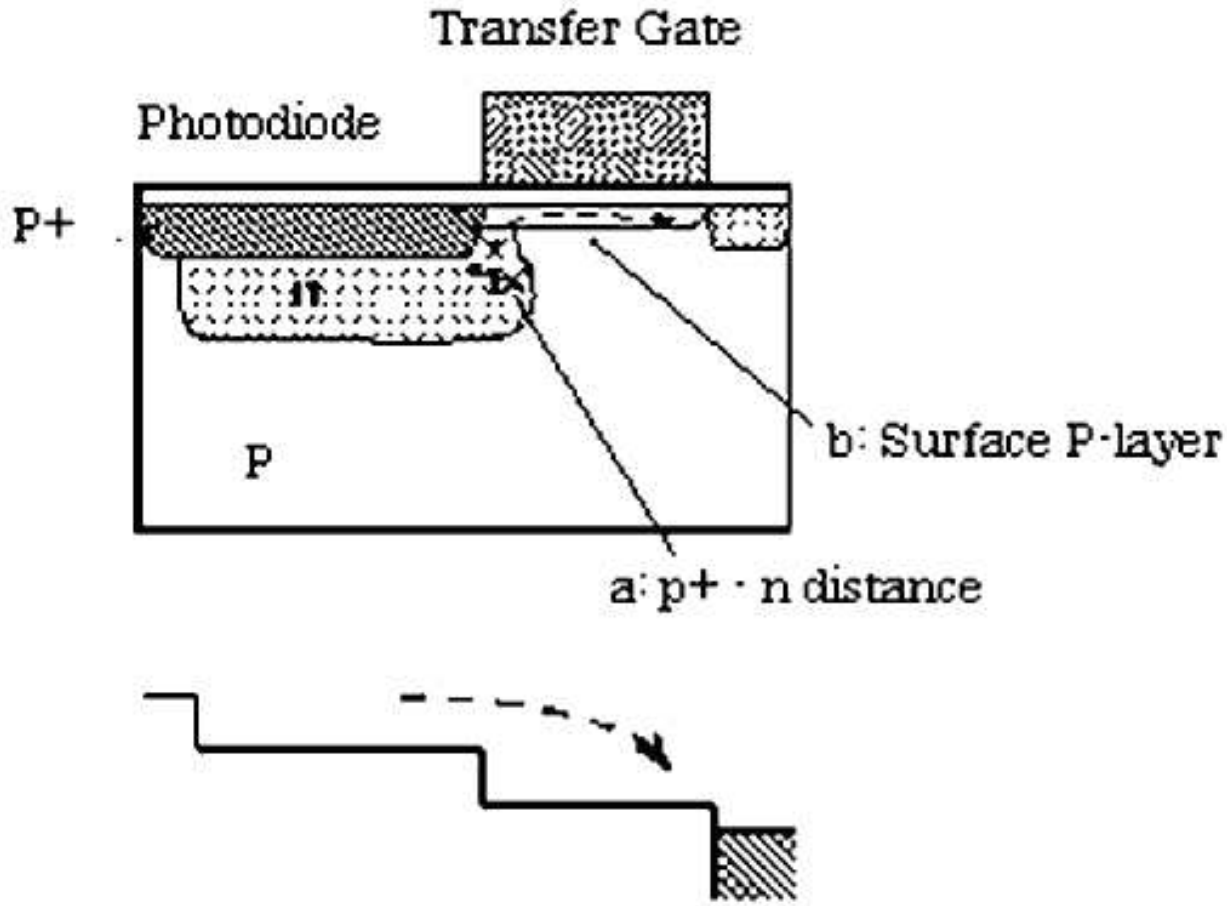
Pinned Photodiode for CMOS



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Summary

- Conversion of light into current:
  - Photodiode
  - Photogate
  - Pinned diode
- Conversion of current into charge/voltage:
  - Direct integration
- CCD operation: well charge capacity, charge transfer
- CCD image sensor architectures:
  - Frame transfer (FT)
  - Interline transfer (IT)
  - FIT
  - Time-Delay-and-Integration

- Some nonidealities and performance measures:
  - QE
  - Dark current
  - Well charge capacity
  - Conversion gain
  - Fill factor
  - Smear
  - Blooming
  - Lag
- Bells and whistles
  - Smear prevention
  - Anti-blooming
  - Electronic shuttering
  - Subsampling and pixel binning
  - Window of interest

Advantages and Disadvantages of CCDs

- Advantages: high quality
  - optimized photodetectors — high QE, low dark current
  - very low noise — no noise introduced during shifting
  - very low fixed pattern noise (nonuniformity) — no FPN introduced by shifting
- Disadvantages:
  - cannot integrate other analog or digital circuits, e.g., for clock generation, control, or A/D conversion
  - high power — entire array switching during readout (high C, high V, and high f result in high CV^2f)
  - limited frame rate (for large sensors) due to required increase in transfer speed (while maintaining acceptable transfer efficiency)
  - highly nonprogrammable, e.g., *window of interest* is difficult to implement