

## Timing Generator and Signal Processor for Frame Readout CCD Image Sensor

### Description

The CXD3412GA is a timing generator and CCD signal processor IC for the ICX412 CCD image sensor.

### Features

- Timing generator functions
  - Horizontal drive frequency 22.5MHz (base oscillation frequency 45MHz)
  - Supports frame readout/draft (sextuple speed)/AF (auto focus)
  - High-speed/low-speed shutter function
  - Horizontal and vertical drivers for CCD image sensor
- CCD signal processor functions
  - Correlated double sampling
  - Programmable gain amplifier (PGA) allows gain adjustment over a wide range (–6 to +42dB)
  - 10-bit A/D converter
- Chip Scale Package (CSP):  
CSP allows vast reduction in the CCD camera block footprint

### Applications

Digital still cameras

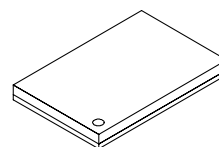
### Structure

Silicon gate CMOS IC

### Applicable CCD Image Sensors

ICX412 (Type 1/1.8, 3240K pixels)

96 pin LFLGA (Plastic)



### Absolute Maximum Ratings

- Supply voltage
 

$V_{DDA}, V_{DDb}, V_{DDc}, V_{DDd}$	$V_{SS} - 0.3$ to $+7.0$	V
$V_{DDe}, V_{DDf}, V_{DDg}$	$V_{SS} - 0.3$ to $+4.0$	V
VL	$-10.0$ to $V_{SS}$	V
VH	$V_L - 0.3$ to $+26.0$	V
- Input voltage (analog)
 

$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
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- Input voltage (digital)
 

$V_I$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
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- Output voltage
 

$V_{O1}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
$V_{O2}$	$V_L - 0.3$ to $V_{SS} + 0.3$	V
$V_{O3}$	$V_L - 0.3$ to $V_H + 0.3$	V
- Operating temperature
 

$T_{opr}$	$-20$ to $+75$	°C
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- Storage temperature
 

$T_{stg}$	$-55$ to $+125$	°C
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### Recommended Operating Conditions

- Supply voltage
 

$V_{DDd}$	$3.0$ to $5.5$	V
$V_{DDA}, V_{DDb}, V_{DDc}, V_{DDd},$ $V_{DDe}, V_{DDf}, V_{DDg}$	$3.0$ to $3.6$	V
VM	$0.0$	V
VH	$14.5$ to $15.5$	V
VL	$-7.0$ to $-8.0$	V
- Operating temperature
 

$T_{opr}$	$-20$ to $+75$	°C
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## Pin Configuration (Top View)

A	NC	NC	SCK2	SSI2	TEST3	AVSS4	C8	AVSS6	AVDD5
B	D2	D1	D0	SEN2	TEST5	AVDD4	C7	AVDD3	AVSS3
C	D5	D4	D3	TEST4	AVSS5	C9	C3	C4	CCDIN
D	D8	D7	D6				C1	C2	AVSS1
E	D9	DVDD1	DVSS1				AVSS2	AVDD2	AVDD1
F	DVSS2	DVSS3	DVDD2				PBLKI	XSHDI	XSHPI
G	ADCLKI	CLPOBI	CLPDMI				PBLK	XSHD	XSHPI
H	ADCLK	CLPOB	CLPDM				XRS	VDD4	VDD3
J	CKI	CKO	VSS5				VSS3	H1	H2
K	OSCO	MCKO	VDD5				VDD2	RG	VSS2
L	OSCI	SSI1	VSS4	VM	V1A	V3A	VSS1	SSGSL	VDD1
M	SCK1	VD	TEST1	V2	VH	VL	TEST2	RST	WEN
N	SEN1	HD	VSS6	V4	V1B	V3B	SUB	SNCSL	ID/EXP
	1	2	3	4	5	6	7	8	9

## Pin Description

Pin No.	Symbol	I/O	Description
A1	NC	—	No connected. (Open)
A2	NC	—	No connected. (Open)
A3	SCK2	I	CCD signal processor block serial interface clock input. (Schmitt trigger)
A4	SSI2	I	CCD signal processor block serial interface data input. (Schmitt trigger)
A5	TEST3	I	CCD signal processor block test input 3. Connect to DVss.
A6	AVss4	—	CCD signal processor block analog GND.
A7	C8	—	Capacitor connection.
A8	AVss6	—	CCD signal processor block analog GND.
A9	AVDD5	—	CCD signal processor block analog power supply.
B1	D2	O	ADC output.
B2	D1	O	ADC output.
B3	D0	O	ADC output (LSB).
B4	SEN2	I	CCD signal processor block serial interface enable input. (Schmitt trigger)
B5	TEST5	I	CCD signal processor block test input 5. Connect to DVDD.
B6	AVDD4	—	CCD signal processor block analog power supply.
B7	C7	—	Capacitor connection.
B8	AVDD3	—	CCD signal processor block analog power supply.
B9	AVss3	—	CCD signal processor block analog GND.
C1	D5	O	ADC output.
C2	D4	O	ADC output.
C3	D3	O	ADC output.
C4	TEST4	I	CCD signal processor block test input 4. Connect to DVss.
C5	AVss5	—	CCD signal processor block analog GND.
C6	C9	—	Capacitor connection.
C7	C3	—	Capacitor connection.
C8	C4	—	Capacitor connection.
C9	CCDIN	I	CCD output signal input.
D1	D8	O	ADC output.
D2	D7	O	ADC output.
D3	D6	O	ADC output.
D7	C1	—	Capacitor connection.
D8	C2	—	Capacitor connection.
D9	AVss1	—	CCD signal processor block analog GND.
E1	D9	O	ADC output (MSB).
E2	DVDD1	—	CCD signal processor block digital power supply. (Power supply for ADC)
E3	DVss1	—	CCD signal processor block digital GND. (GND for ADC)
E7	AVss2	—	CCD signal processor block analog GND.

Pin No.	Symbol	I/O	Description
E8	AV <sub>DD2</sub>	—	CCD signal processor block analog power supply.
E9	AV <sub>DD1</sub>	—	CCD signal processor block analog power supply.
F1	DV <sub>SS2</sub>	—	CCD signal processor block digital GND.
F2	DV <sub>SS3</sub>	—	CCD signal processor block digital GND.
F3	DV <sub>DD2</sub>	—	CCD signal processor block digital power supply.
F7	PBLKI	I	Pulse input for horizontal and vertical blanking period pulse cleaning. (Schmitt trigger)
F8	XSHDI	I	CCD data level sample-and-hold pulse input. (Schmitt trigger)
F9	XSHPI	I	CCD precharge level sample-and-hold pulse input. (Schmitt trigger)
G1	ADCLKI	I	Clock input for analog/digital conversion. (Schmitt trigger)
G2	CLPOBI	I	CCD optical black signal clamp pulse input. (Schmitt trigger)
G3	CLPDMI	I	CCD dummy signal clamp pulse input. (Schmitt trigger)
G7	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
G8	XSHD	O	CCD data level sample-and-hold pulse output.
G9	XSHP	O	CCD precharge level sample-and-hold pulse output.
H1	ADCLK	O	Clock output for analog/digital conversion. Logical phase can be adjusted by serial interface data.
H2	CLPOB	O	CCD optical black signal clamp pulse output. Horizontal/vertical OB pattern can be changed by serial interface data.
H3	CLPDM	O	CCD dummy signal clamp pulse output.
H7	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment.
H8	V <sub>DD4</sub>	—	Timing generator block digital power supply. (Power supply for CDS block)
H9	V <sub>DD3</sub>	—	Timing generator block 3.0 to 5.0V power supply. (Power supply for H1/H2)
J1	CKI	I	Inverter input.
J2	CKO	O	Inverter output.
J3	V <sub>SS5</sub>	—	Timing generator block digital GND.
J7	V <sub>SS3</sub>	—	Timing generator block digital GND.
J8	H1	O	CCD horizontal register clock output.
J9	H2	O	CCD horizontal register clock output.
K1	OSCO	O	Inverter output for oscillation. When not used, leave open or connect a capacitor.
K2	MCKO	O	System clock output for signal processor IC.
K3	V <sub>DD5</sub>	—	Timing generator block digital power supply. (Power supply for common logic block)
K7	V <sub>DD2</sub>	—	Timing generator block digital power supply. (Power supply for RG)
K8	RG	O	CCD reset gate pulse output.
K9	V <sub>SS2</sub>	—	Timing generator block digital GND.
L1	OSCI	I	Inverter input for oscillation. When not used, fix to low.
L2	SSI1	I	Timing generator block serial interface data input. Schmitt trigger input.

Pin No.	Symbol	I/O	Description
L3	V <sub>SS4</sub>	—	Timing generator block digital GND.
L4	VM	—	Timing generator block digital GND. (GND for vertical driver)
L5	V1A	O	CCD vertical register clock output.
L6	V3A	O	CCD vertical register clock output.
L7	V <sub>SS1</sub>	—	Timing generator block digital GND.
L8	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External sync valid (With pull-down resistor)
L9	V <sub>DD1</sub>	—	Timing generator block digital power supply. (Power supply for common logic block)
M1	SCK1	I	Timing generator block serial interface clock input. Schmitt trigger input.
M2	VD	I/O	Vertical sync signal input/output.
M3	TEST1	I	Timing generator block test input 1. Normally fix to GND. (With pull-down resistor)
M4	V2	O	CCD vertical register clock output.
M5	VH	—	Timing generator block 15.0V power supply. (Power supply for vertical driver)
M6	VL	—	Timing generator block -7.5V power supply. (Power supply for vertical driver)
M7	TEST2	I	Timing generator block test input 2. Normally fix to GND. (With pull-down resistor)
M8	RST	I	Timing generator block reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input/No protective diode on power supply side.
M9	WEN	O	Memory write timing pulse output.
N1	SEN1	I	Timing generator block serial interface strobe input. Schmitt trigger input.
N2	HD	I/O	Horizontal sync signal input/output.
N3	V <sub>SS6</sub>	—	Timing generator block digital GND.
N4	V4	O	CCD vertical register clock output.
N5	V1B	O	CCD vertical register clock output.
N6	V3B	O	CCD vertical register clock output.
N7	SUB	O	CCD electronic shutter pulse output.
N8	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync (With pull-down resistor)
N9	ID/EXP	O	Vertical direction line identification pulse output/exposure time identification pulse output. Switching possible using the serial interface data. (Default: ID)

## Electrical Characteristics

## Timing Generator Block Electrical Characteristics

## DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V <sub>DD2</sub>	V <sub>DDa</sub>		3.0	3.3	3.6	V
Supply voltage 2	V <sub>DD3</sub>	V <sub>DDb</sub>		3.0	3.3	5.25	V
Supply voltage 3	V <sub>DD4</sub>	V <sub>DDc</sub>		3.0	3.3	3.6	V
Supply voltage 4	V <sub>DD1</sub> , V <sub>DD5</sub>	V <sub>DDd</sub>		3.0	3.3	3.6	V
Input voltage 1*1	RST, SSI1, SCK1, SEN1	V <sub>I+</sub>		0.8V <sub>DDd</sub>			V
		V <sub>I-</sub>				0.2V <sub>DDd</sub>	V
Input voltage 2*2	TEST1, TEST2, SNCSL, SSGSL	V <sub>IH1</sub>		0.7V <sub>DDd</sub>			V
		V <sub>IL1</sub>				0.3V <sub>DDd</sub>	V
Input/output voltage	VD, HD	V <sub>IH2</sub>		0.8V <sub>DDd</sub>			V
		V <sub>IL2</sub>				0.2V <sub>DDd</sub>	V
		V <sub>OH1</sub>	Feed current where I <sub>OH</sub> = -1.2mA	V <sub>DDd</sub> - 0.8			V
		V <sub>OL1</sub>	Pull-in current where I <sub>OL</sub> = 2.4mA			0.4	V
Output voltage 1	H1, H2	V <sub>OH2</sub>	Feed current where I <sub>OH</sub> = -22.0mA	V <sub>DDb</sub> - 0.8			V
		V <sub>OL2</sub>	Pull-in current where I <sub>OL</sub> = 14.4mA			0.4	V
Output voltage 2	RG	V <sub>OH3</sub>	Feed current where I <sub>OH</sub> = -3.3mA	V <sub>DDa</sub> - 0.8			V
		V <sub>OL3</sub>	Pull-in current where I <sub>OL</sub> = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, XRS, PBLK, CLPOB, CLPDM, ADCLK	V <sub>OH4</sub>	Feed current where I <sub>OH</sub> = -3.3mA	V <sub>DDc</sub> - 0.8			V
		V <sub>OL4</sub>	Pull-in current where I <sub>OL</sub> = 2.4mA			0.4	V
Output voltage 4	CKO	V <sub>OH5</sub>	Feed current where I <sub>OH</sub> = -6.9mA	V <sub>DDd</sub> - 0.8			V
		V <sub>OL5</sub>	Pull-in current where I <sub>OL</sub> = 4.8mA			0.4	V
Output voltage 5	MCKO	V <sub>OH6</sub>	Feed current where I <sub>OH</sub> = -3.3mA	V <sub>DDd</sub> - 0.8			V
		V <sub>OL6</sub>	Pull-in current where I <sub>OL</sub> = 2.4mA			0.4	V
Output voltage 6	ID/EXP, WEN	V <sub>OH7</sub>	Feed current where I <sub>OH</sub> = -2.4mA	V <sub>DDd</sub> - 0.8			V
		V <sub>OL7</sub>	Pull-in current where I <sub>OL</sub> = 4.8mA			0.4	V
Output current 1	V1A, V1B, V3A, V3B, V2, V4	I <sub>OL</sub>	V1A/B, V2, V3A/B, V4 = -8.25V	10.0			mA
		I <sub>OM1</sub>	V1A/B, V2, V3A/B, V4 = -0.25V			-5.0	mA
		I <sub>OM2</sub>	V1A/B, V3A/B = 0.25V	5.0			mA
		I <sub>OH</sub>	V1A/B, V3A/B = 14.75V			-7.2	mA
Output current 2	SUB	I <sub>OSL</sub>	SUB = -8.25V	5.4			mA
		I <sub>OSH</sub>	SUB = 14.75V			-4.0	mA

\*1 This input pin is a schmitt trigger input and it has protective diode of the power supply side in the IC.  
It is not supported to 5V input.

\*2 These input pins are with pull-down resistor in the IC.

**Note)** This table indicates the conditions for 3.3V drive.

**Inverter I/O Characteristics for Oscillation**

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical V <sub>th</sub>	OSCI	LV <sub>th</sub>			V <sub>DDd</sub> /2		V
Input voltage	OSCI	V <sub>IH</sub>		0.7V <sub>DDd</sub>			V
		V <sub>IL</sub>				0.3V <sub>DDd</sub>	V
Output voltage	OSCO	V <sub>OH</sub>	Feed current where I <sub>OH</sub> = -3.6mA	V <sub>DDd</sub> - 0.8			V
		V <sub>OL</sub>	Pull-in current where I <sub>OL</sub> = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	V <sub>IN</sub> = V <sub>DDd</sub> or V <sub>SS</sub>	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

**Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment**

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			VDDd/2		V
Input voltage		VIH		0.7VDDd			V
		VIL				0.3VDDd	V
Input amplitude		VIN	fmax 50MHz sine wave	0.3			Vp-p

**Note)** Input voltage is the input voltage characteristics for direct input from an external source.

Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

**Switching Characteristics**(V<sub>H</sub> = 15.0V, V<sub>M</sub> = GND, V<sub>L</sub> = -7.5V)

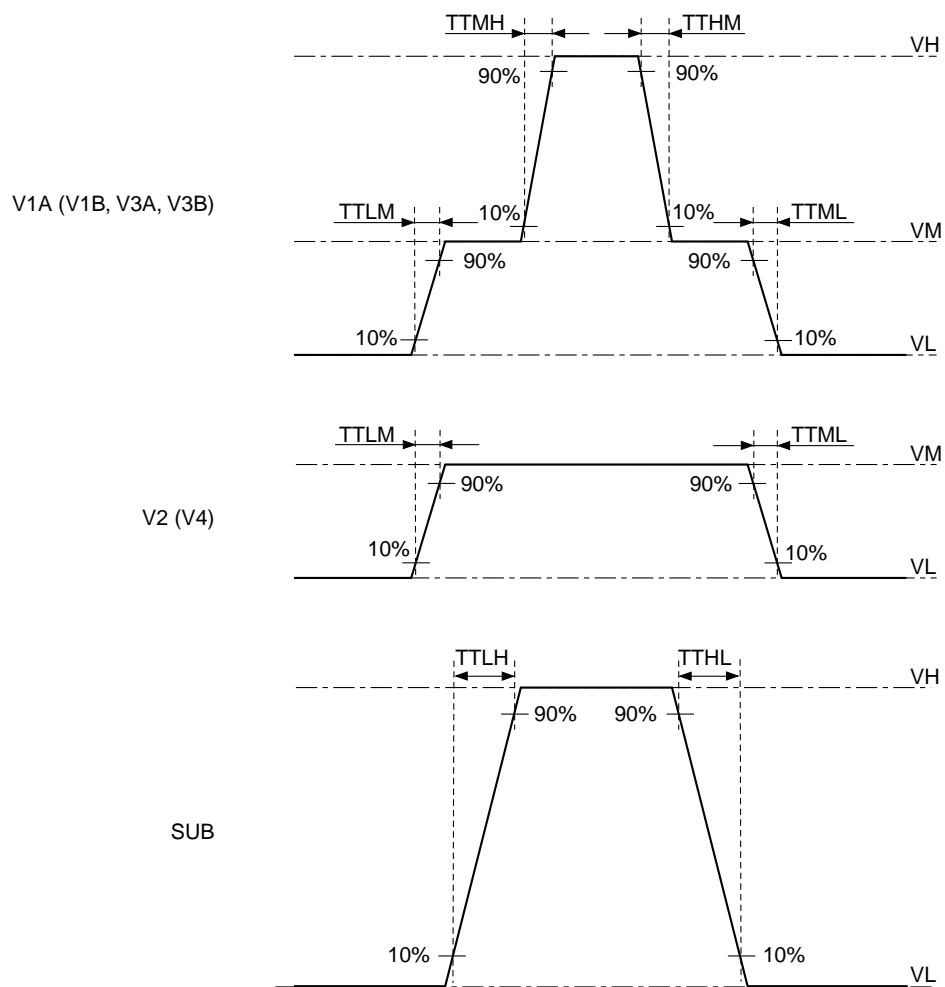
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	V <sub>L</sub> to V <sub>M</sub>	200	350	500	ns
	TTMH	V <sub>M</sub> to V <sub>H</sub>	200	350	500	ns
	TTLH	V <sub>L</sub> to V <sub>H</sub>	30	60	90	ns
Fall time	TTML	V <sub>M</sub> to V <sub>L</sub>	200	350	500	ns
	TTHM	V <sub>H</sub> to V <sub>M</sub>	200	350	500	ns
	TTHL	V <sub>H</sub> to V <sub>L</sub>	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

**Notes)**

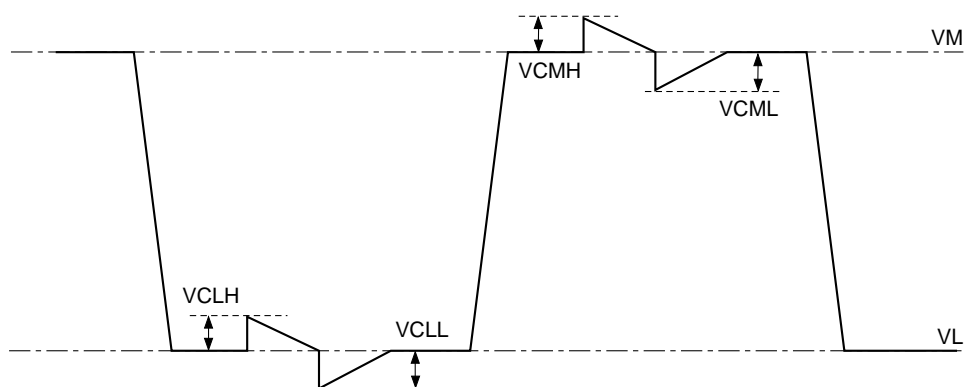
1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1μF or more) between each power supply pin (V<sub>H</sub>, V<sub>L</sub>) and GND.
3. To protect the CCD image sensor, clamp the SUB pin output at V<sub>H</sub> before input to the CCD image sensor.



## Switching Waveforms

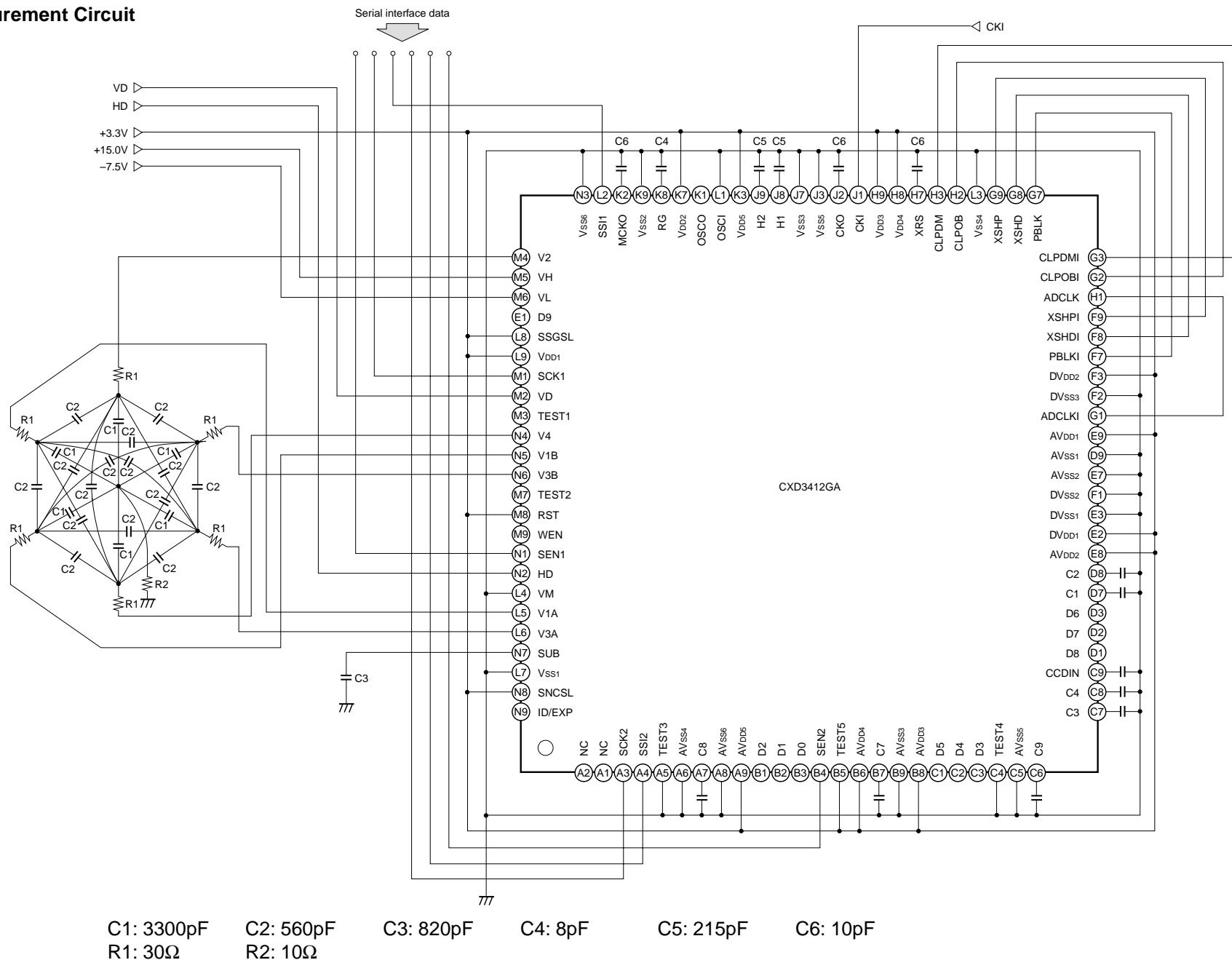


## Waveform Noise



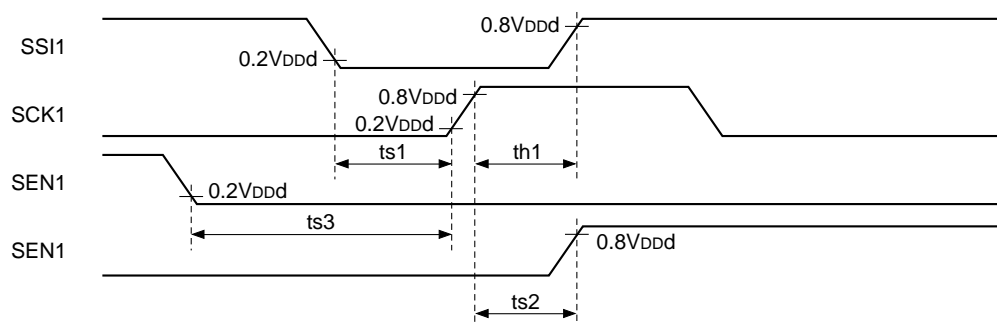
# Measurement Circuit

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## AC Characteristics

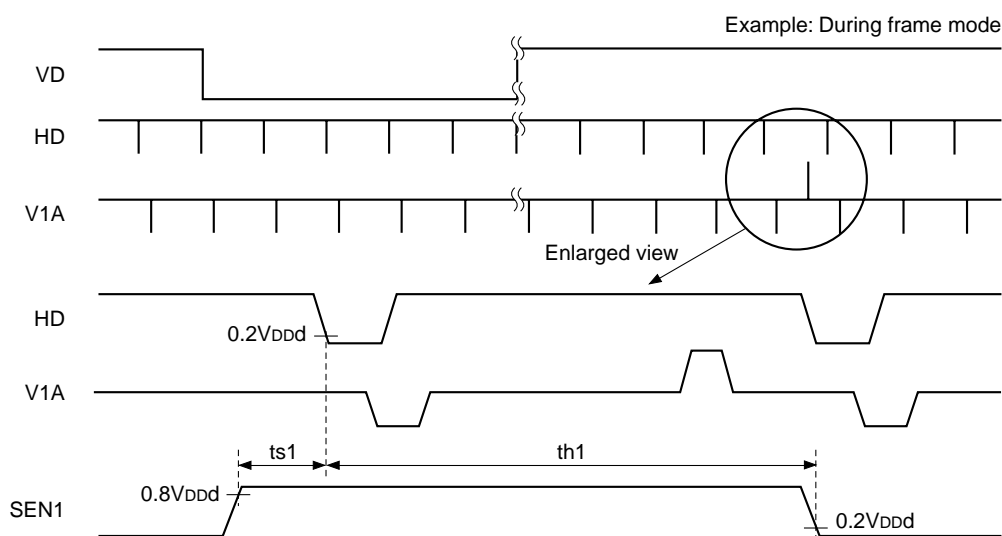
## AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI1 setup time, activated by the rising edge of SCK1	20			ns
th1	SSI1 hold time, activated by the rising edge of SCK1	20			ns
ts2	SCK1 setup time, activated by the rising edge of SEN1	20			ns
ts3	SEN1 setup time, activated by the rising edge of SCK1	20			ns

## Serial interface clock internal loading characteristics (1)

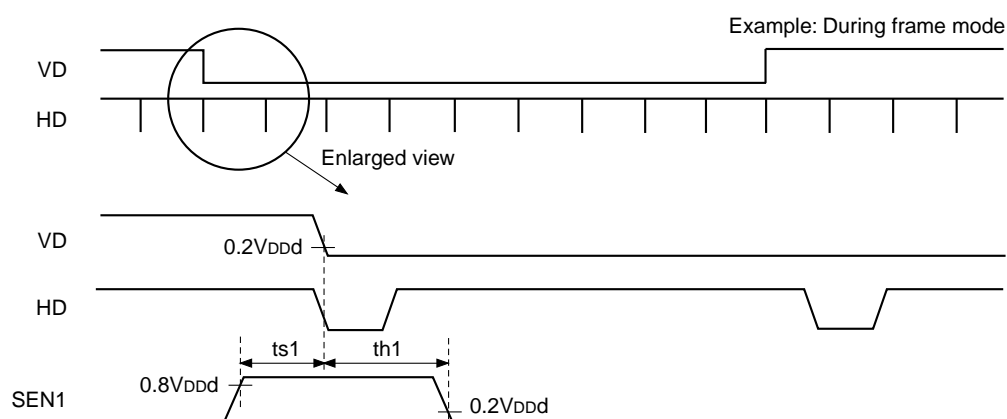


\* Be sure to maintain a constantly high SEN1 logic level near the falling edge of the HD in the horizontal period during which V1A/B and V3A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of HD	0			ns
th1	SEN1 hold time, activated by the falling edge of HD	113			μs

## Serial interface clock internal loading characteristics (2)



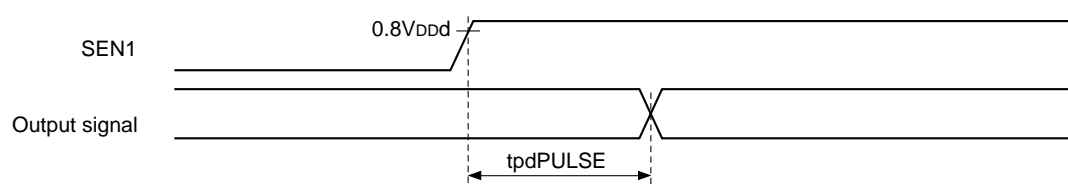
\* Be sure to maintain a constantly high SEN1 logic level near the falling edge of VD.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of VD	0			ns
th1	SEN1 hold time, activated by the falling edge of VD	200			ns

## Serial interface clock output variation characteristics

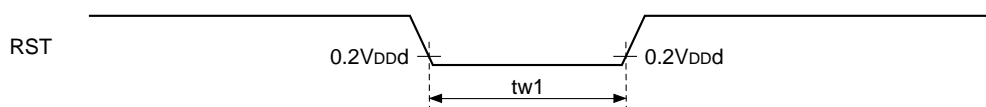
Normally, the serial interface data is loaded to the CXD3412GA at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD3412GA and controlled at the rising edge of SEN1. See "Description of Operation".



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN1	15		100	ns

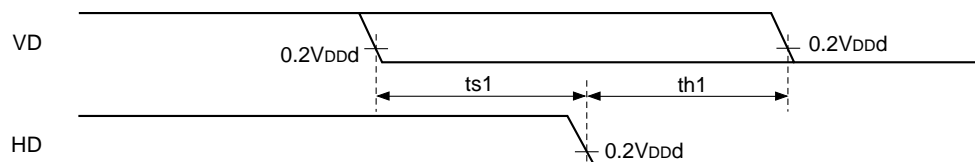
### RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
$tw1$	RST pulse width	28			ns

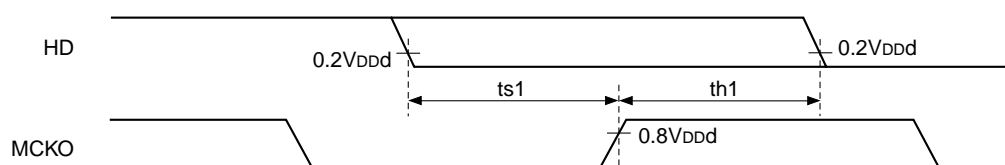
### VD and HD phase characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
$ts1$	VD setup time, activated by the falling edge of HD	0			ns
$th1$	VD hold time, activated by the falling edge of HD	0			ns

### HD loading characteristics

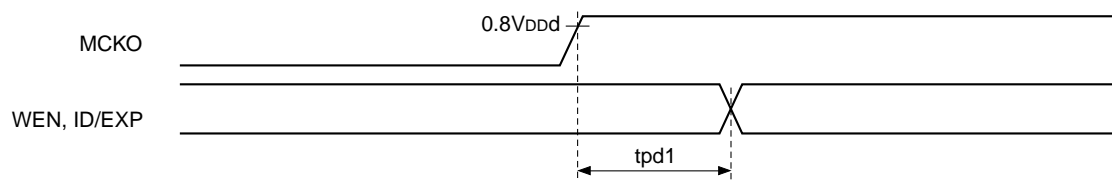


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
$ts1$	HD setup time, activated by the rising edge of MCKO	20			ns
$th1$	HD hold time, activated by the rising edge of MCKO	0			ns

## Output variation characteristics



WEN and ID/EXP load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	25		70	ns

## CCD Signal Processor Block Electrical Characteristics

## DC Characteristics

(Fc = 22.5MSPS, DVDD1, 2 = AVDD1, 2, 3, 4, 5 = 3.3V, Ta = 25°C)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	DVDD1	VDDe		3.0	3.3	3.6	V
Supply voltage 2	DVDD2	VDDf		3.0	3.3	3.6	V
Supply voltage 3	AVDD1, AVDD2, AVDD3, AVDD4, AVDD5	VDDg		3.0	3.3	3.6	V
Analog input capacitance	CCDIN	CIN			15		pF
Input voltage	SCK2, SSI2, SEN2, TEST3, TEST4, XSHDI, XSHPI, ADCLKI, CLPOBI, CLPDMI, PBLKI	VI+			1.8		V
		VI-			1.1		V
A/D clock duty	ADCLKI				50		%
Output voltage	D0 to D9	VOH	Feed current where IOH = -2.0mA	VDDe - 0.9			V
		VOL	Pull-in current where IOL = 2.0mA			0.4	V

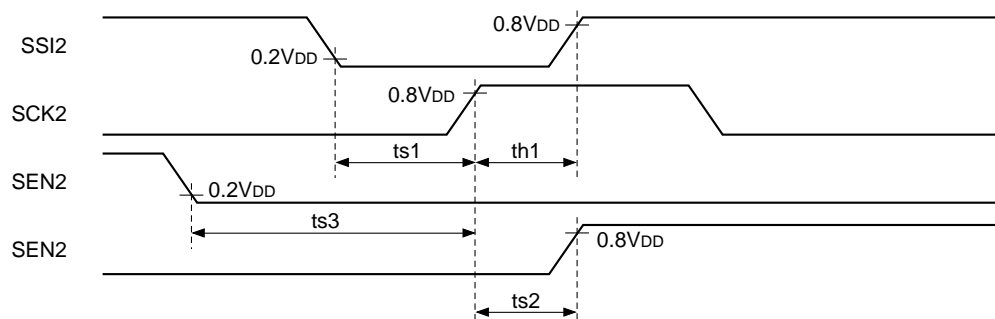
## Analog Characteristics

(Fc = 22.5MSPS, DVDD1, 2 = AVDD1, 2, 3, 4, 5 = 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CCDIN input voltage amplitude	VIN	PGA gain = 0dB, output full scale	900		1100	mV
PGA maximum gain	Gmax	PGA gain setting data = "3FFh"		42		dB
PGA minimum gain	Gmin	PGA gain setting data = "000h"		-6		dB
ADC resolution				10		bit
ADC maximum conversion rate	Fc max		22.5			MHz
ADC integral non-linearity error	EL	PGA gain = 0dB		±1.0		LSB
ADC differential non-linearity error	ED	PGA gain = 0dB		±0.5		LSB
Signal-to-noise ratio	SNR	CCDIN input connected to GND via a coupling capacitor PGA gain = 0dB		77		dB
CCDIN input voltage clamp level	CLP			1.5		V
CCD optical black signal clamp level	OB	OBLVL = "8h" PGA gain = 0dB		32		LSB

## AC Characteristics

## AC characteristics between the serial interface clocks



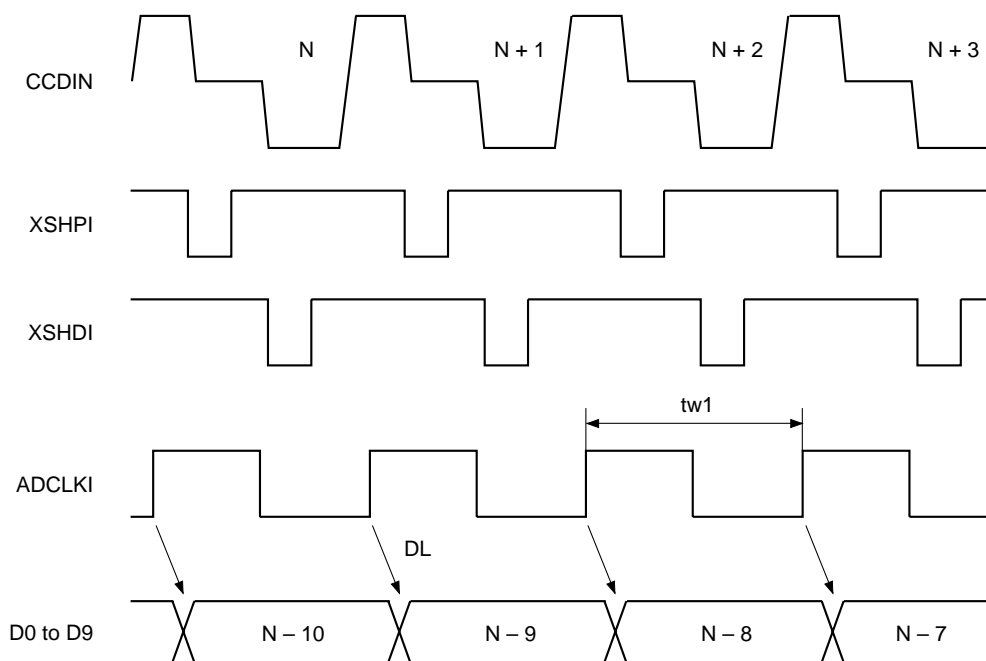
\* The setting values are reflected to the operation 6 ADCLKI clocks after the serial data is loaded at the rise of SEN2.

(F<sub>C</sub> = 22.5MSPS, DV<sub>DD1, 2</sub> = AV<sub>DD1, 2, 3, 4, 5</sub> = 3.3V, T<sub>a</sub> = 25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tp1	SCK2 clock period	100			ns
ts1	SSI2 setup time, activated by the rise of SCK2	30			ns
th1	SSI2 hold time, activated by the rise of SCK2	30			ns
ts2	SCK2 setup time, activated by the rise of SEN2	30			ns
ts3	SEN2 setup time, activated by the rise of SCK2	30			ns



## CDS/ADC Timing Chart

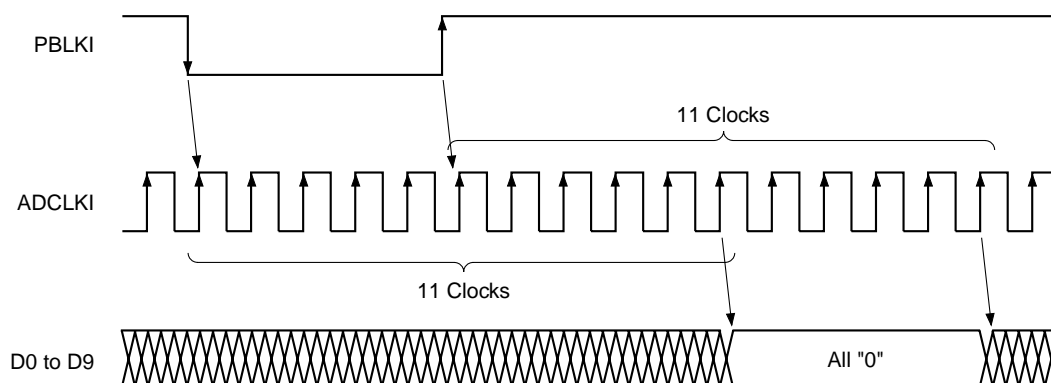


\* Set the input pulse polarity setting data D13, D14 and D15 of the serial interface data to "0".

( $F_c = 22.5\text{MSPS}$ ,  $DV_{DD1, 2} = AV_{DD1, 2, 3, 4, 5} = 3.3\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

Symbol	Definition	Min.	Typ.	Max.	Unit
$tw1$	ADCLKI clock period	44			ns
	ADCLKI clock duty		50		%
DL	Data latency		9		clocks

## Preblanking Timing Chart



## Description of Operation

Pulses output from the CXD3412GA's timing generator block are controlled mainly by the **RST** pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on page 20 and thereafter.

**Pin Status Table**

Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
A1	NC		—			D8	C2			—	
A2	NC		—			D9	AV <sub>SS1</sub>			—	
A3	SCK2		—			E1	D9			—	
A4	SSI2		—			E2	DV <sub>DD1</sub>			—	
A5	TEST3		—			E3	DV <sub>SS1</sub>			—	
A6	AV <sub>SS4</sub>		—			E7	AV <sub>SS2</sub>			—	
A7	C8		—			E8	AV <sub>DD2</sub>			—	
A8	AV <sub>SS6</sub>		—			E9	AV <sub>DD1</sub>			—	
A9	AV <sub>DD5</sub>		—			F1	DV <sub>SS2</sub>			—	
B1	D2		—			F2	DV <sub>SS3</sub>			—	
B2	D1		—			F3	DV <sub>DD2</sub>			—	
B3	D0		—			F7	PBLKI			—	
B4	SEN2		—			F8	XSHDI			—	
B5	TEST5		—			F9	XSHPI			—	
B6	AV <sub>DD4</sub>		—			G1	ADCLKI			—	
B7	C7		—			G2	CLPOBI			—	
B8	AV <sub>DD3</sub>		—			G3	CLPDMI			—	
B9	AV <sub>SS3</sub>		—			G7	PBLK	ACT	L	L	H
C1	D5		—			G8	XSHD	ACT	L	L	ACT
C2	D4		—			G9	XSHP	ACT	L	L	ACT
C3	D3		—			H1	ADCLK	ACT	L	L	ACT
C4	TEST4		—			H2	CLPOB	ACT	L	L	H
C5	AV <sub>SS5</sub>		—			H3	CLPDM	ACT	L	L	H
C6	C9		—			H7	XRS	ACT	L	L	ACT
C7	C3		—			H8	V <sub>DD4</sub>			—	
C8	C4		—			H9	V <sub>DD3</sub>			—	
C9	CCDIN		—			J1	CKI	ACT	ACT	ACT	ACT
D1	D8		—			J2	CKO	ACT	ACT	L	ACT
D2	D7		—			J3	V <sub>SS5</sub>			—	
D3	D6		—			J7	V <sub>SS3</sub>			—	
D7	C1		—			J8	H1	ACT	L	L	ACT

Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
J9	H2	ACT	L	L	ACT	M2	VD* <sup>1</sup>	ACT	L	L	H
K1	OSCO	ACT	ACT	ACT	ACT	M3	TEST1	—			
K2	MCKO	ACT	ACT	L	ACT	M4	V2	ACT	VM	VM	VM
K3	V <sub>DD5</sub>	—				M5	VH	—			
K7	V <sub>DD2</sub>	—				M6	VL	—			
K8	RG	ACT	L	L	ACT	M7	TEST2	—			
K9	V <sub>SS2</sub>	—				M8	RST	ACT	ACT	ACT	L
L1	OSCI	ACT	ACT	ACT	ACT	M9	WEN	ACT	L	L	L
L2	SSI1	ACT	ACT	ACT	DIS	N1	SEN1	ACT	ACT	ACT	DIS
L3	V <sub>SS4</sub>	—				N2	HD* <sup>1</sup>	ACT	L	L	H
L4	VM	—				N3	V <sub>SS6</sub>	—			
L5	V1A	ACT	VH	VH	VM	N4	V4	ACT	VM	VM	VL
L6	V3A	ACT	VH	VH	VL	N5	V1B	ACT	VH	VH	VM
L7	V <sub>SS1</sub>	—				N6	V3B	ACT	VH	VH	VL
L8	SSGSL	ACT	ACT	ACT	ACT	N7	SUB	ACT	VH	VH	VL
L9	V <sub>DD1</sub>	—				N8	SNCSL	ACT	ACT	ACT	ACT
M1	SCK1	ACT	ACT	ACT	DIS	N9	ID/EXP	ACT	L	L	L

\*<sup>1</sup> It is for output. For input, all items are "ACT".

**Note)** ACT means that the circuit is operating, and DIS means that loading is stopped.

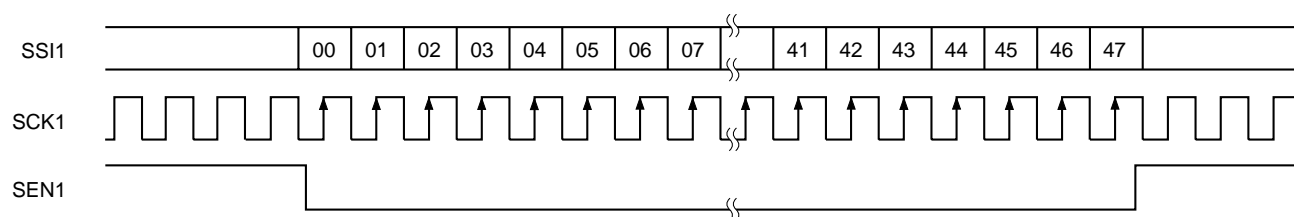
L indicates a low output level, and H a high output level in the controlled status.

Also, VH, VM and VL indicate the voltage levels applied to VH (Pin M5), VM (Pin L3) and VL (Pin M6), respectively, in the controlled status.

## Timing Generator Block Serial Interface Control

The CXD3412GA's timing generator block basically loads and reflects the timing generator block serial interface data sent in the following format in the readout portion at the falling edge of HD. Here, readout portion specifies the horizontal period during which V1A/B and V3A/B, etc. take the ternary value.

Note that some items reflect the timing generator block serial interface data at the falling edge of VD or the rising edge of SEN1.



There are two categories of timing generator block serial interface data: CXD3412GA timing generator block drive control data (hereafter "control data") and electronic shutter data (hereafter "shutter data").

The details of each data are described below.

## Control Data

Data	Symbol	Sunction	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08, D09	CTG	Category switching	See [D08] to [D09] CTG.		All 0
D10 to D12	MODE	Drive mode switching	See [D10] to [D12] MODE.		All 0
D13	SMD	Electronic shutter mode switching* <sup>1</sup>	OFF	ON	0
D14	HTSG	HTSG control switching* <sup>1</sup>	OFF	ON	0
D15	PTSG	Internal SSG function switching	NTSC equivalent	PAL equivalent	0
D16 to D31	—	—	—	—	All 0
D32	FGOB	Wide CLPOB generation switching* <sup>2</sup>	OFF	ON	0
D33	EXP	ID/EXP output switching	ID	EXP	0
D34, D35	PTOB	CLPOB waveform pattern switching	See [D34] to [D35] PTOB.		All 0
D36, D37	LDAD	ADCLK logic phase switching	See [D36] to [D37] LDAD.		1 0
D38, D39	STB	Standby control	See [D38] to [D39] STB.		All 0
D40 to D47	—	—	—	—	All 0

\*<sup>1</sup> See [D13] SMD.\*<sup>2</sup> See [D32] FGOB.

## Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08, D09	CTG	Category switching	See <span style="border: 1px solid black;">D08</span> to <span style="border: 1px solid black;">D09</span> CTG.		All 0
D10 to D19	SVD	Electronic shutter vertical period specification	See <span style="border: 1px solid black;">D10</span> to <span style="border: 1px solid black;">D19</span> SVD.		All 0
D20 to D31	SHD	Electronic shutter horizontal period specification	See <span style="border: 1px solid black;">D20</span> to <span style="border: 1px solid black;">D31</span> SHD.		All 0
D32 to D41	SPL	High-speed shutter position specification	See <span style="border: 1px solid black;">D32</span> to <span style="border: 1px solid black;">D41</span> SPL.		All 0
D42 to D47	—	—	—		All 0

## Detailed Description of Each Data

### Shared data: **D08**, **D09** CTG [Category]

Of the data provided to the CXD3412GA by the serial interface, the CXD3412GA loads **D10** and subsequent data to each data register as shown in the table below according to the combination of **D08** and **D09**.

D09	D08	Description of operation
0	0	Loading to control data register
0	1	Loading to shutter data register
1	X	Test mode

Note that the CXD3412GA can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

### Control data: **D10** to **D12** MODE [Drive mode]

The CXD3412GA timing generator block drive mode can be switched as follows. However, the drive mode bits are loaded to the CXD3412GA and reflected at the falling edge of VD.

D12	D11	D10	Description of operation
0	0	0	Draft mode (sextuple speed: default)
0	0	1	Frame mode (A field read out)
0	1	0	Frame mode (B field read out)
0	1	1	Frame mode
1	0	X	AF1 mode
1	1	X	AF2 mode

### Control data: **D15** PTSG [Internal SSG output pattern]

The CXD3412GA internal SSG output pattern can be switched as follows. However, the internal SSG output pattern bits are loaded to the CXD3412GA and reflected at the falling edge of VD.

D15	Description of operation
0	NTSC equivalent pattern output
1	PAL equivalent pattern output

VD period in each pattern is defined as follows. However, care should be taken that HD period is changing by the mode.

	Frame mode	Draft mode	AF1 mode	AF2 mode
NTSC equivalent pattern	885H + 810ck	285H + 1455ck × 2	142H + 1384ck + 1383ck	71H + 1384ck
PAL equivalent pattern	884H + 1104ck	342H + 2592ck	171H + 1296ck	85H + 1960ck

See the Timing Charts for the actual operation.

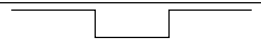



**Control data: D32 FGOB [Wide CLPOB generation]**

This controls wide CLPOB generation during the vertical OPB period. See the Timing Charts for the actual operation. The default is "OFF".

D32	Description of operation
0	Wide CLPOB generation OFF
1	Wide CLPOB generation ON

**Control data: D34, D35 PTOB [CLPOB waveform pattern]**

This indicates the CLPOB waveform pattern. The default is "Normal".

D35	D34	Waveform pattern
0	0	 (Normal)
0	1	 (Shifted rearward)
1	0	 (Shifted forward)
1	1	 (Wide)

**Control data: D36, D37 LDAD [ADCLK logic phase]**

This indicates the ADCLK logic phase adjustment data. The default is 90° relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

**Control data: D38, D39 STB [Standby]**

The operating mode is switched as follows. However, the standby bits are loaded to the CXD3412GA and control is applied immediately at the rising edge of SEN1.

D39	D38	Symbol	Operating mode
X	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	1	STB	Standby mode

See the Pin Status Table for the pin status in each mode.



**Control data/shutter data: [Electronic shutter]**

The CXD3412GA realizes various electronic shutter functions by using control data D13 SMD and D14 HTSG and shutter data D10 to D19 SVD, D20 to D31 SHD and D32 to D41 SPL.

These functions are described in detail below.

First, the various modes are shown below. These modes are switched using control data D13 SMD.

D13	Description of operation
0	Electronic shutter stopped mode
1	Electronic shutter mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHD as an example. However, MSB (D31) is a reserve bit for the future specification, and it is handled as a dummy on this IC.

MSB								LSB			
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

SHD is expressed as 1C3h.

**[Electronic shutter stopped mode]**

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

**[Electronic shutter mode]**

During this mode, the shutter data items have the following meanings.

Symbol	Data	Description
SVD	<span style="border: 1px solid black;">D10</span> to <span style="border: 1px solid black;">D19</span>	Number of vertical periods specification ( $000h \leq SVD \leq 3FFh$ )
SHD	<span style="border: 1px solid black;">D20</span> to <span style="border: 1px solid black;">D31</span>	Number of horizontal periods specification ( $000h \leq SHD \leq 7FFh$ )
SPL	<span style="border: 1px solid black;">D32</span> to <span style="border: 1px solid black;">D41</span>	Vertical period specification for high-speed shutter operation ( $000h \leq SPL \leq 3FFh$ )

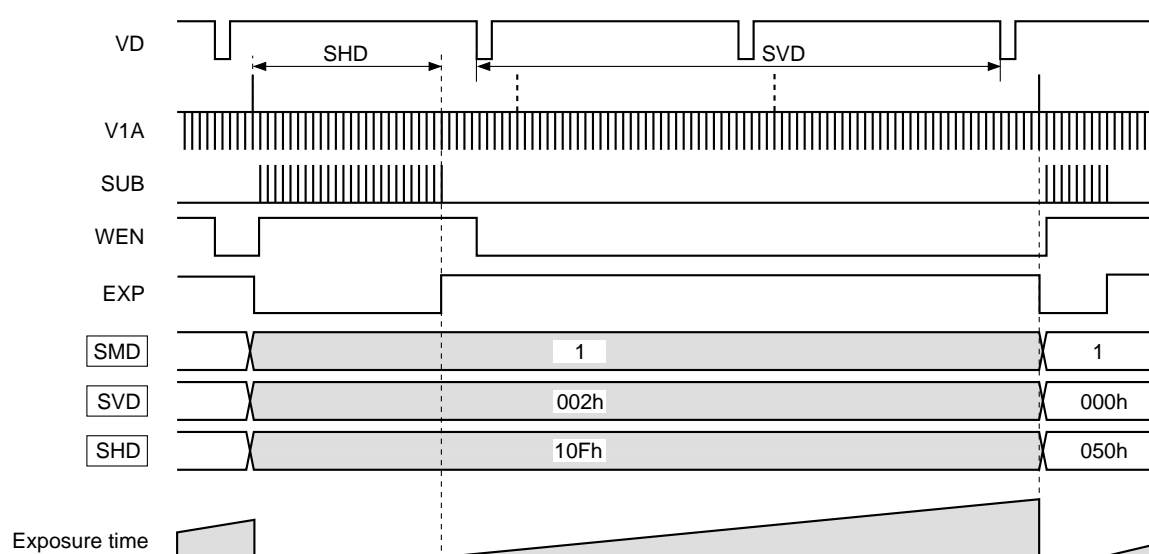
**Note)** The bit data definition area is assured in terms of the CXD3412GA functions, and does not assure the CCD characteristics.

The period during which SVD and SHD are specified together is the shutter speed. An image of the exposure time calculation formula is shown below. In actual operation, the precise exposure time is calculated from the operating frequency, VD and HD periods, decoding value during the horizontal period, and other factors.

$$(\text{Exposure time}) = \text{SVD} + \{(\text{number of HD per 1V}) - (\text{SHD} + 1)\}$$

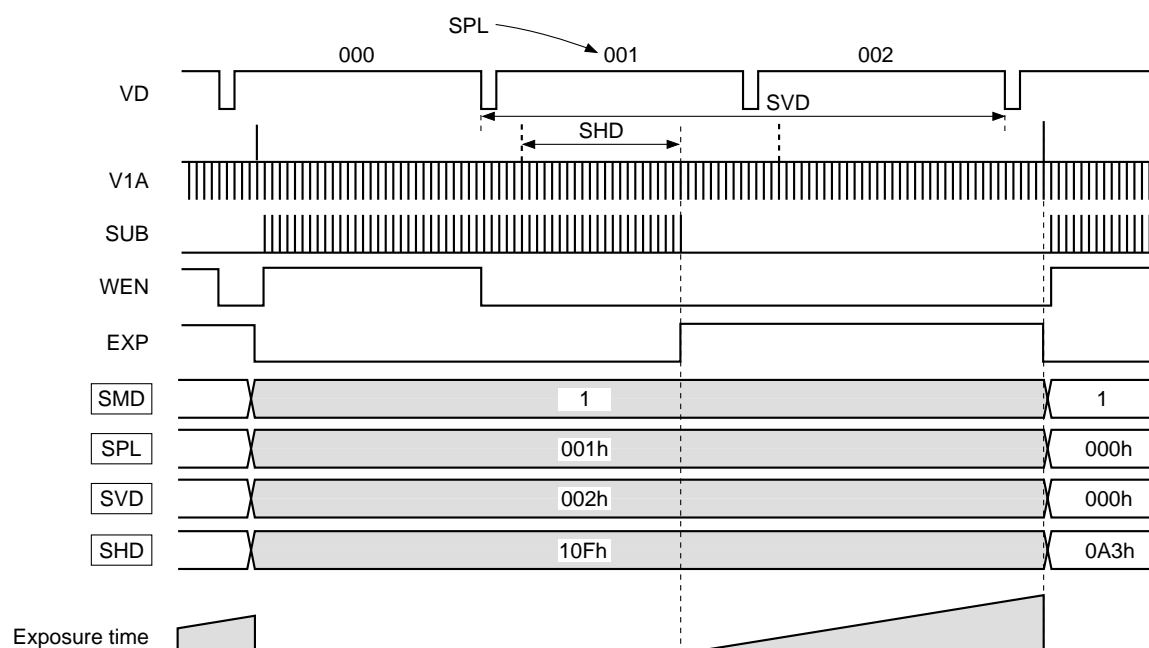
Concretely, when specifying high-speed shutter, SVD is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVD is set to "001h" or higher, the serial interface data is not loaded until this period is finished.

The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1).



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.

In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.



Incidentally, SPL is counted as "000h", "001h", "002h" and so on in conformance with SVD. At this time, performing  $SPL > SVD$  setting applies to the state of  $SPL = SVD$  correspondingly.

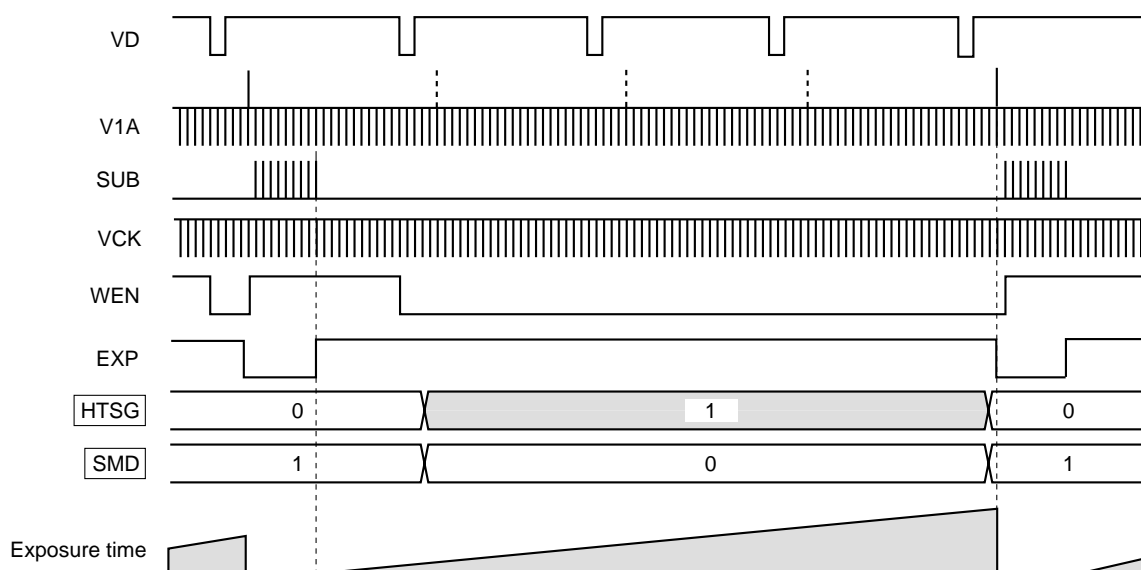
Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

**[HTSG control mode]**

This mode controls the V1A/B and V3A/B ternary level outputs (readout pulse block) using **[D14]** HTSG.

When control starts, V pulse modulation during readout period is not generated and the normal V transfer is performed.

D14	Description of operation
0	Readout pulse (SG) normal operation
1	HTSG control mode

**[EXP pulse]**

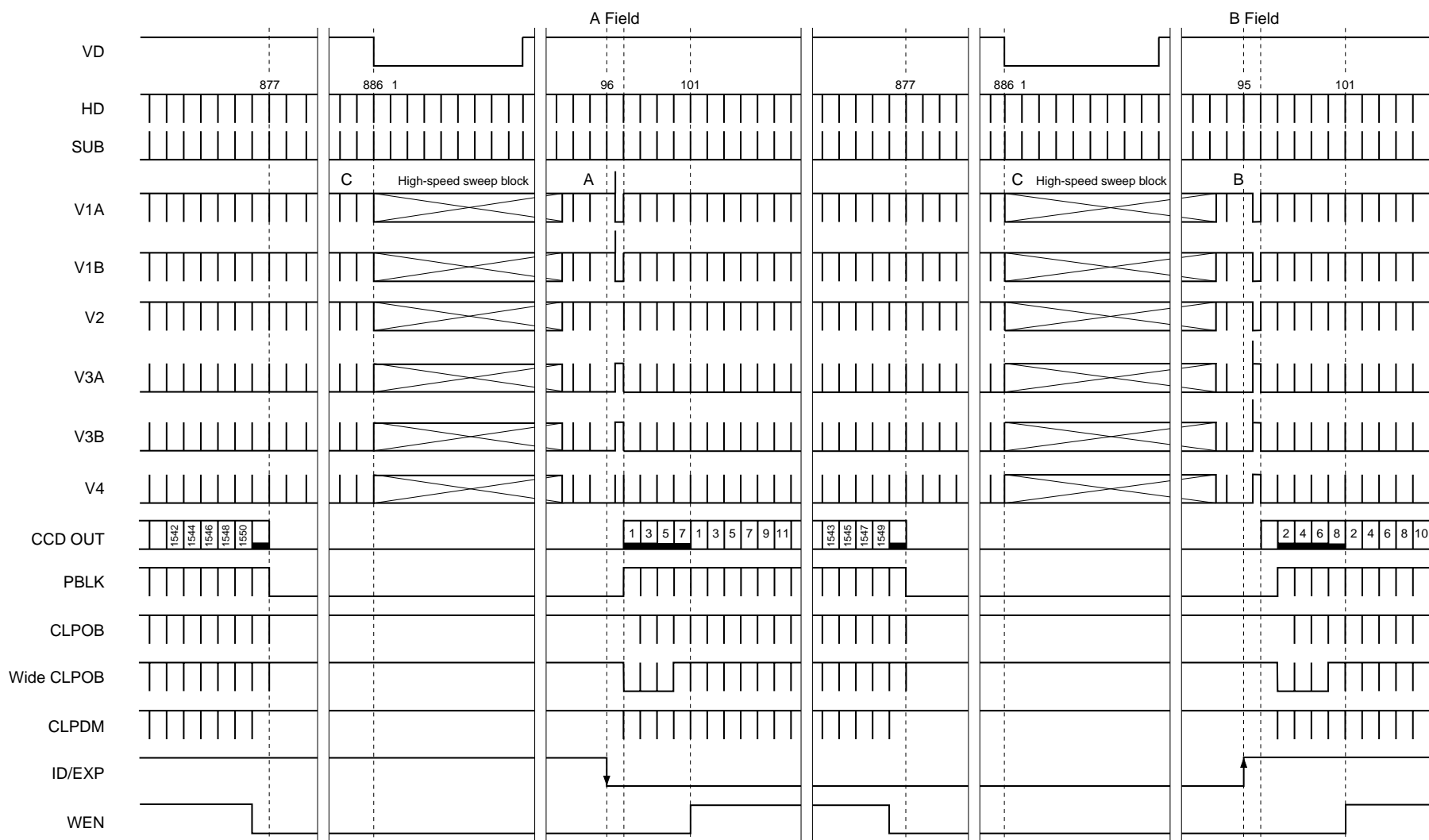
The ID/EXP (Pin 9) output can be switched between the ID pulse or the EXP pulse using **[D33]** EXP. The default is the "ID" pulse. See the Timing Charts for the ID pulse. The EXP pulse indicates the exposure time when it is high. In the draft mode, the transition point is the last SUB pulse falling edge, and midpoint value (1443ck) of each V1A/B and V3A/B ternary output falling edge. When there is no SUB pulse, the later ternary output falling edge (1538ck) is used. In the frame mode, the transition point is the last SUB pulse falling edge, and each V1A/B and V3A/B ternary output falling edge (1348ck). When there is no SUB pulse, the V pulse modulation falling edge just after ternary output (1386ck) is used. In addition, switching from ID to EXP is performed at the timing (ID transition point of the horizontal period where V1A/B and V3A/B ternary output) and reset to low.

See the EXP pulse indicated in the explanatory diagrams under Electronic Shutter for an image of operation.

Chart-1 Vertical Direction Timing Chart

MODE  
Frame mode

Applicable CCD image sensor  
• ICX412

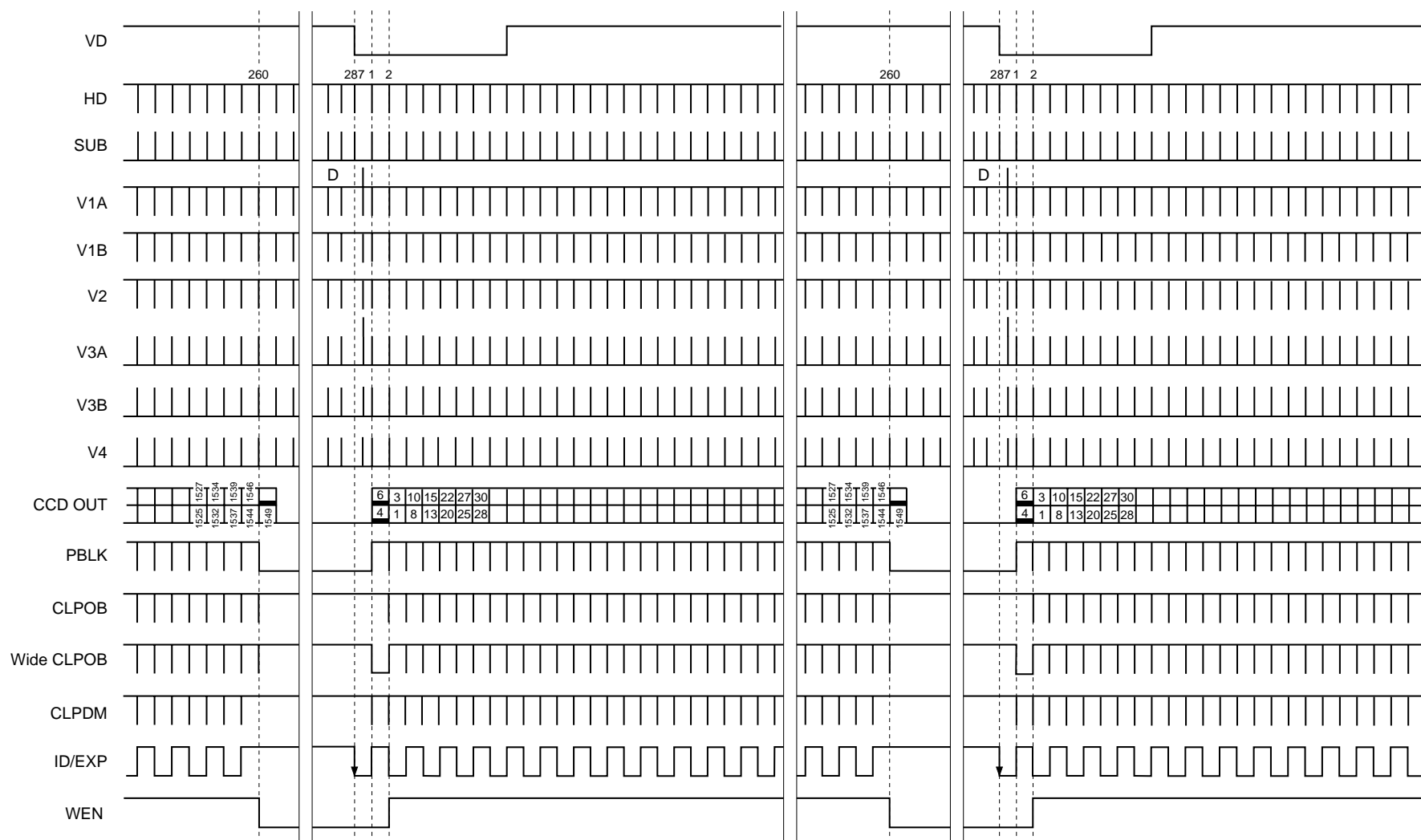


- \* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
- \* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
- \* 1560 stages are fixed for high-speed sweep block.
- \* VD of this chart is NTSC equivalent pattern (885H + 810ck units). For PAL equivalent pattern, it is 884H + 1104ck units.

Chart-2 Vertical Direction Timing Chart

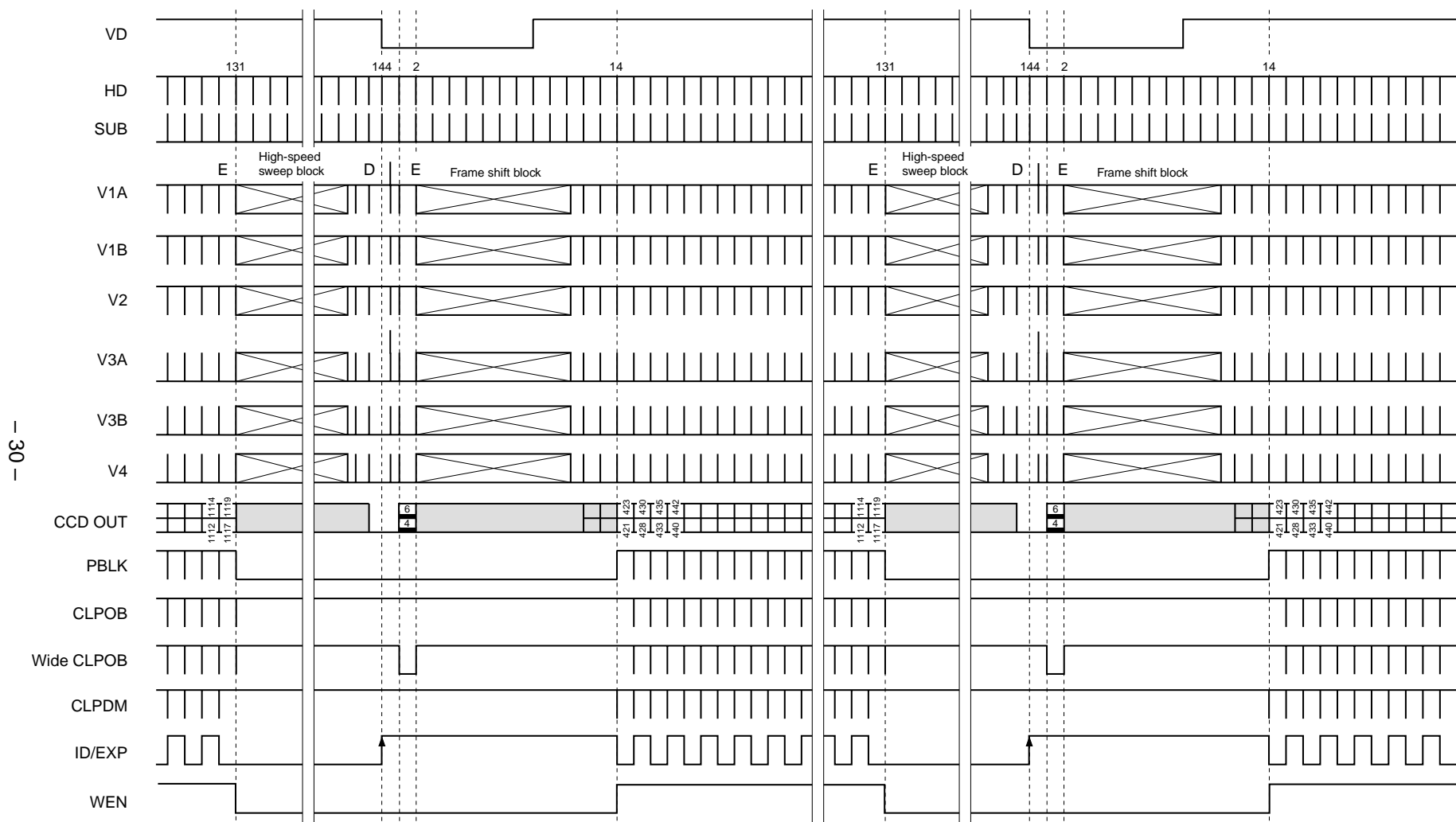
MODE  
Draft mode

Applicable CCD image sensor  
• ICX412



- \* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
- \* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.
- \* VD of this chart is NTSC equivalent pattern (285H + 1455ck + 1455ck units). For PAL equivalent pattern, it is 342H + 2592ck units.

Chart-3 Vertical Direction Timing Chart

MODE  
AF1 modeApplicable CCD image sensor  
• ICX412

\* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

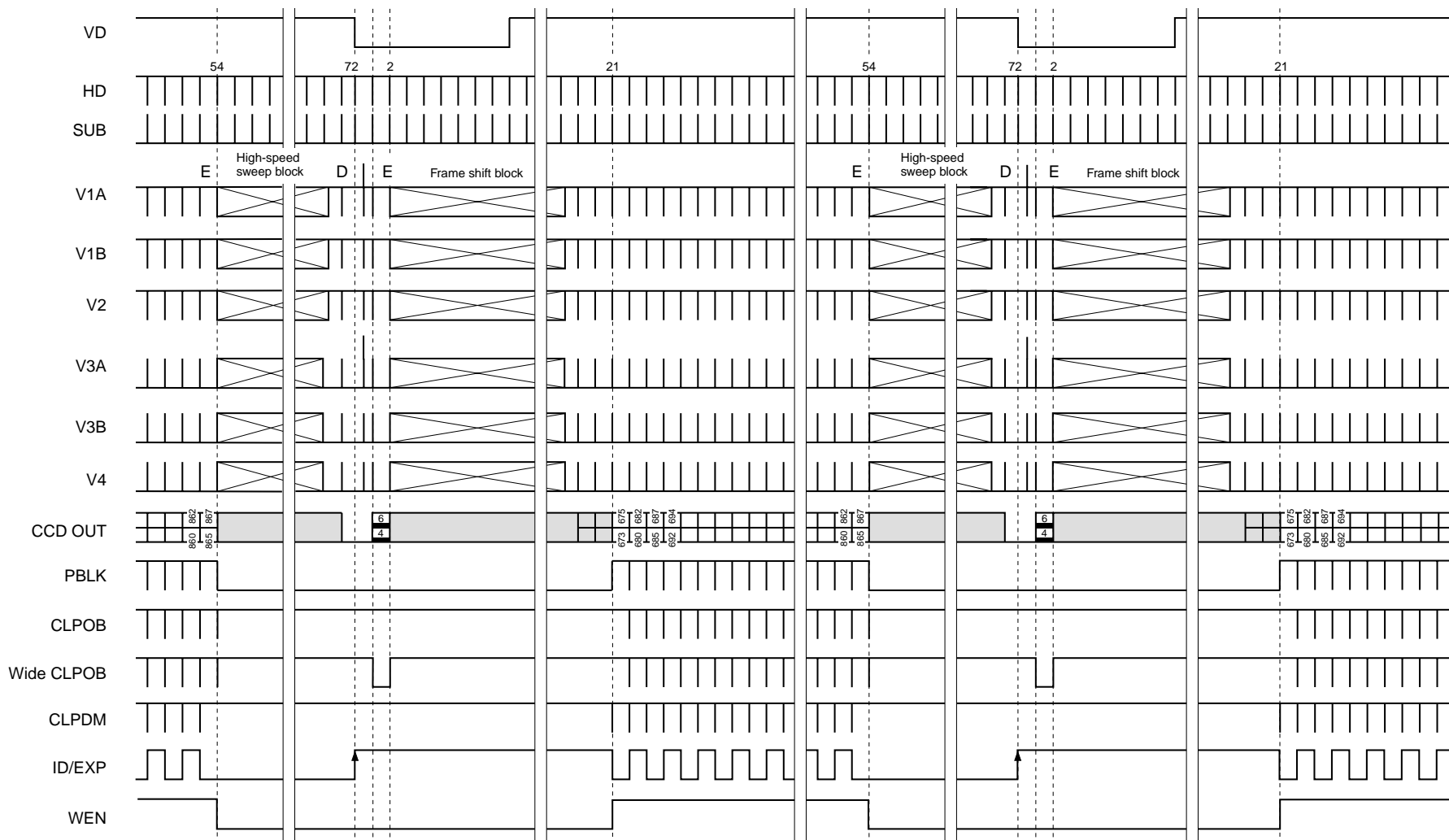
\* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

\* 75 stages are fixed for high-speed sweep block; 68 stages are fixed for frame shift block.

\* VD of this chart is NTSC equivalent pattern (142H + 1384ck + 1383ck units). For PAL equivalent pattern, it is 171H + 1296ck units.

High-speed sweep block starts from 159H.

Chart-4 Vertical Direction Timing Chart

MODE  
AF2 modeApplicable CCD image sensor  
• ICX412

\* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.

\* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

\* 116 stages are fixed for high-speed sweep block; 110 stages are fixed for frame shift block.

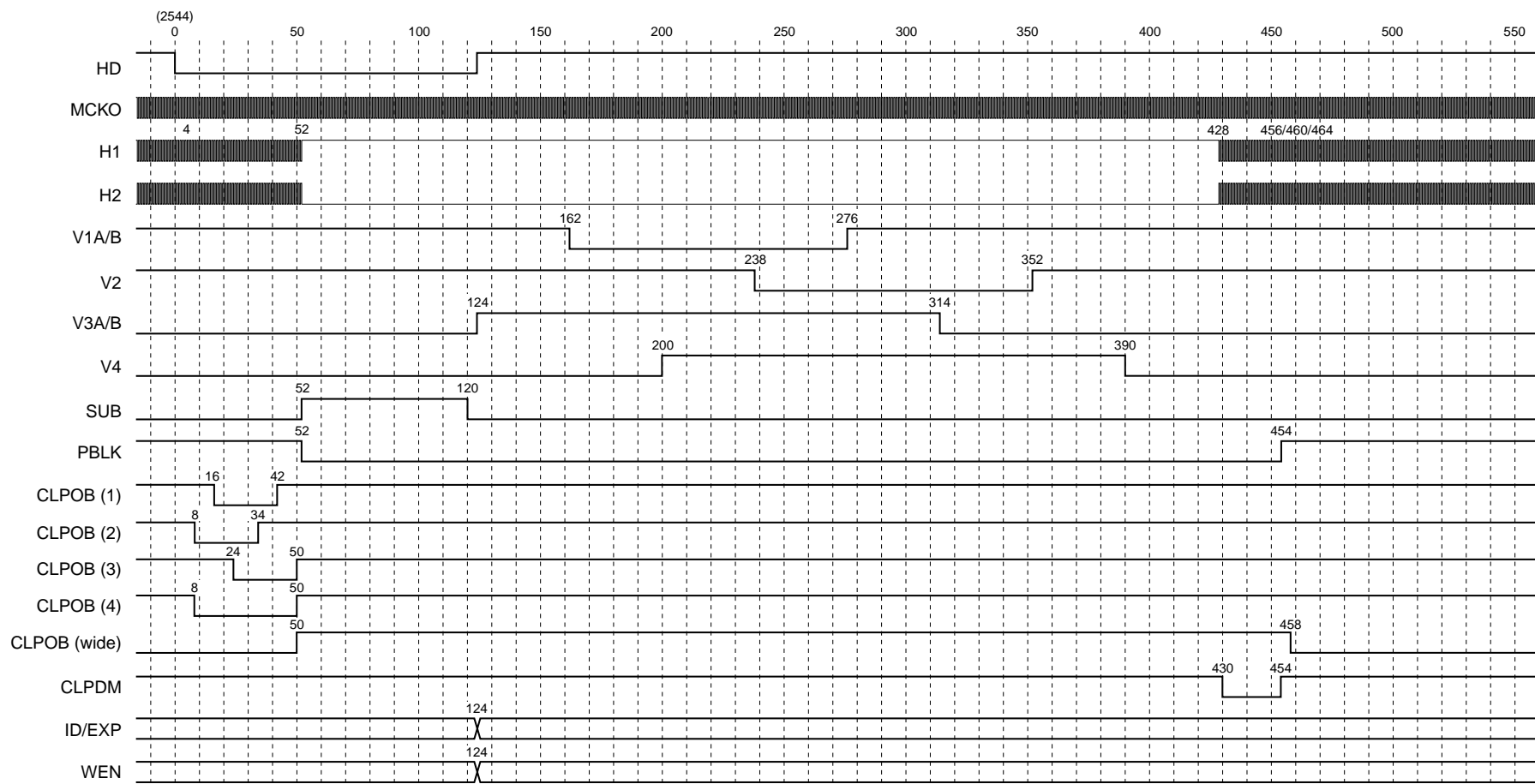
\* VD of this chart is NTSC equivalent pattern (71H + 1384ck units). For PAL equivalent pattern, it is 85H + 1960ck units.

High-speed sweep block starts from 68H. However, in this case, NTSC equivalent pattern frame rate is 0.5ck longer than 1/120s.

Chart-5 Horizontal Direction Timing Chart

MODE  
Frame mode

Applicable CCD image sensor  
• ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).

This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

\* SUB is output at the timing shown above when output is controlled by the serial interface data.

\* ID/EXP of this chart shows ID. ID/EXP and WEN are output at the timing shown above at the position shown in Chart-1.

\* CLPOB (wide) is output at the timing shown above at the position shown in Chart-1.



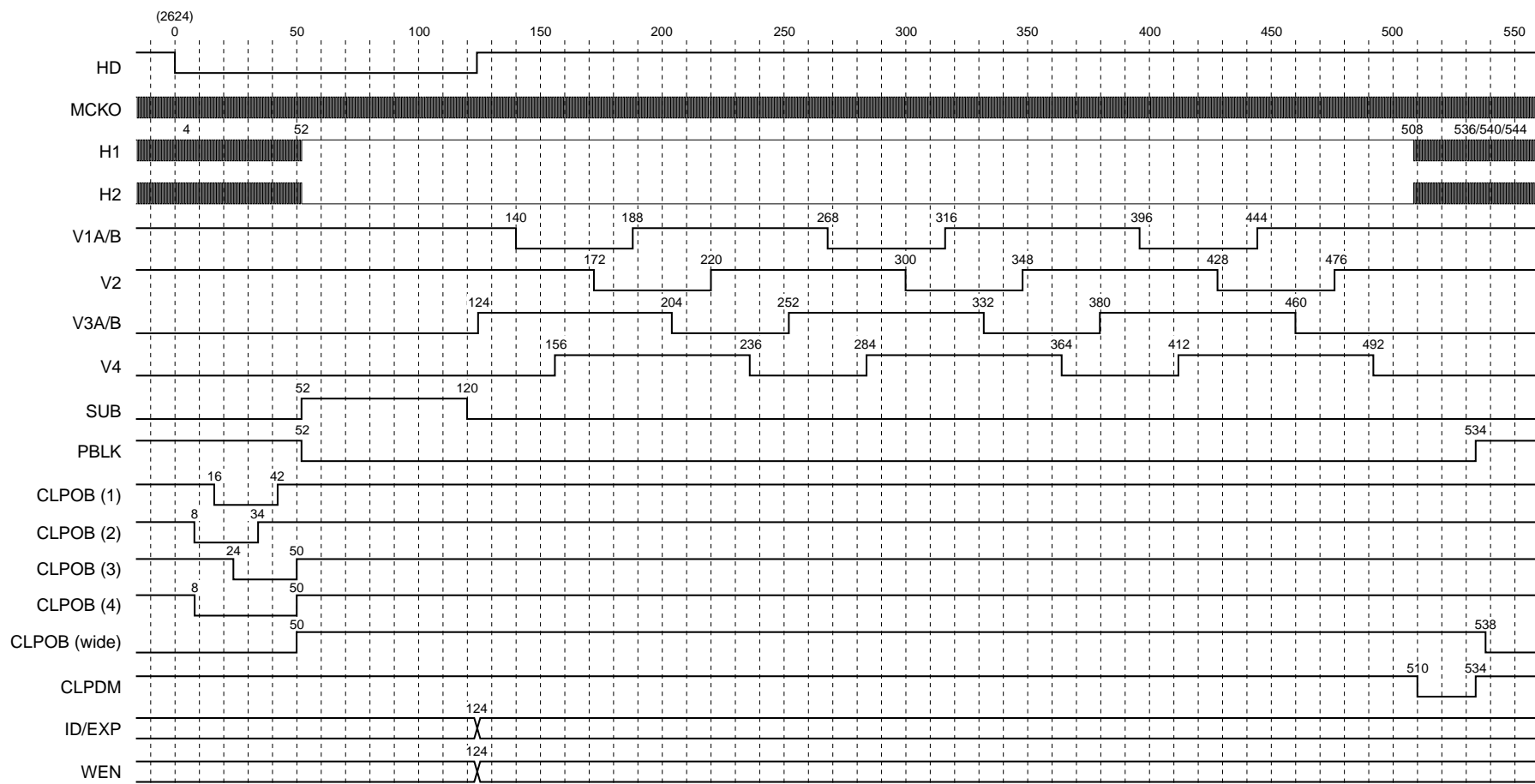
Chart-6 Horizontal Direction Timing Chart

MODE

Draft mode, AF1 mode, AF2 mode

Applicable CCD image sensor

• ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).

This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

\* SUB is output at the timing shown above when output is controlled by the serial interface data.

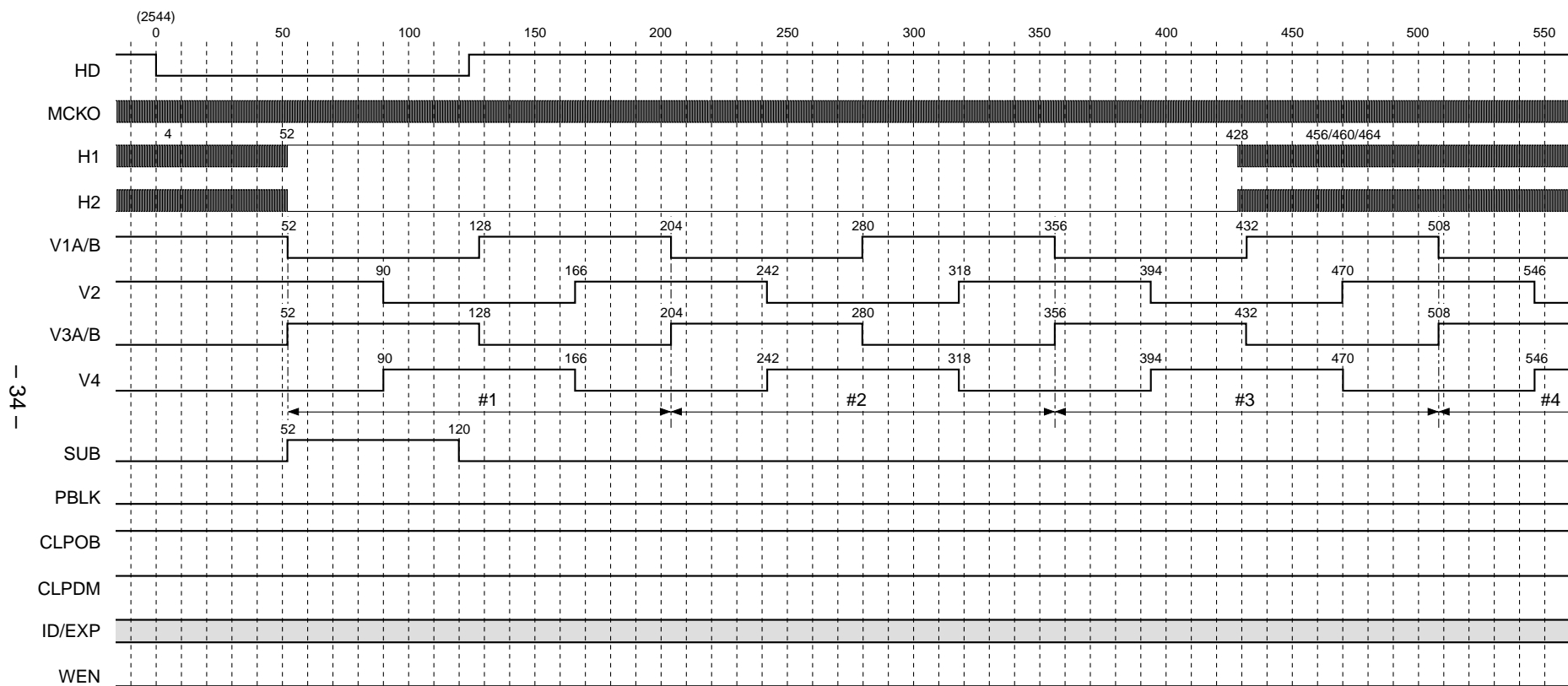
\* ID/EXP of this chart shows ID. ID/EXP and WEN are output at the timing shown above at the position shown in Chart-2, 3 and 4.

\* CLPOB (wide) is output at the timing shown above at the position shown in Chart-2, 3 and 4.

**Chart-7 Horizontal Direction Timing Chart**  
(High-speed sweep: C)

**MODE**  
Frame mode

**Applicable CCD image sensor**  
• ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).

This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

\* SUB is output at the timing shown above when output is controlled by the serial interface data.

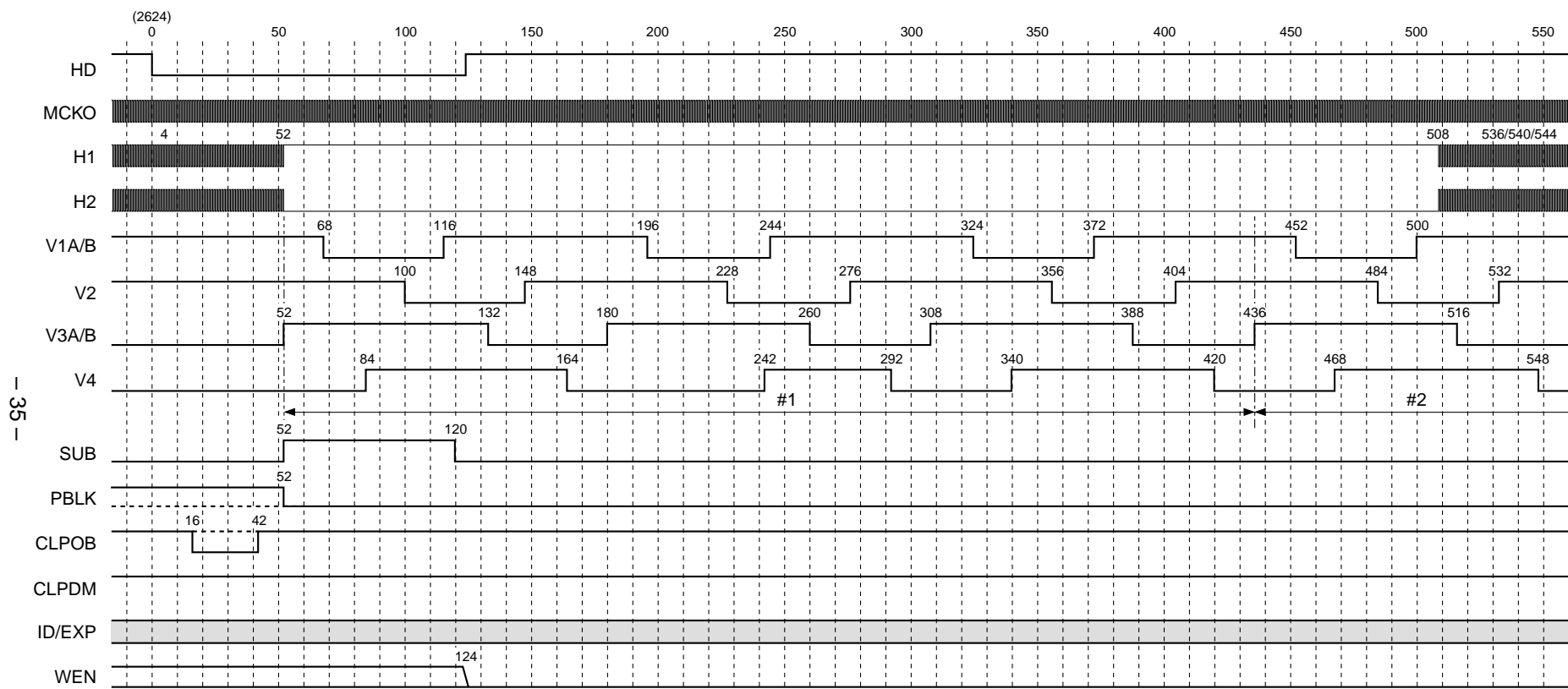
\* ID/EXP of this chart shows ID.

\* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 93H 580ck (#1560).

**Chart-8 Horizontal Direction Timing Chart**  
**(Frame shift, High-speed sweep: E)**

**MODE**  
 AF1 mode, AF2 mode

**Applicable CCD image sensor**  
 • ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).

This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

\* SUB is output at the timing shown above when output is controlled by the serial interface data.

\* ID/EXP of this chart shows ID. PBLK, CLPOB, ID/EXP and WEN are output at the timing shown above at the position shown in Chart-3 and 4.

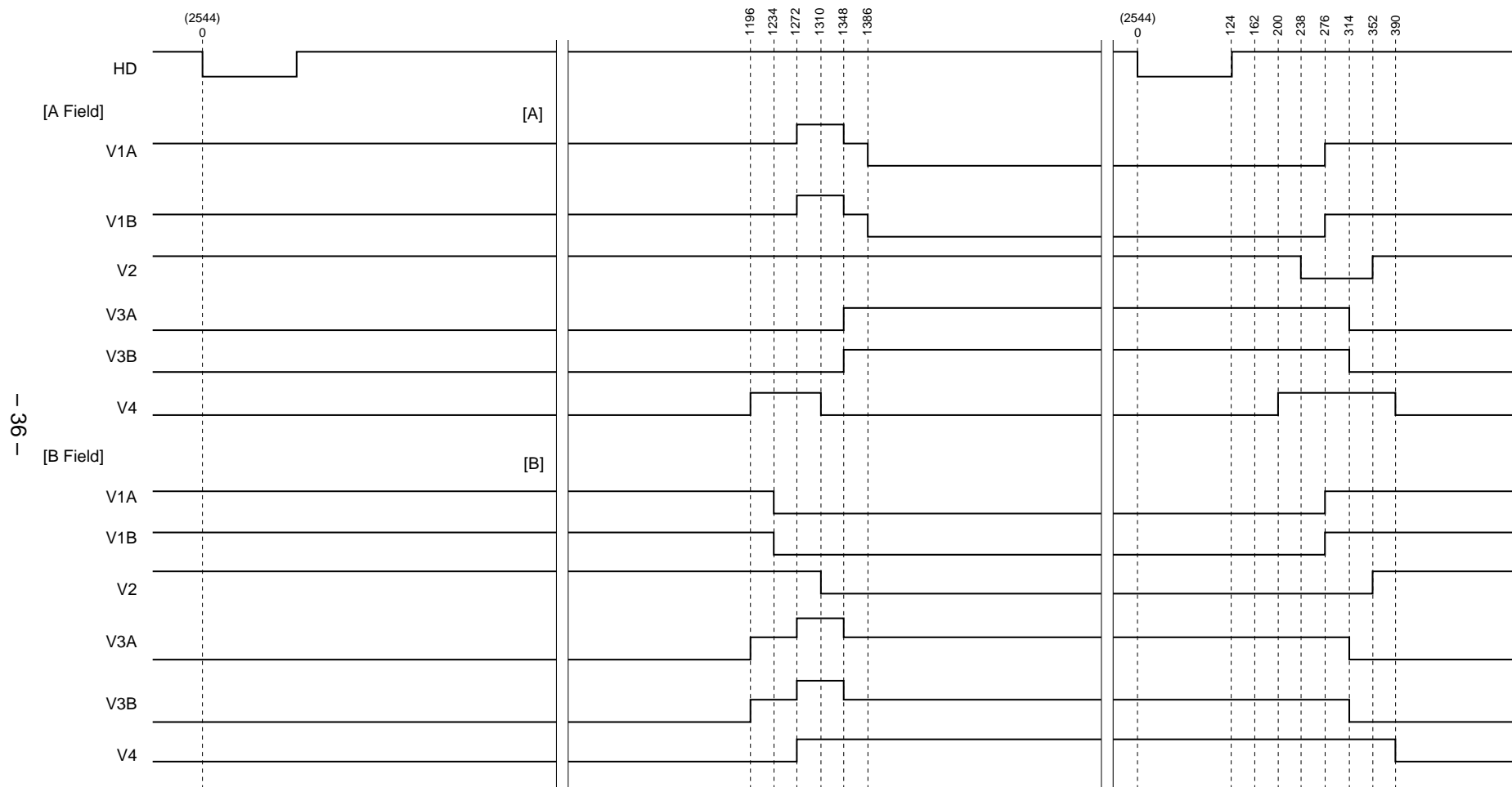
\* Frame shift of V1A/B, V2, V3A/B and V4 is performed up to 11H 2548ck (#68) in AF1 mode and 18H 308ck (#110) in AF2 mode.

In addition, high-speed sweep is performed up to 141H 2612ck (#75) in AF1 mode and 70H 2612ck (#116) in AF2 mode.

Chart-9 Horizontal Direction Timing Chart

MODE  
Frame mode

Applicable CCD image sensor  
• ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).  
This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

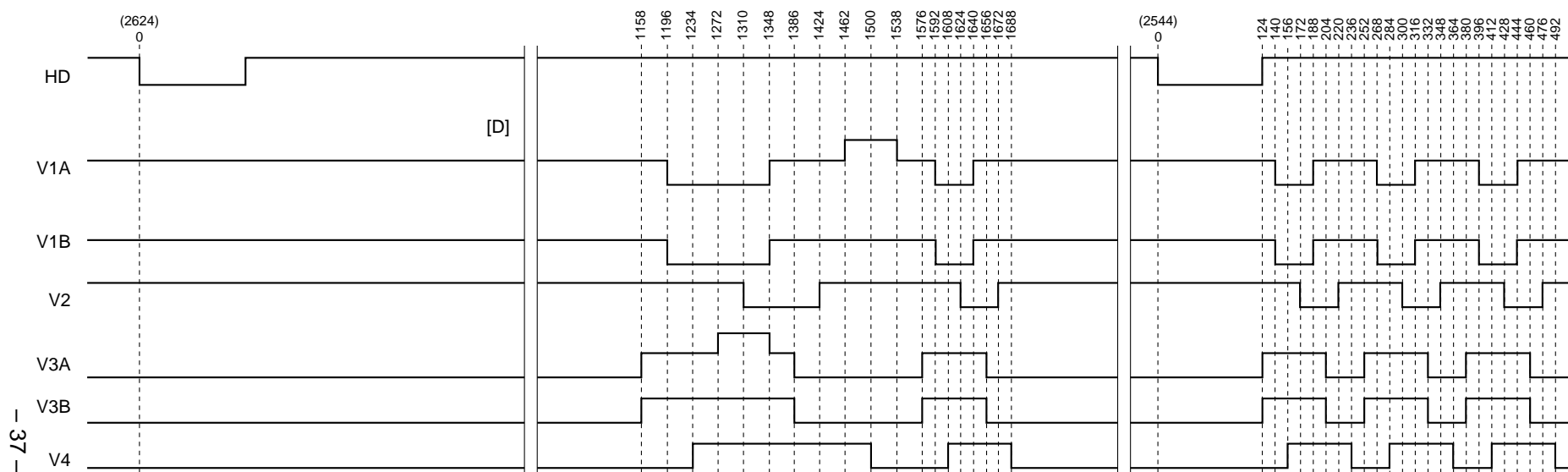
Chart-10 Horizontal Direction Timing Chart

## MODE

Draft mode, AF1 mode, AF2 mode

## Applicable CCD image sensor

• ICX412



\* The HD of this chart indicates the actual CXD3412GA load timing.

\* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

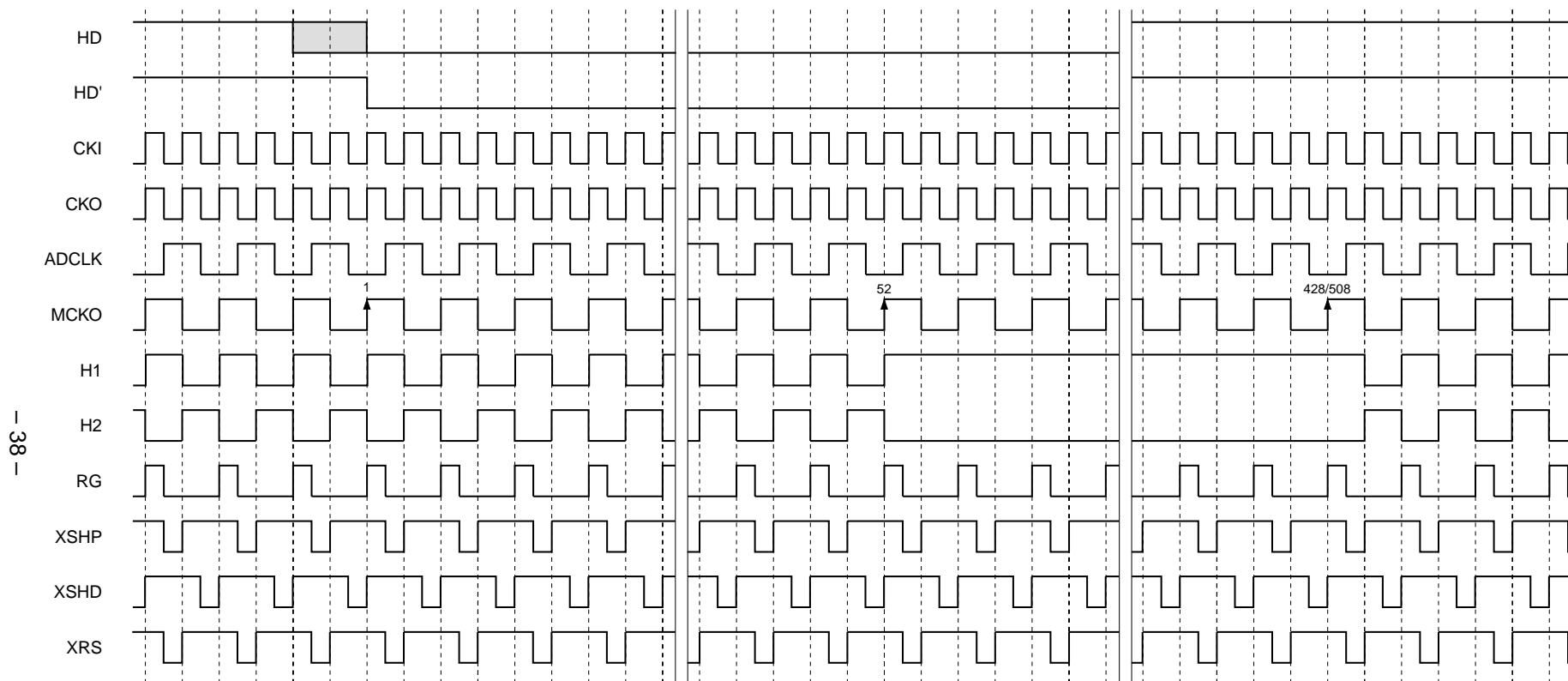
\* The HD fall period should be between approximately 2.3 to 19.0μs (when the drive frequency is 22.5MHz).  
This chart shows a period of 124ck (5.5μs). Internal SSG is at this timing.

Chart-11 High-Speed Phase Timing Chart

MODE

Applicable CCD image sensor

• ICX412



\* HD' indicates the HD which is the actual CXD3412GA load timing.

\* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.

\* The logical phase of ADCLK can be specified by the serial interface data.

Chart-12 Vertical Direction Sequence Chart

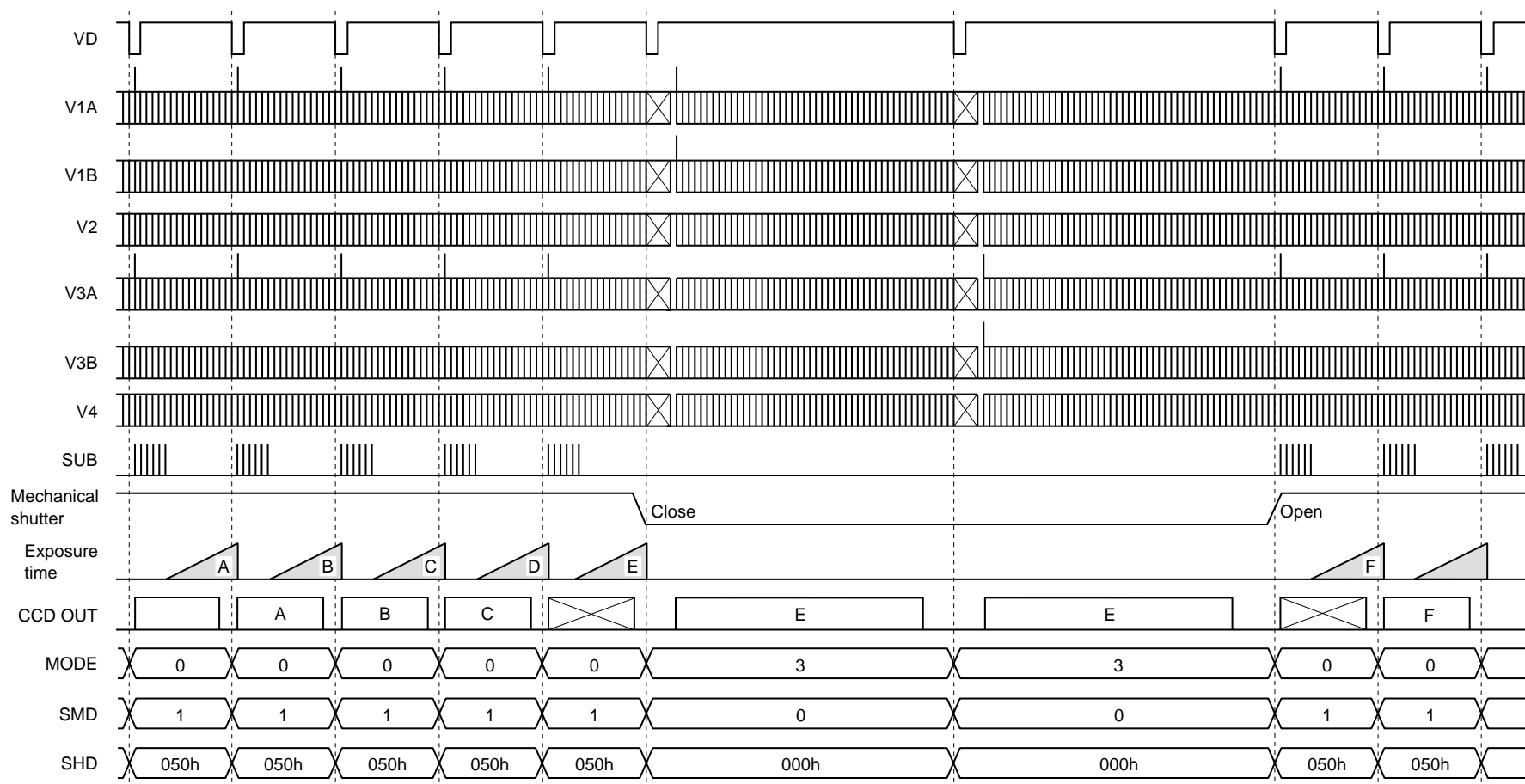
MODE

Draft → Frame → Draft

Applicable CCD image sensor

• ICX412

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\* This chart is a drive timing chart example of electronic shutter normal operation.

\* Data exposed at D includes a blooming component. For details, see the CCD image sensor data sheet.

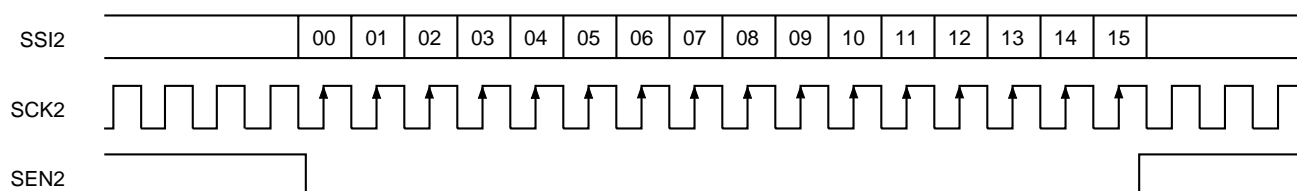
\* The CXD3412GA does not generate the pulse to control mechanical shutter operation.

\* The switching timing of drive mode and electronic shutter data is not the same.

## CCD Signal Processor Block Serial Interface Control

The CXD3412GA's CCD signal processor block basically loads the CCD signal processor block serial interface data sent in the following format at the rising edge of SEN2, and the setting values are then reflected to the operation 6 ADCLKI clocks after that.

CCD signal processor block serial interface control requires clock input to ADCLKI in order to load and reflect the serial interface data to operation, so this should normally be performed when the timing generator block is in the normal operation mode.



There are four categories of CCD signal processor block serial interface data: standby control data, PGA gain setting data, OB clamp level setting data, and input pulse polarity setting data.

Note that when data from multiple categories is loaded consecutively, the data for the category loaded last is valid and data from other categories is lost. When transferring data from multiple categories, raise SEN2 for each category and wait until the setting value 6 ADCKLI clocks after that has been reflected to operation, then transmit the next category.

The detail of each data are described below.

### Standby Control Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D14	FIXED	—	Set to All 0.	
D15	STB	Standby control	Normal operation mode	Standby mode

### PGA Gain Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04, D05	FIXED	—	Set to All 0.	
D06 to D15	GAIN	PGA gain setting data	See D06 to D15 GAIN.	



**OB Clamp Level Setting Data**

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D11	FIXED	—	Set to All 0.	
D12 to D15	OBLVL	OB clamp level setting data	See D12 to D15 OBLVL.	

**Input Pulse Polarity Setting Data**

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to 0.	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D12	FIXED	—	Set to All 0.	
D13 to D15	POL	Input pulse polarity setting data	Set to All 0.	

## Detailed Description of Each Data

### Shared data: **D01** to **D03** CTG [Category]

Of the data provided to the CXD3412GA by the CCD signal processor block serial interface, the CXD3412GA loads **D04** and subsequent data to each data register as shown in the table below according to the combination of **D01** to **D03**.

D01	D02	D03	Description of operation
0	0	0	Loading to standby control data register
0	0	1	Loading to PGA gain setting data register
0	1	0	Loading to OB clamp level setting data register
0	1	1	Loading to input pulse polarity setting data register
1	X	X	Access prohibited

### Standby control data: **D15** STB [Standby]

The operating mode of the CCD signal processor block is switched as follows. When the CCD signal processor block is in standby mode, only the serial interface is valid.

D00	Description of operation
0	Normal operating mode
1	Standby mode

### PGA gain setting data: **D06** to **D15** GAIN [PGA gain]

The CXD3412GA can set the programmable gain amplifier (PGA) gain from –6dB to +42dB in 1024 steps by using PGA gain setting data **D06** to **D15** GAIN.

The PGA gain setting data is expressed as shown in the table below using **D06** to **D15** GAIN.

MSB						LSB			
D06	D07	D08	D09	D10	D11	D12	D13	D14	D15
0	1	1	1	0	0	0	0	1	1
↓			↓				↓		
1			C				3		

GAIN is expressed as **1C3h**.

For example, when GAIN is set to "000h", "080h", "220h", "348h" and "3FFh", the respective PGA gain setting values are –6dB, 0dB, +20dB, +34dB and +42dB.

**OB clamp level setting data: [D12] to [D15] OBLVL [OB clamp output]**

The CXD3412GA can set the OPB clamp output value from 0 to 60LSB in 4LSB steps by using CCD signal processor block control data [D12] to [D15] OBLVL.

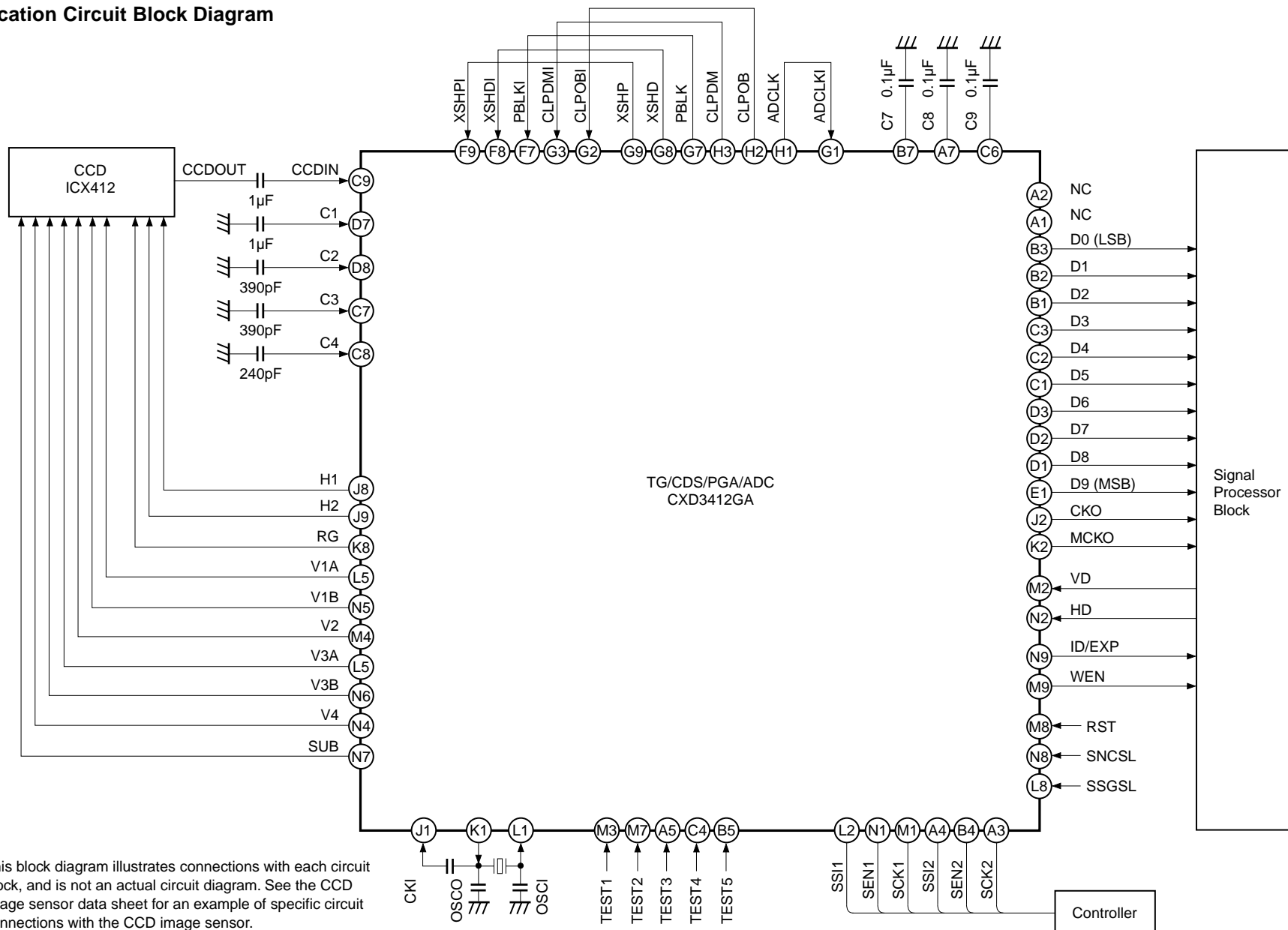
The OPB clamp output setting data is expressed as shown in the table below using [D12] to [D15] OBLVL.

MSB			LSB
D12	D13	D14	D15
0	1	1	0
		↓	
		6	

OBLVL is expressed as [6h].

For example, when OBLVL is set to "0h", "1h", "8h" and "Fh", the respective OPB clamp output setting values are 0LSB, 4LSB, 32LSB and 60LSB.

# Application Circuit Block Diagram

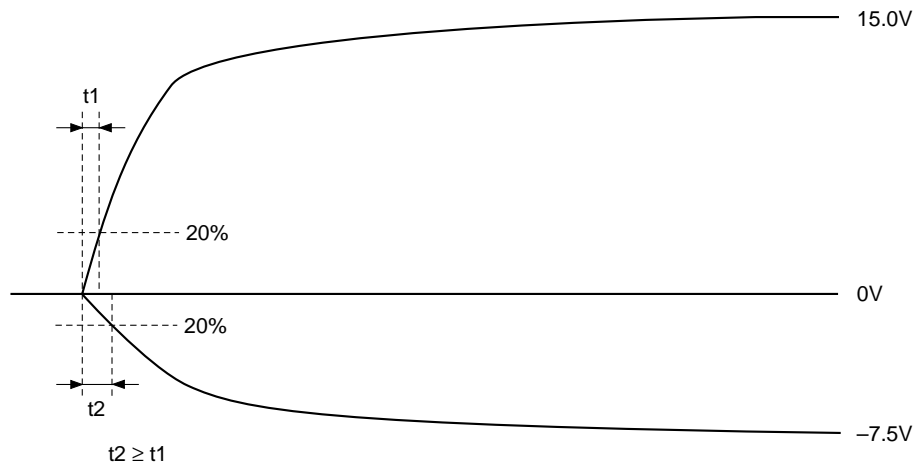


This block diagram illustrates connections with each circuit block, and is not an actual circuit diagram. See the CCD image sensor data sheet for an example of specific circuit connections with the CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

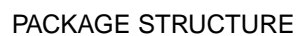
## Notes on Operation

1. Be sure to start up the timing generator block VL and VH pin power supplies at the timing shown in the figure below in order to prevent the SUB pin of the CCD image sensor from going to negative potential. In addition, start up the timing generator block VDD1, VDD2, VDD3, VDD4 and VDD5 pin and CCD signal processor block DVDD1, DVDD2, AVDD1, AVDD2, AVDD3, AVDD4 and AVDD5 pin power supplies at the same time either before or at the same time as the VH pin power supply is started up.



2. Reset the timing generator block and CCD signal processor block during power-on. The timing generator block is reset by inputting the reset signal to the RST pin. The CCD signal processor block is reset by initializing the serial data.
3. Separate the timing generator block VDD1, VDD2, VDD3, VDD4 and VDD5 pins from the CCD signal processor block DVDD1, DVDD2, AVDD1, AVDD2, AVDD3, AVDD4, and AVDD5 pins.  
Also, the ADC output driver stage is connected to the dedicated power supply pin DVDD1. Separating this pin from other power supplies is recommended to avoid affecting the internal analog circuits.
4. The difference in potential between the timing generator block VDD4 pin supply voltage 3 VDDC and the CCD signal processor block DVDD1, DVDD2, AVDD1, AVDD2, AVDD3, AVDD4 and AVDD5 pin supply voltages 1 VDDe, 2 VDdF and 3 VDdG should be 0.1V or less.
5. The timing generator block and CCD signal processor block ground pins should use a shared ground which is connected outside the IC. When the set ground is divided into digital and analog blocks, connect the timing generator block ground pins to the digital ground and the CCD signal processor block ground pins to the analog ground. The difference in potential between the timing generator block VSS1, VSS2, VSS3, VSS4, VSS5, VSS6 and VM and the CCD signal processor block DVSS1, DVSS2, DVSS3, AVSS1, AVSS2, AVSS3, AVSS4, AVSS5 and AVSS6 should be 0.1V or less.
6. Do not perform serial communication with the CCD signal processor block during the effective image period, as this may cause the picture quality to deteriorate. In addition, using SCK2, SSI2 and SEN2, which are used by the CCD signal processor block, use of the dedicated ports is recommended. When using these pins as shared ports with the timing generator block or other ICs, be sure to thoroughly confirm the effects on picture quality before use.

## Unit: mm



PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.3g