HT82V806
CCD 6 Channel Vertical Driver

Features
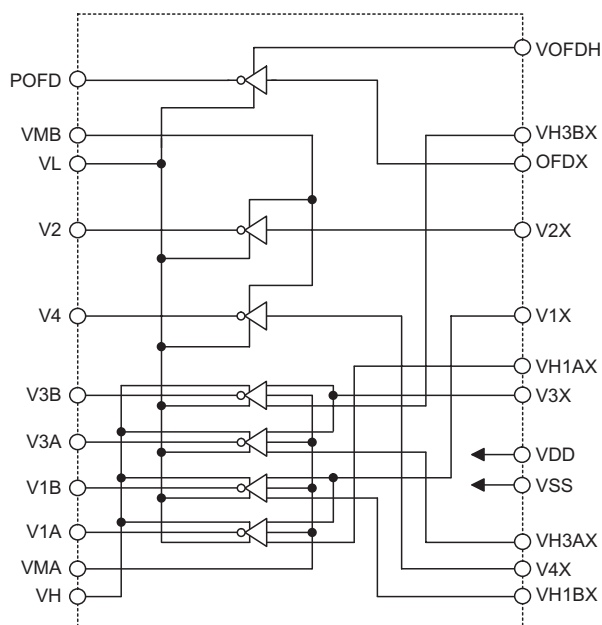
- Operating voltage: 3.0V~5.5V
- Built-in seven circuits
  - 2-level output:
    2 circuits for vertical CCD clock driver
    Output voltage level (typ.) = −9V to 0V
  - 3-level output:
    4 circuits for vertical CCD clock driver
    Output voltage level (typ.) = −9V to 15V
  - 2-level output:
    1 circuit for shutter driver
    Output voltage level (typ.) = −9V to 17V

- Switchable between NTSC (EIA) and PAL (CCIR) modes
- 24-pin SSOP (150mil) package
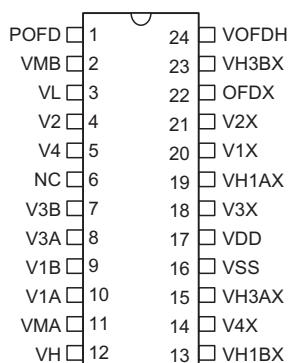
General Description

HT82V806 is a CMOS vertical clock driver and shutter driver IC for CCD area sensors. It has the capability of converting the voltage and impedance from the CMOS level.

Block Diagram

Pin Assignment

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            POFD  1       24  VOFDH
            VMB   2       23  VH3BX
            VL    3       22  OFDX
            V2    4       21  V2X
            V4    5       20  V1X
            NC    6       19  VH1AX
            V3B   7       18  V3X
            V3A   8       17  VDD
            V1B   9       16  VSS
            V1A  10       15  VH3AX
            VMA  11       14  V4X
            VH   12       13  VH1BX
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**HT82V806
－24 SSOP-A
(150mil)**

Pin Description

Pin No.	Pin Name	I/O	Description
1	POFD	O	Electronic shutter pulse output (High level=V_{OFDH}, low level=V_L)
2	VMB	—	Power supply for high level V2 and V4
3	VL	—	Power supply for all low level output pulses
4	V2	O	Pulse to drive vertical CCD shift register; Connect to V2
5	V4	O	Pulse to drive vertical CCD shift register; Connect to V4
6	NC	—	No connection
7	V3B	O	Pulse to drive vertical CCD shift register; Connect to V3B
8	V3A	O	Pulse to drive vertical CCD shift register; Connect to V3A
9	V1B	O	Pulse to drive vertical CCD shift register; Connect to V1B
10	V1A	O	Pulse to drive vertical CCD shift register; Connect to V1A
11	VMA	—	Power supply for intermediate level V1A, V1B, V3A and V3B
12	VH	—	Power supply for high level V1A, V1B, V3A and V3B
13	VHIBX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register.
14	V4X	I	Vertical transfer pulse input
15	VH3AX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register.
16	VSS	—	Negative power supply, ground
17	VDD	—	Positive power supply
18	V3X	I	Vertical transfer pulse input
19	VH1AX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register.
20	V1X	I	Vertical transfer pulse input
21	V2X	I	Vertical transfer pulse input
22	OFDX	I	Electronic shutter pulse input
23	VH3BX	I	Pulse that transfers the charge of the photo-diode to the vertical shift register.
24	VOFDH	—	Power supply for high level POFD

Absolute Maximum Ratings

Supply Voltage ....GND$-$0.3V to GND+6V

Input Voltage ....V$_{SS}$$-$0.3V to V$_{DD}$+34V

Storage Temperature ....$-$55°C to 150°C

Operating Temperature ....$-$25°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under ″Absolute Maximum Ratings″ may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{DD}$	Supply Voltage	3.0	3.3	5.5	V
V$_H$		—	15	—	
V$_L$		—	$-$9	—	
V$_{MA}$, V$_{MB}$		—	0	—	
V$_{OFDH}$		—	17	—	
V$_{IN}$ (LOW)	Input Voltage	0	—	0.3V$_{DD}$	V
V$_{IN}$ (HIGH)		0.7V$_{DD}$	—	V$_{DD}$	
NTSC	Operating Frequency	—	15.734	—	kHz
PAL		—	15.625	—	
T$_{OPR}$	Operating Temperature	$-$20	—	+70	°C

D.C. Characteristics

V$_H$=15V, V$_L$=$-$9V, V$_{MA}$=0V, V$_{MB}$=0V, V$_{OFDH}$=15V, Ta=25°C

Symbol	Parameter	Test Conditions V$_{DD}$	Test Conditions Conditions	Min.	Typ.	Max.	Unit
V$_{IL}$	Input Low Voltage	3.3V	—	0	—	0.3V$_{DD}$	V
V$_{IH}$	Input High Voltage	3.3V	—	0.7V$_{DD}$	—	V$_{DD}$	V
V$_{IL1}$	Input Low Current	3.3V	V$_{IL}$=0V	—	—	200	μA
V$_{IH1}$	Input High Current	3.3V	V$_{IH}$=3.3V	—	—	1	μA
V$_{OL}$	Output Low Voltage	3.3V	I$_{OL}$<1μA	—	—	$-$8.9	V
V$_{OMLa}$	Output Intermediate Voltage	3.3V	I$_{OMLa}$<1μA		—	0.1	V
V$_{OMHa}$			I$_{OMHa}$<1μA		—	0.1	V
V$_{OMLb}$			I$_{OMLb}$<1μA		—	0.1	V
V$_{OMHb}$			I$_{OMHb}$<1μA		—	0.1	V
R$_{ONH}$	Output ON Resistance	3.3V	I$_{OH}$=20mA	—	30	—	Ω
R$_{ONOFH}$			I$_{OFDH}$=20mA	—	20	—	Ω
R$_{ONM}$			I$_{OM}$=20mA	—	25	—	Ω
R$_{ONL}$			I$_{OL}$=20mA	—	20	—	Ω
I$_{DD}$	Static Current	3.3V	—	—	—	2.0	μA
I$_H$				—	—	200	μA
I$_{OFDH}$				—	—	200	μA
I$_M$				—	—	200	μA
I$_L$				—	—	200	μA

A.C. Characteristics

V_H=15V, V_L=−9V, V_{MA}=0V, V_{MB}=0V, V_{OFDH}=15V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{TRM} ($V_L{\rightarrow}V_M$)		3.3V	V_{IN} to V_M (V_{1A}, V_{1B}, V_2, V_{3A}, V_{3B}, V_4)	—	430	900	ns
t_{TFL} ($V_M{\rightarrow}V_L$)		3.3V	V_{IN} to V_L (V_{1A}, V_{1B}, V_2, V_{3A}, V_{3B}, V_4)	—	370	800	ns
t_{TRH} ($V_M{\rightarrow}V_H$)	Sequential Delay	3.3V	V_{IN} to V_H (V_{1A}, V_{1B}, V_{3A}, V_{3B})	—	550	1100	ns
t_{TFM} ($V_H{\rightarrow}V_M$)		3.3V	V_{IN} to V_M (V_{1A}, V_{1B}, V_{3A}, V_{3B})	—	630	1300	ns
t_{TROFDH} ($V_L{\rightarrow}V_{OFDH}$)		3.3V	V_{IN} to V_{OFDH} (POFD)	—	70	140	ns
t_{TFOFDL} ($V_{OFDH}{\rightarrow}V_L$)		3.3V	V_{IN} to V_L (POFD)	—	60	120	ns

Timing Diagrams
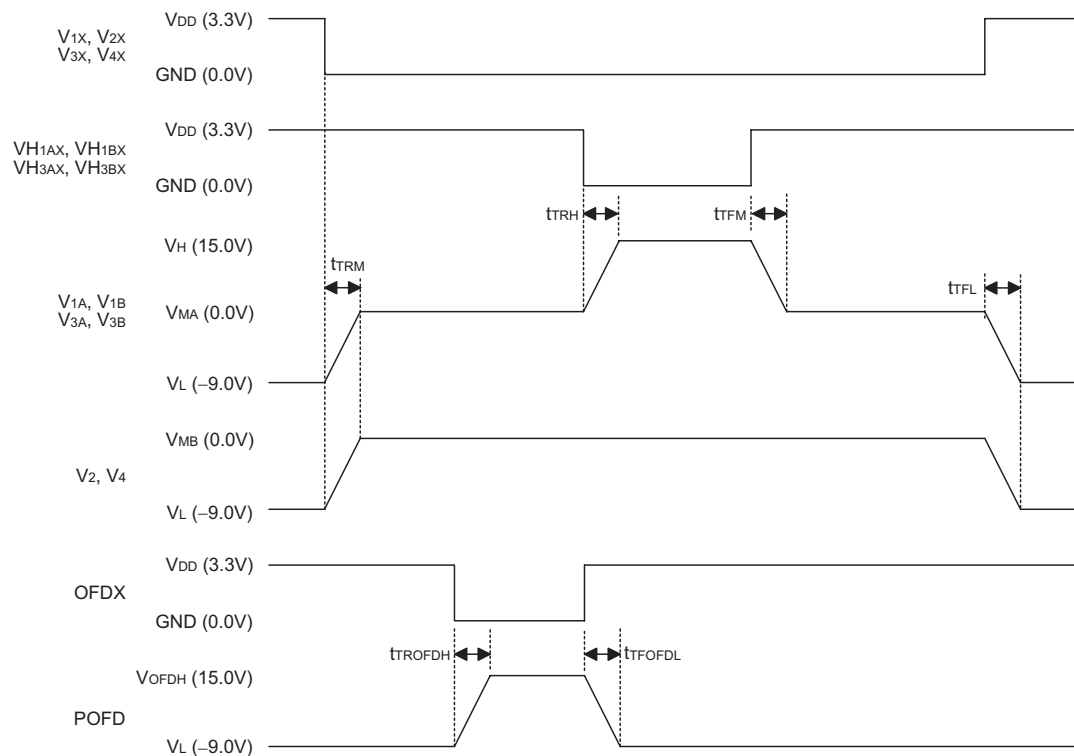
Application Circuits

Equivalent Circuits

While V_{1A} and V_{3A} (or V_{1B} and V_{3B}) are measured, V_{1B} and V_{3B} (or V_{1A} and V_{3A}) are open.

R_1 to $R_4 = 27\Omega$
$RG = 5\Omega$
C_1 to $C_4 = 3300pF$
$C_{12}, C_{23}, C_{34}, C_{41} = 1500pF$

CSUB=500pF
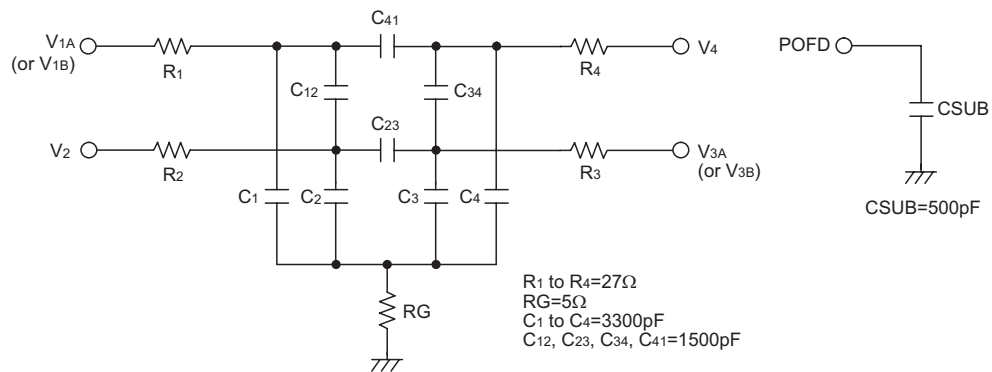
Package Information

24-pin SSOP (150mil) Outline Dimensions
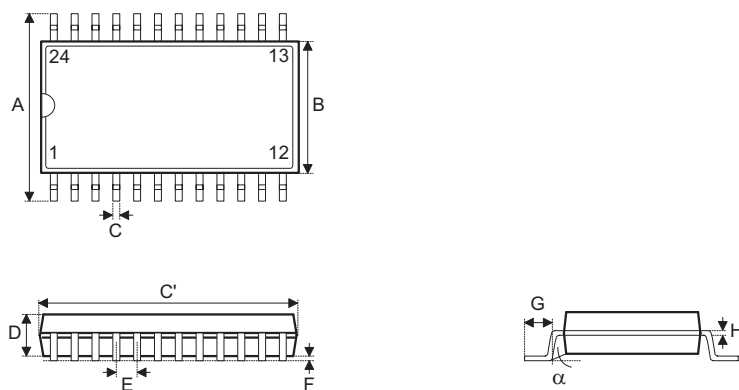
Symbol	Dimensions in mil		
	Min.	**Nom.**	**Max.**
A	228	—	244
B	150	—	157
C	8	—	12
C′	335	—	346
D	54	—	60
E	—	25	—
F	4	—	10
G	22	—	28
H	7	—	10
α	0°	—	8°

Product Tape and Reel Specifications

Reel Dimensions
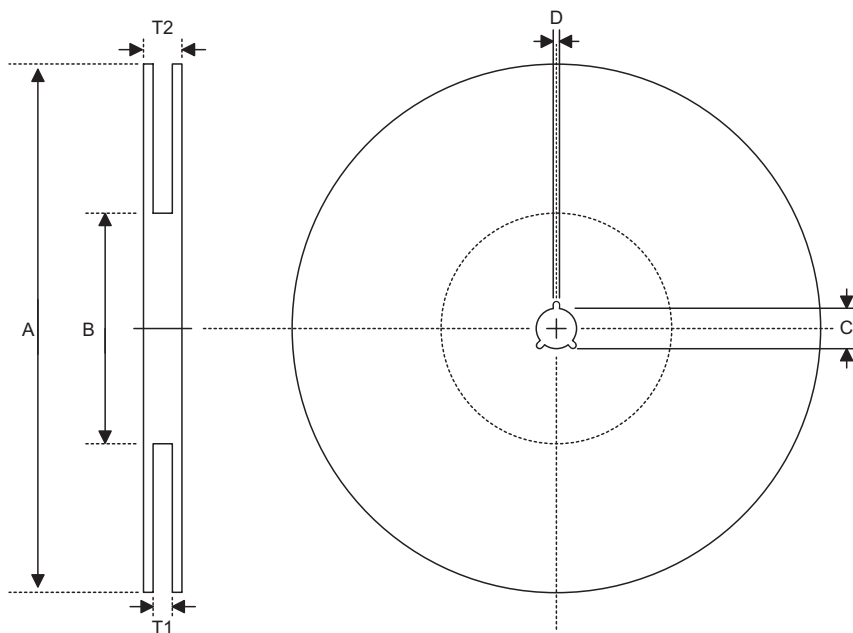
SSOP 24N (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8+0.3 −0.2
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions
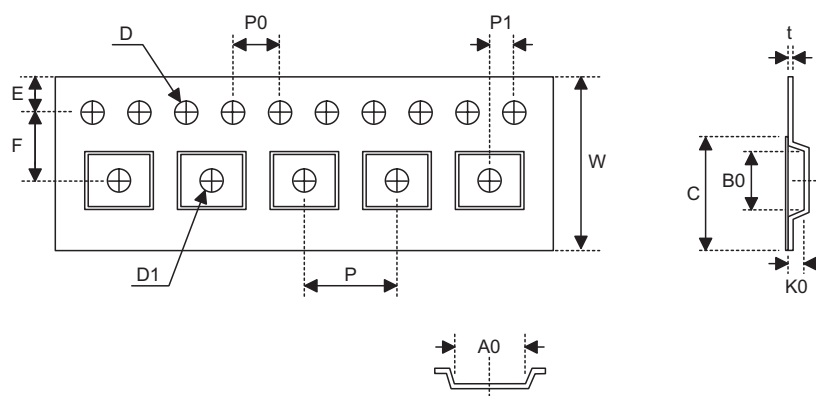
SSOP 24N (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0+0.3 −0.1
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	8.2±0.1
B0	Cavity Width	8.6±0.1
K0	Cavity Depth	3.0±0.1
t	Carrier Tape Thickness	0.35±0.05
C	Cover Tape Width	13.3