Wireless IC Design - Final Project Report

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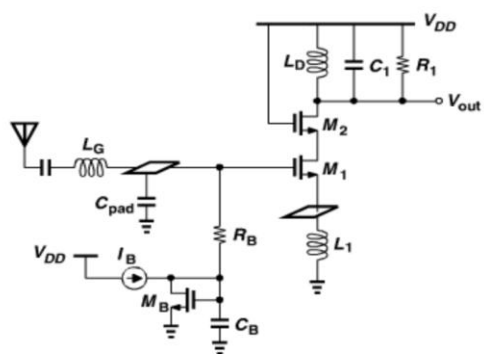
1. LNA Topology

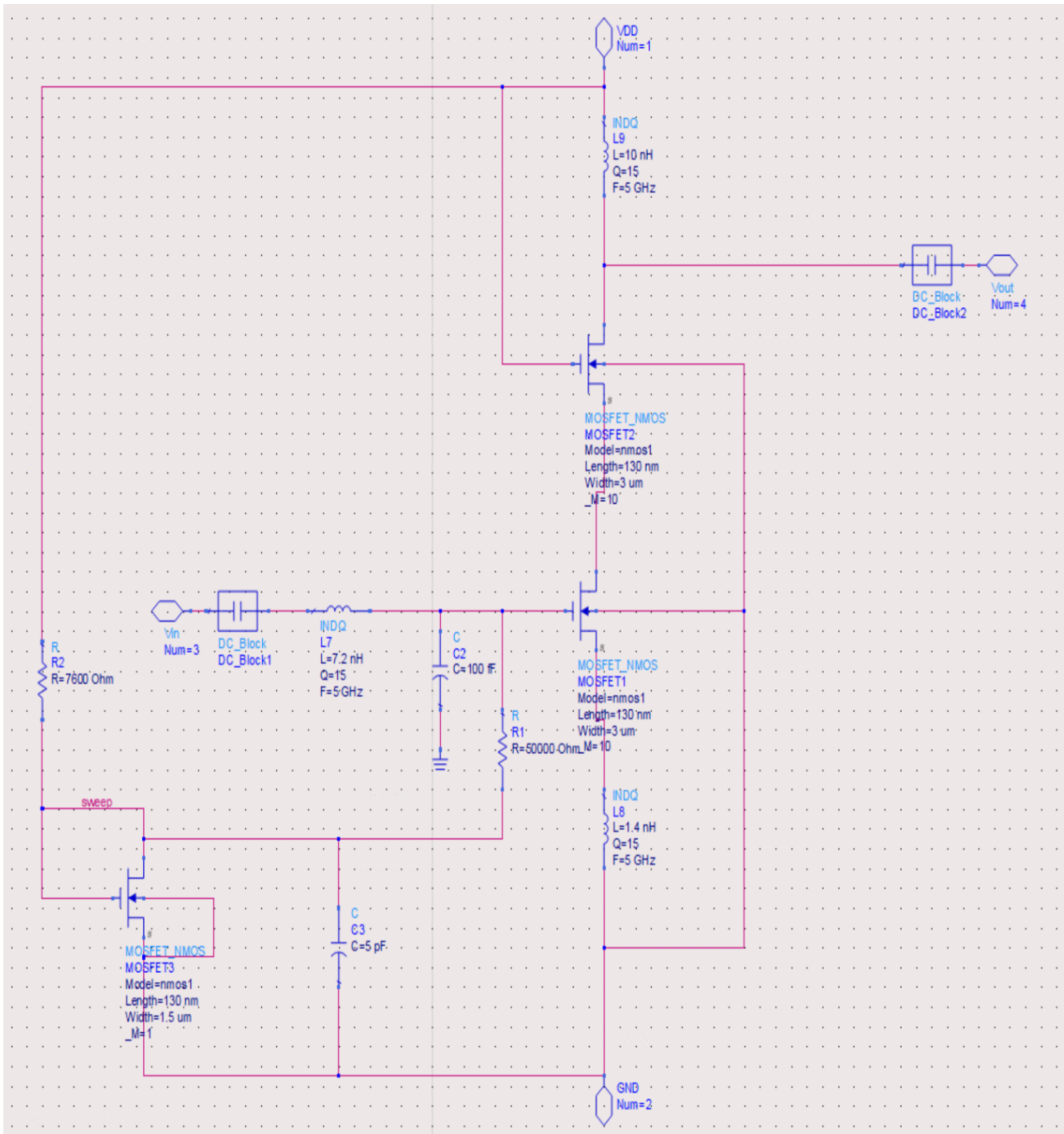
The targeted LNA for this project is a Cascode Common Source stage with Inductive degeneration. The LNA is a single stage amplifier. The inductive source degeneration allows for a good tradeoff between the input matching and the NF of the circuit, since the current noise contribution of the driving transistor appears to be smaller at the output. Furthermore, the cascode configuration improves the stability of the LNA because it creates some isolation between the output and the input. In order to match the LNA to 50 ohm, we placed a pad capacitor in order to have life-like inductor values that can be implemented using bonding wires. The schematic of the designed LNA is shown in the figure below. LG and L1 are used for the input matching transformation. MB is used to bias the gate of M1 to the desired DC gate voltage. LD was selected to resonate the output capacitance.



2. Desired Specs and Achieved Specs

	Specs	Simulated Performance
DC current	<7.5mA	2.416mA
|S11|	<-10dB	-41.19
Peak Voltage Gain	20dB	21.4dB
Bandwidth	200MHz	780MHz
Noise Figure	3dB	1.688
IP_{1dB}	-25dBm	-12.75dBm
P_{IIP3}	-15dBm	-2.99dBm
Total Inductance	<20nH	18.6nH

3. **Schematic of the Inductively Degenerated Cascode LNA including the biasing circuit.**

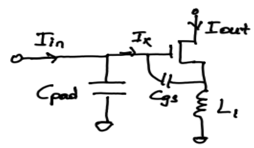


4. **NF:**

In order to calculate the NF of this topology, we must take into consideration the the fT of the MOSFET 1 (which appears in the NF figure formula of the Inductively Degenerated Cascode LNA) changes because of the added capacitance C2. To account for that, the following derivation was performed. By doing the following derivations, and by knowing the transistors parameters from ADS, we were able to hand calculate the fT of the loaded transistor to be 13MHz. We did find the H21 parameter of the loaded nmos to be 0dB at around 14MHz in ADS. This change in the fT may happen for different reasons. The main reason is that we assumed the Cgd capacitance is very small, and it does not affect the fT.

f_T and NF calculation

$$NF = 1 + g_m \gamma R_s \left(\frac{f_0}{f_T}\right)^2 + \frac{4 \cdot R_s}{R_1}\left(\frac{f_0}{f_T}\right)^2$$



The f_T has changed because of the presence of Cpad.

$$\Rightarrow Z_{pad} = \frac{1}{sC_{pad}}$$

$$Z_{in} = Z_{gs} + Z_s + \omega_T' \cdot L_1$$

$$\omega_T' = \frac{g_m}{C_{gs}} \rightarrow \text{unloaded Mosfet } \omega_T.$$

$$\Rightarrow I_x = \frac{Z_{pad} \cdot I_{in}}{Z_{in} + Z_{pad}}$$

$$\Rightarrow I_{out} = g_m \cdot I_x \cdot Z_{gs} = g_m \cdot Z_{gs} \cdot \frac{Z_{pad}}{Z_{pad} + Z_{in}} \cdot I_{in}$$

$$\Rightarrow \frac{I_{out}}{I_{in}} = g_m Z_{gs} \cdot \frac{Z_{pad}}{Z_{pad} + Z_{in}} \Rightarrow \text{At } \omega_T \quad \frac{I_{out}}{I_{in}} = 1$$

$$\Rightarrow g_m \cdot \frac{1}{j\omega C_{gs}} \cdot \frac{\frac{1}{jC_{padd} \cdot \omega}}{\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{pad}} + j\omega L_1 + \omega_T' L} = 1$$

we need to solve this equation for ω. We used MatLab

$$\left.\begin{aligned} C_{gs} &= 15fF \\ g_m &= 27.7mS \\ C_{padd} &= 100fF \\ L_1 &= 1.4nH \end{aligned}\right\} f_T = 13\ MHz$$

For $\gamma = 2$, $R_S = 50\Omega$, $R_1 = 200\Omega$

$$\underline{NF = 1.557 = 1.92\,dB}$$

We assumed a value of 2 for lambda, assuming this is one of the short technology nodes. Although this is only a 130nm process node, the gamma value should not be this high but just for first order calculations, we assumed it to be 2. So, the calculated NF = 1.557 or 1.92dB. The value that we took from the simulator was 1.688. I think this is coming because of the small difference that we have on the fT calculation and the unknown value of gamma. I think the major contributor comes from the assumed value of gamma. The cascode transistor is not included in the calculation because it’s source is degenerated.

Input matching:
CGS1 = 15 fF
Cpad = 100 fF
Solving the two equations shown in the figure below, we calculated the values of LG and L1.
LG = 7.2 nH
L1 = 1.4 nH
S11 = -31 dB

$$\frac{1}{(L_G+L_1)(C_{GS1}+C_{pad})} = \omega_0^2$$

$$\Rightarrow \frac{1}{(7.2\times10^{-9}+1.4\times10^{-9})\left(100\times10^{-15}+\frac{27m}{250\times10^{9}\times2\pi}\right)} = 9.92\times10^{20} = (31.5\times10^{10})^2 = (2\pi\times5.01\times10^{9})^2$$

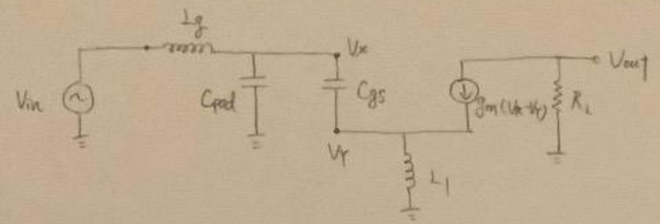
$$\left(\frac{C_{GS1}}{C_{GS1}+C_{pad}}\right)^2 L_1\,\omega_T = R_S$$

$$\Rightarrow \left(\frac{27m/250G\times2\pi}{27m/250G\times2\pi+100f}\right)^2 \times 1.4\times10^{-9} \times 2\pi\times250\times10^{9} = 47.31$$

Gain:

For the gain calculation, we had to firstly calculate the inductor value which resonates the output capacitance. Assuming the output capacitance node is dominated by the capacitance of the load, we calculated an LD of 10nH to be enough to resonate the output node at 5 GHz. The quality of the inductor was 15, so the parallel Rp = Q*w*LD = 15*2*pi*5G*10n = 4.7k ohm. Rp >> RL, thus we are not considering its effect on the gain calculation. Also, the output cascode resistance is quite high because the source of the cascode transistor is degenerated, thus leading to a high impedance at the output. It was for these reasons why we assumed the output impedance to be 200 ohms. Please find below how we calculated the theoretical gain. Theoretical gain is very close to the simulated one.

Gain Caculation



$$\begin{cases} \dfrac{V_{in}-V_X}{sL_g} = sC_{pad}V_X + (V_X-V_Y)sC_{gs} \\ sC_{gs}(V_X-V_Y) + g_m(V_X-V_Y) = \dfrac{V_Y}{sL_1} \end{cases}$$

$$\Rightarrow (sC_{gs}+g_m)V_X = \left(sC_{gs}+g_m+\frac{1}{sL_1}\right)V_Y$$

$$\Rightarrow V_X = \frac{s^2C_{gs}L_1 + sg_mL_1 + 1}{s^2C_{gs}L_1 + sg_mL_1} V_Y$$

$$\frac{V_{in}}{sL_g} = V_X\left(\frac{1}{sL_g} + sC_{pad} + sC_{gs}\right) - sC_{gs}V_Y$$

$$= \frac{s^2C_{gs}L_1 + sg_mL_1 + 1}{s^2C_{gs}L_1 + sg_mL_1}\left(\frac{1}{sL_g} + sC_{pad} + sC_{gs}\right)V_Y - sC_{gs}V_Y$$

$$\Rightarrow V_Y = \frac{V_{in}}{sL_g} \times \frac{s^2C_{gs}L_1 + sg_mL_1}{(s^2C_{gs}L_1 + sg_mL_1 + 1)(sC_{gs} + sC_{pad} + \frac{1}{sL_g}) - sC_{gs}(s^2C_{gs}L_1 + sg_mL_1)}$$

$$(V_X - V_Y)g_mR_L = \left(\frac{\cancel{s^2C_{gs}L_1} + \cancel{sg_mL_1} + 1 - \cancel{s^2C_{gs}L_1} - \cancel{sg_mL_1}}{s^2C_{gs}L_1 + sg_mL_1} - 1\right)V_Y\, g_mR_L$$

$$= g_mR_L \times \left(\frac{1}{s^2C_{gs}L_1 + sg_mL_1} - 1\right) \times \frac{V_{in}}{sL_g} \times \frac{s^2C_{gs}L_1 + sg_mL_1}{(s^2C_{gs}L_1 + sg_mL_1 + 1)(sC_{gs} + sC_{pad} + \frac{1}{sL_g}) - sC_{gs}(s^2C_{gs}L_1 + sg_mL_1)}$$

$\omega = 2\pi \times 5 \times 10^9$ $\quad L_g = 7.2\,nH$

$R_L \cong 200$ $\quad L_1 = 1.4\,nH$ $\quad \Rightarrow$ using Matlab to calculate

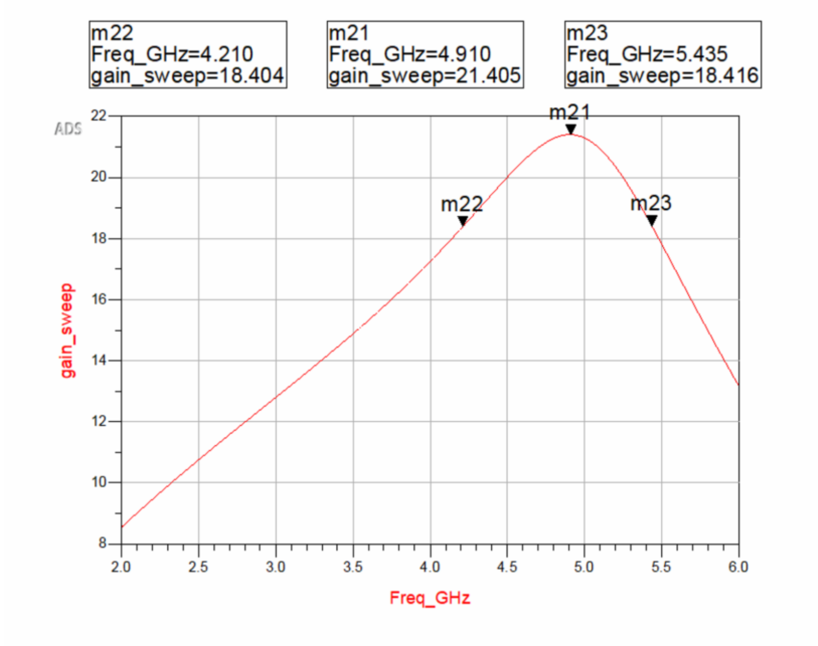
$C_{gs} \approx 15 \times 10^{-15} F$ $\quad \Rightarrow \dfrac{V_{out}}{V_{in}} \approx -8.23 - 20.27i \Rightarrow \left|\dfrac{V_{out}}{V_{in}}\right| \approx 21.88$

$C_{pad} = 100\,fF$

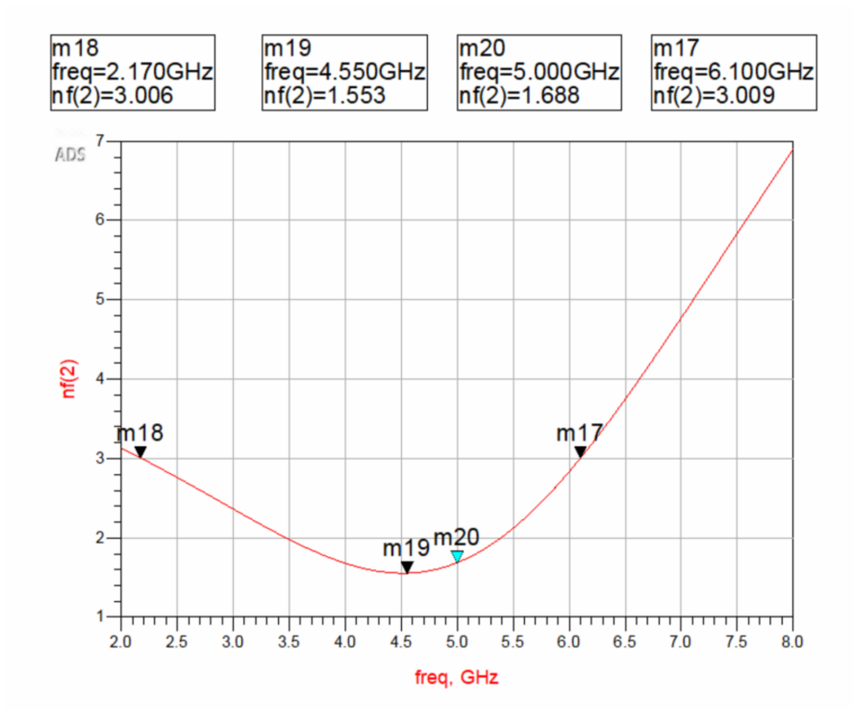
$$\Rightarrow \text{Gain} = \frac{1}{2} \times \left|\frac{V_{out}}{V_{in}}\right| = 10.94 = 20.78\,dB$$

5. Simulated Values

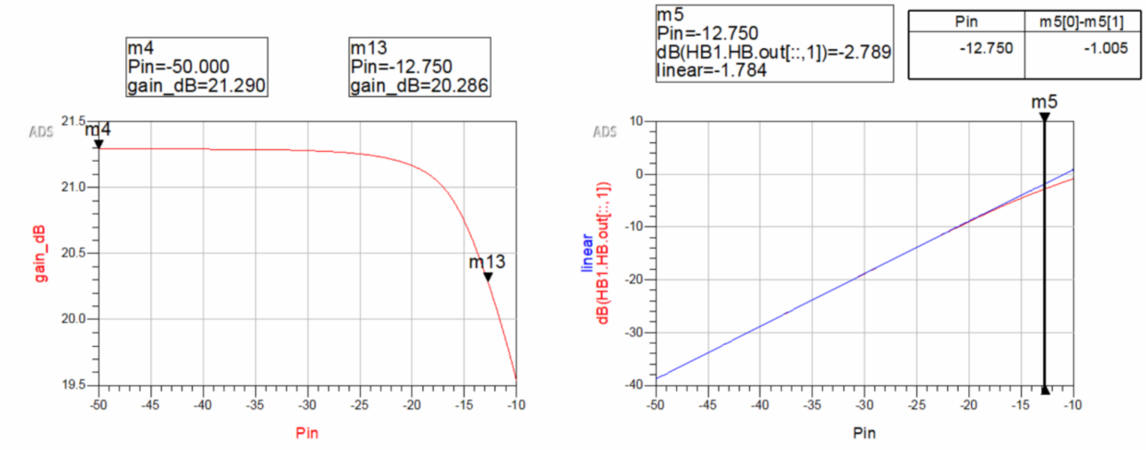
Gain Plot: -3dB Bandwidth 4.21GHz - 5.435GHz



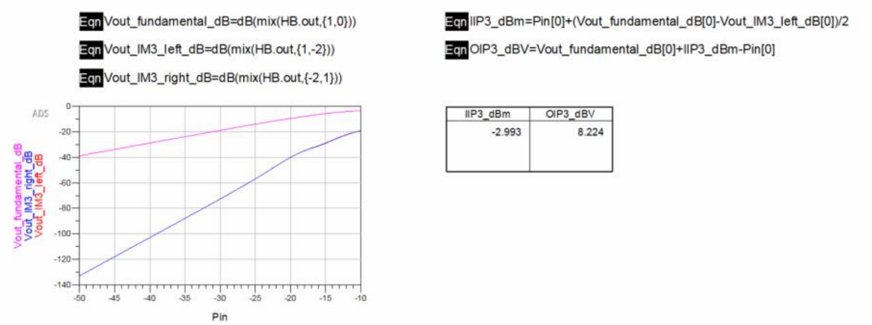
Noise Figure Plot



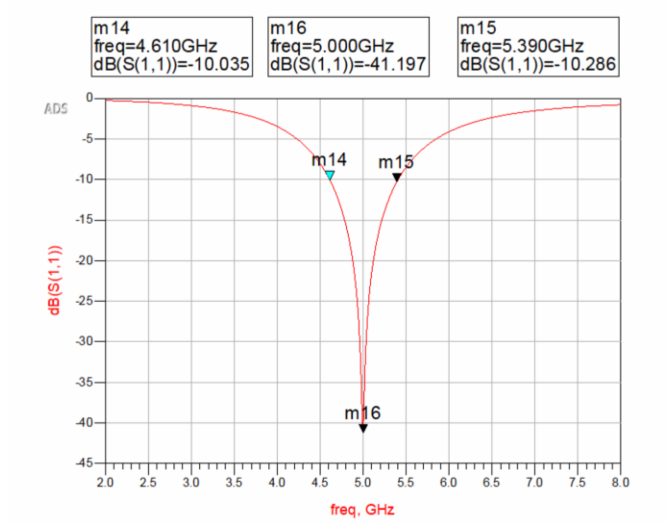
IP1dB: The calculated IP1dB = -12.75dBm



IIP3_dBm: The measured IIP3_dBm = -2.99 dBm



S11: The bandwidth of S11 4.6GHz - 5.39GHz. This is also the bandwidth of the LNA.



6. Performance comparison

Parameters	Hand-Calculated	Simulated
NF	1.92 dB	1.66 dB
Gain	20.8 dB	21.4 dB
Input Resistance	47.3 ohms	50.8 ohms

The big change in the NF I think happens because of the assumed gamma value for the 130nm process.

The calculated and simulated values of Gain and Input Resistance are very close to each other. Minor differences happen because of device non-idealities.

$$FoM = \frac{10^{\frac{21.4}{20}} \times 10^{\frac{-12.75}{10}} \times 780M}{1.2 \times 2.416 \times (10^{\frac{1.688}{10}} - 1) \times 5G} \times 10^{6} = 70653$$