ISTANBUL TECHNICAL UNIVERSITY
ELECTRICAL-ELECTRONICS FACULTY

DESIGN OF A FAST PLL IN CMOS

SENIOR DESIGN PROJECT

Gerald TOPALLI
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Gerald TOPALLI
(040160911)

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(040160912)

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İSTANBUL TEKNİK ÜNİVERSİTESİ
ELEKTRİK-ELEKTRONİK FAKÜLTESİ

CMOS'DA HIZLI PLL TASARIMI

LİSANS BİTİRME TASARIM PROJESİ

Gerald TOPALLI
(040160911)

Kamela DOKAJ
(040160912)

Proje Danışmanı: Prof. Dr. Nil TARIM

ELEKTRONİK VE HABERLEŞME MÜHENDİSLİĞİ BÖLÜMÜ

TEMMUZ, 2018

We are submitting the Senior Design Project Report entitled as “DESIGN OF A FAST PLL IN CMOS”. The Senior Design Project Report has been prepared as to fulfill the relevant regulations of the Electronics and Communication Engineering Department of Istanbul Technical University. We hereby confirm that we have realized all stages of the Senior Design Project work by ourselves and we have abided by the ethical rules with respect to academic and professional integrity .

Name SURNAME	**Gerald TOPALLI**.
(Student ID)	040160911
Name SURNAME	**Kamela DOKAJ**.
(Student ID)	040160912

FOREWORD

As students of Electronic and Communication engineering we found it meaningful and practically important to do our thesis on a very important electronic component that is also very useful in communication field. We would like to thank Prof. Dr. Nil Tarim for her help and guidance as our adviser during our work for the senior project "DESIGN OF A FAST PLL IN CMOS". Also, we greatly appreciate and thank Ali Doğuş Güngördü for being especially helpful in the Cadence realization of the project. It is our greatest hope that our project takes even one step further in the PLL design.

July 2020

Gerald TOPALLI
Kamela DOKAJ

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ABBREVIATIONS

PLL **:** Phase Locked Loop

VCO **:** Voltage Controlled Oscillator

PID **:** Proportion-Integral Derivative

PD **:** Proportional Derivative

PFD **:** Phase Frequency Detector

TSMC **:** Taiwan Semiconductor Manufacturing Company

OTA **:** Operational Transconductance Amplifier

FD **:** Frequency Divider

LF **:** Loop Filter

CP **:** Charge Pump

SYMBOLS

C	**:** Capacitance
R	**:** Resistance
W	**:** Width
L	**:** Channel length
L	**:** Inductor
t	**:** Time
μ	**:** electron mobility
Cox	**:** Oxide Capacitance
Vov	**:** Voltage Overdrive
φ	**:** Phase
ζ	**:** dumping factor
ω	**:** freq in rad
τ	**:** time constant

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DESIGN OF A FAST PLL IN CMOS

SUMMARY

In this project we tried to design a fast PLL using 180nm CMOS technology firstly by optimizing the main block (basic PLL) and then by adding the controller, which is a PD controller with the function of controlling the error between the two input signals so that the inputs become closer (in phase) to each other. This is helpful in the PLL settling time since helps the main block reach the phase matching. Designing the PLL in such a way that it has a good settling time as a main block and also such that the current injected by the controller is properly implemented is crucial. The PLL blocks are: PFD (Phase frequency detector), Charge Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO) and Frequency Detector. Each of this components was analyzed, researched and designed carefully to optimize the performance. The optimizaton process was a process of setting the required parameters for each of the components and then optimize for them while keeping the nonimportant parameters to accepted values. This work was done individually for each component. In PFD the right detection of the difference between the inputs was the important parameter, while making sure that each state of the inputs was recognised and properly dealt. The charge pump had to take this difference and produce a current representing it while properly mirroring the input differences. In charge pump you can model the difference of inputs (or merely UP and DOWN signals in our case) such that it shapes a voltage in the required way for the VCO input. The current to voltage transition needed here is achieved by using the loop filter which at the same time filters the signal to further regulate the input of the VCO. Because the design in this part is very dynamic this part was dealt roughly by using simulation results to optimize. This part's operation is not easily predictable due to the dynamism of the charging and discharging of the capacitors and the loop filter. That is why adding the injected current from the PD controller at the loop filter is actually rather troublesome and the reason why it was difficult to get good results in reality, even though the theoritical part shows this implementation method of PID PLL to be successful. The frequency divider is the easiest circuit just designed by adding multiple stages of a D-Flip Flop and connecting the consecutive stages properly. Since we designed the VCO for 2.4 GHz output frequency we needed a 128 division to match with the frequency of the input. That is

done by 7 stages of division by two blocks. For the controller we followed the design which will be shown later in the report. The most important block of the controller is the OTA (Operation Transconductane amplifier) which is the building block for 3 of the components of the controller. Its design was rather focused in achieving a required gm annd current. The OTAs used in the design had slight changes fitting to their purpose in the circuit, which is the required gm. Except for the main controller parts which are : 1st Order Filter, PD controller and V/I converter (whose output is the current to be injected to the loop filter) we have a second block which checks some condition and decides accordingly if the current from the main controller block should be injected or not. This way we avoid the situation where the controller damages the PLL performance or adds noise to it. This secondary block is: Comparator, Finite state machine, and switch. Adding a PD controller, significantly reduced the settling time of PLL proving that the proposed PID PLL circuit is valid.

CMOS'DA HIZLI BIR PLL TASARIMI

ÖZET

Bu projede, önce ana bloğu (temel PLL) optimize ederek ve ardından iki giriş sinyali arasındaki hatayı kullanan bir PID kontrolörü ekleyerek, 180nm CMOS teknolojisini kullanarak hızlı bir PLL tasarlamaya çalıştık. Bu kontrolör giriş sinyaleri birbirine daha yakın (faz halinde) olması için değiştirilmesi gereken yönu buluyor ve boyle hatayi azaltırıyor. Ana bloğun faz eşleşmesine ulaşmasına yardımcı olduğundan, bu PLL çöktürme süresini azaltır. PLL'yi ana blok olarak iyi bir çökelme süresine sahip olmasi gerekir ve ayrıca kontrolör tarafından enjekte edilen akımın düzgün şekilde uygulanacağı şekilde tasarlanması çok önemlidir. PLL blokları şunlardır: PFD (Faz frekans dedektörü), Şarj Pompası, Döngü Filtresi, VCO(Voltaj Kontrollü Osilatör) ve Frekans Dedektörü. Bu bileşenlerin her biri, performansı optimize etmek için dikkatle analiz edildi, araştırıldı ve tasarlandı. Optimizasyon işlemi, bileşenlerin her biri için önemli olmayan parametreleri kabul edilen değerlerde tutarken, onemli parametreleri ayarlandi ve optimize edildi .

Bu çalışma'da her bileşen için ayrı ayrı çalışıldı. PFD'de, önemli olan girişler arasındaki farkın doğru tespit edilmesiydi ve girişlerin her durumu uygun şekilde tanımakti. Şarj pompası bu farkı almalı ve doğru şekilde onu temsil eden bir akım üretmelidir. Şarj pompası, girişlerin farkını (veya bizim durumumuzda sadece UP ve DOWN sinyalleri), VCO girişi için gereken şekilde bir voltajı uretmelidir. Burada gereken akım-voltaj geçişi, aynı zamanda VCO'nun giriş sinyalini daha fazla düzenlemek için döngü filtresi kullanıyoruz. Bu bölümdeki tasarım çok dinamik olduğu için, bu bölümü optimize etmek için simülasyon sonuçları analiz edildi . Bu parçaların çalışması, kapasitörlerin ve döngü filtresinin şarj ve deşarj dinamizmi nedeniyle kolayca dengelemez ve gerekli sonuc alamaz. Bu nedenle, enjekte edilen akımı buraya eklemek oldukça zordur ve teorik olarak PID'nin bu uygulama yönteminin başarılı olduğunu rağmen, gerçekte iyi sonuçlar almanın zordur.

Frekans bölücü, bir D-Flip Flop'un birçok aşamasını ekleyerek ve ardışık aşamaları doğru şekilde bağlayarak, tasarlanan en kolay devredir. VCO'yu 2.4 GHz çıkış frekans ıle tasarladığımız için, giriş frekansıyla eşleşmesi için 128 ile bölmek gerekliydi. Bu, ikiye bölen 7 bloklarla yapılır.

Kontrolör için daha sonra raporda gösterilecek tasarımı takip ettik. Buradaki en önemli blok, kontrolörün bileşenlerinden 3'ünün yapı taşı OTA'dır. Bu bileşenin tasarımı, gerekli bir gm ve akım elde etmeye odaklanmıştır. Tasarımda kullanılan OTA'lar, gerekli gm olan devrede amaçlarına uygun küçük değişiklikler yapildi. Aşağıdaki ana kontrolör parçaları hariç: 1.Order Filtresi, PD kontrolör ve V / I dönüştürücü (bu bileşenin çıkış akımı PLL-e enjekte edilecek), bazı koşulları kontrol ederek ana kontrolör bloğundan gelen akımın eğer enjekte edebilir karar veren baska bir blok var. Bu şekilde kontrolörün PLL performansına zarar verdiği veya gürültü eklenmiyor. Bu ikincili blok: Comparator, FSM ve Switch. Sonuç olarak, PID kontrolör kullanarak ve V/I Converter'in çikiş akımını enjekte ederek PLL'in çöktürme süresi azaltı.

1. INTRODUCTION

1.1 Designing a fast PLL

The synthesis of a frequency related to some input frequency has always been a very big challenge in Communication Engineering. The need to tune the input frequency with output frequency is very important in communication receivers and transmitters. Scaling the output frequency with regard to input frequency is a very old problem which has been observed for decades by mechanical engineers and is mostly solved by using mechanical gear systems. Gear systems have been a very elegant solution for frequency scaling in mechanical systems but this is a much greater problem in electronic systems. Many different solutions have been proposed to solve the frequency tuning problem but only few of them are efficient enough to be used in practice. The PLL is one of the most important circuits in phase matching. If two signals are in phase that means that their frequencies are equal. For a sinusoidal signal, frequency is the first derivative of phase with respect to time. This means that if phases are equal, the frequencies are equal also. Mainly, the PLL block is comprised of 4 blocks which are the PD, LF, VCO and FD. The general PLL circuit is shown in (Figure 1.1).

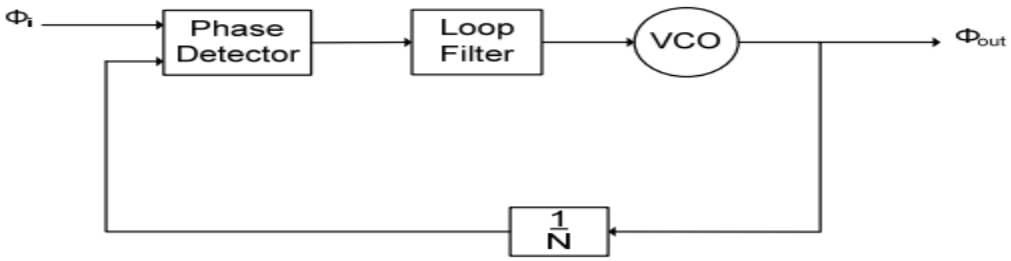

Figure 1.1: PLL block diagram.

Since the target PLL for this project is supposed to work for communication systems, the settling time, phase noise and power are of primary concern. There are a lot of aspects that a designer should be taking under consideration when designing a PLL for low settling time like higher currents in the CP circuit, higher bandwidth etc. But

higher current in CP will mean higher power consumption and higher capacitances used in the LF. Higher bandwidth would mean higher noise contribution. All these aspects should be taken under consideration when desiging a PLL. In order to overcome these problems different practical techniques are utilized.

1.2 Literature Review

One of the most used communication blocks for frequency tuning is Phase Locked Loop (PLL). PLL works under the concept of feedback. In 1927, Harold Stephen Black had the idea of implementing feedback in electronic circuits. His idea was very ingenious and it is used extensively nowadays in electronics. PLL as a circuit is able to produce an output waveform which is in-phase with the input signal. The first appearance of PLL dates back to 1932 when a Homodyne or direct-conversion receiver was produced. In the Homodyne circuits, one oscillator was tuned to the desired frequency but it was seen that the local oscillator frequency was not stable. At this point the Black's idea was utilized to create a circuit which would be able to keep the frequency intact. Engineers proposed to create some circuit that would be able to compare the phase difference between input and output of the device and to control the oscillation frequency depending on the amount of phase difference between the two signals. This circuit was called a Phase Locked Loop because the circuit is able to lock (settle) when the phase of the input and output signals is equalized. If two signals are in phase that means that their frequencies are equal. With PLL as a closed-loop controller that also includes a filter, its implementation is not unique. In the literature, there are designs that properly filter harmonics, compensate unbalanced conditions and reduce the delay and the error with which the phase is tracked. By choosing the design that is the most efficient for each of the components we intended to design a PLL which is superior in working in high frequency. For each of the components we analyzed different papers in order to be able to understand what we should do in order to optimize the design. In this project, the PLL will be seen as a controller block and it will be optimized in that way. It is well known that the best type of controller is the PID controller. In this project we will try to turn the PLL into a PID PLL which would be able to reduce the settling time by a significant amount.

Chapter 2 presents basic properties of PLL blocks and equations related to settling time.

Chapter 3 presents Cadence design of each element of PLL along with simulations.

Chapter 4 presents the tentative to design the PID controller in Cadence and PID implementation of the PLL.

Chapter 5 contains the conclusions.

2. PLL BLOCK

PLL circuits are comprised of four essential blocks. These blocks are Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO), and Frequency Divider (FD). Almost all PLLs are comprised of these four blocks. In this section general explanations of components along with equations are shown.

2.1 Phase Detector

The first block is the Phase Detector (PD) which is able to sense the phase difference between two input signals and is able to produce a current which is a measure of the phase difference between the two inputs. The higher the phase difference, the greater the current produced by the PD. The PD circuit is usually implemented by means of a Phase Frequency Detector (PFD) and a Charge Pump (CP) circuit.

2.1.1 Phase frequency detector

PFD state diagram is shown in Figure 2.1. The PFD circuit is a sequential circuit which produces UP and DOWN outputs which inform the CP to charge or discharge the loop filter depending on the phase difference between the two input signals of PFD. Depending on which signal becomes high first, the REF signal or the FB signal in Figure 2.1, the circuit goes either to state 1 or to state 2. Supposing the circuit goes to state 1, if the FB signal becomes high, the circuit goes back to state 0. The longer it takes the FB to transit to 1, the longer will UP high signal remain high. This wider pulse on the other hand serves as a control voltage for the CP. The bigger the width of the UP signal, the greater the input voltage to the VCO will be, increasing the frequency of the output signal. Basically, the circuits let the CP know if the phase of the Frequency Divider (FD) circuit is higher or lower than some reference signal and helps to discharge or charge the node right after the CP circuit. If the frequency of the input signal is higher than the frequency of the output signal, the circuit will only go from state 0 to state 1 and will keep charging up the LF. On the other scenario, if the input frequency is lower than the output frequency, the output of the CP will be discharged leading to reduced frequencies on the VCO circuit.

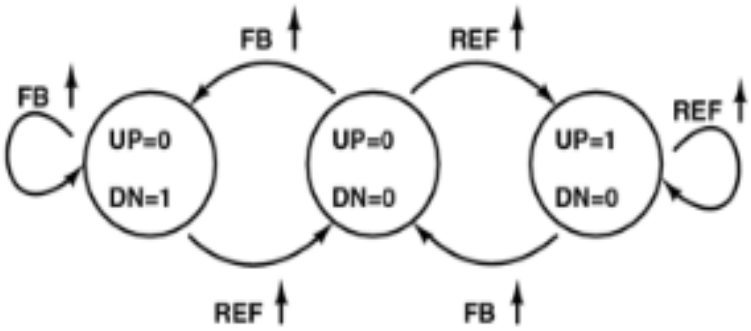

Figure 2.1: PFD state diagram.

This PFD circuit senses the 0 to 1 transitions of V_{REF} and V_{FB} and produces UP and DOWN signals depending on which of the input signal rises quicker. Theoretically, this is a very easy circuit to be build and it should work very close to the ideal circuit. One of the problems that is faced in real PFD blocks is the dead-zone of the PFD which happens for very small phase differences. The block diagram of PFD is shown in Figure 2.2.

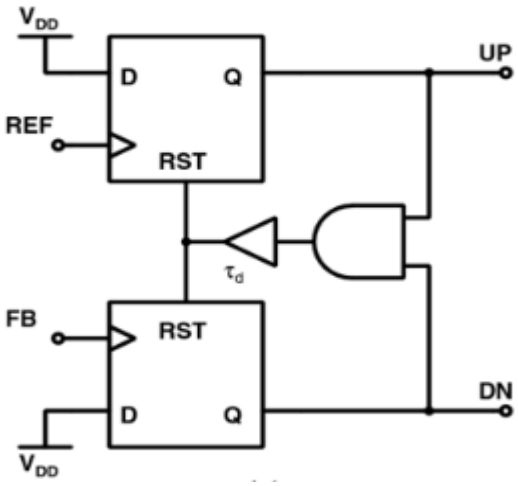

Figure 2.2: Block diagram of PFD.

For the input waveforms REF and FB in Figure 2.3, based on the State Diagram of Figure 2.1, the UP and DOWN signals are as in Figure 2.3.

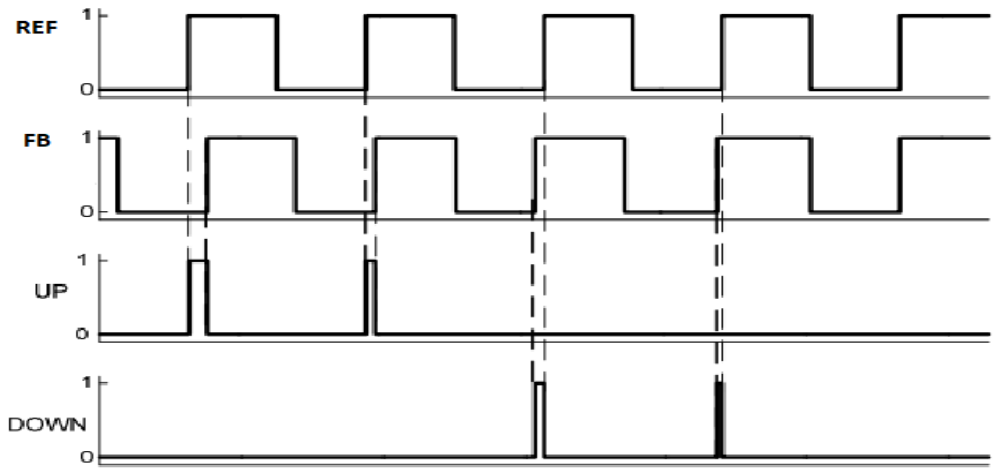

Figure 2.3: PFD waveforms.

2.1.2 Charge pump

Charge Pump circuit is the circuit that follows the PFD. PFD gives a measure of the phase difference between the two input signals. But as seen from the signals in Figure 2.3, the amount of phase difference is found on the width of up and down signals. A method is needed to convert the width of the pulses into currents which can then be converted into voltages at the Loop Filter (LF). For this the CP block is utilized. CP, as the name suggests, acts like a pump which charges something. The block has two inputs and those two inputs are UP and DOWN signals from Figure 2.2 The conventional CP circuit is shown in Figure 2.4.

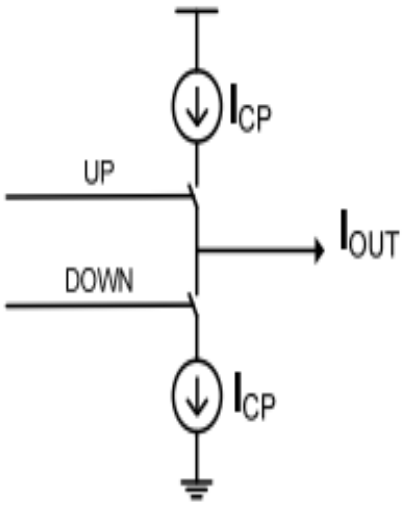

Figure 2.4: Ideal charge pump circuit

The CP circuit should ideally behave as in Table 2.1.

UP	DOWN	IOUT
0	0	0
0	1	-ICP
1	0	+ICP
1	1	0

Table 2.1: Charge Pump Functionality.

2.1.3 Phase detector circuit

Considering the PFD and CP circuit behaviours, the waveform of Figure 2.5 would be a perfect visualization of the behavior of PFD-CP circuit connected together, result which also complies with Equation 2.1.

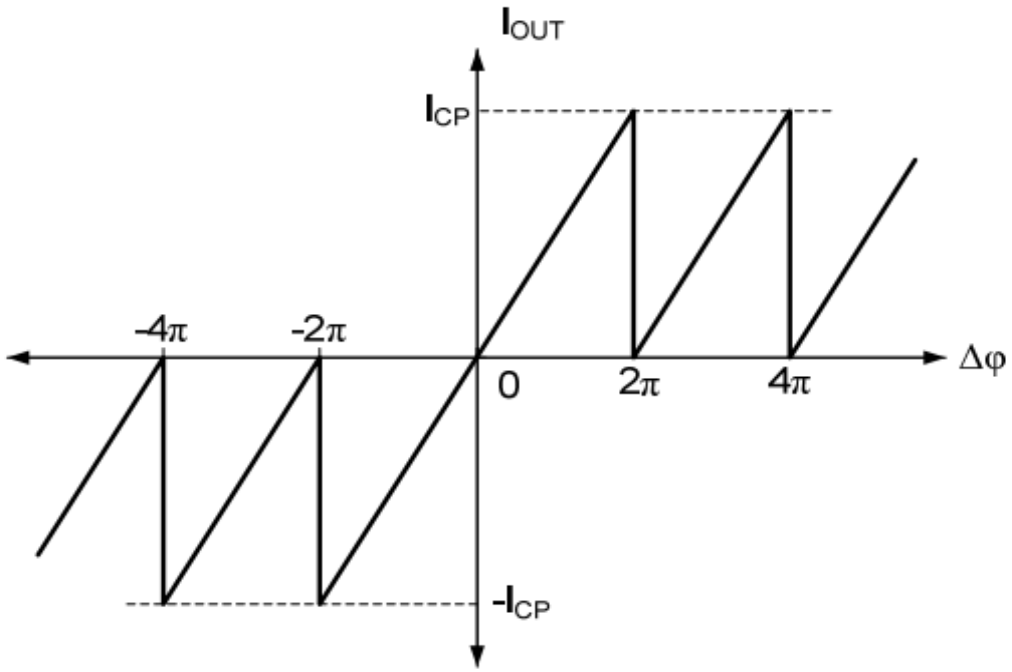

Figure 2.5: PFD-CP waveform.

$$K_{PD} = \frac{I_{cp}}{2\pi}\ [A/rad] \qquad (2.1)$$

2.2 Loop Filter

Almost every PLL has a loop filter (LF) which is generally used to achieve the proper transfer function. LF is used to achieve the necessary phase margin. The target phase margin for this project is a phase margin of 60^o, margin for which the PLL does not have a peaking behaviour and it is also stable. Whenever feedback is used in systems, there is a chance to have unstable circuits if the elements are not tuned to proper values. For a Charge Pump PLL (CPPLL), if the VCO is voltage controlled, the LF needs to supply a voltage output. Since the output of the CP is a current, the LF should act as a current to voltage converter. The tentative LF used in this project is shown in Figure 2.6

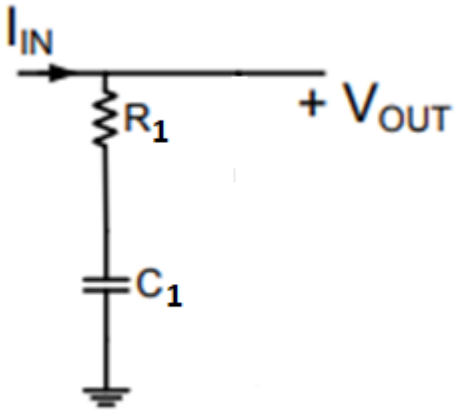

Figure 2.6: Loop Filter.

Current to voltage relationship of the LF on Figure 2.6 is shown at Equation 2.2:

$$\frac{\boldsymbol{V_{out}}}{\boldsymbol{I_{IN}}} = \boldsymbol{R_1} + \frac{\mathbf{1}}{\boldsymbol{s \cdot C_1}} = \frac{\mathbf{1} + \boldsymbol{sR_1C_1}}{\boldsymbol{s \cdot C_1}} = \boldsymbol{LF(s)} \qquad (\mathbf{2.2})$$

Keeping the LF as in Figure 2.6 causes a lot of ripples at the V_{out} because of imperfections of the CP circuit. Another capacitance C_2 is added in parallel with the LF of Figure 2.6 to filter these ripples as shown in Figure 2.7. The addition of C2 complicates the PLL equations very much but it is necessary to place it because there will be a lot of ripples otherwise. LF also controls the bandwidth of the PLL. For this project the bandwidth will be kept around 1MHz. Practically the Loop Bandwidth should be 5% of the reference frequency in the circuit.

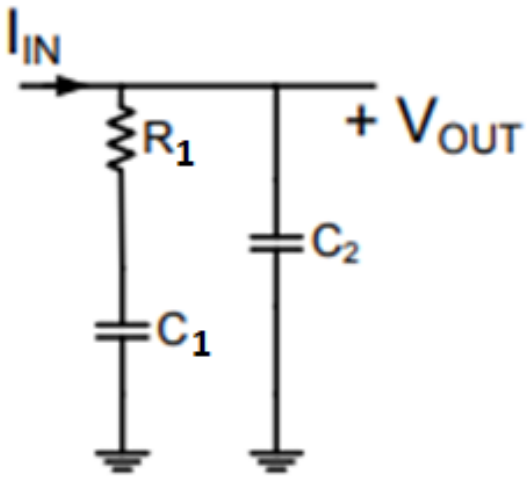

Figure 2.7: Loop filter For smaller ripples.

As a rule of thumb, C_2 is as shown in Equation 2.3:

$$\boldsymbol{C_2 = 0.1 \cdot C_1} \qquad (\mathbf{2.3})$$

The capacitance C2 will not be considered for the settling time calculations for the sake of simplicity of equations.

2.3 Voltage Controlled Oscillators

Voltage controlled oscillators (VCO), are blocks whose output frequency is controlled by an input signal. The control signal can either be a voltage or current. An ideal VCO is represented by Equation 2.4 :

$$\mathbf{f_{out} = K_{vco} \cdot V_{in} + f_{min}} \qquad (\mathbf{2.4})$$

The output signal of the VCO is fed directly to the phase detector if there is no frequency divider circuit. By means of this feedback the circuit continuously compares the output-input phase difference until phase difference is ideally 0. VCO ideal characteristic is shown in Figure 2.8.

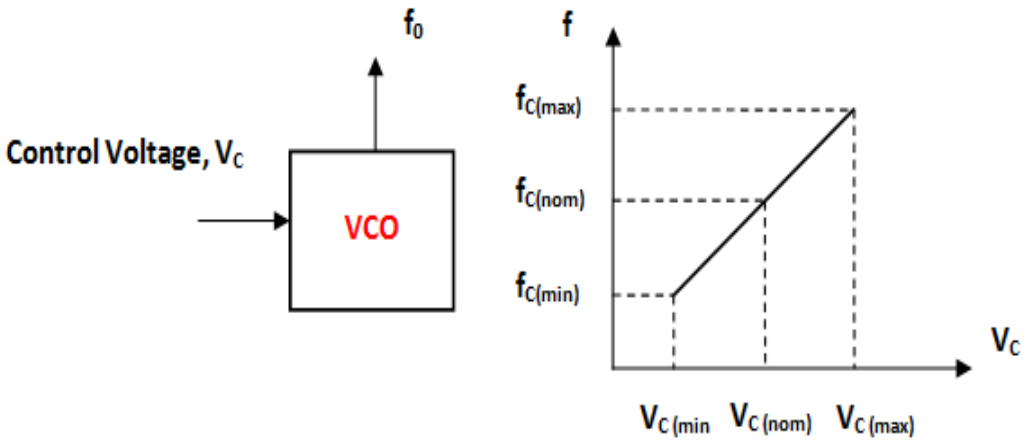

Figure 2.8: VCO characteristic.

The VCO transfer function should be derived as in Equation 2.5:

$$\boldsymbol{H_{vco}(s) = \frac{\phi_o(s)}{v_o(s)} = \frac{K_{vco}}{s}} \qquad (\mathbf{2.5})$$

K_{VCO} factor is an important factor of the PLL settling time calculations. Usually this factor is required to be as high as possible. There are different types of VCO-s which can be used for Charged Pumped PLL such as: Cross Coupled LC VCO, Current Starved VCO, Colpitts Oscillator. For this project, LC VCO is used.

2.4 Frequency Divider

Depending on the application, there may or may not be a Frequency Divider (FD) in the circuit. Since the center frequency of the PLL we want to design is 2.4GHz, for sure we need to use a FD because the reference frequency should be 18.75 MHz. FD divides the frequency of the input signal by a constant factor. The circuit shown in Figure 2.9 is able to divide the frequency of the signal by 32 times. In this project we will design a PLL whose reference frequency is 128 times smaller than the output's frequency. There will be seven D Flip-Flops (DFF) cascaded as in shown in Figure 2.9.

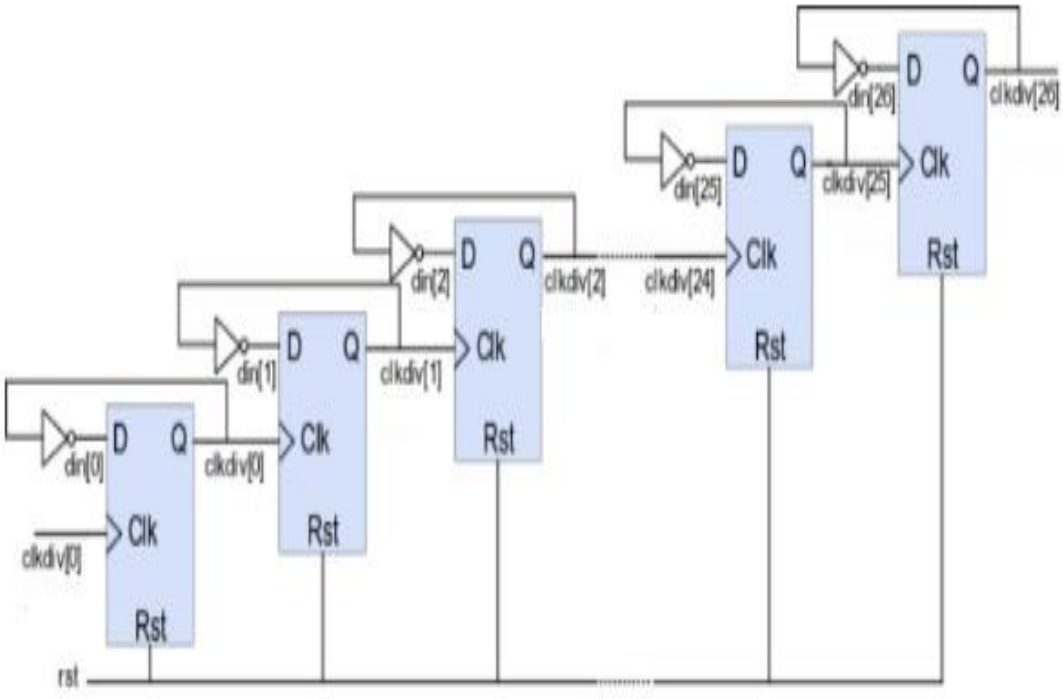

Figure 2.9: Frequency divider.

Practical aspect that need to be considered for the design of an FD is the maximum operating frequency of the first 3 DFF. The input frequencies for the first three DFF-s will be 2.4 GHz, 1.2 GHz and 0.6 GHz. DFF-s should be designed carefully, possibly around minimum technology so they can work on these frequencies.

2.5 Settling Time Calculations

The signal flow graph of the PLL is shown in Figure 2.10. K_{PD} is the transfer function of PD circuit. LF(s) is the transfer function of LF. K_{VCO} is the VCO frequency factor.

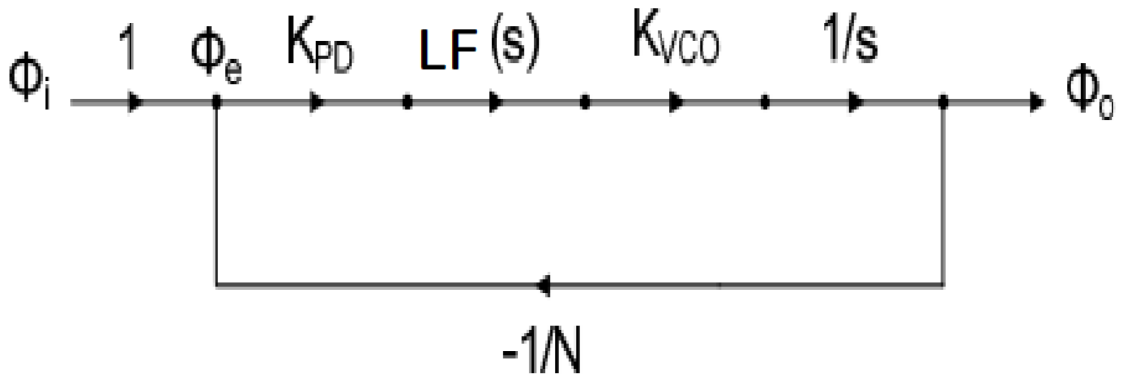

Figure 2.10 Signal flow diagram of PLL

Using the signal flow diagram shown in Figure 2.10, phase error ϕ_e is calculated as shown in Equation 2.6:

$$\boldsymbol{\phi_e = \phi_i - \frac{\phi_o}{N}} \quad \textbf{(2.6)}$$

Following the diagram, the output ϕ_o can be written as shown in Equation 2.7:

$$\boldsymbol{\phi_o = K_{PD} * LF(s) * \frac{K_{VCO}}{s}\ \phi_e} \quad \textbf{(2.7)}$$

$$\boldsymbol{K = K_{PD} \cdot K_{VCO}} \quad \textbf{(2.8)}$$

By using Equations 2.6, 2.7 and 2.8, equation 2.9 can be easily derived.

$$\boldsymbol{\frac{\phi_0}{\phi_i} = K \cdot R_1 \frac{s+\frac{1}{R_1 C_1}}{s^2+s\frac{K \cdot R_1}{N}+\frac{K}{NC_1}}} \quad \textbf{(2.9)}$$

By means of Equation 2.9, the natural frequency and dumping factor paramters can be calculated as follow:

$$\boldsymbol{\omega_n = \sqrt{\frac{K}{NC_1}}} \quad \textbf{(2.10)}$$

$$\boldsymbol{\zeta = \frac{1}{2}\sqrt{\frac{KR_1^2 C_1}{N}}} \quad \textbf{(2.11)}$$

The time constant of the circuit can be calcualted as in Equation 2.12.

$$\boldsymbol{\tau = \frac{1}{\omega_n \cdot \zeta}} \qquad \textbf{(2.12)}$$

On Equations 2.6 – 2.12, the RC filter in Figure 2.6 has been used. The 2% settling time of this PLL can be approximated as in Equation 2.13:

$$\boldsymbol{T_s = 4 \cdot \tau} \qquad (\textbf{2.13})$$

3. DESIGN OF PLL BLOCKS

There are numerous blocks that need to be designed for the CPPLL and there are a lot of practical aspects which will need to be targeted. In this Chapter 3, the design of PD, LF, VCO and FD circuits will be discussed.

3.1 Phase Detector

As seen on Chapter 2, the Phase Detector is made of two main blocks which are the PFD and CP circuit. Their ideal block diagrams are shown in Figure 2.2 and Figure 2.4 respectively. The design of PFD and CP will be shown in the upcoming sections.

3.1.1 Phase frequency detector

As shown in Figure 2.2, PFD circuit requires two D flip-flops, and one AND gate. A very fast RESET is required in order to reduce the PFD dead-zone. Dead-zone sets a low margin on the phase difference that the PFD can detect and the main reasons why it happens are the dealys at AND block and RESET delay.

3.1.1.1 D flip-flop

In this section a D flip-flop (DFF) for the PFD application will be designed. It is crucial for the PFD application to have an asynchronous RESET DFF because the circuit should RESET as fast as possible. If the circuit was a synchronous RESET, PFD would not produce the correct UP and DOWN signals until the clock rising edges to the DFF-s. This would yield potential problems and the PLL would not be able to lock with input frequency. The DFF used for the PFD is shown in Figure 3.1 whereas the sizing of the device is shown in Table 3.1. The sizes are kept at minimum sizes in order to reduce the delays coming because of the capacitances in the circuit. The supply voltages to the DFF are 1.5 V and 0 V.

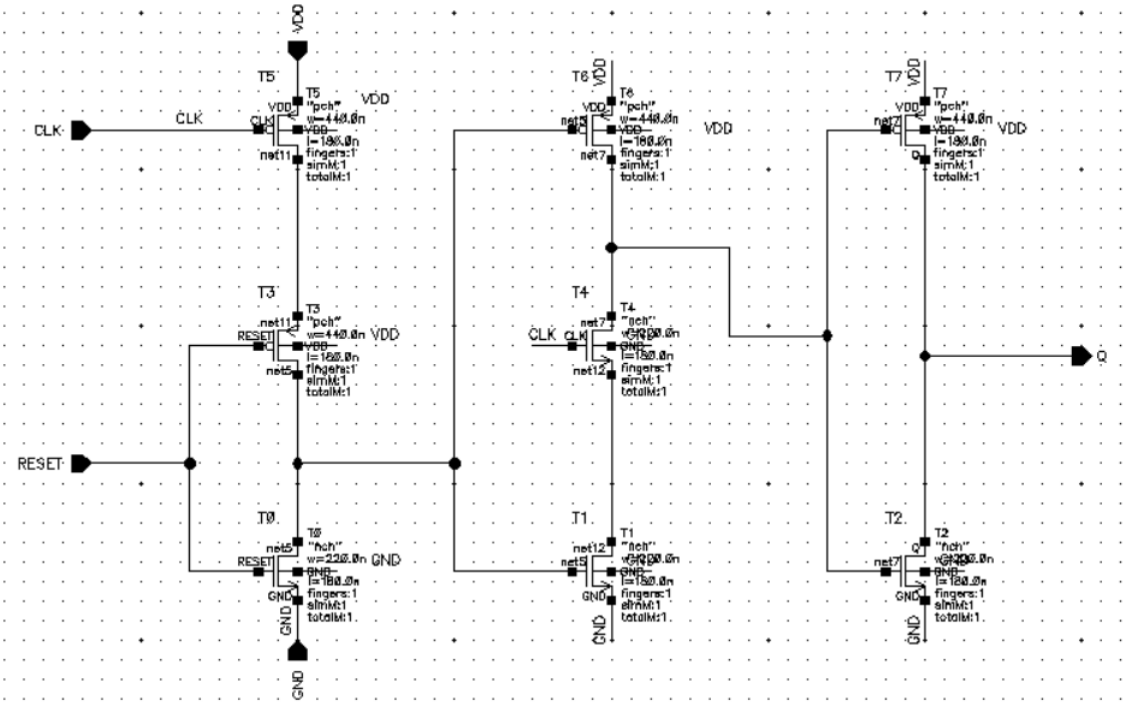

Figure 3.1: DFF for PFD

MOS	T0	T1	T2	T3	T4	T5	T6	T7
W/L	220n/180n	220n/180n	220n/180n	440n/180n	220n/180n	440n/180n	440n/180n	440n/180n

Table 3.1: DFF transistor sizing

If the DFF nodes are charged as in the Figure 3.2 what happens when clock transitions from low to high and RESET is low? T5 turns off and since the RESET is low, the drains of T5 and T3 remain high. Since the drain of T3 is high, that means that T6 will be off whereas T1 will be on, allowing the drain of T4 to discharge and transition to ground. T2 and T7 are essentially an inverter. Since its input transitions to ground, the output will transition to VDD. Essentially, any time the CLK raises up, the output will become high unless RESET is high.

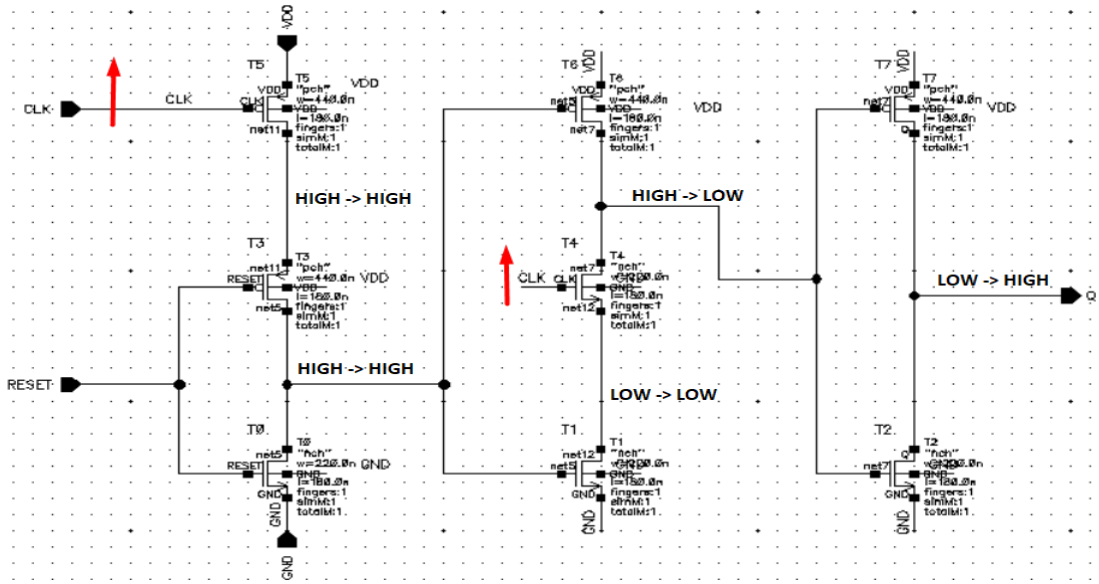

Figure 3.2: DFF transitions at positive edge of clock.

When RESET becomes high the voltage levels are shown in Figure 3.3. T0 is on whereas T3 is off. This makes the capacitance at the drain of T3 and T0 discharge. If that capacitance discharges, T1 will turn off and T6 will be on. Thus, we will be charging up the drain of T4 which then turns on T2 which will be able to discharge its drain, making the output low. RESET has priority over CLK. This means that if RESET is high, the output will remain low even at the positive edges of the clock.

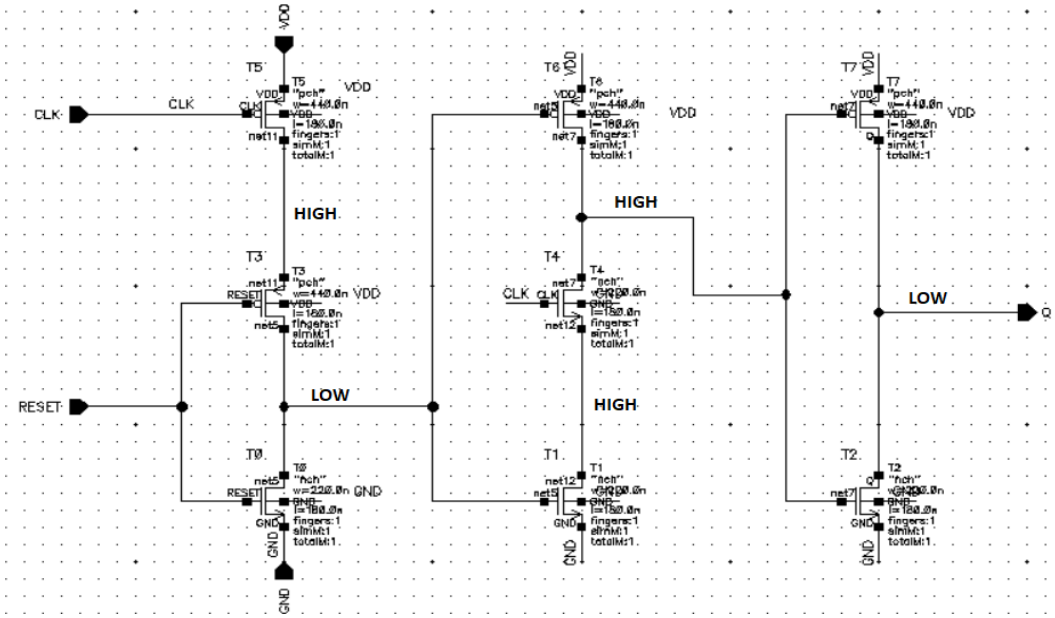

Figure 3.3: RESET voltage transitions.

In Figure 3.4, a transient simulation of DFF block is shown. The circuit reacts properly to RESET and CLK signals. The time between the vertical markers V_1-V_2 is the RESET delay whereas the time between the vertical markers V_3-V_4 is the required delay for a low to high transistion of DFF.

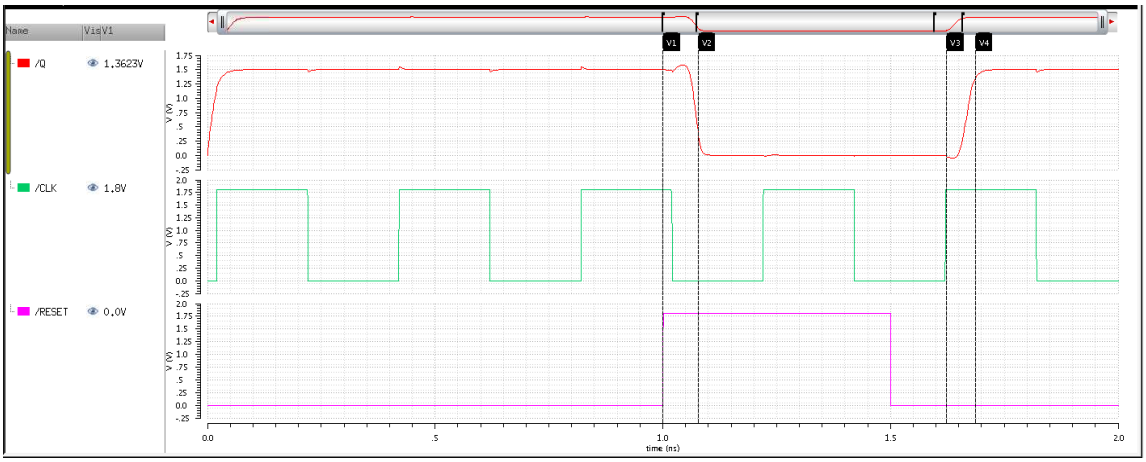

Figure 3.4: Transient simulation of DFF

3.1.1.2 AND gate

One CMOS NAND gate and inverter are cascaded to design the AND gate. NAND gate is shown in Figure 3.5.

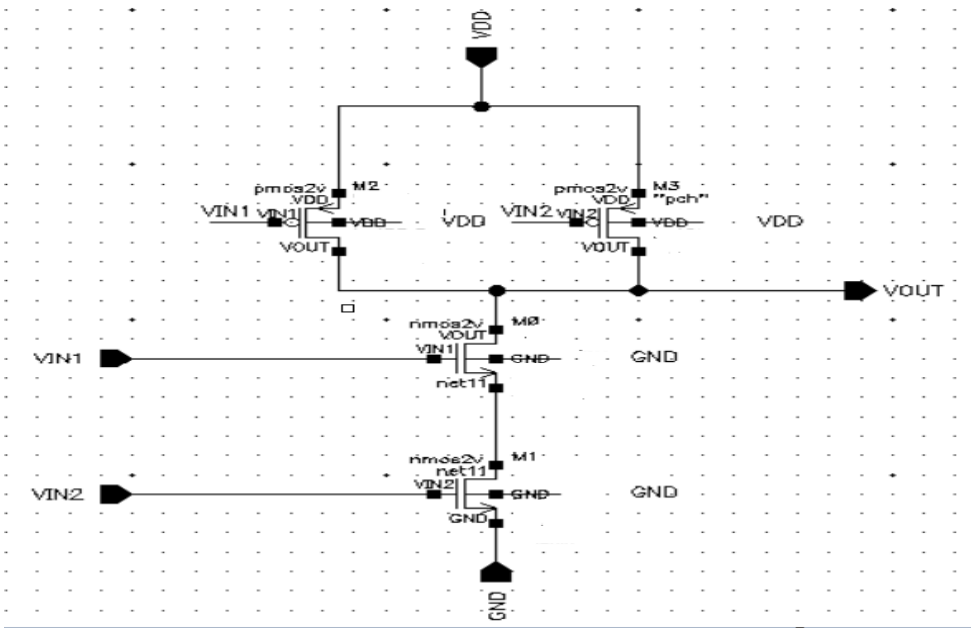

Figure 3.5: NAND gate.

The transistor sizes for the NAND gate are shown in Table 3.2.

Transistor	M0	M1	M2	M3
W/L	220n/180n	220n/180n	450n/180n	450n/180n

Table 3.2: NAND gate transistor sizes.

CMOS inverter circuit and transistor size are shown in Figure 3.6 and Table 3.3 respectively.

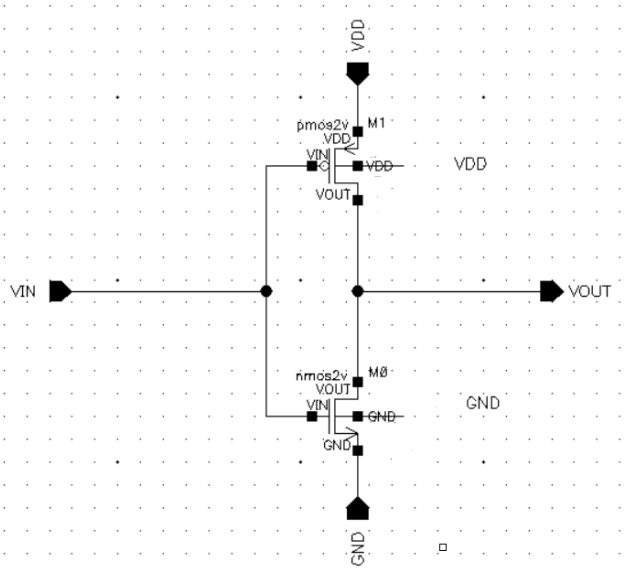

Figure 3.6: CMOS inverter.

Transistor	M0	M1
W/L	220n/180n	440n/180n

Table 3.3: Inverter Sizes.

3.1.1.3 Simulations of phase frequency detector

After adding DFF-s, NAND gate and the inverter together as in Figure 2.2, the circuit shown in Figure 3.7 is formed. A very usual problem that is faced on these designs are the delays. Since the signal needs to propagate, the output will need some time to change to their appropriate values. This is actually the source of the PFD dead-zone. The dead-zone of PFD is formed because of the time the signal needs to propagate from the input of NAND to the output of the inverter plus the time the DFF needs to reset. If the phase difference between the two sensed inputs is very small, for instance 10ps, the PFD will not be working properly and will assume the two input's phase are equal.

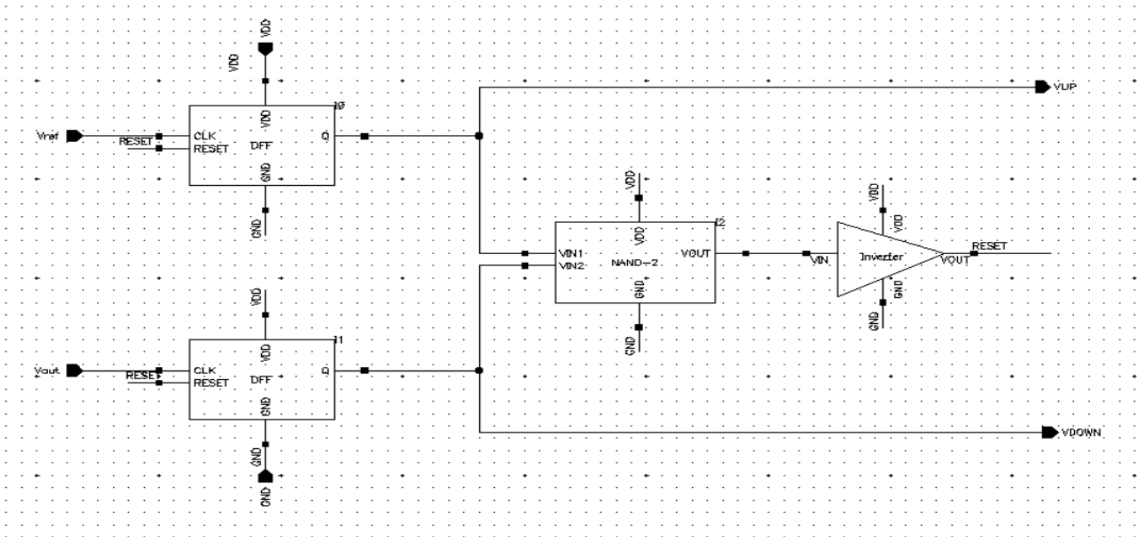

Figure 3.7: PFD circuit.

As mentioned in Chapter 2, if the phase of reference signal is greater than the phase of the output of the FD circuit, the circuit should be able to produce some VUP pulses whose width is dependent on the amount of phase difference between the two inputs. In Figure 3.8, the FD signal transitions from low to high earlier than the reference signal. This in turn makes the circuit to produce high pulses in the DOWN output. In Figure 3.8 the phase of the output of frequency divider is greater than the phase of the reference signal. It is clear form Figure 3.8 that the width of DOWN signal is approximately equal to the time difference between low to high transistions of the PFD inputs.

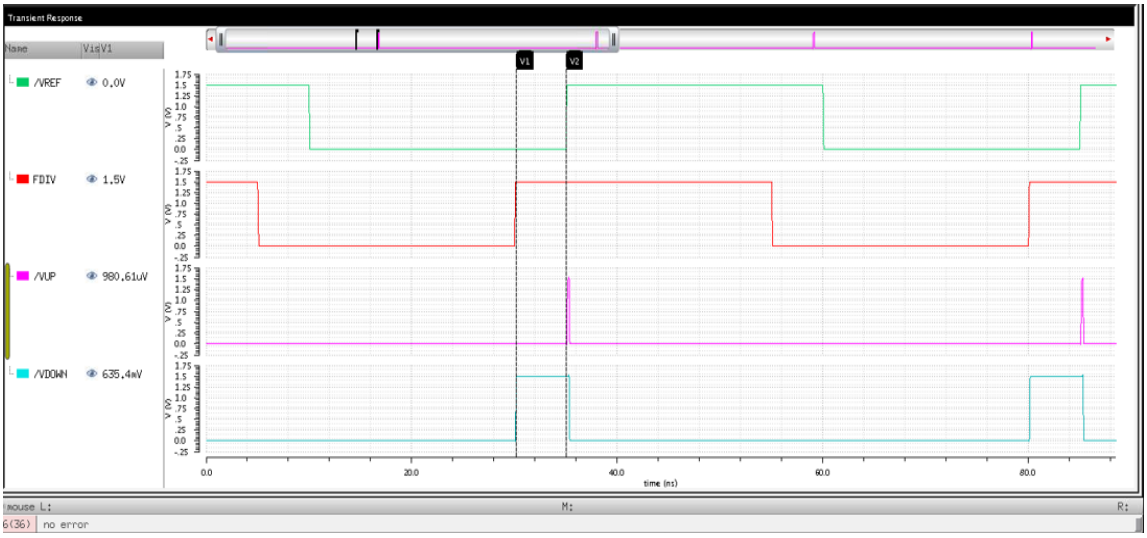

Figure 3.8: Phase of FDIV greater than VREF signal

In Figure 3.9, VREF phase is greater than the FDIV phase. PFD is correctly calculating the phase difference and similarly to the previous simulation, the width of the VUP signal is equal to the time difference between low to high tranistions of the inputs.

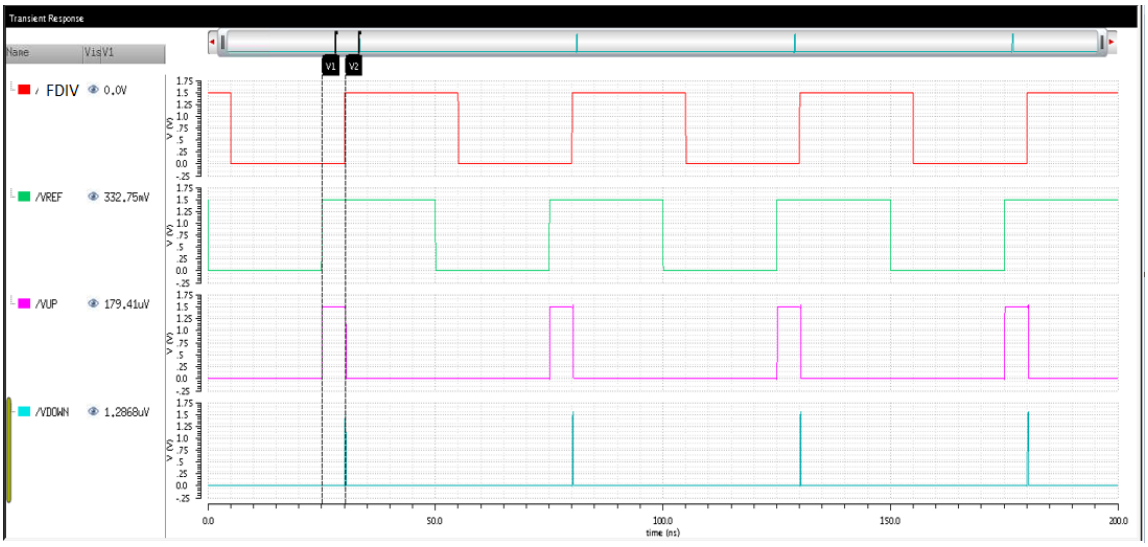

Figure 3.9: Phase of VREF greater than FDIV signal.

Ideally, the spikes in VUP signal in Figure 3.8 and VDOWN signal in Figure 3.9 should not happen but since the RESET signal needs some time to take effect, the DFF update the output to high and then after the RESET starts effecting, the outputs are discharged again. Besides the dead-zone effect, this is also another problem that happens usually in hardware but because of the properties of the charge pump, those

spikes do not cause a lot of problems. Figure 3.10 shows the response of the PFD if the two inputs are in-phase.

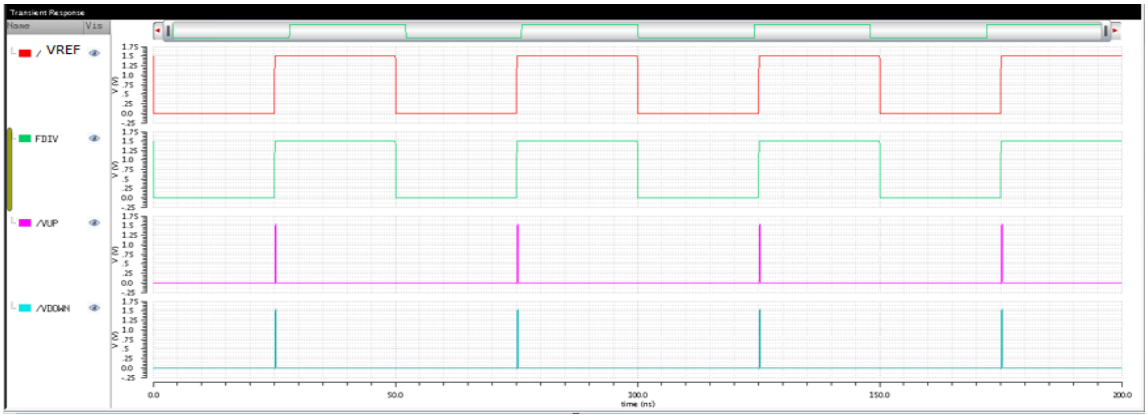

Figure 3.10: Phase of input signals are equal

From the calculations in Figure 3.11, the dead zone is 298ps. This means that if the two inputs phase difference is lower than that 298ps, the circuit will not be able to distinguish any phase difference between the two.

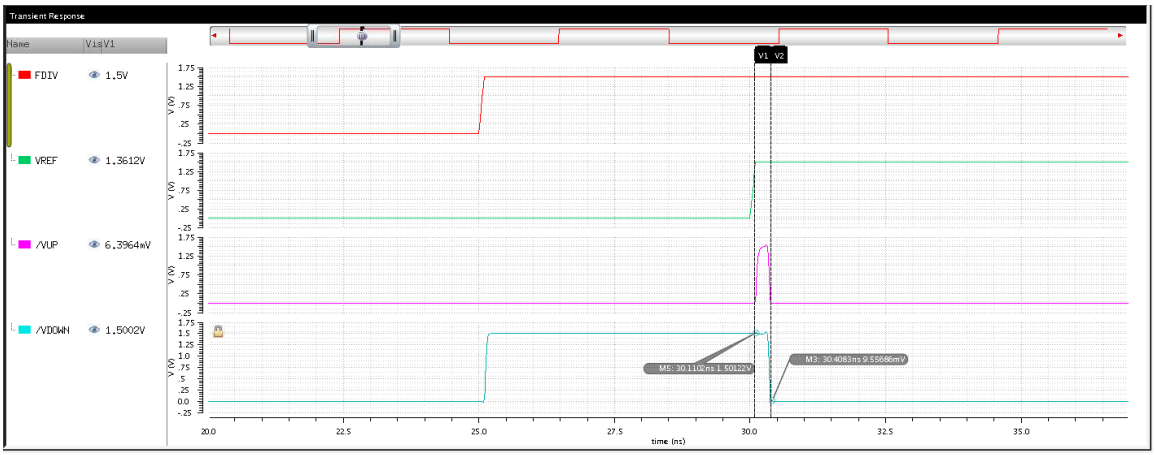

Figure 3.11: Dead-zone calculation.

3.1.2 Charge pump

A conventional CP circuit is shown in Figure 3.12. The inverter just after the U signal in Figure 3.12 is added because of the technology being used. If the PLL is trying to charge the output of the CP, the Up and Down signals of the PFD will be high and low respectively. But a high input to the transistor Q1 in Figure 3.12 turns the transistor off and thus the output node of CP will not be charged. That is the reason for adding an inverter. Everytime there is a high signal produced by the PFD on Up signal, that

signal will be inverted to make M1 work. There will be a couple of additions to this circuit because inverting the U signal throught a NOT gate creates some delays. Thus, the UP and DOWN signals do not arrive at the same time at the inputs of the Q1 and Q2 transistors. For the solution of this problem there are different methods that can be used. The most usual solution is passing the DOWN signal through an always ON transmission gate that is able to produce almost the same delay the inverter is causing in the UP signal.

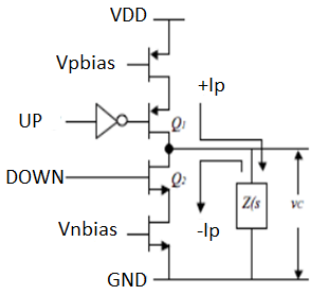

Figure 3.12: Charge pump circuit.

Having said that, the design of the CP circuit is very easy. For this block it will be necessary to know the unCox and upCox of nmos and pmos transistors as they will be used to produce the correct currents in the circuit. The TSMC0.18 transistors have the parameters shown in Figure 3.13.

Parameter	Symbol	N MOS	P MOS	Unit
Maximum supply voltage	$V_{DD,max}$	1.8		V
Zero-bias threshold voltage	V_{th0}	0.50	−0.48	V
Bulk effect parameter	γ	0.42	−0.67	$\sqrt{V}$
Twice Fermi potential	$2\phi_F$	0.87	−0.90	V
Zero-bias sub-threshold slope	n	1.31	−1.29	
Channel length modulation constant	k_λ	0.041	−0.039	$\mu m/V$
Current factor	$K' = \mu C_{ox}$	316	−62	$\mu A/V^2$
Gate area capacitance	C_{ox}	8.4	8.4	$fF/\mu m^2$
Gate width overlap capacitance	C_{ov}	0.72	0.68	$fF/\mu m$
Junction area zero-bias capacitance	C_{j0}	1.0	1.2	$fF/\mu m^2$
Junction perimeter zero-bias capacitance	C_{jsw0}	0.25	0.20	$fF/\mu m$
Flicker noise coefficient (not KF)	K_f	$3.3{\cdot}10^{-25}$	$1.6{\cdot}10^{-25}$	J
Minimum channel length	L_{min}	0.18		μm
Typical source/drain length	ℓ_{SD}	0.6		μm
Mosis scalable design rules unit	λ_{SUBM}	0.1		μm
Thermal voltage (kT/q)	V_T	26		mV

Figure 3.13: TSMC 0.18 parameters.

Initially current mirrors which are supplying charging and discharging currents to the output node of the CP are designed. The first one to be built is the PMOS current mirror. Using the values in the Figure 3.13, it is calculated that for an Id = 250uA, the transistor W/L and R2 of Figure 3.14 should respectively be 2.5u/180n and 1.31 K ohms. For these values, the transistor stands in saturation with a Vov = 356.9mV and most importantly it has 250uA of current flowing. This will create the appropriate VP_{BIAS} in Figure 3.12 as shown in Figure 3.14.

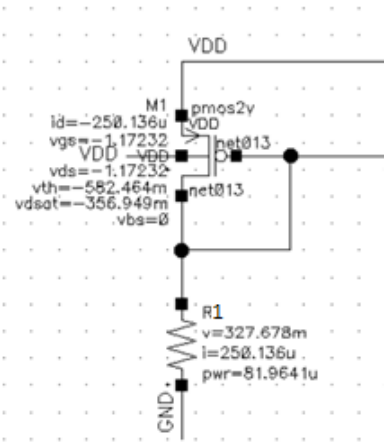

Figure 3.14: PMOS current mirror.

Using the same logic with the NMOS current mirror, we can have 250uA of current by having R_2=1.3k and W/L_2 = 1u/0.18u.

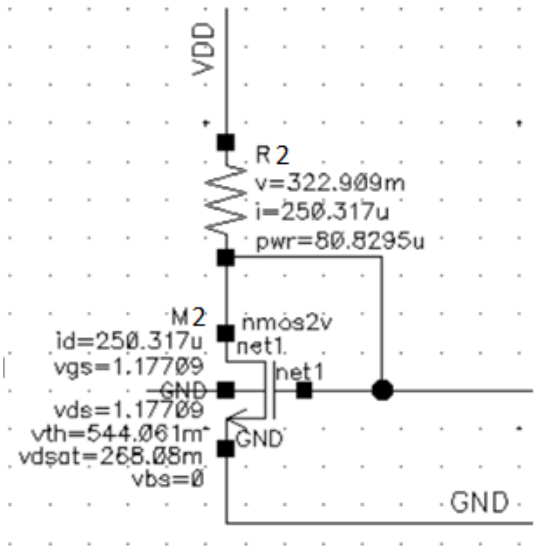

Figure 3.15: NMOS current mirror.

The complete circuit including the delay equalizing elements of the UP and DOWN inputs is shown in Figure 3.16.

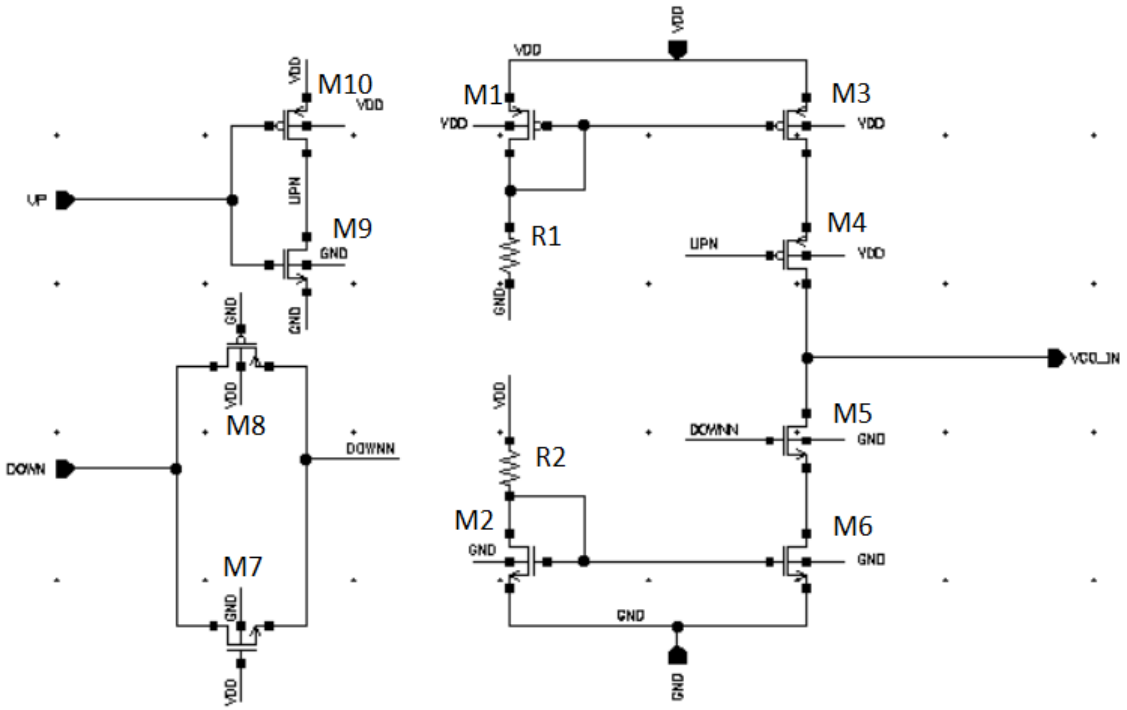

Figure 3.16: Charge pump circuit.

Transistor sizes M3 – M12 are shown in Table 3.4.

Transistor	M3	M4	M5	M6-M7	M8	M9	M10
W/L	2.5/0.18	20/0.18	10/0.18	1/0.18	2/0.18	0.45/0.18	0.9/0.18

Table 3.4: Transistor sizes for CP circuit.

Figures 3.17 and 3.18 are the simulations of the CP circuit. In Figure 3.17, CP inputs are two square signals of the same frequency but out of phase. For the red signal, the phase difference is 2ns. The phase difference is increased to 6ns. Clearly, for greater phase differences, the output of the charge pump charges faster.

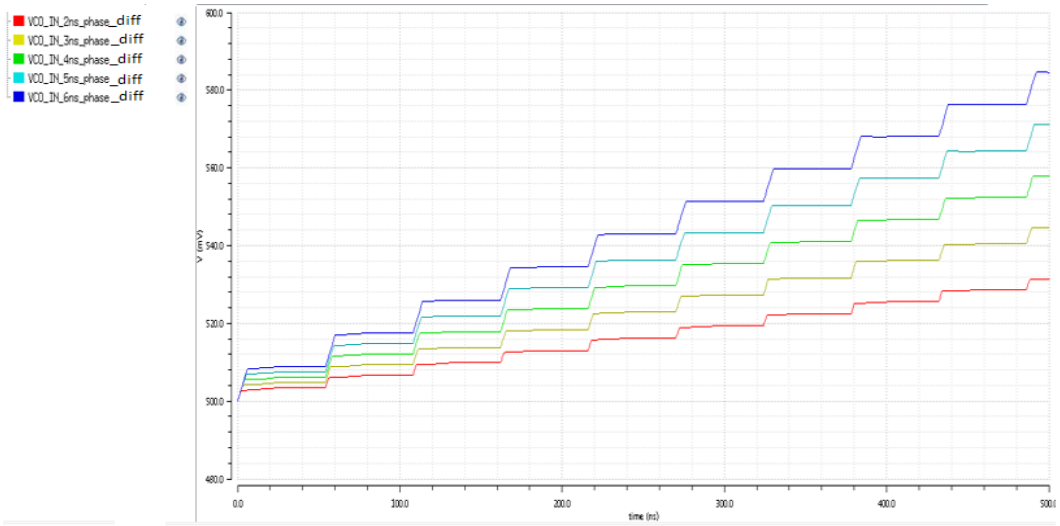

Figure 3.17: Charging of CP.

In Figure 3.18, CP inputs are two square signals of the same frequency but out of phase. For the red signal, the phase difference is 2ns. The phase difference is increased to 6ns. Clearly, for greater phase differences, the output of the charge pump discharges charges faster.

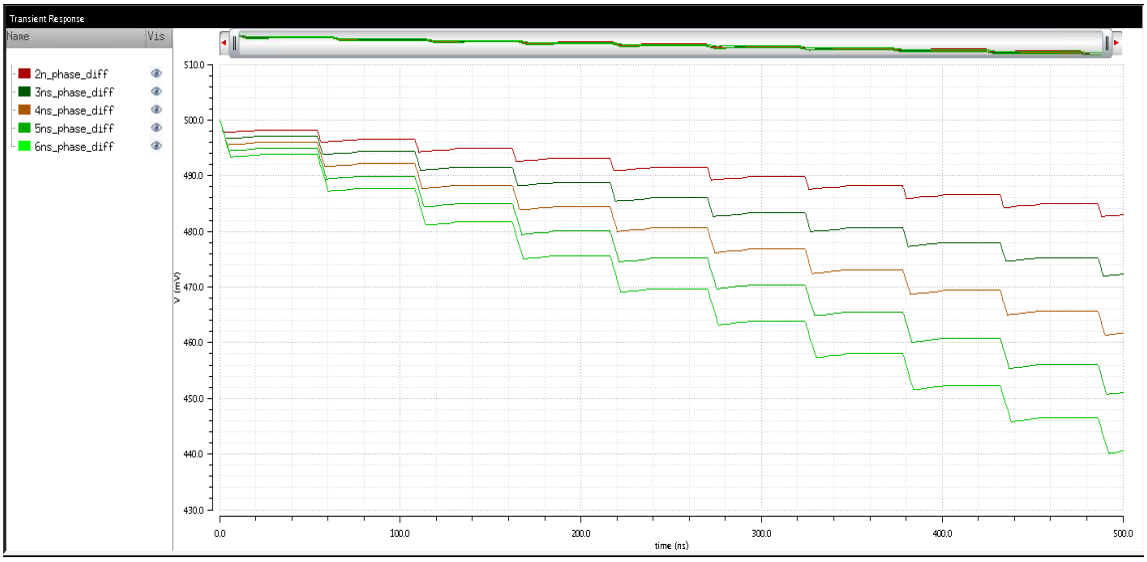

Figure 3.18: Discharging of CP.

3.2 Voltage Controlled Oscillator

In this section the design of VCO will be shown. For our application, an oscillator whose output frequency is controlled by the input voltage of the oscillator is needed. As mentioned in the previous sections, the PFD-CP block converts the phase-frequency difference into a current which eventually charges up the Loop Filter which is also the input of the VCO. If the input node of VCO charges up, that means that the VCO should increase the frequency because the input frequency is greater than the outputs frequency. If the input node of VCO discharges, that means that the VCO should reduce the output frequency. In theory, the frequency of the VCO should be linearly controlled by the input voltage but because of device parasitic and imperfections, the circuit will not have a perfect linear behavior. Usually the VCO is required to be linear over some specific region. The PLL built in this project will be used for 2.4GHz applications so it is very important to make the VCO work around that region. The tentative VCO for this project is a cross coupled VCO as shown in Figure 3.19.

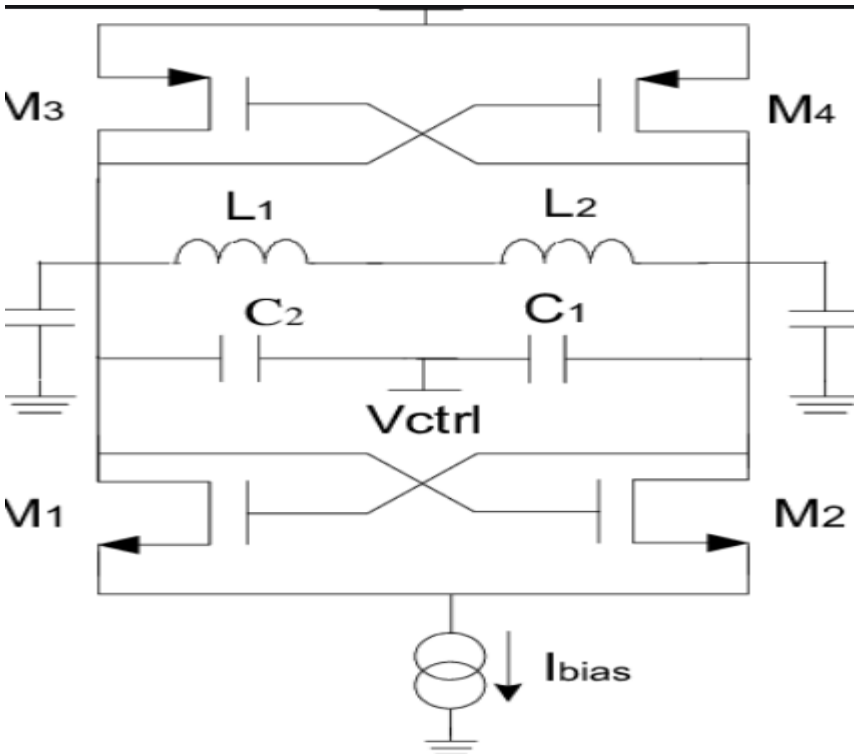

Figure 3.19: Cross coupled VCO.

The C_1 and C_2 in Figure 3.19 are very important elements as they are used to alter the output frequency of the VCO. NMOS transistor-based varactors are used on this project to sweep the frequency of the output of VCO circuit.

At $\omega = \frac{1}{\sqrt{L_1 \cdot C_1}}$ the LC tank completely resonates and the circuit starts to oscillate. For this project $L_1 = L_2 = 1.75nF$. In order to have the circuit oscillating at 2.4GHz, the capacitance should be:

$C_1 = C_2 = 2.51pF$

Firstly, the oscillator part of the VCO is designed. Varactors are designed later in this section. This was preferable because the calculation of the capacitors of transistors $M_{1\text{-}4}$ in Figure 3.19 is quite difficult. Figure 3.20 shows the cross coupled oscillator and the varactors enclosed in the rectangle. $M_{1\text{-}4}$ contain a lot of parasitic capacitors because they are big. They were intentionally selected big to satisfy the starting condition of the oscillator.

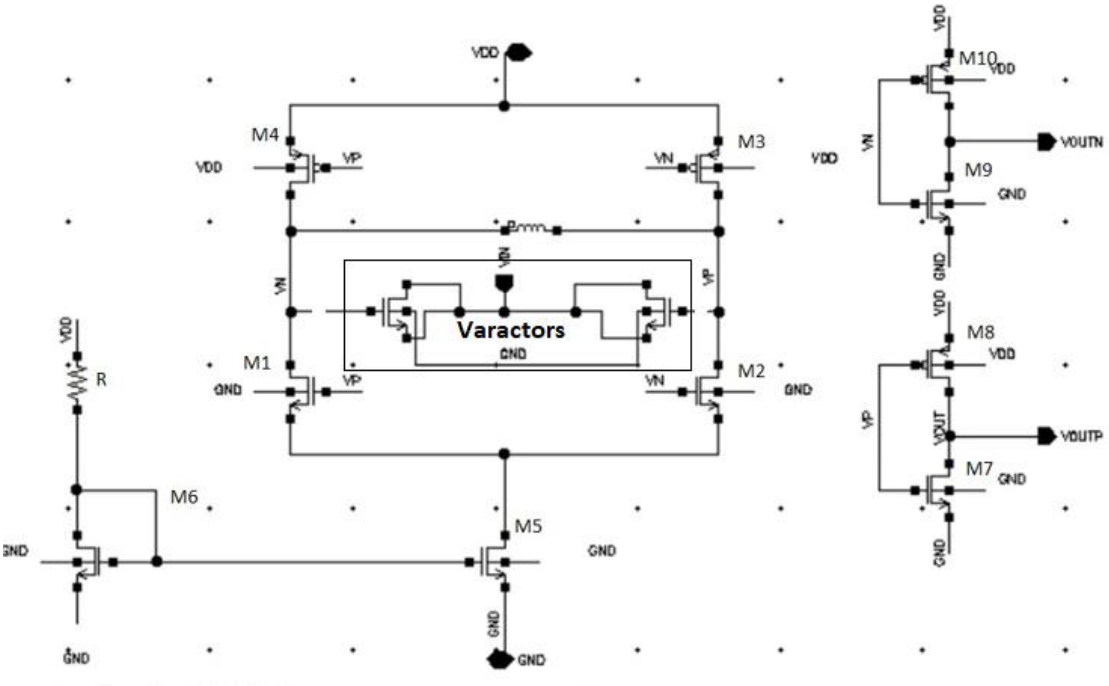

Figure 3.20: Cross couple oscillator.

Current mirror formed by transistors $M_{5\text{-}6}$ is supplying current to the circuit. In order to have high gm transistors, high currents will be possible by means of the current mirror. The current mirror is supplying 3.5mA of current to the oscillator. By means

of Equations 3.1, 3.2, 3.3 and 3.4, the calculation of the sizes of $M_{5\text{-}6}$ and resistor value were found.

$$\mu_n C_{ox} = 313 \frac{\mu A}{V^2} \quad \textbf{(3.1)}$$

$$V_{ov\,5-6} = 0.2V \quad \textbf{(3.2)}$$

$$\left(\frac{w}{L}\right)_n = \frac{2I_D}{\mu_n c_{ox}} \cdot \left(\frac{1}{v_{ov}}\right)\text{^}2 \quad \textbf{(3.3)}$$

$$R = \frac{V_{DD} - (V_{ov} + V_{th})}{3.5mA} \quad \textbf{(3.4)}$$

Table 3.5 and Equations 3 show the selected values for the oscillator in Figure 3.20. The resistance required is R = 234 ohms.

MOSFET	M1-M2	M3-M4	M5-6	M7 & M9	M8	M10
W/L	50/0.4	200/0.4	559/1	1/0.18	2/0.18	2/0.18

Table 3.5: Oscillator transistor sizes.

Figure 3.21 shows the bias current of the current mirror used in Figure 3.20.

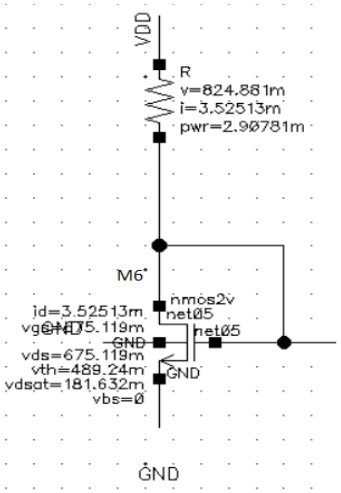

Figure 3.21: Operating point of current mirror.

In Figure 3.22, the transient simulation of the oscillator in Figure 3.20 is shown.

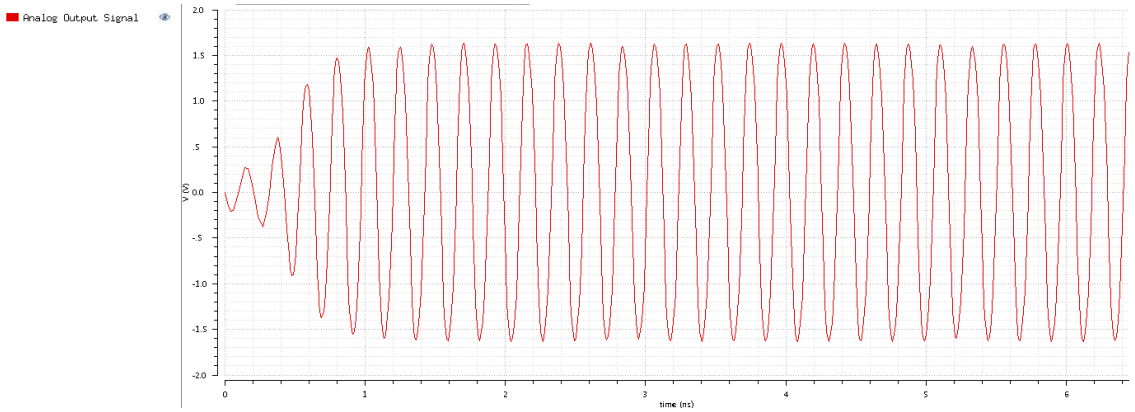

Figure 3.22: Vp – Vn of oscillator on Figure 3.20.

If the oscillator is not loaded with varactors, the oscillation frequency is 4.3 GHz. Based on calculations, the node to ground parasitic capacitance of both V_N and V_P is 0.753 pF. In order to make the oscillator work at 2.4GHz, the varactors should contribute with approximately 1.8 pF each. Using the TSMC transistor in the configuration shown in Figure 3.23 the behavior of NMOS varactors can be analyzed as a function of V1. It would be great if we could make the varactor have parasitic capacitor values from 1pF to 2.6pF.

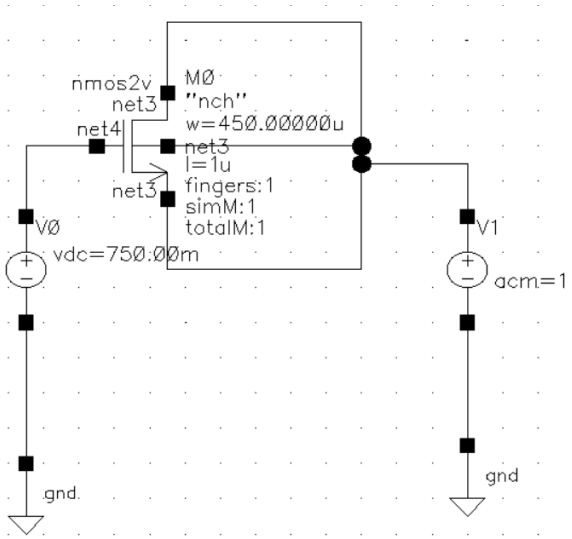

Figure 3.23: NMOS varactor test bench setup.

There is a way to measure the capacitance of a node. The equation that does that is shown in Equation 3.5.

$$C(V) = \frac{I}{2\Pi f V}\Big|_{f=1} \tag{3.5}$$

Equation 3.5 can be implemented by means of an AC analysis in Cadence. Figure 3.24 shows how to configure the AC analysis in order to get the proper calculated value.

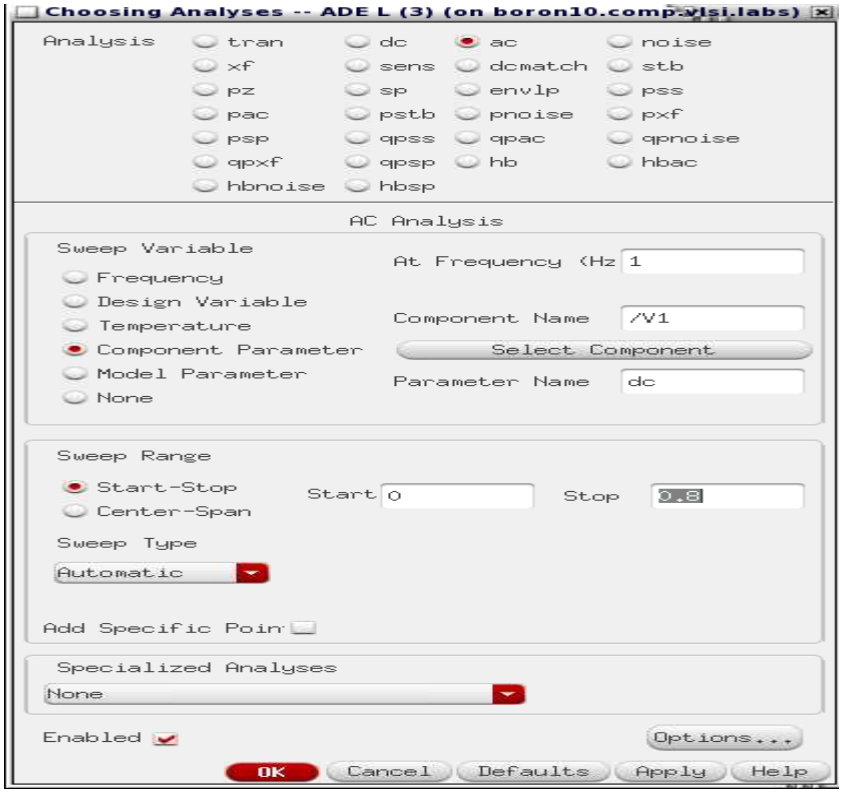

Figure 3.24: AC simulation setup.

The selected W/L for the transistor in Figure 3.23 is 450um/1um. This value has been previously found by means of trial and error and parametric simulations of parasitic capacitances. This value provides 1pF to 4pF parasitic capacitance which can load the VCO and produce the correct range of frequencies. Figure 3.25 shows a plot of capacitance over a range of DC applied voltages.

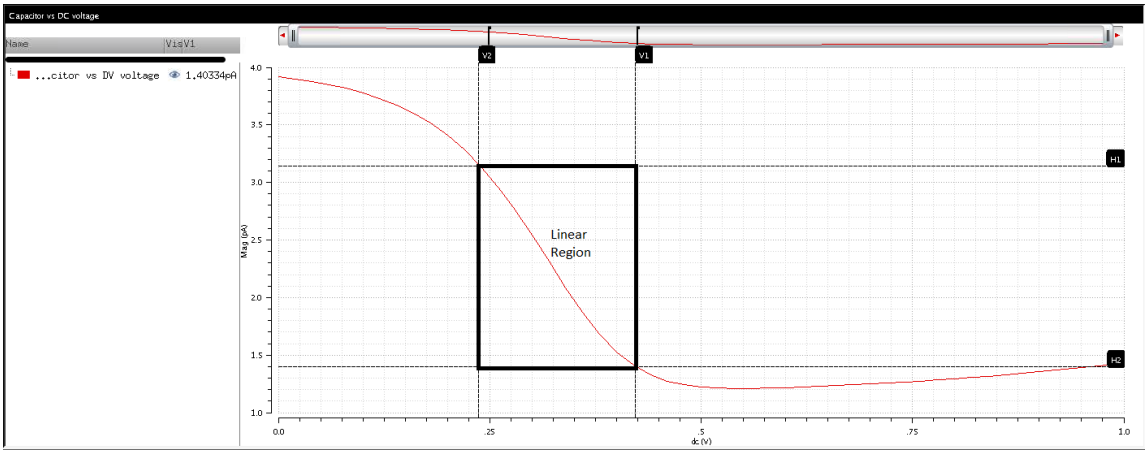

Figure 3.25: Capacitance vs DC voltage.

A PSS analysis can show the Frequency vs VCO_in plot as shown in Figure 3.26. The gain of VCO is:

K_{VCO} = 1.42 GHz/V **(3.7)**

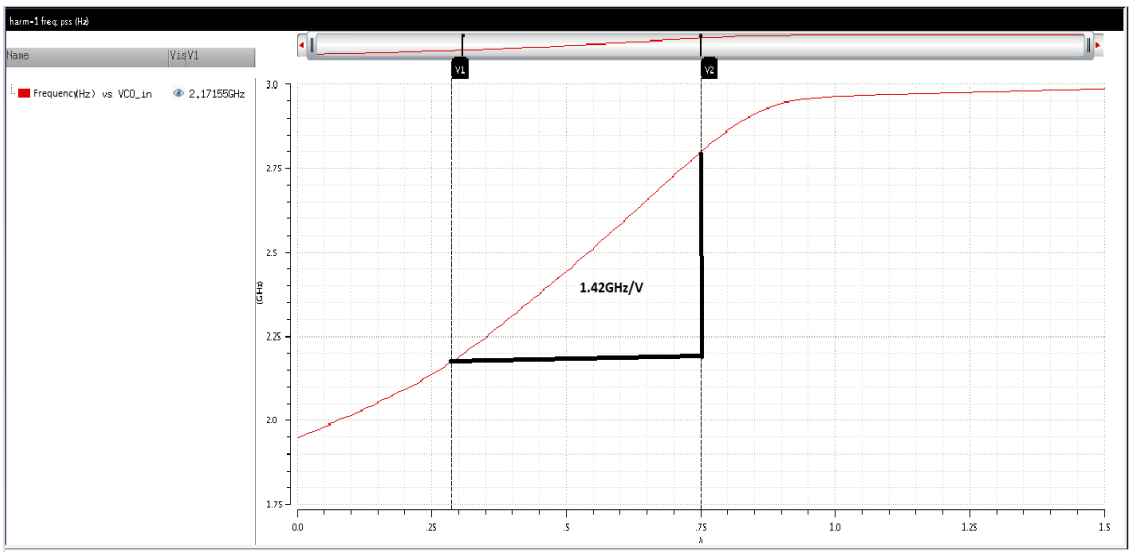

Figure 3.26: Frequency vs VCO_in.

The phase noise of the VCO is shown in Figure 3.27. At 2.4GHz, the phase noise is -155.89 dBc/Hz.

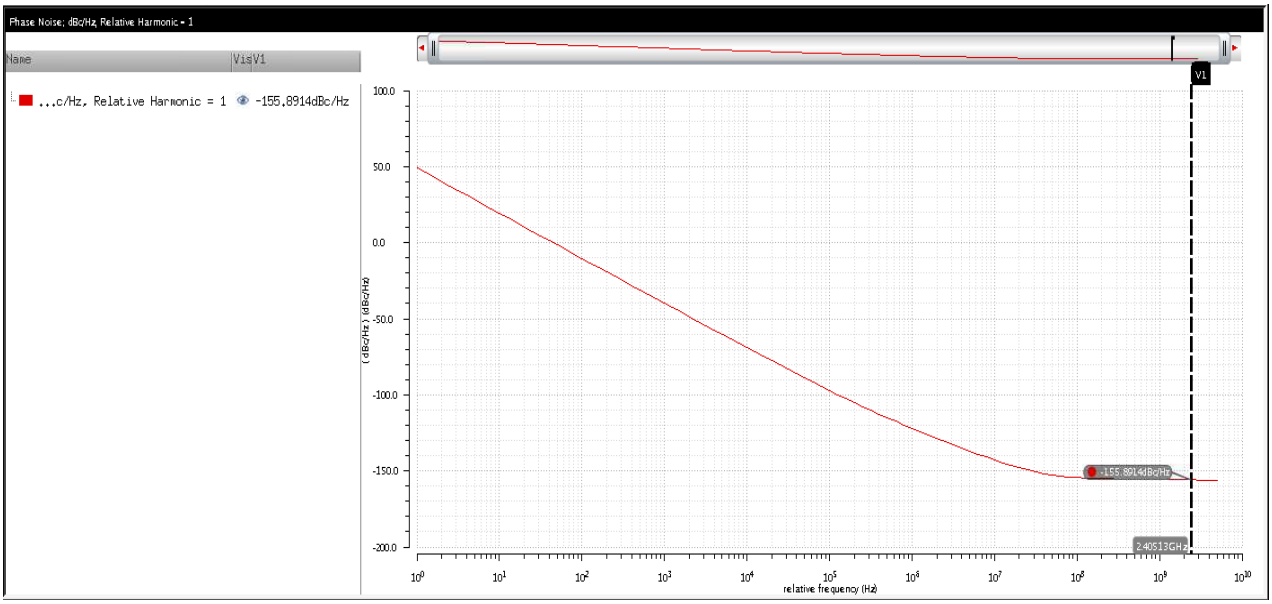

Figure 3.27: Phase noise of VCO.

At 495mV, the VCO should oscillate at 2.4GHz. Figure 3.28 shows the transient simulation of the VCO with an input voltage of 495mV.

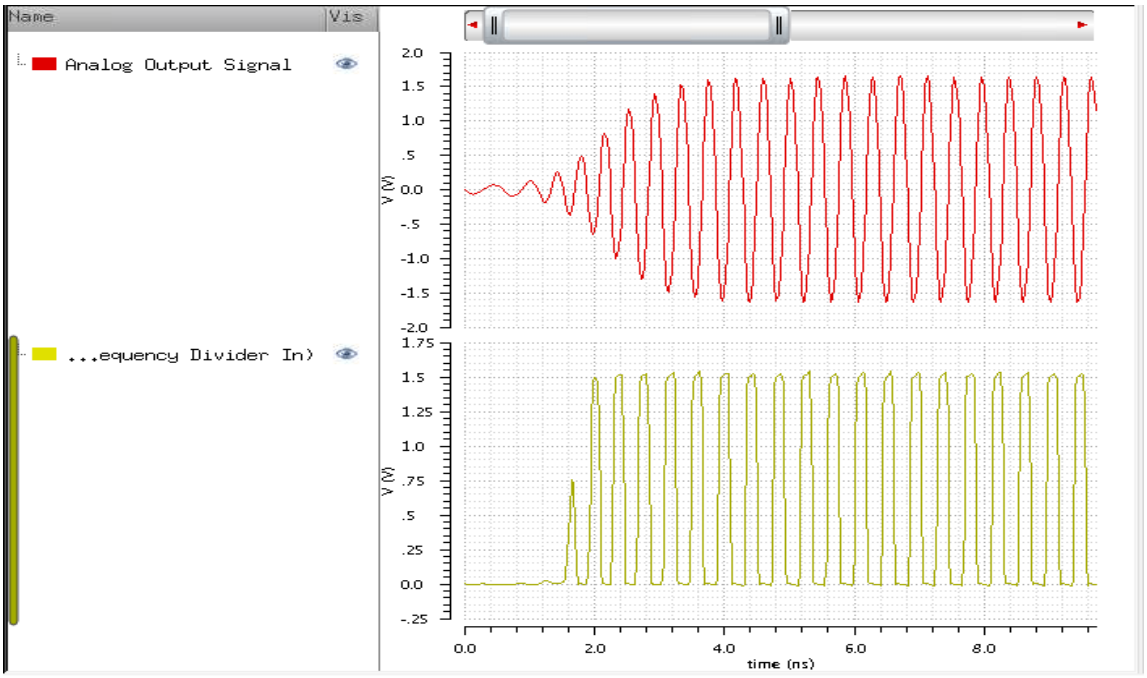

Figure 3.28: Transient simulation of VCO.

Figure 3.29 shows the DFT analysis for this input voltage. The output frequency is standing at 2.4GHz but there are some other spikes at some very close frequencies which in fact are not very dominant.

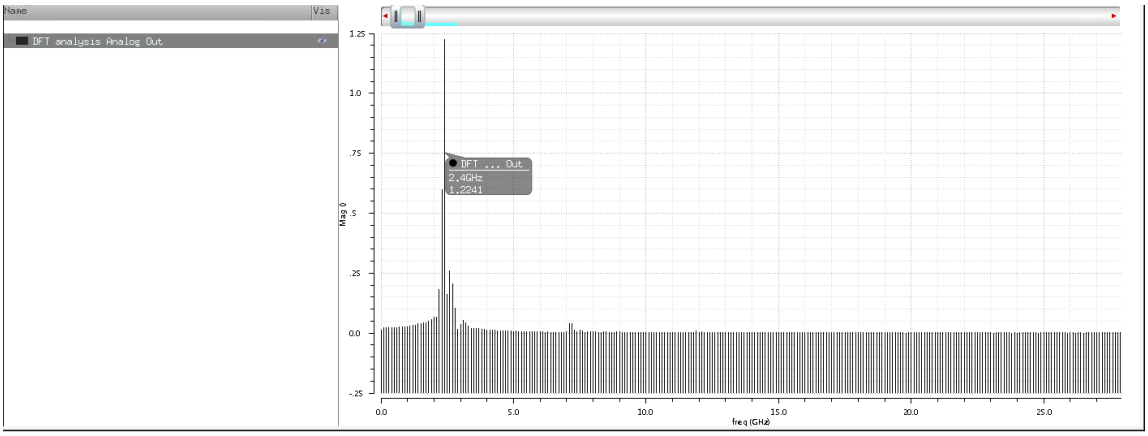

Figure 3.29: DFT analysis of the VCO for input voltage of 495mV.

3.3 Frequency Divider

PLL performs frequency devision of the input signal by a factor N. The overall circuit was shown in Chapter 2 also. The D Flip Flop used for the FD circuit is shown in Figure 3.30.

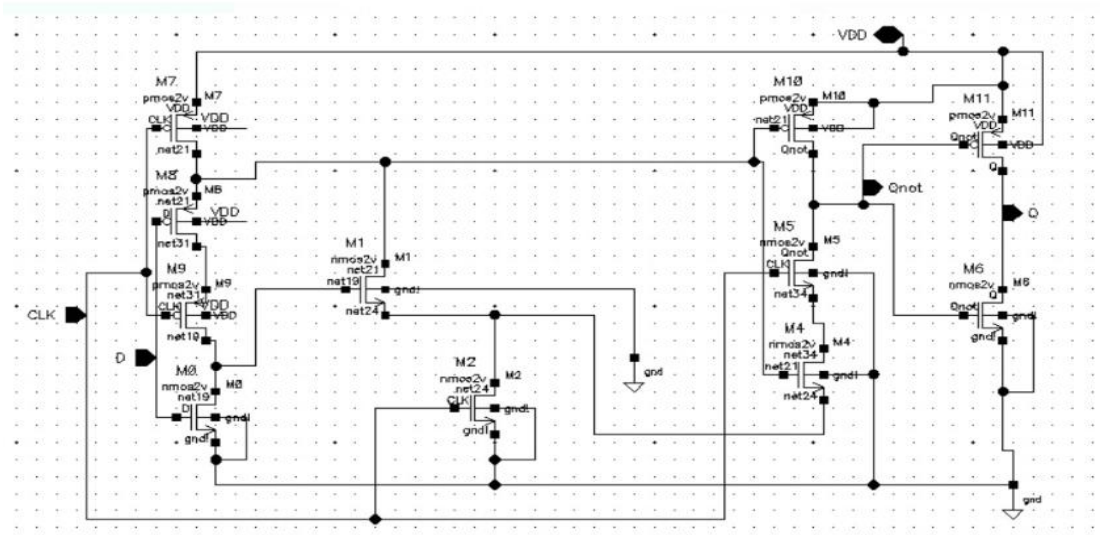

Figure 3.30: 2 by 2 frequency divider in Cadence.

The transistor widths (in um) for the D flip-flop are :

MOSFET	M0	M1	M2	M4	M5	M6	M7	M8	M9	M10	M11
W	0.36	0.36	0.36	0.36	0.36	0.36	0.54	0.54	0.54	0.54	0.54

Table 3.6: D Flip Flop transistor sizes

The channel length L of the transistors is : L=0.18 um. The connections and stages shown in Figure 3.31.

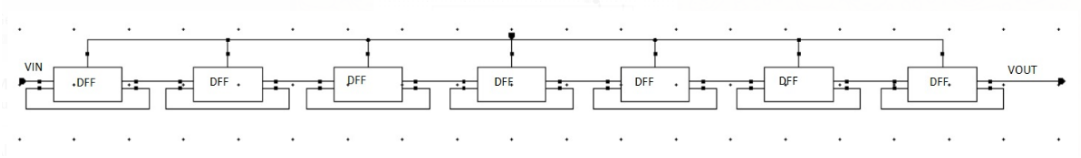

Figure 3.31: Frequency divider circuit N = 128.

The simulations for input 1st stage and the output are shown below:

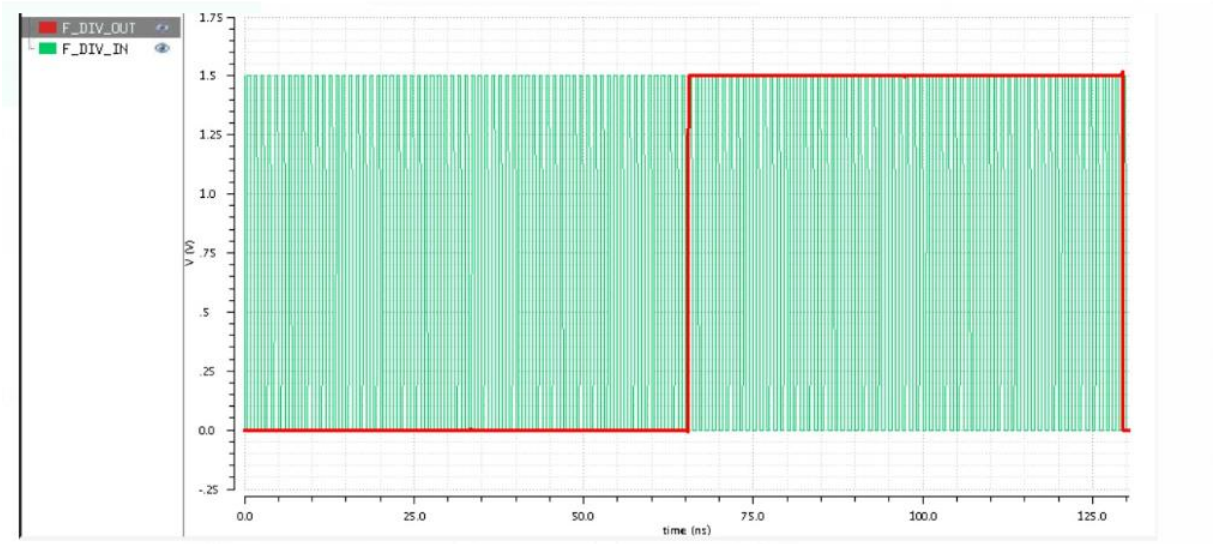

Figure 3.32: The result of the frequency divider input and output signals.

The output has a period of 1ns and the input a period of 128 ns.The output of the divider has 2^7 times the period of the 1st signal. This concludes the frequency divider.

3.4 Loop Filter

As mentioned at previous sections also, the loop filter will be a second order passive loop filter. Using an online calculator, second order loop filter values are calculated as shown in Figure 3.33.

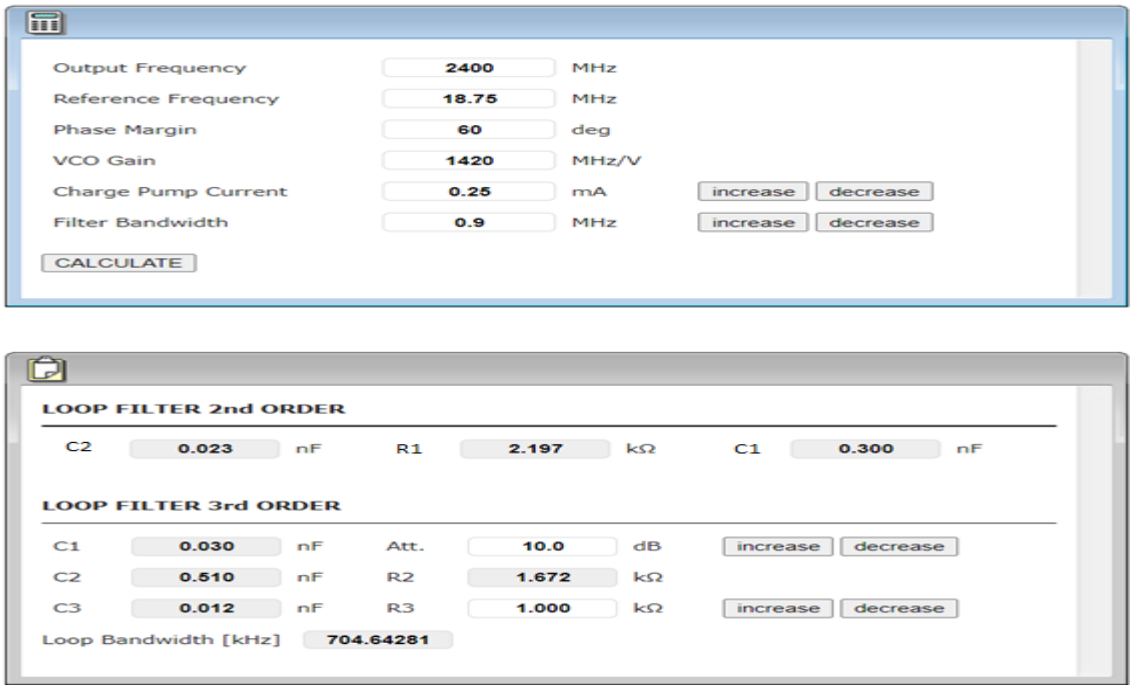

Figure 3.33: Loop filter values.

For the shown values in Figure 3.33 the circuit is expected to have no peaking behavior. Figure 3.34 is the transient analysis simulation of VCO input voltage when all the blocks are added to build the PLL.

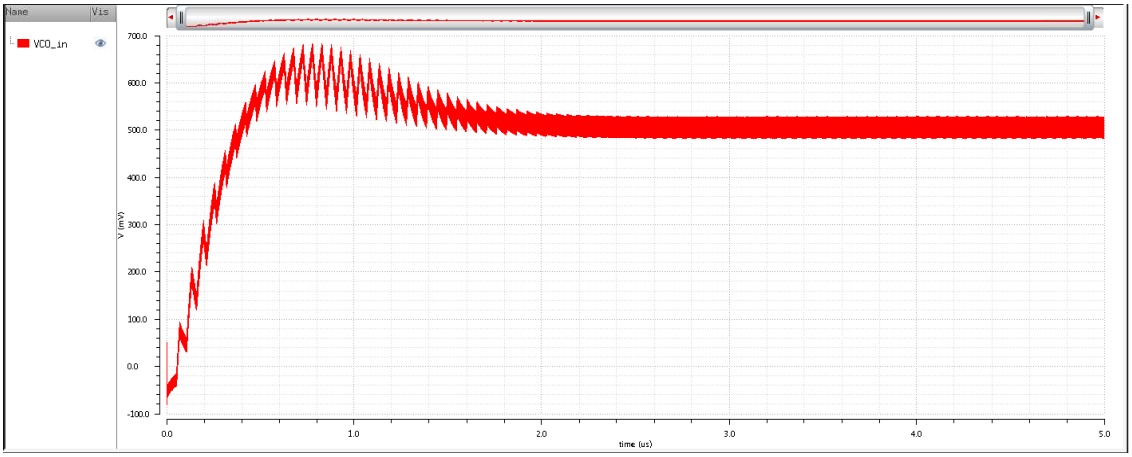

Figure 3.34: Transient analysis of VCO control voltage.

The waveform of Figure 3.34 is not good enough because there is a lot of high frequency content sitting on top of the desired signal. After numerous investigations, the problem was tackled. The reason why the high frequency signal stands on top of the actual signal is the designed VCO. The noise in Figure 3.33 usually happens when high capacitances are present in the circuit and is known as “Kick Back Noise”. As

shown in Figure 3.34, PLL is not locked properly. Because of the high frequency content on top of the desider signal, the output changes its phase and this is not desired. For this an OTA will be designed for a buffer application.

3.5 OTA Buffer Design

The designed OTA is shown in Figure 3.35.

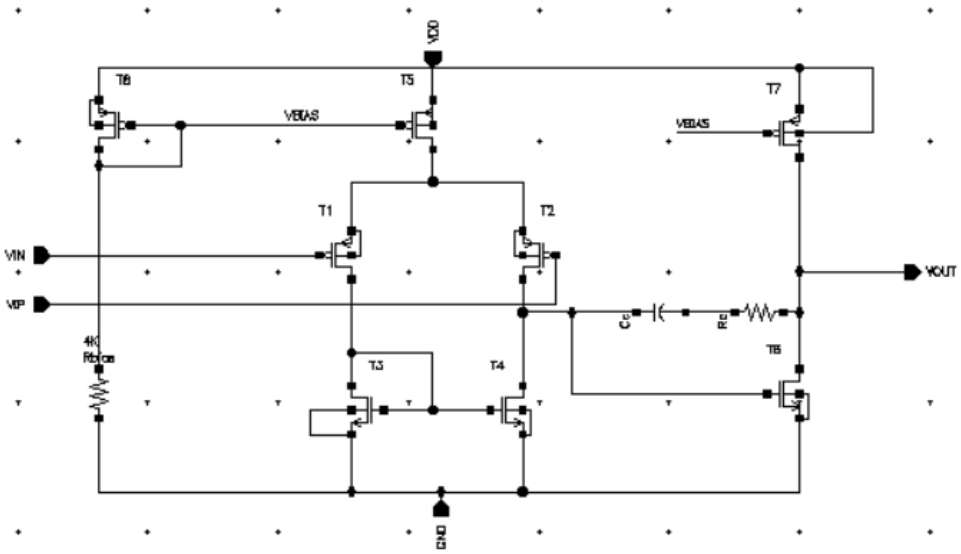

Figure 3.35: 1.5V OTA in TSMC0.18.

The sizes of elements are shown in Table 3.7. All transistors have a length of 1 um. This length is used in order to approximate the current equation with the equation studied on classes. R_{bias} = 4k ohm, C_c = 4pF and R_c = 145 ohm.

MOS	T1	T2	T3	T4	T5	T6	T7	T8
W/L	66/1um	66/1	16/1	16/1	112/1	192/1	572/1	112/1

Table 3.7: Sizes of OTA in Figure 3.35.

The AC analysis of the OTA in Figure 3.35 is shown in Figure 3.36. The designed OTA acts similar to a one pole amplifier circuit, which is usually a desirable scenario.

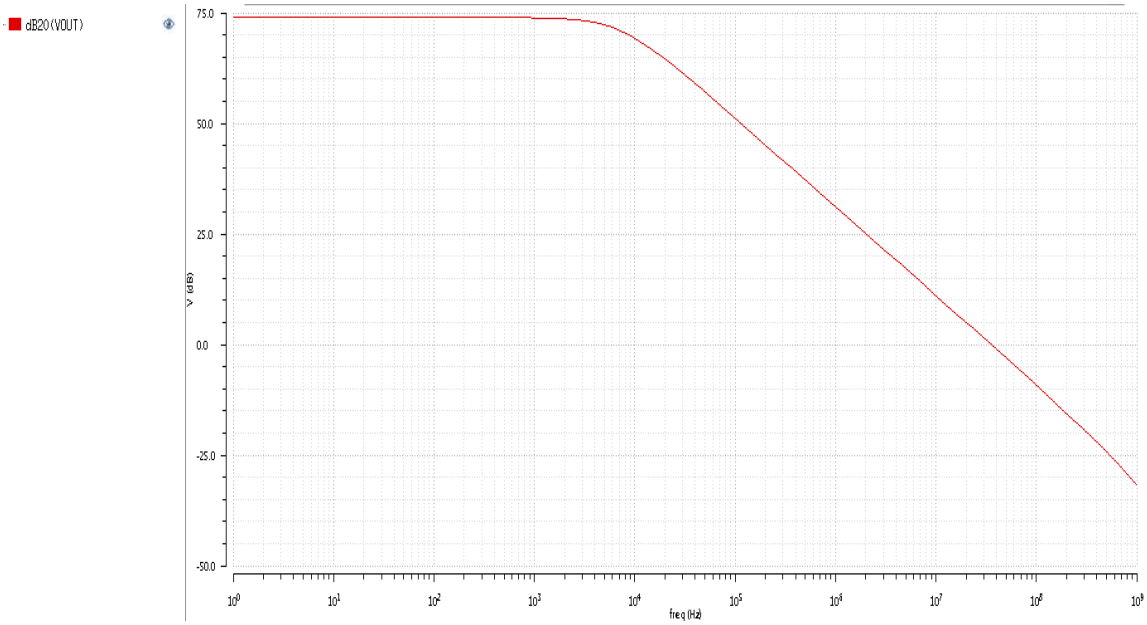

Figure 3.36: AC simulation of OTA in Figure 3.35.

Since the OTA will be used as a buffer circuit, it is very important if the output follow the input in a feedback configuration. Figure 3.37 shows how the output of OTA follows the input. As shown, the output of the buffer follows the input DC level. OTA will be loaded at the output with a low frequency node. Any high frequency signal coming from "VCO Kick Back" noise will be filtered out by that node. This buffer is added at the input of the VCO and it is used in a negative feedback configuration.

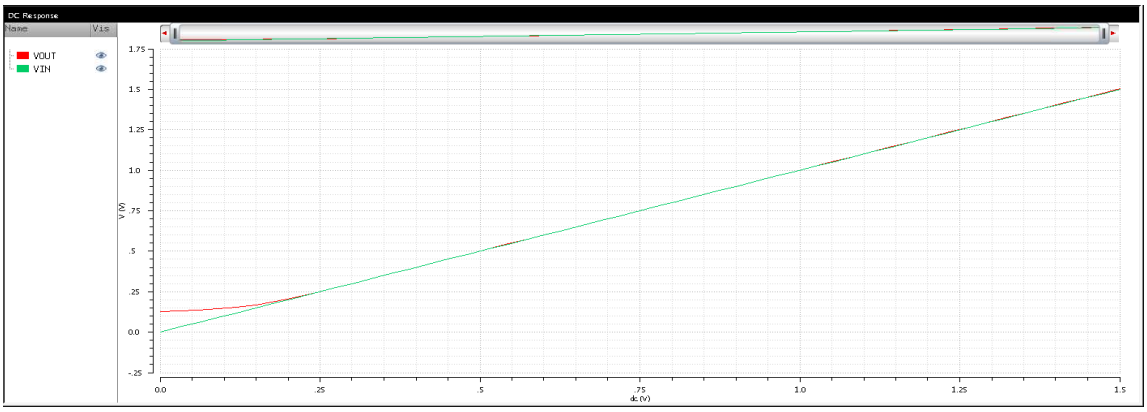

Figure 3.37: Output-Input Buffer dc simulation.

3.6 PLL

The whole PLL containing PFD-CP, LF, VCO and FD circuits is shown in Figure 3.38.

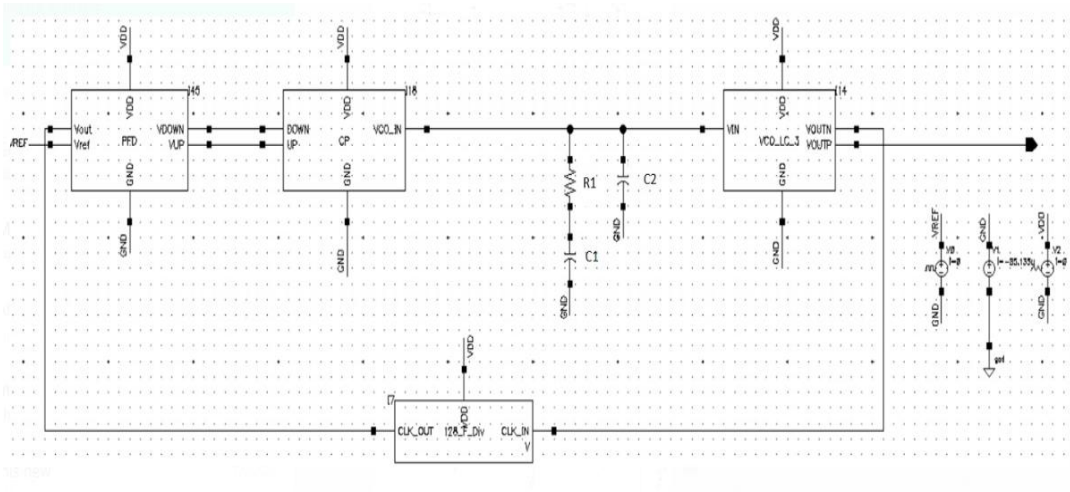

Figure 3.38: PLL Circuit.

Using the LF values shown in Figure 3.33 the transient analysis of VCO input is as shown in Figure 3.39. The VCO_in converges within 2% of the final value in 2.02us.

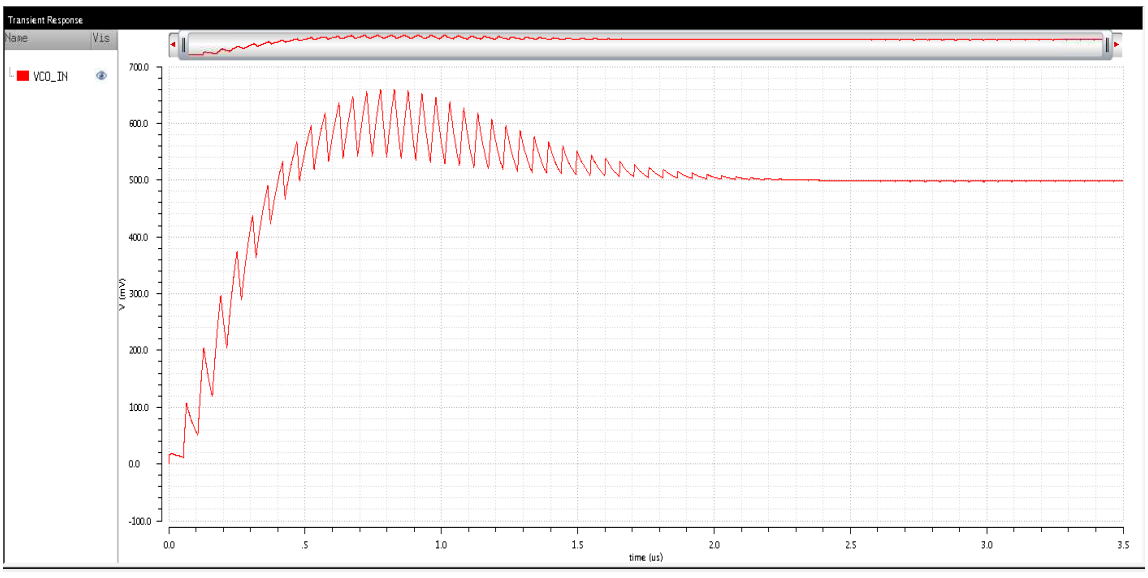

Figure 3.39: Transient simulation of VCO_in.

The high frequency content is removed from the signal. In Figure 3.26, for a voltage of 495mV, the oscillator is oscillating at almost 2.4GHz. The reference frequency for the PLL is 18.75MHz. The output of VCO should be 2.4GHz. From Figure 3.39, it can

be seen that the VCO_in settles to around 498mV. This value is very close to the 495mV calculated at Figure 3.26. Figure 3.40 shows how the output and input signal become phase equalized.

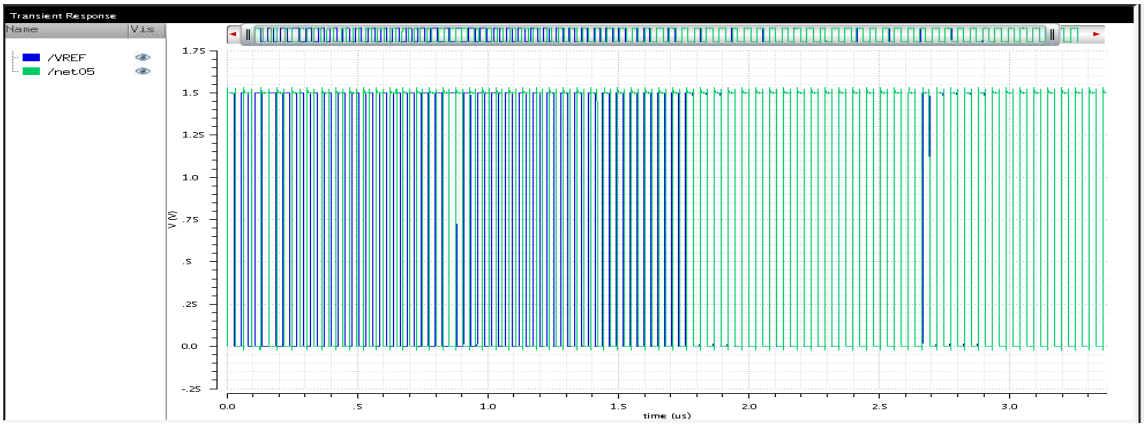

Figure 3.40: Input-Output phase matching.

The LF was changed several times in order to see the transient behaviour of PLL for different phase margins. The LF values are shown in Table 3.8 and the results are shown in Figure 3.41.

Phase Margin	R1	C1	C2
20	3.5k ohm	71pF	69pF
45	2.154k ohm	196pF	41pf
60	1.922k ohm	340pF	26pf

Table 3.8: Loop filters for different PM.

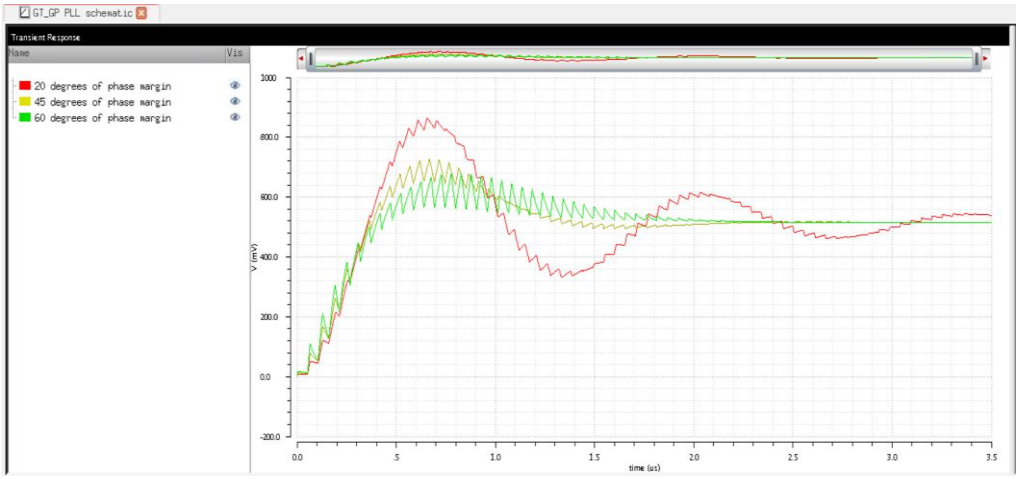

Figure 3.41: Transient response for different phase margins.

4. DESIGN OF CONTROLLER

The controller accompanying the PLL with the purpose of increasing its efficiency is going to be discussed and shown in this part. The controller' s parts are: 1st order filter, PD controller, V/I converter, Comparator and Enable/Disable Switch.

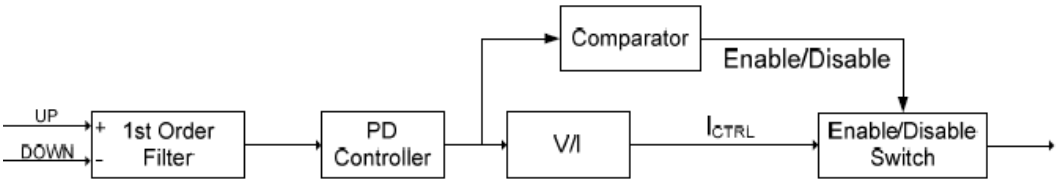

Figure 4.1: The general structure of PID controller.

4.1 1st order Filter

The 1st order filter is a type of filter which reduces the signal amplitude when the frequency of the signal increases above a certain limit. In our case it needs to filter the difference of the DOWN and UP signals, by using an OTA (Operational Transconductance Amplifier) which produces a current using a differential input. Since we want to detect and filter the change in the UP and DOWN signals it is appropriate to use an OTA producing a current based on this difference and then this current is filtered using a simple RC filter. The filter shown in the Figure 4.2 is a filtered voltage representing the error (difference) between the input signals.

The scheme of the 1st order filter is shown in figure 4.2 :

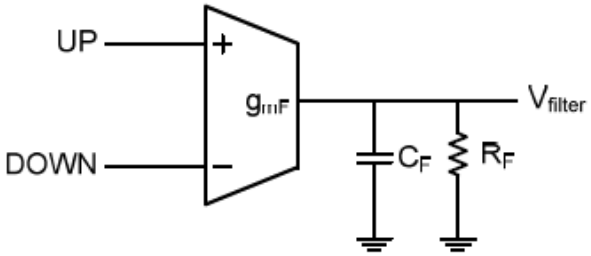

Figure 4.2: 1st order filter.

The most important circuit here is the OTA.

4.1.1 OTA design in Cadence

The OTA or the operational transconductance amplifier is an amplifier whose differential input voltage produces an output current. Basically, it is a voltage

controlled current source (VCCS).The transconductance of the amplifier is controlled by an additional current source. Basic operation:

Iout=gm(Vin+-Vin-);

Also, the input and output impedance variation is another characteristic of the OTA. OTA is characterized by a very high output impedance.

As stated by Uyanik(2007) "Since the difference between the UP and DOWN signals are either VDD or –VDD, the maximum output current, rather than the gm of the OTA, determines the filter behavior". So, in our design the maximum current and the bandwidth are the most important parameters to keep in mind during design.With the structure shown below in Figure 4.3, we designed OTA in cadence as shown in Figure 4.4

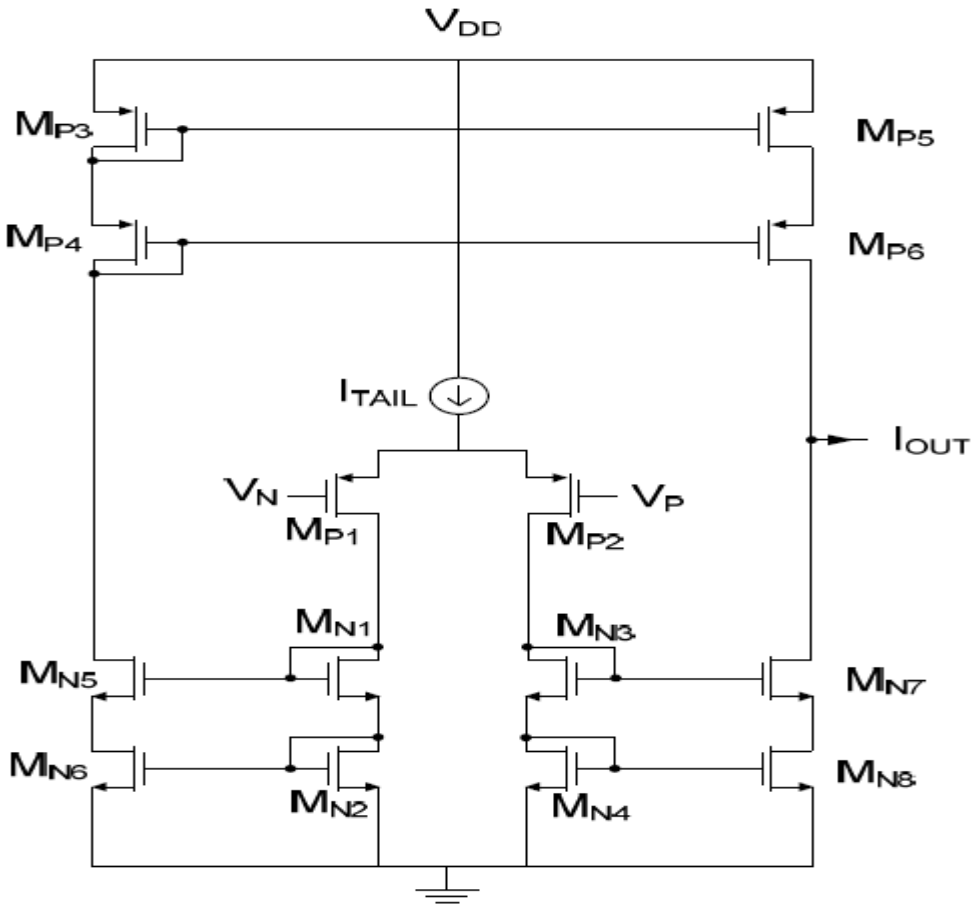

Figure 4.3: OTA general structure.

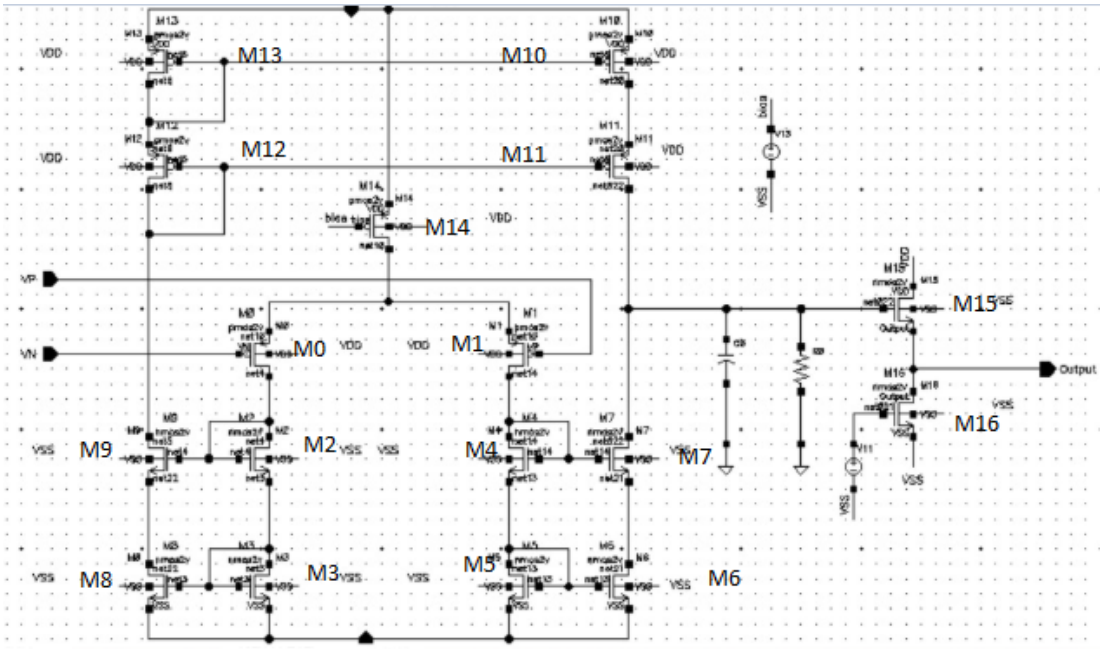

Figure 4.4: The 1st Order filter design in Cadence.

The sizes for the transistors are shown in the table below:

Transistor	M0 -M1	M2-M9	M10-M13	M14	M15-M16
W/L	5.68u/1u	2/1	4.31/1	5/1	1.6/1

Table 4.1: the OTA transistor sizes in Cadence for the 1st order filter.

As we notice from the figure 4.3 and 4.4 we have used a biased mosfet instead of the current source. The bias voltage is 0.97 V. The transistor sizing changes with application and with the block used (according to the required gm, maximum current and bandwidth required for the application). Also, the circuit in the Figure 4.4 contains the whole 1st Order filter design, not only that of the OTA. The general structure of this design was shown in Figure 4.2. The chosen R and C values are R=25K and C=1pF.

To demonstrate the working function of the 1st Order filter its AC analysis is given in Figure 4.5:

Figure 4.5: The AC analysis of the 1st Order filter.

The 1st Order Filter's cut-off frequency is 7.2542 MHz as given in figure 4.5. By this AC analysis we understand that the whole design does work as a filter. Depending on the application the filter can be designed for different bandwidths (changing the gm of the OTA and different RC values).

4.2 The PD Controller Design in Cadence

The PD controller is one of the most important parameters of the PID PLL controller. The PD controller is the part of the controller circuit proposed which controls the error. It increases the stability to the system since the D block is connected with the output response thus anticipating errors. To implement it we will be using an adder circuit using OTA-s and the derivative block. So the structure of the used PD controller is:

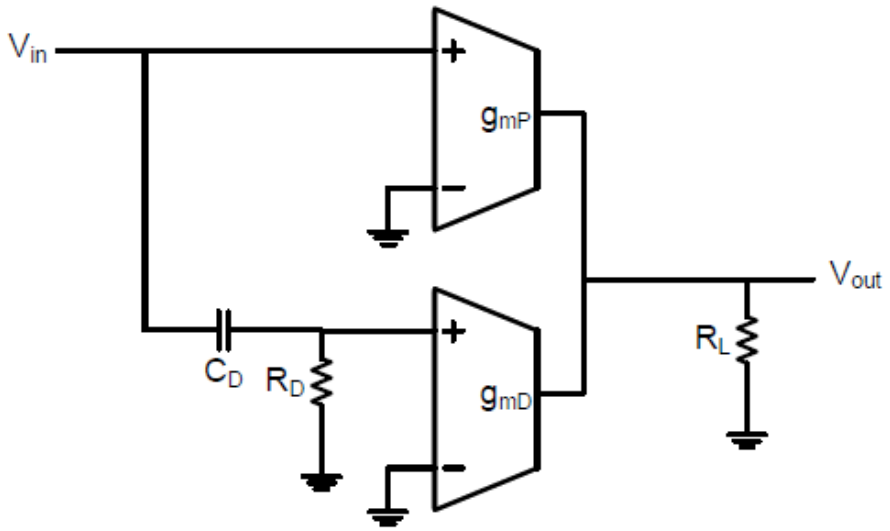

Figure 4.6 : The general structure of the PD controller.

$$H_D(s) = \frac{sR_DC_D}{sR_DC_D + 1} = \underbrace{sR_DC_D}_{Derivative} \underbrace{\frac{1}{sR_DC_D + 1}}_{1st\ order\ filter} \tag{4.1}$$

$$H_{PD}(s) = g_{mP}R_L + \frac{sR_DC_D}{sR_DC_D + 1} g_{mD}R_L \tag{4.2}$$

We can see from the (4.1) and (4.2) equations of the transfer function of the derivative block that the derivative block is realized using R_D and C_D. The resistance and capacitance product seems to give an important value, the K_D coefficient. The overall transfer function is then obtained by adding a coefficient Kp which basically just multiplies the input (4.3).

$$\text{: } K_D = g_{mD}R_L \text{ and } K_P = g_{mP}R_L \text{ .} \tag{4.3}$$

So, the PD controller changes the signal in a way that the input signal is transferred to the output and is added the derivative of itself in order to predict the change and that way prevent errors.

After understanding its working principle the Cadence design follows the figure 4.6: The OTA-s used in this part are the same as the one discussed in the 1st Order Filter except the sizes of the transistors which are instead like given below:

Transistor	M0 -M1	M2-M9	M10-M13	M14
W/L	57u/1u	16u/1u	57u/1u	90u/1u

Table 4.2 : The transistor sizes for the OTA-s used in PD controller.

This change in the transistor sizes is just to match the required gm, current and bandwidth.

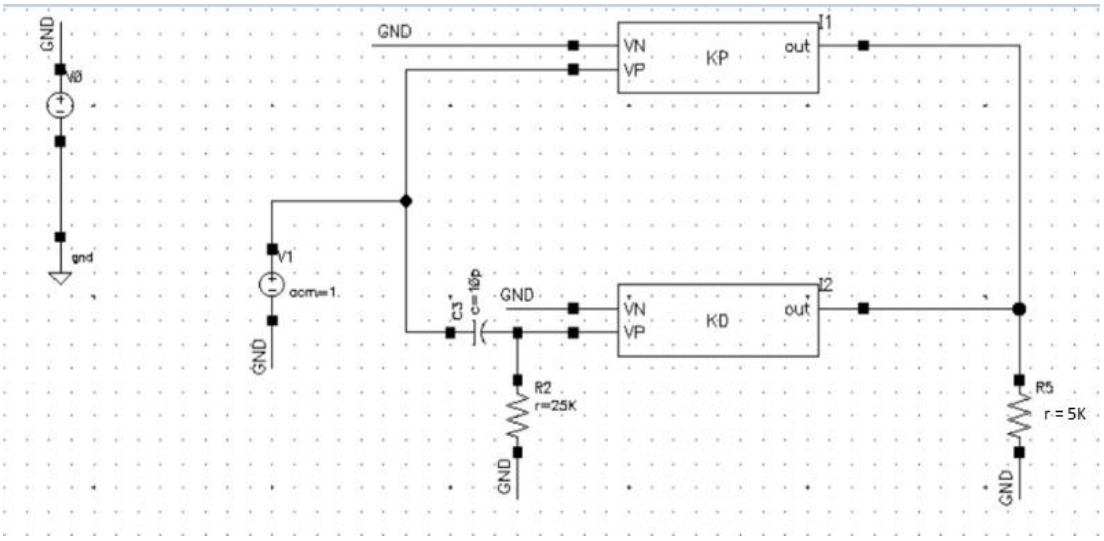

Figure 4.7: The PD controller design in Cadence.

From Figure 4.7, the PD controller contains two OTA-s (KP and KD). The output resistance R5 = 5K. The derivative circuit: R=25K and C=10p.

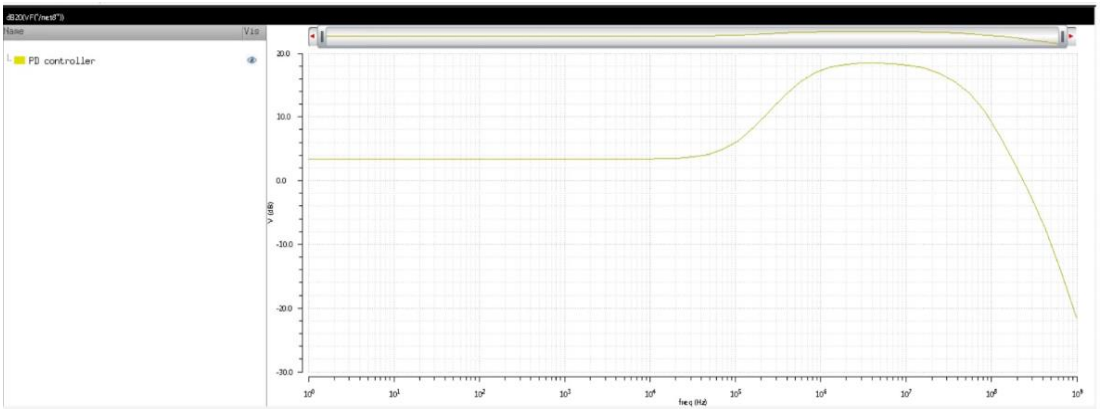

Figure 4.8: The PD controller AC analysis.

In figure 4.8 the PD controller's gain increases from almost 0 in low frequencies into almost 20dB in MHz range, which is our range of interest. Since 1st Order filter output AC analysis was shown in Figure 4.5 we can clearly see the change in the signal due to PD controller. This increase in gain of the signal will be later on important in deriving the control current.

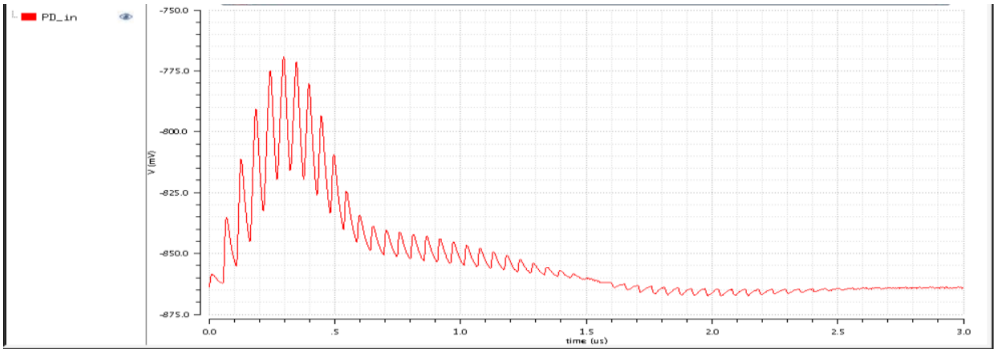

Figure 4.9 : The transient analysis of the PD controller.

The transient analysis of PD controller in Figure 4.9 shows that the signal becomes stable around -863 mV which is the DC level of the 1st Order filter.

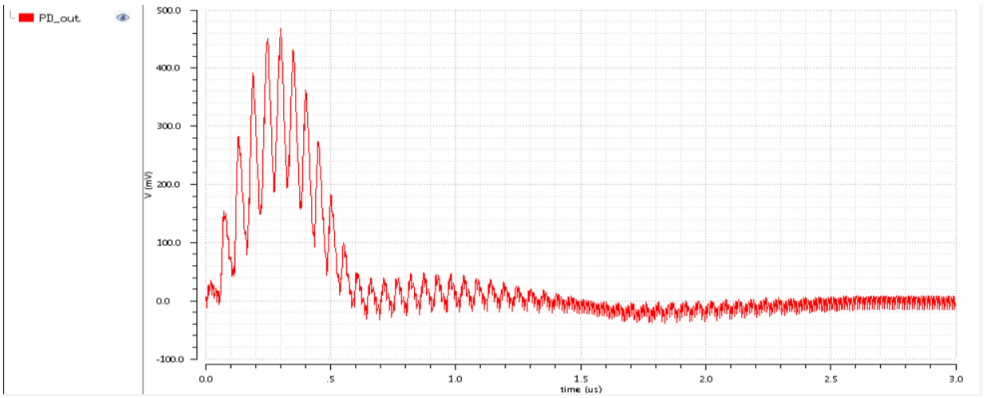

Figure 4.10 : The transient analysis of PD for no phase difference.

The signal in Figure 4.10 becomes stable for 0 V when there is no phase difference. This would automatically mean a 0 control current produced by the converter. The PD controllers' output is input to two different components.

4.3 V/I Converter

The V/I converter is a circuit that converts voltage into current. Since it has a very similar function with the OTA the only thing, we need to do is turn the input from differential into a single input. The inverting input is grounded so the OTA turns into V/I converter.

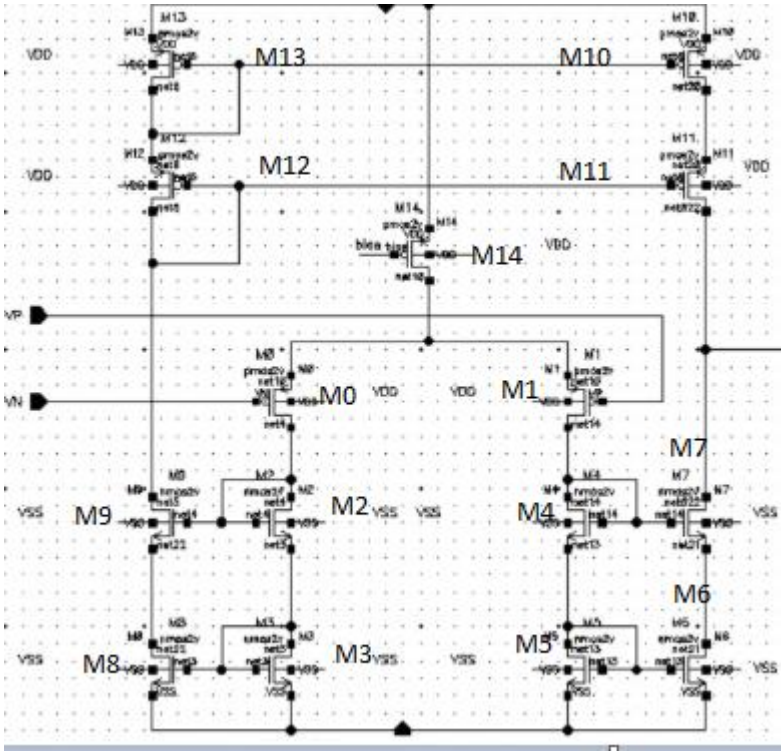

Figure 4.11: The V/I converter OTA.

The Cadence circuit for the controller is composed of only the OTA with its inverting input grounded. The OTA used in here is the same as the other OTA-s and with transistor sizes:

Transistor	M0 -M1	M2-M9	M10-M13	M14
W/L	57u/1u	16u/1u	57u/1u	90u/1u

Table 4.3 : The transistor sizes for the OTA used in the converter.

The V_P input is connected to the output of the PD controller.

The current output of the controller is Ictrl which is the current to be injected in the main PLL block in order to increase the efficiency by reducing the error faster and thus decreasing the settling time for the circuit. The Ictrl is going to be injected right before the VCO since here the oscillations are created and the current can regulate the voltage (by using the filter) which in turn controls the frequency and phase in VCO. But, we need to take measures so that the control current is helpful in the decreasing of error and not damage it as would happen if it is too large or too unstable so we should add another part on the PID. A circuit which checks conditions and takes an action for conditions being true or not. That is the comparator followed by a finite state machine (to check condition) and enable/disable switch.

4.4 Comparator, Finite State Machine and Enable/Disable Switch

4.4.1 Comparator

Comparator is a circuit which compares two voltages and takes two values, one for each condition. The circuit we used is the comparator circuit shown below:

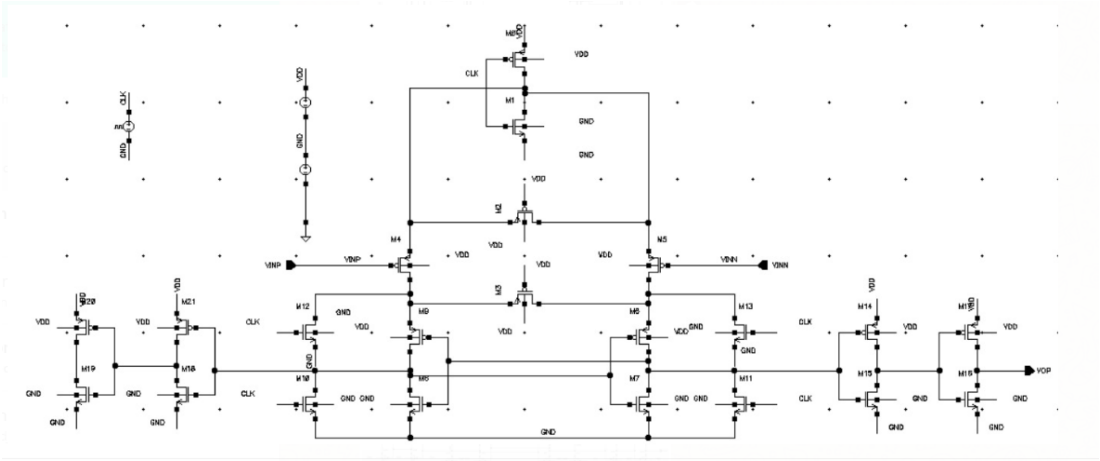

Figure 4.12 : Dynamic latched comparator design in Cadence.

The transistor values are given in the table 4.4:

MOS	M0	M1	M2-M3	M4-M5	M6,M9	M7,M8,M10, M11	M12, M13	M14	M15
W/L	1u/360n	500/360	500/180	4u/180	450/180	360/180	220/180	1u/360	500/360

Table 4.4: The transistor sizes for the Comparator

But for our comparation we need to check between two values so we need two comparators one for each value to be checked. -Vcomp = 50mV and Vcomp = 50mV.The general structure is shown in Figure 4.13:

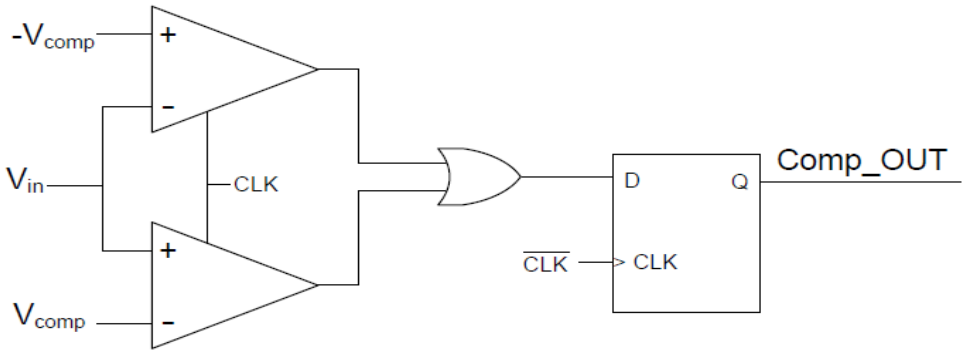

Figure 4. 13 : The comparator overall circuit.

Logically, the output of comparators is 1 or 0 when CLK is high and in the threshold value when the CLK is low. To keep the output constant during CLK changes, a D flip-flop is used .This kind of structure keeps Vin (Output of PD) between -Vcomp

and Vcomp. When Vin is not in the interval, Comp_OUT becomes logic high and the switch is enabled. After this the Comp_Out Output is analyzed by the finite state machine.

4.4.2 Finite State Machine

It is actually a simple circuit that uses 3 D-flip flops in order to check the conditions from the comparator. The structure is shown below:

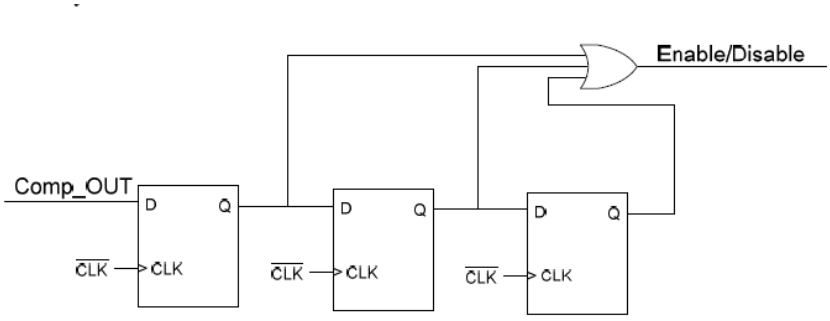

Figure 4.14: The general structure of the finite state machine

From this Figure we can clearly see that each of the flip-flops is used to preserve 3 states of the Comp_OUT or for 3 clock cycles. In this way it checks using an OR gate if there is any logic high present in the 3 cycles. Only if there is not the output of the OR gate will be 0 and so the controller will be disabled. It means that as long as the output of the PD controller is not out of the -50mV to 50mV region (and is staying there for at least 3 consecutive cycles) the PLL is working fine without the PD controller. When the PD controller's output is out of this range the PD controller is enabled to inject the Ictrl current. The cadence circuit for this finite state machine is shown in Figure 4.15:

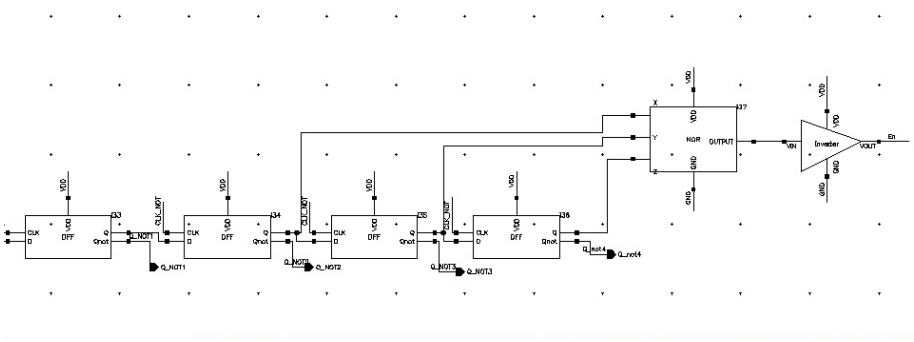

Figure 4.15: The finite state machine design in Cadence.

In the Figure 4.15 the input of the first D Flip Flop is the Q of the D-Flip flop of the Comparator. The OR circuit is realized by the NOR and NOT gates realized and explained before. We see that the output of this component is the En – Enable signal.

4.4.3 Enable/Disable Switch

The enable/disable switch is a simple switch which is enable for input high and disable for input low. It is easily realized is CMOS. The general structure is shown below:

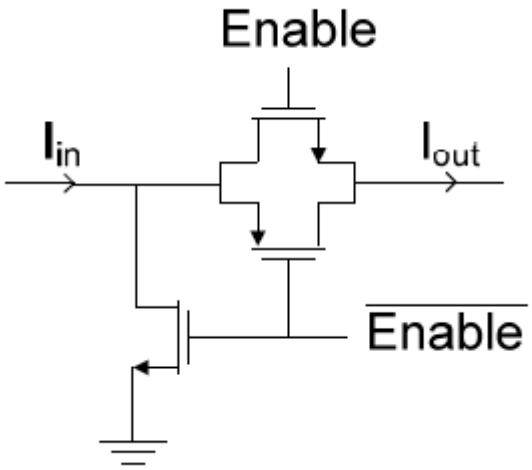

Figure 4.16: The enable/disable switch in CMOS.

The structure is very straightforward to understand. When Enable is high the Enable_not is 0 so the upper NMOS and PMOS transistors are on and Iout = Iin since the lower NMOS is off. So, in this case the current can pass through. The other case when Enable is low and Enable_not is high the only on transistor is the low NMOS that completely grounds the current and does not let it pass through to Iout and so

Iout = 0. In this case the current is blocked so the controller is not interfering in the PLL block.

The cadence circuit for the switch is shown in Figure 4.17.

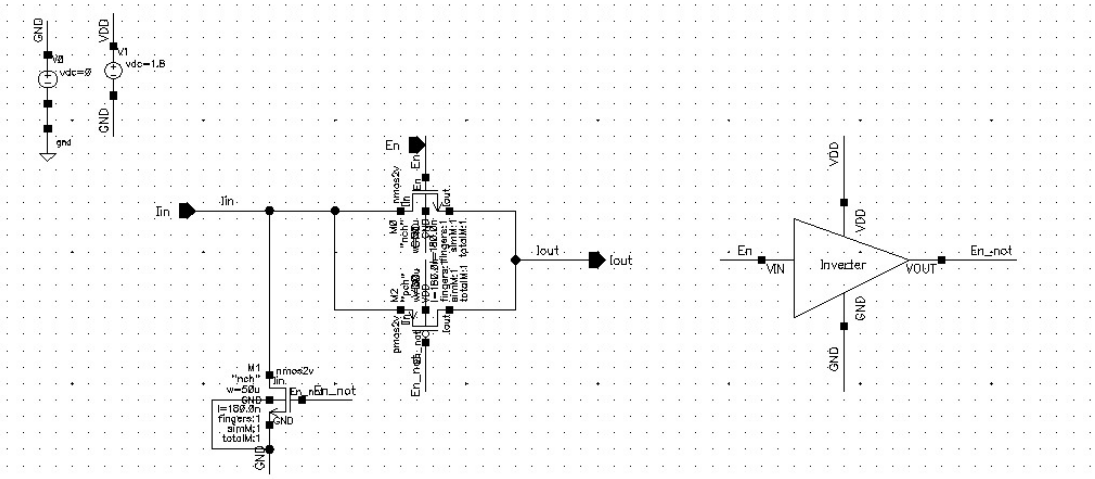

Figure 4.17: The switch in Cadence.

The final controller circuit is:

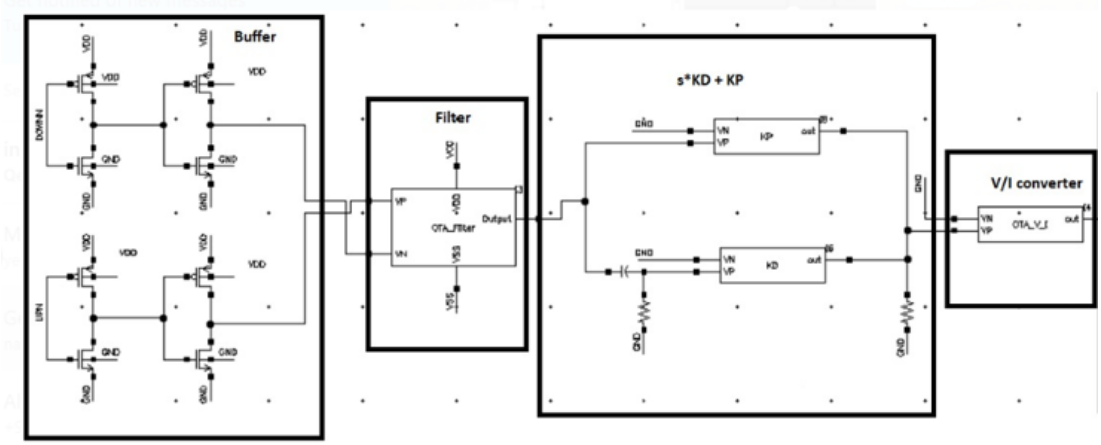

Figure 4.18: Final controller circuit.

After simulations, the comparasion between PLL and PID PLL are shown in Figure 4.19. It can be seen very clearly that the settling time decreases.

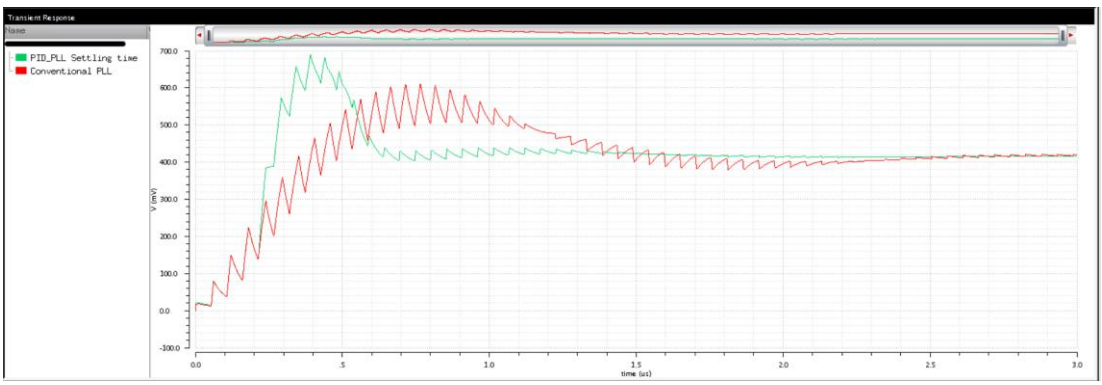

Figure 4.19: Comparison between the settling time of PLL and PID PLL.

5. Conclusions

The goal of this thesis was the design of a PLL which can be used boradly in communication systems. The basic PLL has these main blocks: PFD, CP, LF, VCO and FD. All these circuits where designed and optimized to get a good settling time. In this project, we have seen the PLL as a controller block also and by knowing how the PID systems work, we have tried to reduce the settling time of the PLL by means of a PD controller added to the circuit. The PID controller finds the derivative and the integral of the phase error and adds those contributions to the actual phase difference. This makes the circuit settle much faster than usual cases. All the PLL components are analysed and designed it in Cadence and optimized using methods and circuits explained in the previous chapters. But, the additon of PD controller improved the settling time as can be seen from the graph in the Figure 4.14 from almost 2.3 us to 1.3 us. So the settling time is improved by almost 43%. This is a result of the injected control current which works in changing the output phase faster in the direction of the input phase. This is done by not disturbing the main circuit when the phases are already near. When detecting a very large phase difference the controller interferes by injecting a current that contains the derivative of this difference, so the output phase is forced to change in the direction of the input phase. This current is injected in VCO input so it directly affects the phase of the output which in conclusion helps improve the settling time. There is of course big room for improvments but in this project we showed that this type of PLL implementation works and to improve the settling time even further, we need to optimize the design components even further.

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CURRICULUM VITAE

Name Surname **:** Gerald Topalli

Place and Date of Birth **:** Babrru Qender, Albania, 09.03.1998

E-Mail **:** topalli16@itu.edu.tr

EDUCATION

- **B.Sc.** **:** 2016-2020- ITU, Electronics&Communication Engineering

PROFESSIONAL EXPERIENCE:

01/2019–02/2019 Intern- ITU VLSI Labs

During this Short-Term internship, I gained insight on Cadence by building and simulating different types of Analog and Digital Circuits. Some of the circuits that I built during the internship were the 2-stage Folded Cascode OTA, Digital Comparators, 8-bit counters and some simple registers. In the end I used the digital comparators and 8-bit counter to build a simple A/D.

03/2019–05/2019 Intern- ITU VLSI Labs

In this internship I designed various blocks such as Phase Frequency Detector, Charge pump and VCO. All these blocks are core components of Phase locked loops. The designs were made in TSMC 0.18um technology.

SKILLS:

- Analog Circuit Design (VLSI)
- RF Microelectronics
- Digital Circuit Design
- Active Microwave Circuits
- Cadence
- Verilog (FPGA, Nexys 4DDR, Xylinx) / Vivado
- PSpice
- Assembly
- C/C++
- AWR beginner
- Electromagnetic Field/waves
- Microwave Engineering
- Matlab

REWARDS:

- Upper First-Class Student
- Ranking 3-rd in the Electronics and Communication department
- 7 Semesters in the Deans' High Honor List
- Albanian Ministry of Education Scholarship for very high achievements in High School Exams → Full Scholarship in Istanbul Technical University
- Seven times Olympiad winner in Math and Physics in Albania.

CURRICULUM VITAE

Name Surname **:** Kamela Dokaj

Place and Date of Birth **:** Albania, 12.03.1998

E-Mail **:** dokaj16@itu.edu.tr

EDUCATION

- **B.Sc.** **:** 2016-2020- ITU, Electronics&Communication Engineering

PROFESSIONAL EXPERIENCE:

Intern- ITU VLSI Labs

Designed Digital Circuits components like Schmit Trigger, Ring Oscillators, buffers etc.

Intern- ITU Wireless Communication Labs

Helped in a new project in OFDM for wireless communications by writing matlab codes and designing in Labview.

SKILLS:

- Cadence
- Lab View
- Matlab
- Vivado
- Filters
- Receivers / Transmitters

REWARDS:

- Upper First-Class Student
- Albanian Golden medal for high achievements in Matura exams
- “The Best Student of the Year” Certificate by Bab Dude Karbunara High School.