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MOS Gilbert Cell

Introduction

Gilbert Cells are very common blocks encountered in RF circuits. By means of Gilbert Cell multiplication, modulation and phase detection can be done. This are all very important functionalities. For instance, by means of the multiplication property, we can produce an AM modulation circuit, natural sampling circuit, PFD circuit etc. On the next couple of pages, I will try to explain every step that I did for the design of the Mosfet Gilbert Cell.

Circuit Design

The very first thing that I did is building a current mirror. I will be supplying 2 mA to the Gilbert Cell and for that I build a current mirror to handle that. The DC value of the output of the final Gilbert Cell should be around 0.8 to 0.9 V for a VDD = 1.8. The supply voltages that I am using for the design of the circuit are 0 and VDD. The current mirror that I build is shown in Figure 1. I have calculated their sizes and I assumed having a vdsat of 150mV for T7 and T8 because I will need to fit a lot of transistors in only 0.8 V (output to ground). Having a smaller vdsat will mean that I will make [the transistor bigger, thus being able to conduct enough current for small vds values.

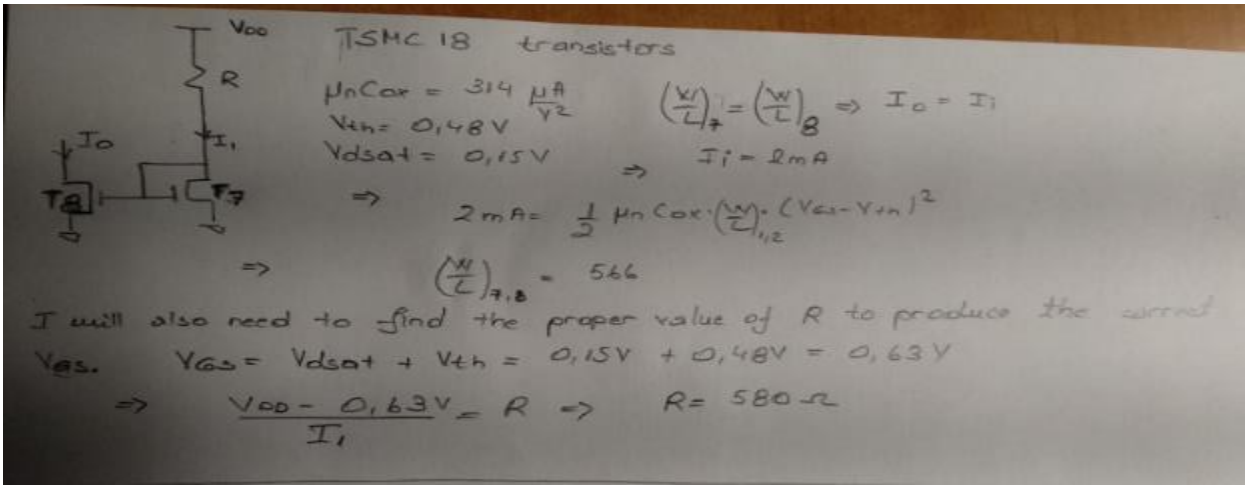


Figure 1

I then put these sizes in Cadence design environment and I run a dc analysis. The results from the dc analysis are showing in Figure 2. Please note that the current mirror is the circuit within the red box. I think the produced values are fine and please note that I have all the transistors saturated.

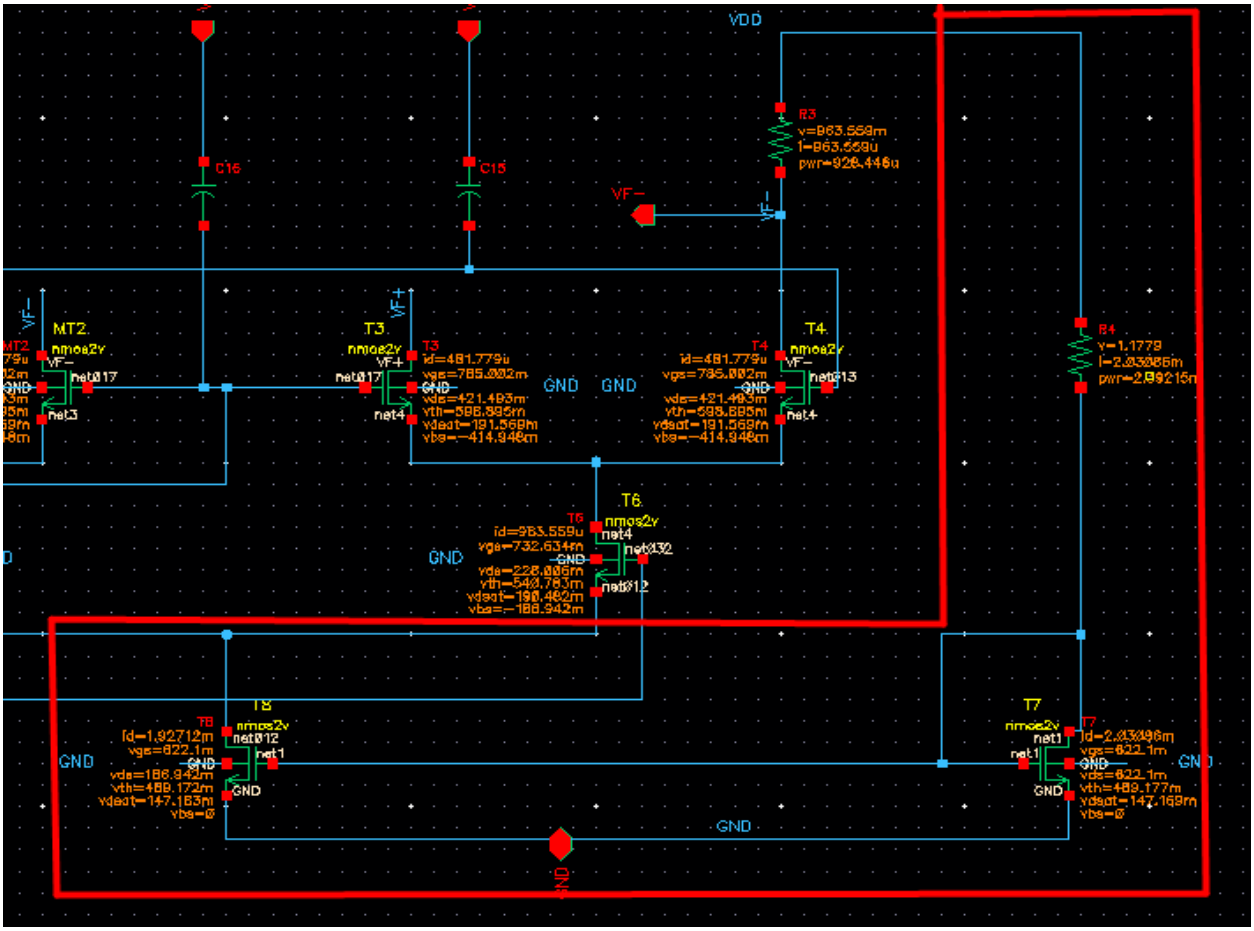


Figure 2

In the next step I studied the DC biasing of the transistors. Please refer to Figure 3 for the explanation.

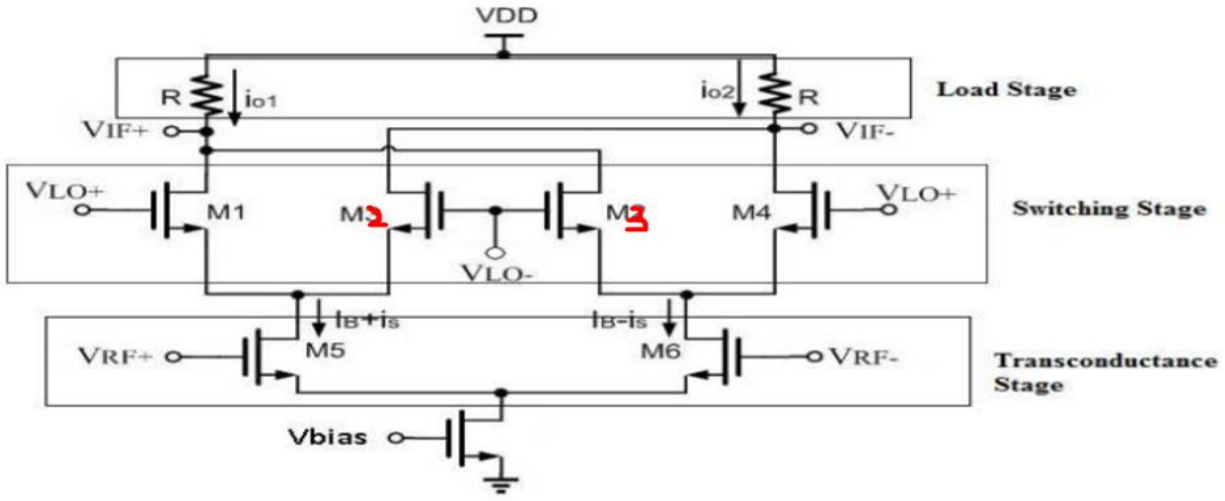


Figure 3

VIF+/- will stay at around 800mV. That would mean that I can connect the DC of VLO signals at values VLO < 0.8 + vth. Since the source of the switching stage transistors of Figure 3 is not connected to ground, I expect the vth for those transistors to increase to at least 600mV. So roughly, VLO < 1.4 but it cannot be too low because I need the transistors of the transconductance stage and the current mirror to be biased in saturation for proper functioning. I decided to give the VLO a DC value of 1.2 V. I decided to bias the current mirror near the edge of saturation, so I decided to leave about 150mV to the current mirror. From my past experiences, the transistor needs around 780mV of VGS in order to work on the strong inversion region. By doing that I selected the DC of VRF = 150m + 780m = 920 mV. I designed this circuit by using some voltage dividers as is shown in Figure 4. The Cadence simulations also confirms these values.

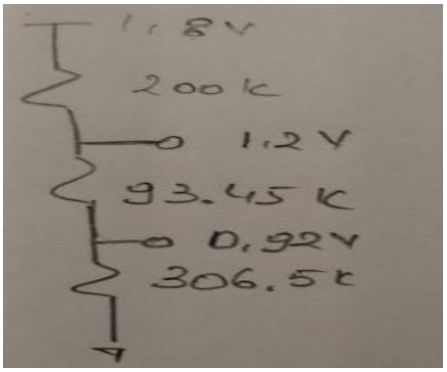


Figure 4

On the next step I went onto the design of the Gilbert Cell. I used tsmc18 cadence library for its design. Figure 5 shows my hand calculations for their sizes. In order not to make them very big, I increased the vdsat of the transistors M3-8 to 200 mV.

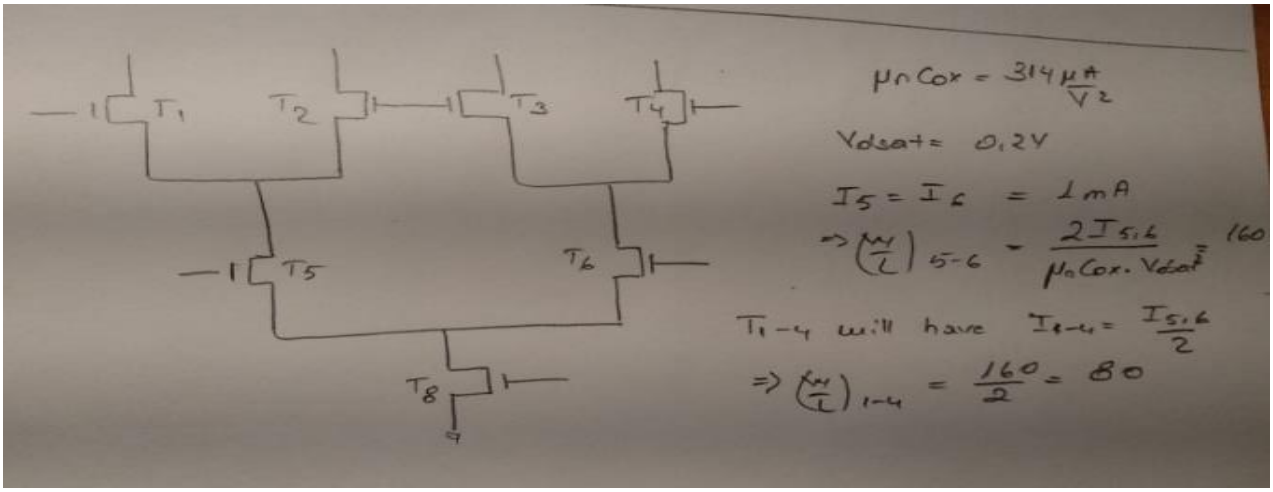


Figure 5

The current to voltage converter for this circuit is a resistor and I added a 1k ohm resistor. The Gilbert Cell implemented in cadence is shown in Figure 6.

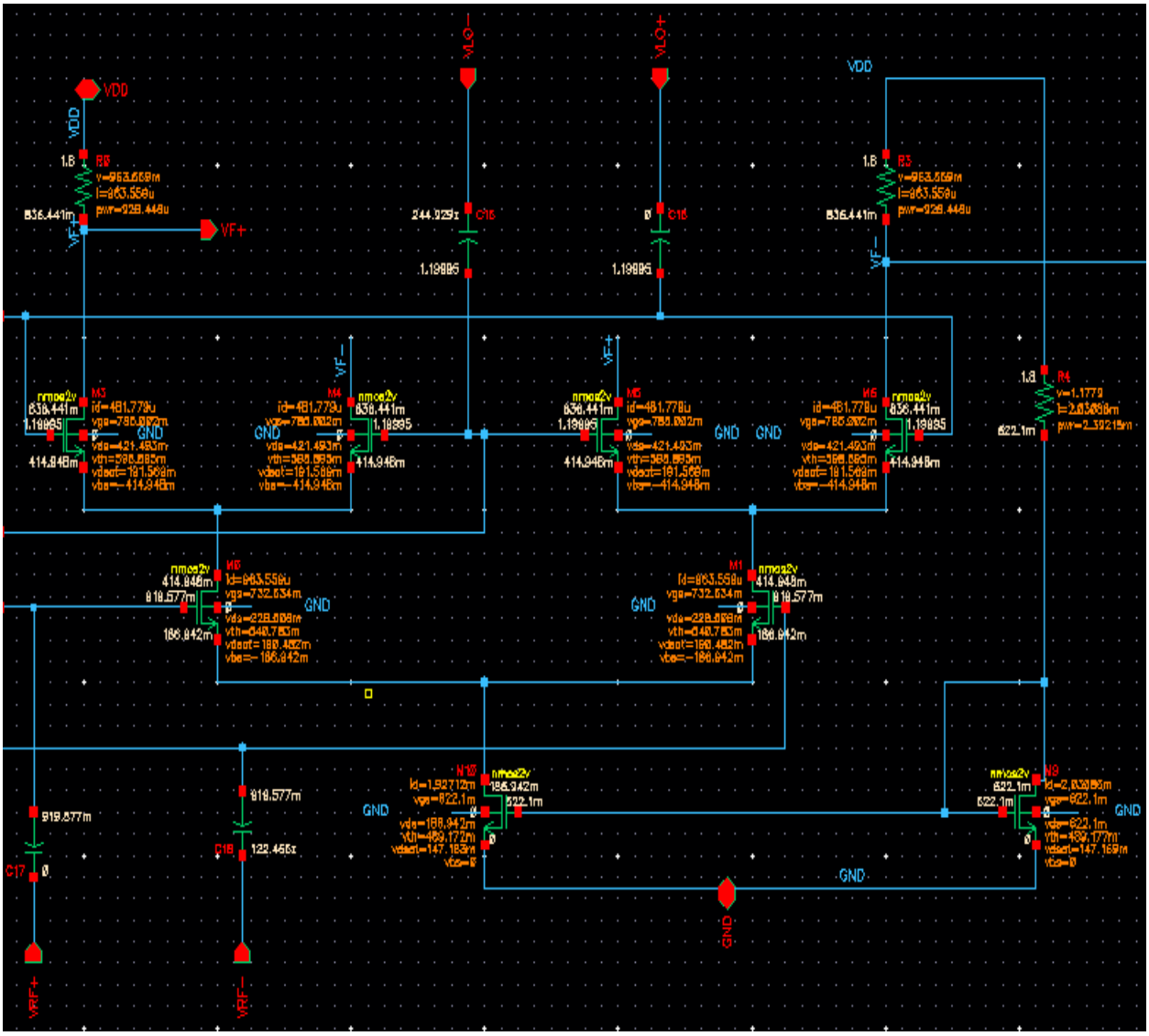


Figure 6

This is the circuit I designed. There are major problems to be solved here. Firstly, I haven't biased the inputs of the transistors yet because I need to come up with a biasing method where the dc and the ac parts of the circuit will be separated. For this, I used some coupling capacitors and resistors with respective values of 0.1uF and 2.2k. In Figure 7 I have included the coupling capacitors and the resistors. The coupling capacitors will be considered a short for the frequencies that we are working whereas the resistors are important for the input impedances of the device. The input impedances are important in RF circuits because in order to achieve the highest possible power transfer, we need to match the input of the device with the output of the previous stage. The new added elements are shown in red boxes in Figure 7.

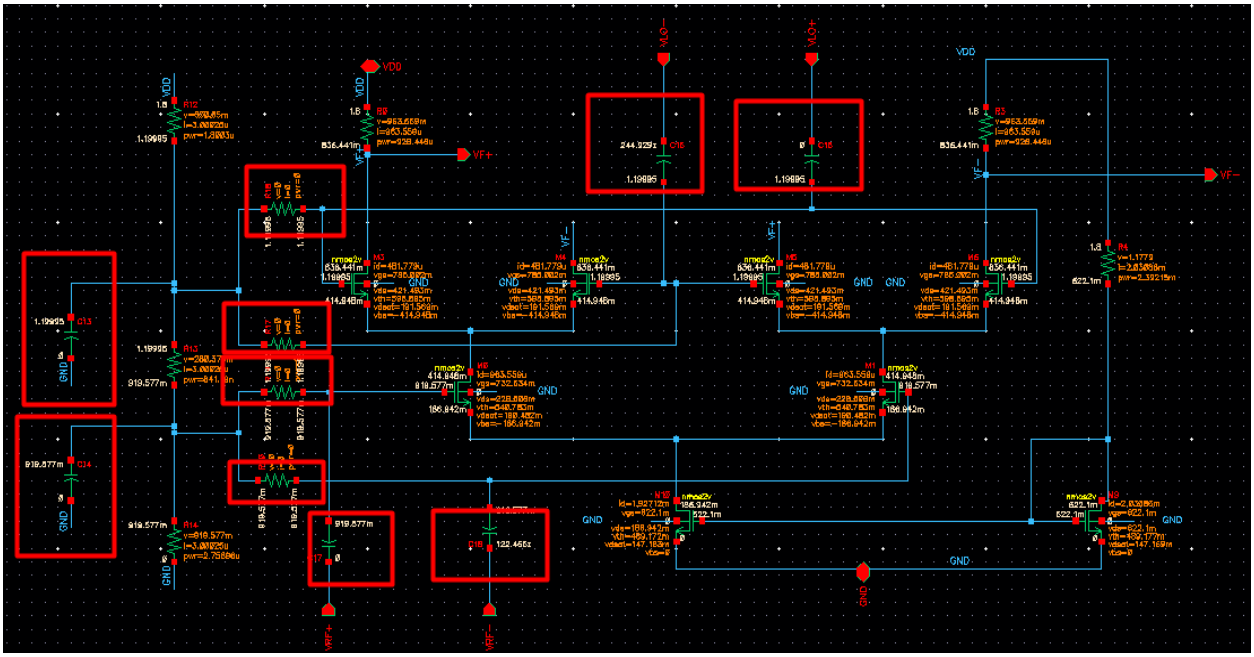


Figure 7

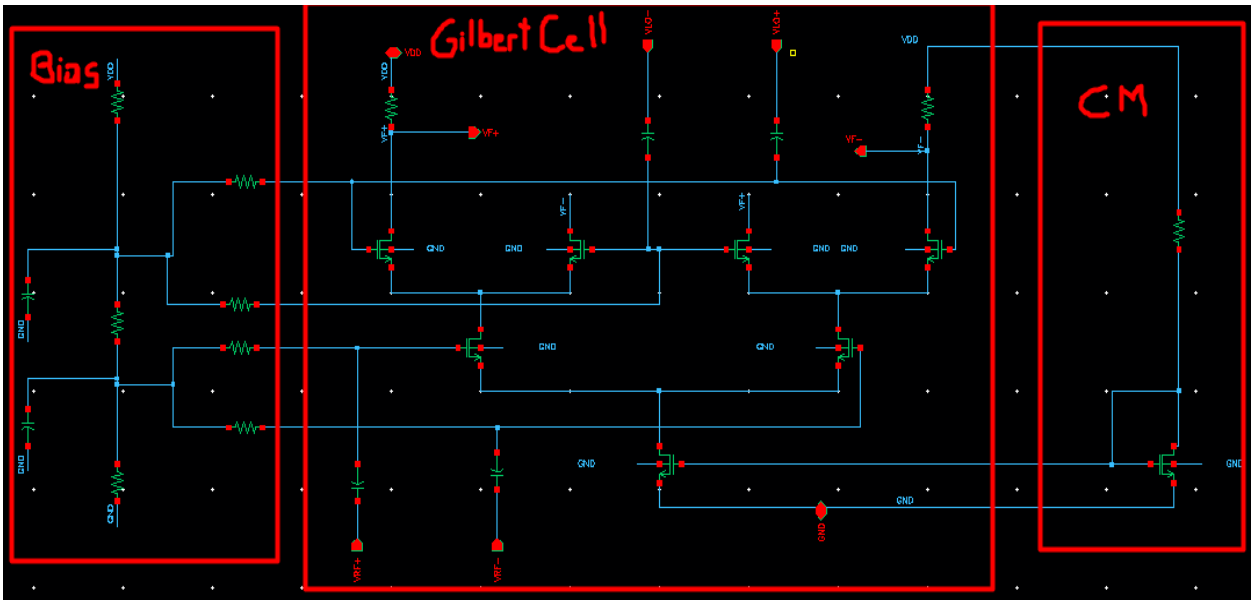


Figure 8

Figure 8 shows all the stages that I am using to build the Gilbert Cell that I will use for the purposes I talked on the introduction section. All the transistors are placed in saturation and I think they are well functioning. I will also need to make the output differential and for that I designed the differential pair shown in Figure 9. This is an extra circuit if we need the output single ended.

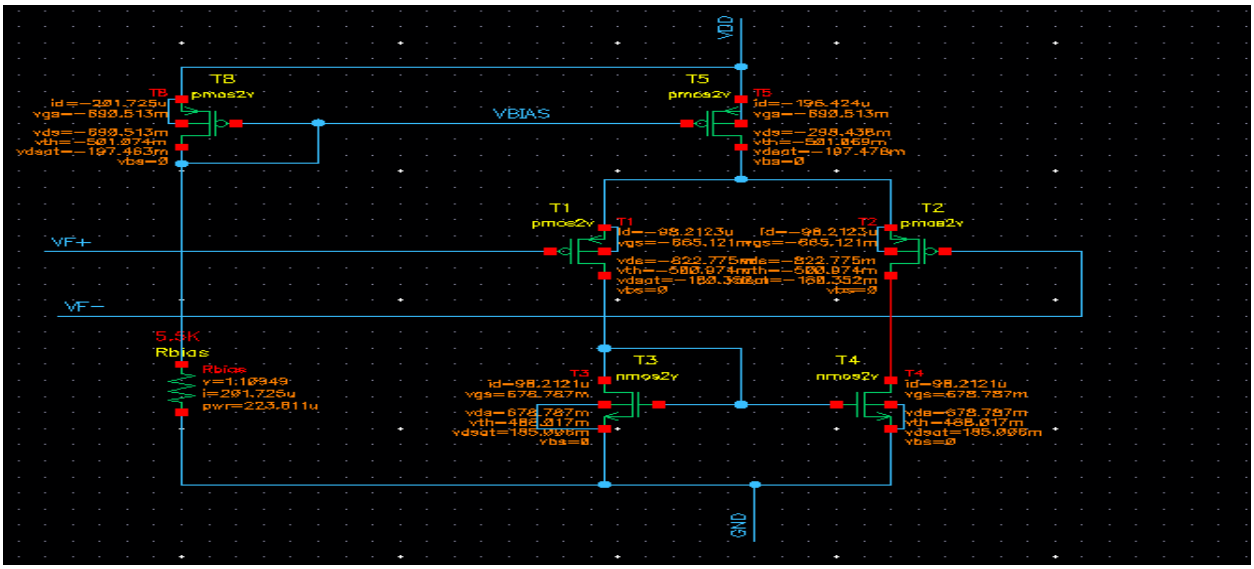


Figure 9

I wanted to have around 100uA flowing through T1 and T2, so the tail current which is supplied by T5 should be 200uA. I usually select equal sizes of T5 and T8. T5 and T8 and the Rbias is a very simple current mirror. To produce 200uA at T8 I showed the calculations in Figure 10.

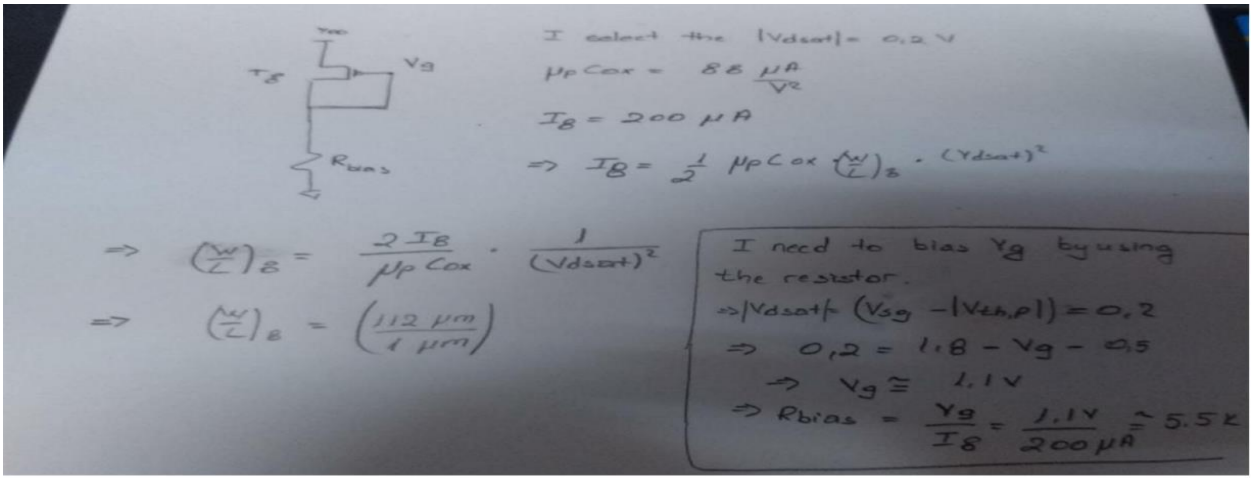


Figure 10

T5 = T8 are equal and the Rbias = 5.5k Ohms. For these values I run a DC test in the circuit and I found a current of 201uA at the T8 and T5. Without much effort, I selected the T1 and T2 just by knowing that the current of T5 will be twice the current in T1 or T2, thus I just need to divide the width of T5 by 2. So (W/L)1 = (W/L)2 = 66. For T3 and T4, I need to do an analysis since they are implemented in NMOS. Figure 11 shows the calculation I did to select the widths of T3 and T4.

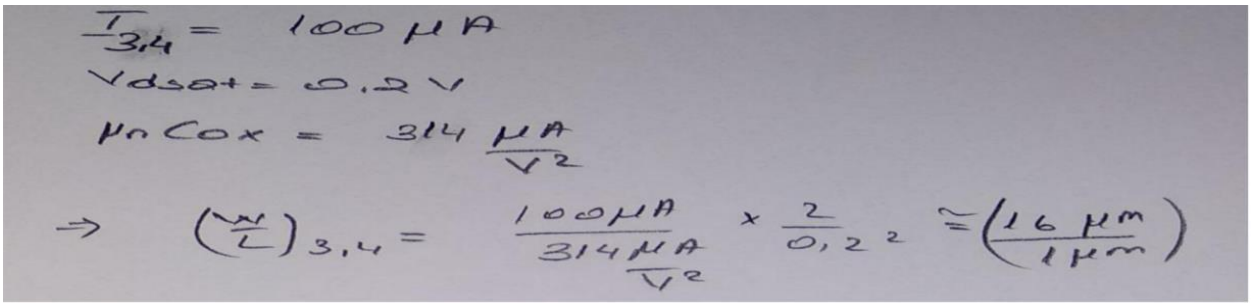


Figure 11

The results from using these calculated values for the differential pair design are shown in Figure 12.

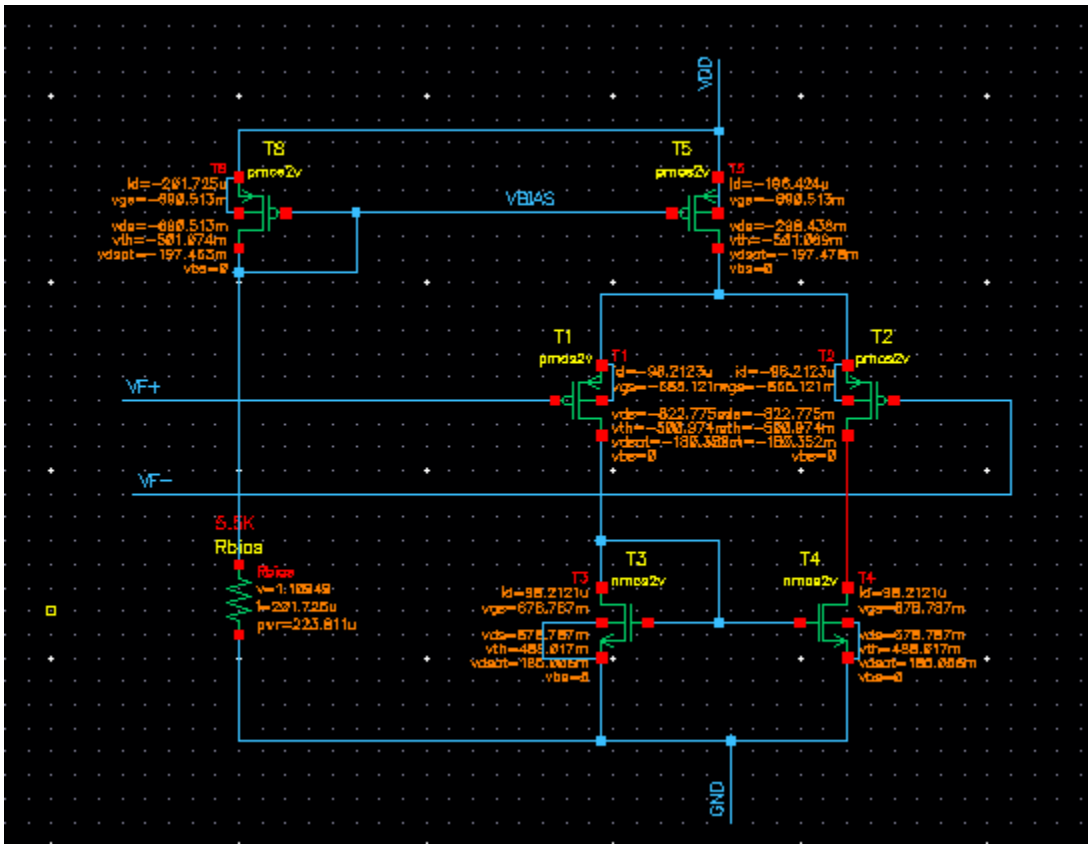


Figure 12

With the design of the differential pair, I think I have finished the design of the Gilbert Cell and I now I need to go into the simulations and applications. As a final note, I have all the transistors operating in the strong inversion region, so I think everything is working up for the good up to this point. I am making the output single ended by means of a differential pair because that's how you instructed me on the email.

Multiplication

Firstly, I would like to go on to the calculation of the conversion gain of the Gilbert Cell. Please follow, the Figure 13. The calculations for Figure 13 are based on Figure 3.

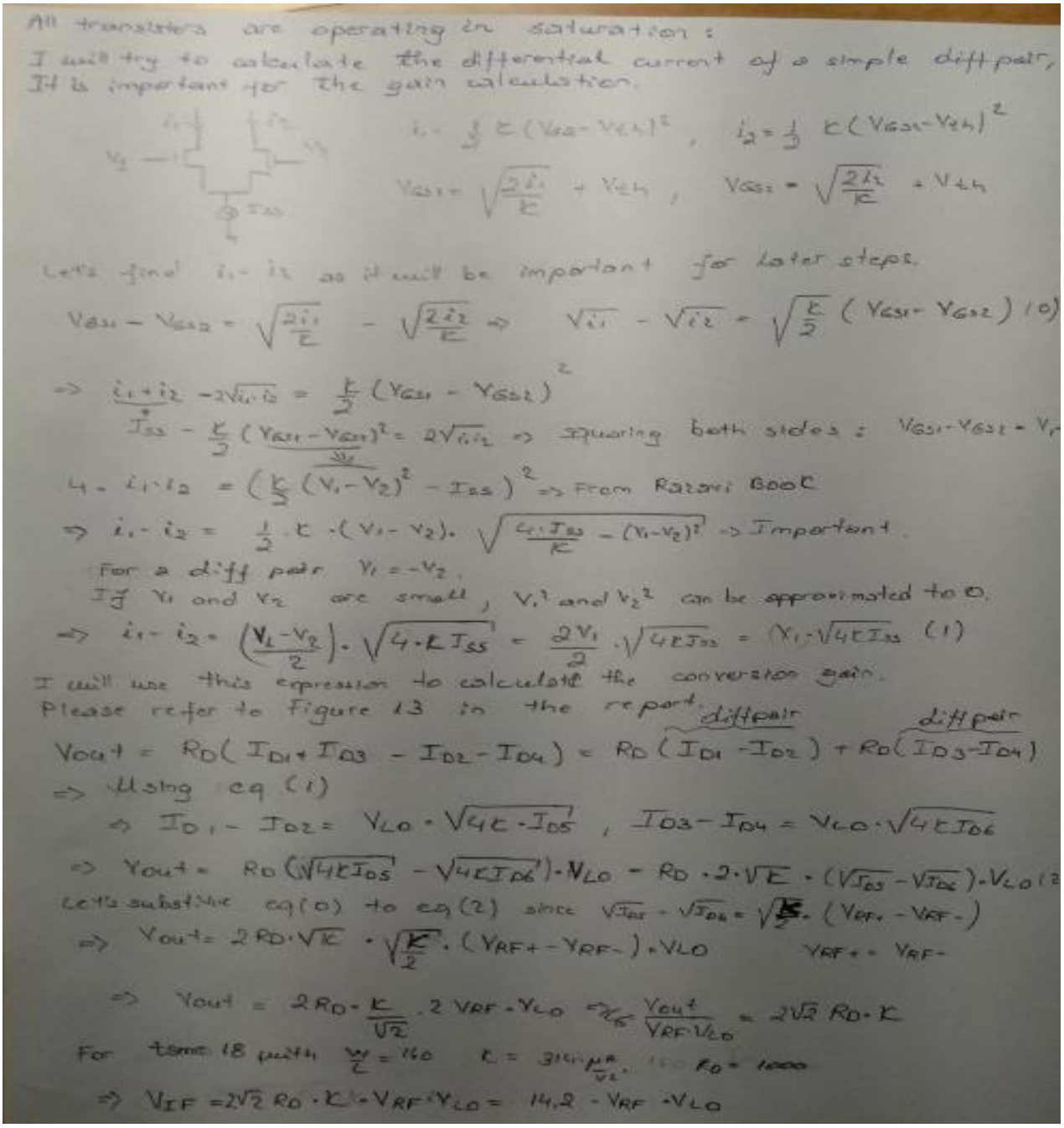


Figure 13

The conversion gain that I calculate is 14.2. The circuit seems to be multiplying but for small voltages. For high voltages that wouldn't be the case because of the approximation we have done in Figure 13. For each of the test I will do in the next couple of pages I will be using small

signals at the RF and LO inputs of the Gilbert Cell. I now will try to see how much conversion gain I have for the Gilbert Cell that I have designed. I entered 1mV LO and 1 mV RF with respective frequencies of 1MHz and 50kHz. I wrote a simple code in Matlab to find the waveform of the multiplication of the RF and LO signals. The code and the plot are shown in the Figure 14.

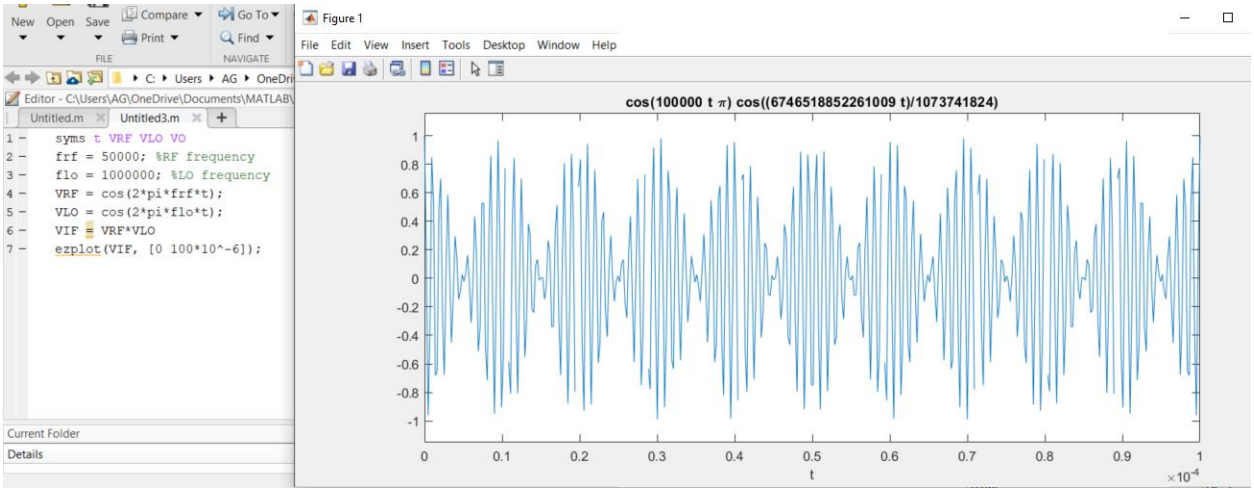


Figure 14

I will now test the circuit in cadence for the same inputs and see what the outputs are and how similar to the waveforms in Figure 14. I will try now to plot the output of the differential pair and the differential output of the Gilbert Cell to see if the waveforms are similar to Figure 14 waveform.

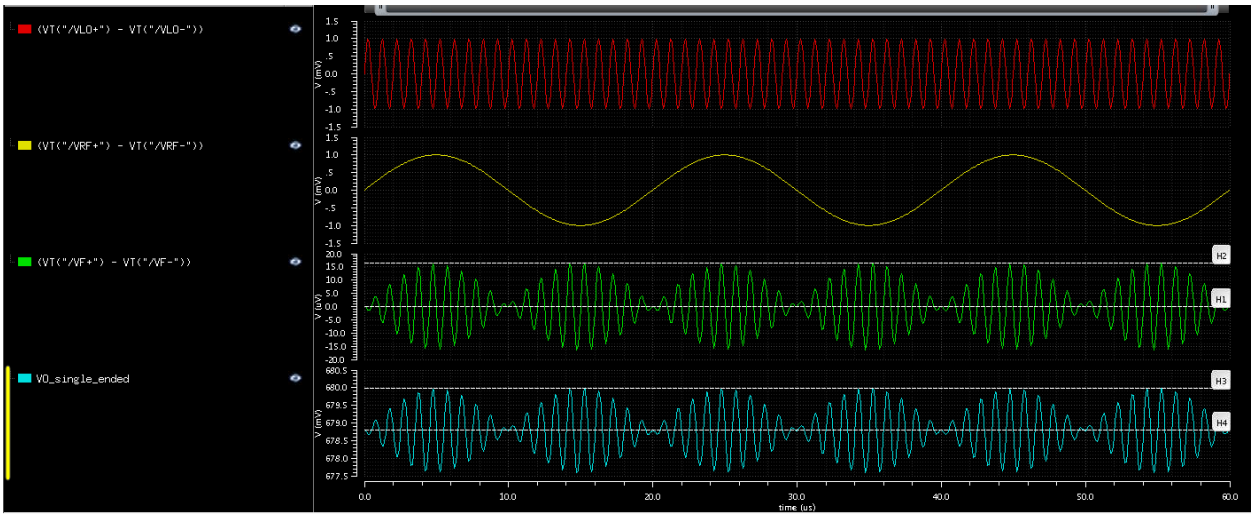


Figure 15

In Figure 15, you can see that VF+ - VF- and Vo_single_ended are very similar to one another and they are also similar to the waveform shown in Figure 14. So, by means of this I can surmise that the multiplication is being done. VRF*VLO has peak envelope amplitude of 1uV. From

Figure 15 we can see that the amplitude of the envelope is 15uV letting me know that the Conversion gain of the Gilbert Cell is around 16 very close to the calculated gain in Figure 13. Also, I have a differential pair whose gain of is 72. Thus, the total gain should be around 1152 at the output of the differential pair. Thus, the total gain should be around 1152 at the output of the differential pair. The amplitude of the envelope of the VO_single_ended is (679.9849V-678.8mV) = 1.1849mV as seen on Figure 16. Thus, the output envelope is 1184 times greater than the amplitude of the VRF*VLO which once again confirms our calculations.

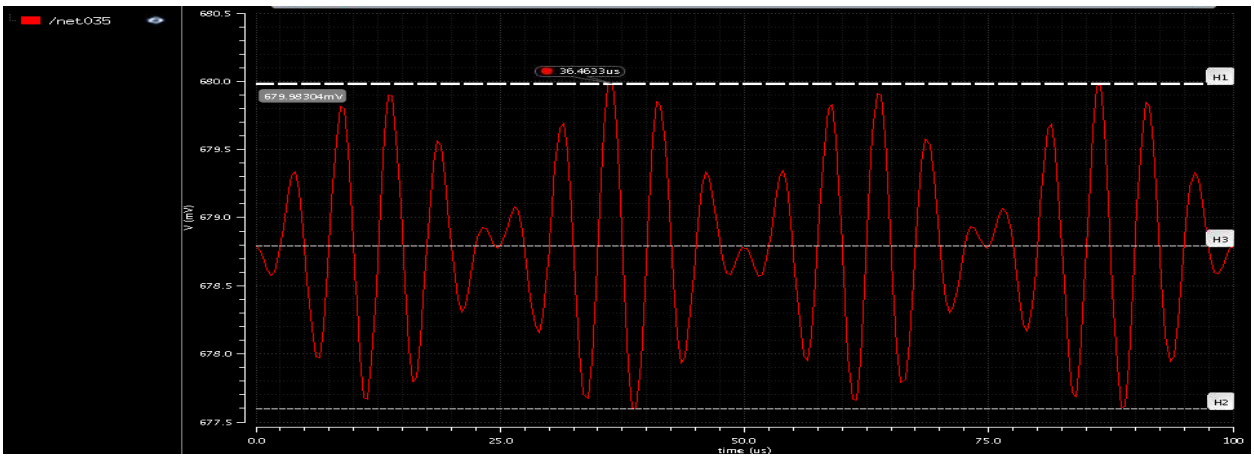


Figure 16

It seems that the circuit is working fine up to now. I would like to go on and test the circuit with different input signals. I will do the simulations in Matlab also so we can see the similarities on the waveforms. In Figure 17 I multiplied an RF signal with a sinusoidal LO signal and the output waveform should be similar to that shown in Figure 17.

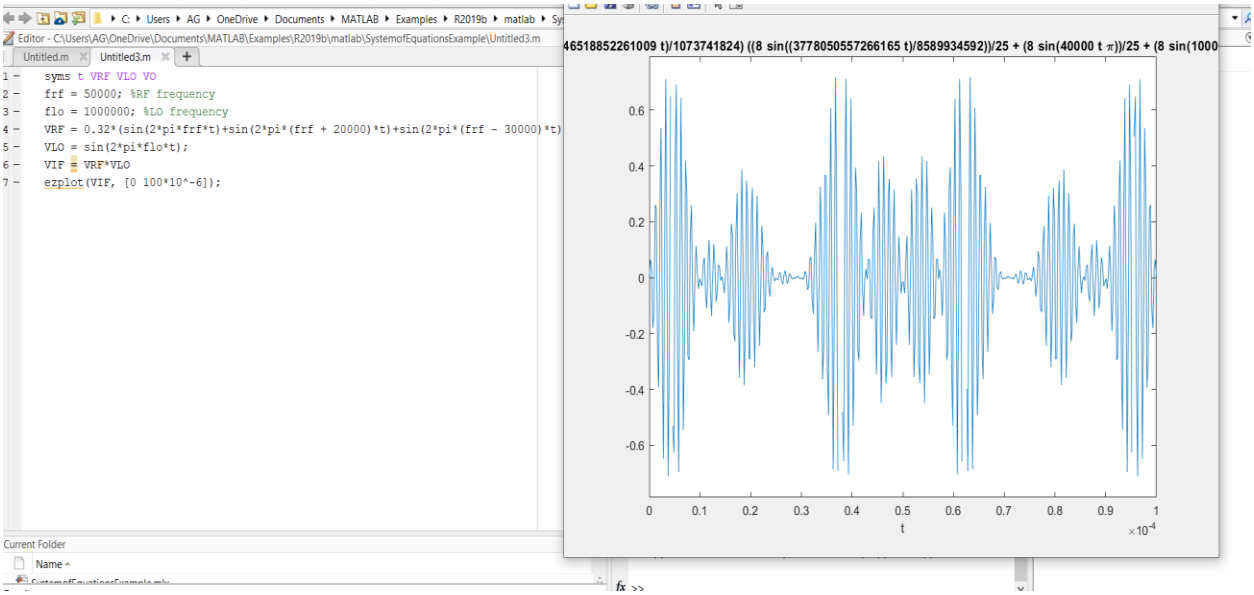


Figure 17

Since the transistors are working on saturation and the input signals are small, I don't see any reason for the circuit not to work. As it seen on Figure 18, the VF+ - VF- and V_single_ended are scaled versions of one another and also, they are very similar to the waveform that is shown in Figure 17.

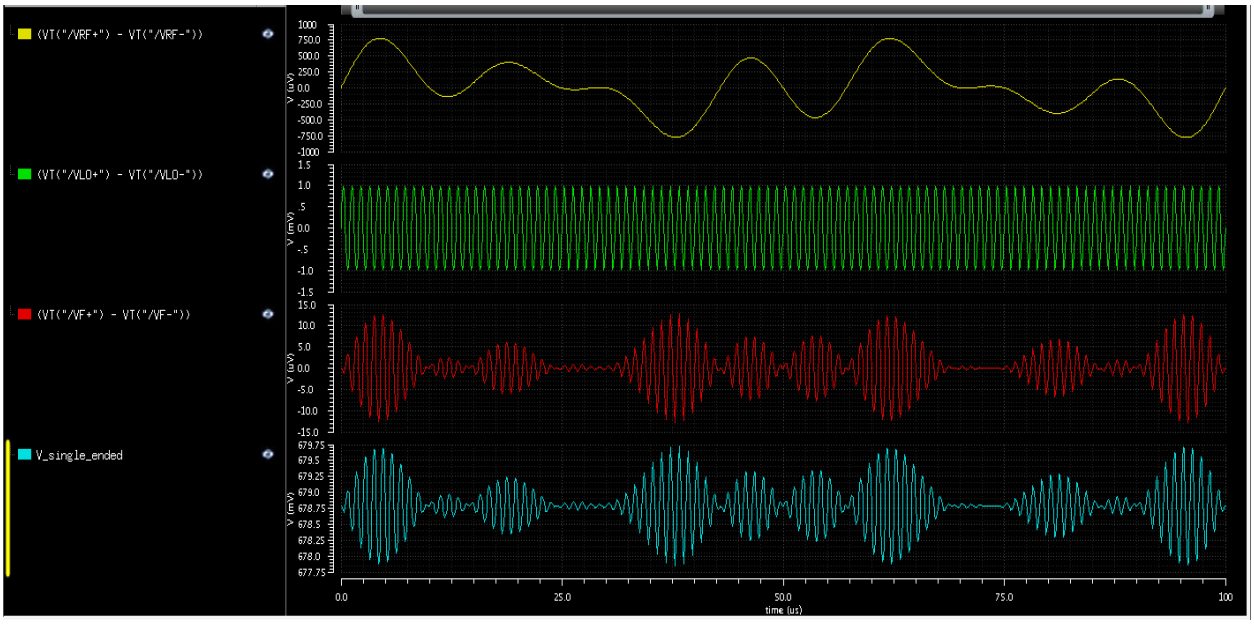
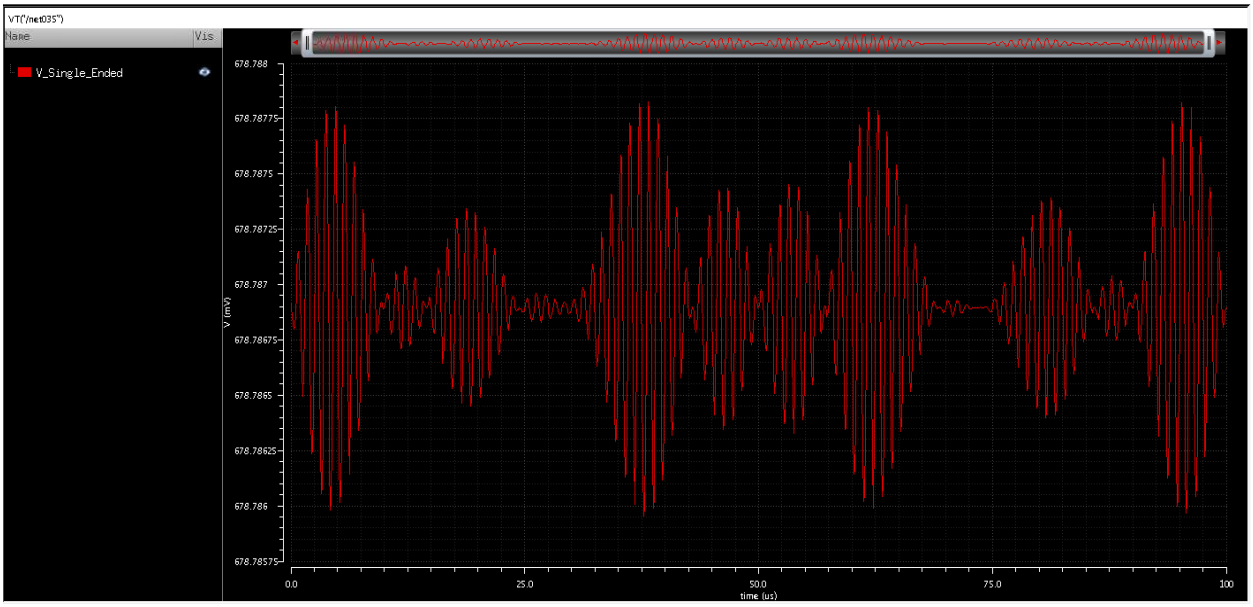


Figure 18

Below I have shown an enlarged version of V_single_ended of Figure 18. Please see that the waveform is identical to Figure 17 waveform.



I will now change the LO signal also, I will make it complex. I will run a matlab code for that also so we can see the true waveform and the waveform I receive on Cadence. In Figure 19 I am

showing the Matlab script and the resulting VIF output. Please see that I have changed the LO signal now.

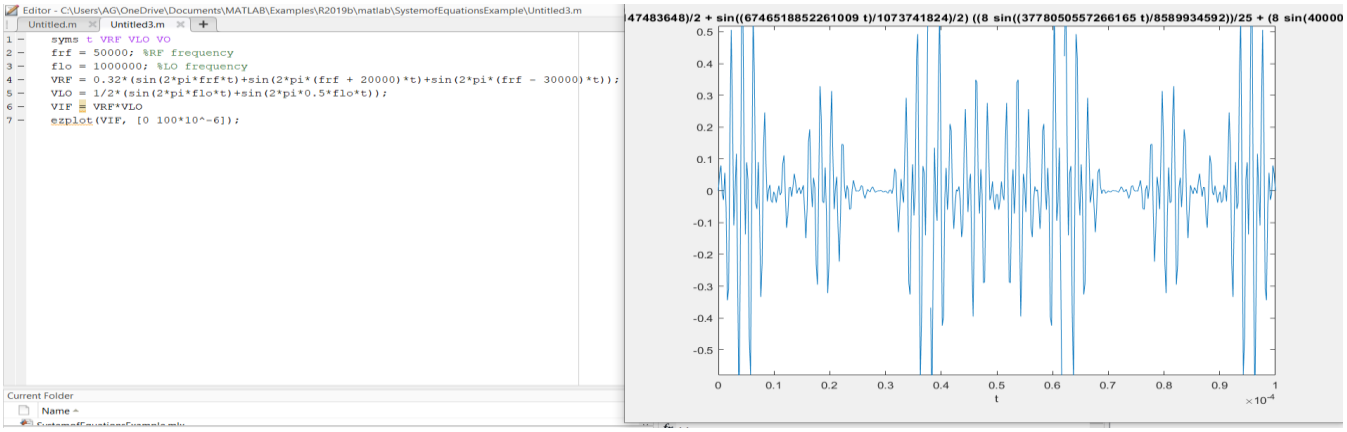


Figure 19

In Figure 20 I have shown the Cadence simulations for the LO and RF signals that I have defined in Figure 19 scripts. Please see that VF+ - VF- and VO_single_ended have the same waveform but their amplitudes are higher in the VO_signle_ended case. Please also note that the VF and VO_single_ended waveform is same with the waveform taken from Matlab simulations. This makes me believe that the circuit is multiplying for small LO and RF inputs.

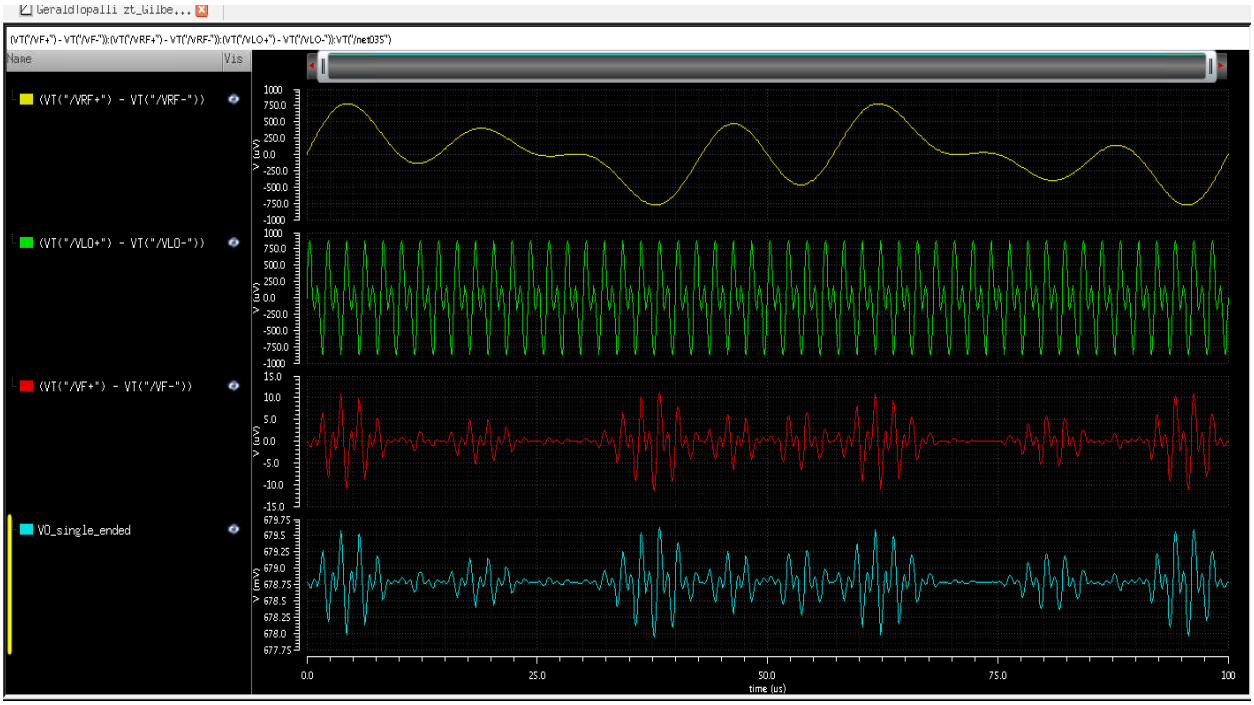
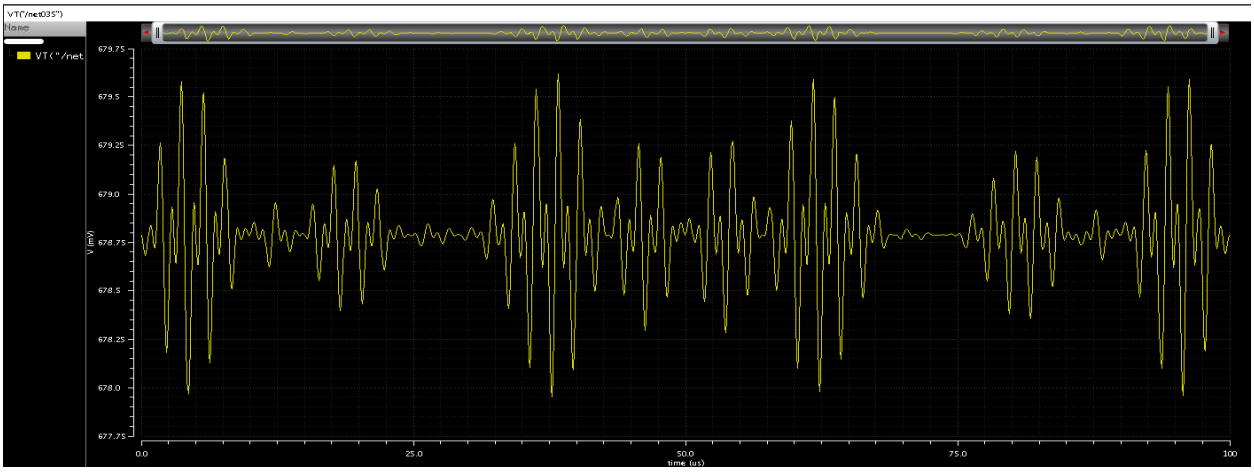


Figure 20

Below I have shown an enlarged version of VO_single_ended of Figure 20. Please see that the waveform is identical to Figure 19 waveform.



I would like now to show that the circuit is linear also. I will make a simple test bench to show that when one of the inputs is multiplied by a number, the output will be multiplied by the same number also. I will use 1mV RF and LO signals and I will supply them on respective frequencies of 50kHz and 1MHz. Initially I will multiply the RF signal by 4 and we will see 4 times increment on the VF output. I will then make another simulation where the LO signal will be multiplied by 7, and we will see that the output has increased by 7 times.

For VRF = 1mV * sin(50k*2*pi*t) and VLO = 1mV * sin(1M*2*pi*t) the output is shown in Figure 21. The envelope amplitude of VF+-VF- is 16.038uV.

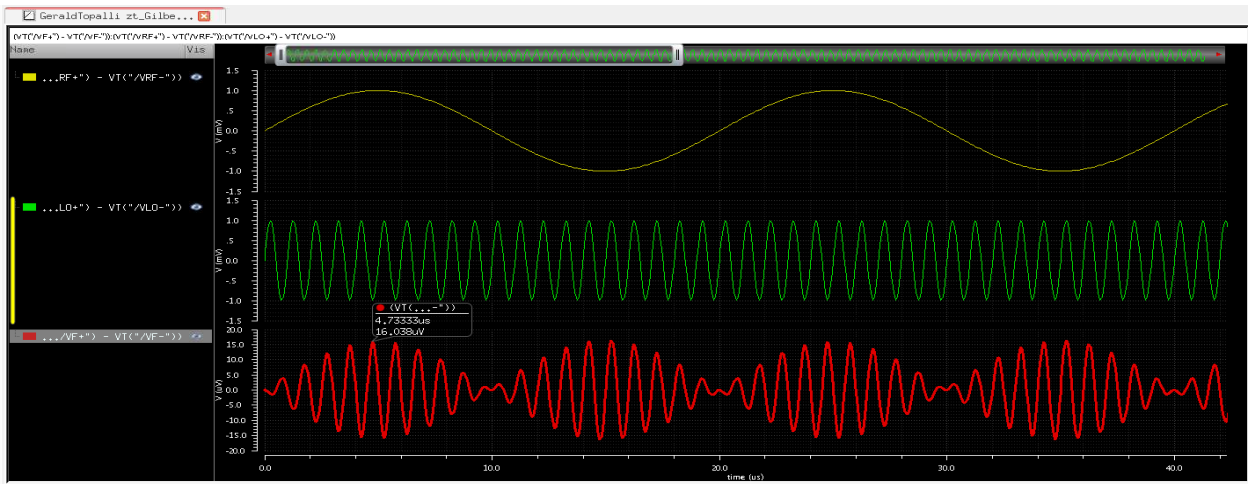


Figure 21

I will now make the RF signal 4 times greater. Please see the change in amplitude envelope of VRF and VF in Figure 22. VRF amplitude is 4 times higher and the VF amplitude has multiplied by 4 from previous time. In Figure 21 VF envelope amplitude was 16.038uV and in Figure 22

VF envelope amplitude is 64.148uV so the second VF signal is about 3.99997 than the first VF signal.

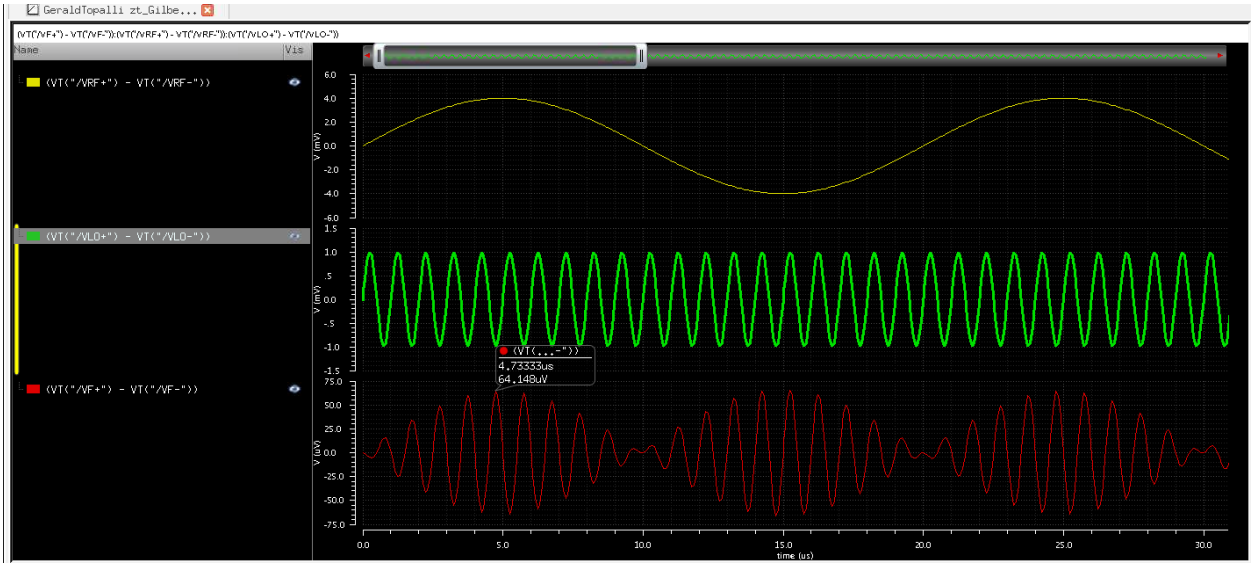


Figure 22

For VRF = 1mV * sin(50k*2*pi*t) and VLO = 7mV * sin(1M*2*pi*t). The amplitude of the envelope of VF is 112uV. Please see Figure 23. In Figure 21, VF was 16uV. 112u/16u = 7, so the output is 7 times greater because of multiplication properties.

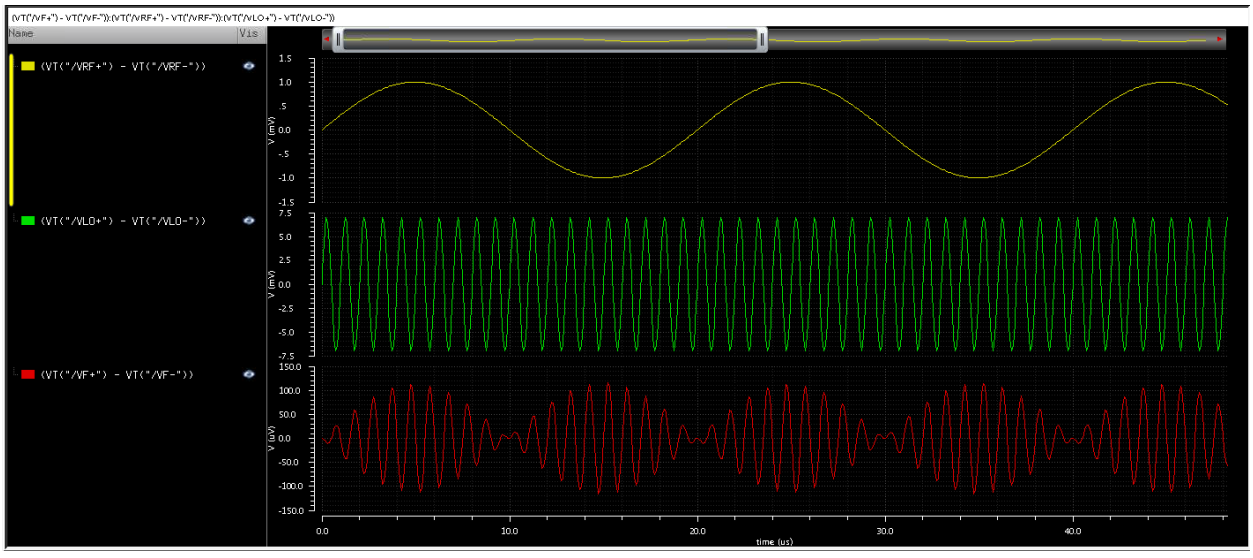


Figure 23

I think there is enough evidence showing that multiplication is working correctly. I would like to go on now on finding the cutoff frequency but it won't be very high with the differential pair that I am using becuase the output node of the differential pair is problematic as it contains a high

impedance node and thus it has a low pole. For the cutoff frequency calculations, I will remove the differential pair and I will increase both the frequency of the RF and IF.

RF = 1MHz, VLO = 20 MHz, the gain hasn't decreased even for these high frequencies as seen in Figure 24.

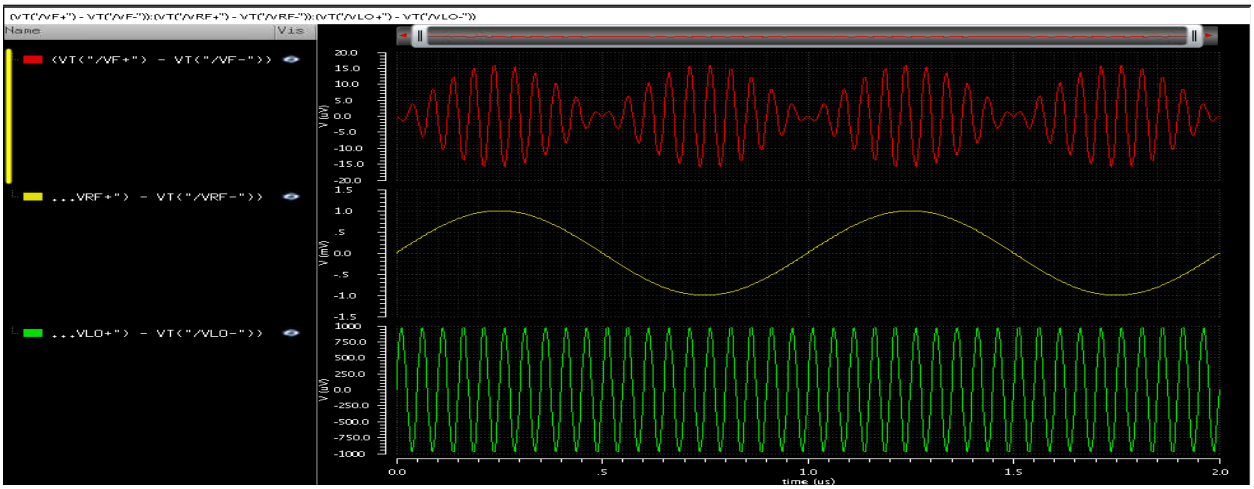


Figure 24

RF = 20MHz, VLO = 2000 MHz

The circuit is multiplying but the conversion gain is decreasing because of the parasitic caps shorting out as shown in Figure 25.

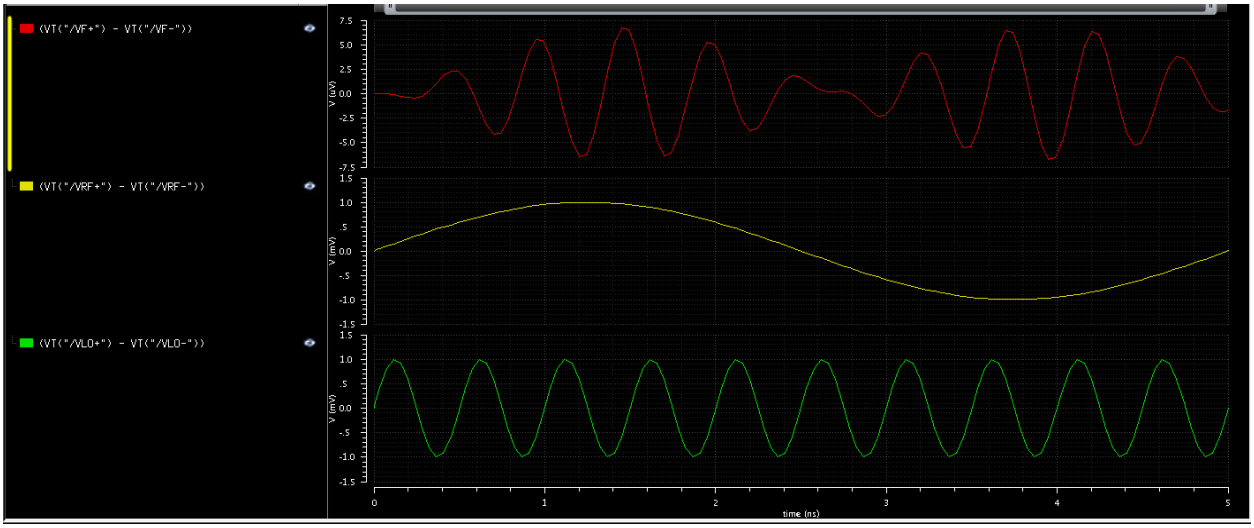


Figure 25

RF = 1G, VLO = 20 GHz

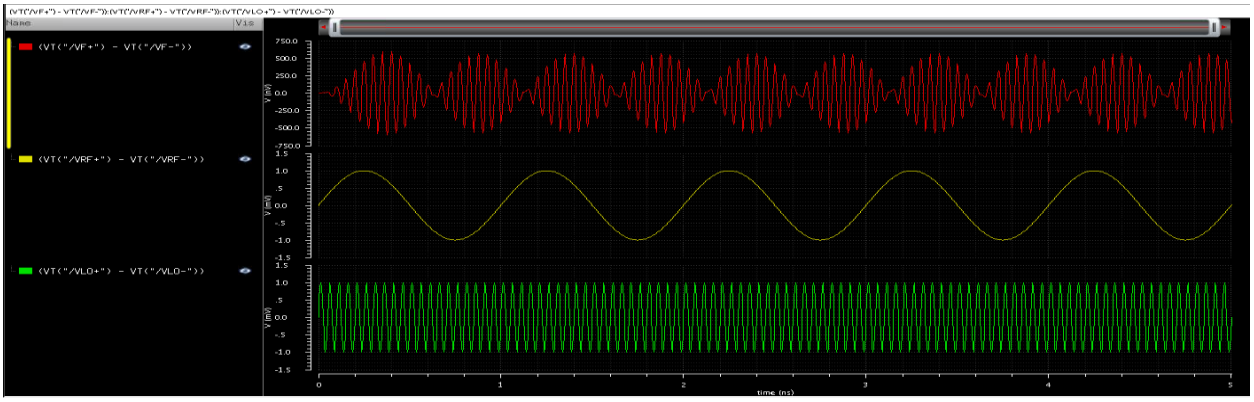


Figure 26

As it seems, the circuit works even for these high frequencies but the conversion gain has dropped significantly as shown in Figure 26. I tried running AC analysis for this circuit but since it has to different inputs, it could not be run in cadence environment. I can see that the circuit can work for very high frequencies but I can't give a correct value for the cutoff frequency as usually the Gilbert Cells are built to be used at a single frequency, or over a band of frequencies.

Modulation

Modulation is a process that can very easily be implemented by means of the Gilbert Cell. If we make the LO signal high enough, we can modulate the signal very appropriately. This is a very used circuit when trying to modulate the signals by means of natural sampling. VRF is being modulated by means of the VLO signal which in this case is high. But how does the circuit work. If VLO is high, the current will only go through M1 and M4. If the VLO is low, the current will only go through M2 and M3.

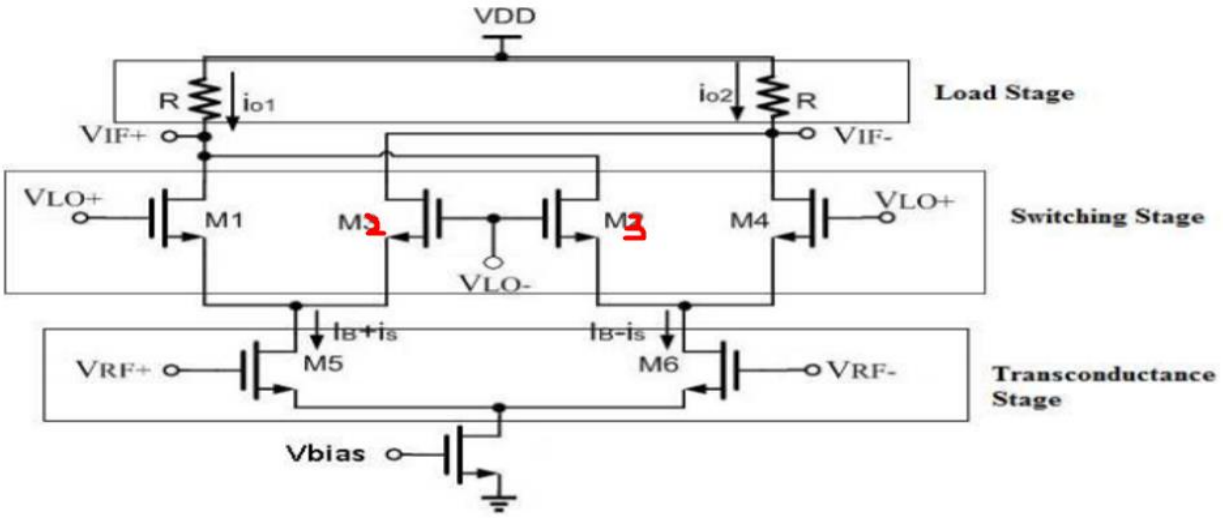


Figure 27

Note for Figures 28 and 29: By the red arrows I have shown where there will be current flowing. On the wires where I haven't put arrows, there will ideally be 0 current or very small.
With blue arrows I have shown high voltages (upward)and low voltage (downwards).

When VLO is high: io = io1-io2 = gm5,6*(VRF+ - VRF-) (differential pair M5-M6) assuming that VLO is so high that the whole Iss current goes through M1 and M4. Please see the current flow in Figure 28. That means that VIF = R * io = -gm5,6*R*VRF. Please find io1 and io2 in Figure 28.

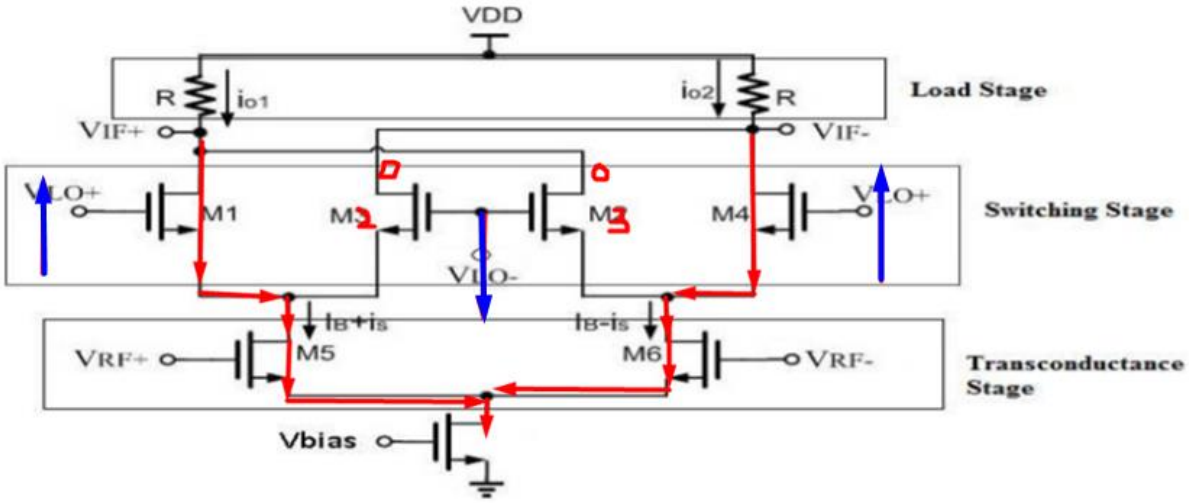


Figure 28

When VLO is low: io = io1-io2 = gm5,6*(VRF- - VRF+) (differential pair M5-M6) assuming that VLO is so low that the whole Iss current goes through M2 and M3. Please see the current flow in Figure 29 and please note the io1 and io2. That means that VIF = R * io=gm5,6*R*VRF.

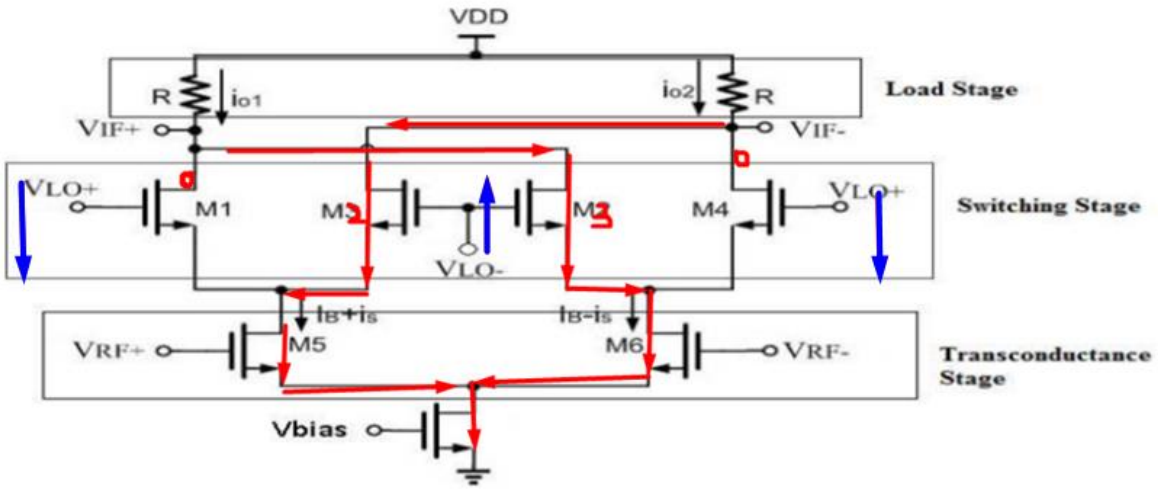


Figure 29

What I want to show by means of Figures 28 and 29 is that when VLO is high, we should see the VIF = -gm5,6*R*VRF and we should see VIF = +gm5,6*R*VRF when VLO is low. In Figure 30 I have shown the gm of transistors M5 and M6.

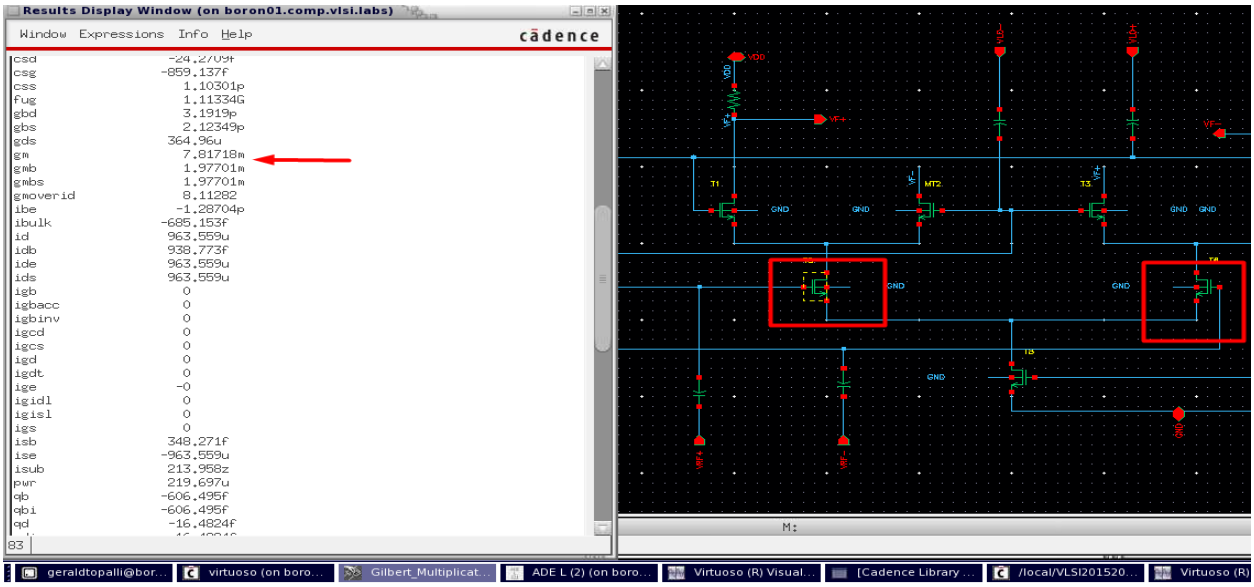


Figure 30

The R resistor is 1000 ohms. So, the input RF should be modulated with a gain of A=7.8m*1000*VRF = 7.8*VRF. Let's see this by means of the simulation seen on Figure 31.

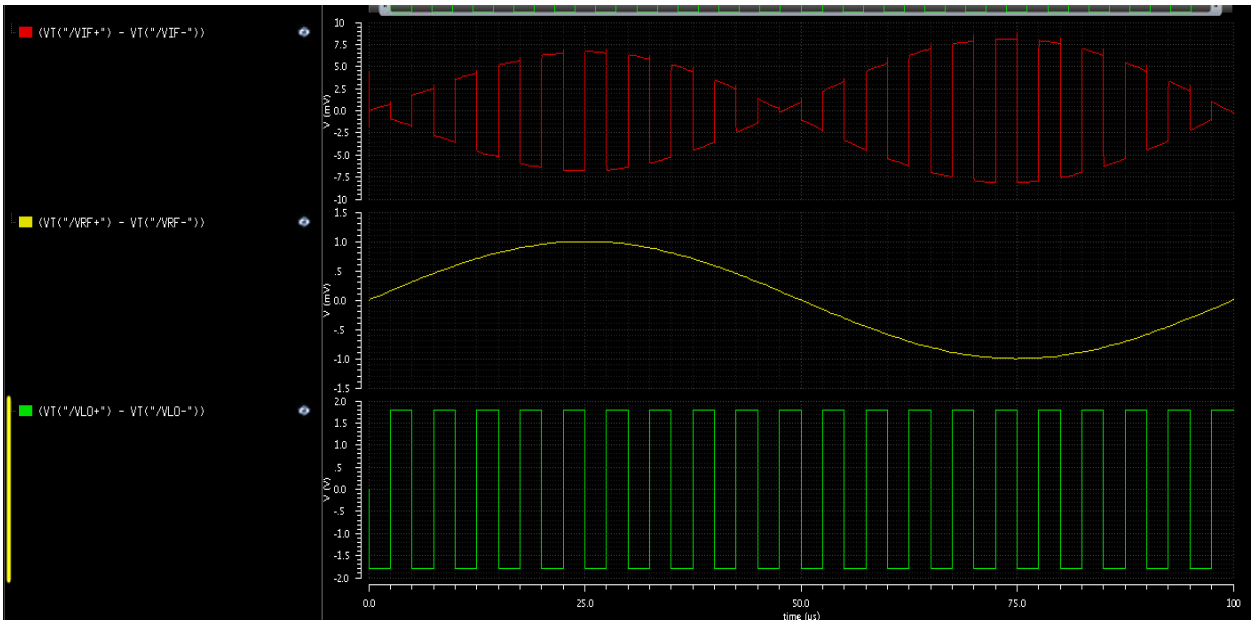


Figure 31

Please see that the RF signal is 1mV and the VIF signal amplitude is 7.5mV roughly so the gain is roughly 7.5 (very close to the 7.8 gain I calculated above). This proves my point that I wanted

to prove on Figures 28, 29 and 30. Please also see that when VLO is high the VIF is negative and when VLO is low the VIF is positive complying to the equations that I wrote for Figures 28 and 29. I will do another test for some higher frequencies in order to check how the circuit works for higher frequencies. Please see Figure 32 for the simulations on higher frequency signals. The circuit seems to be working fine for high frequencies also.

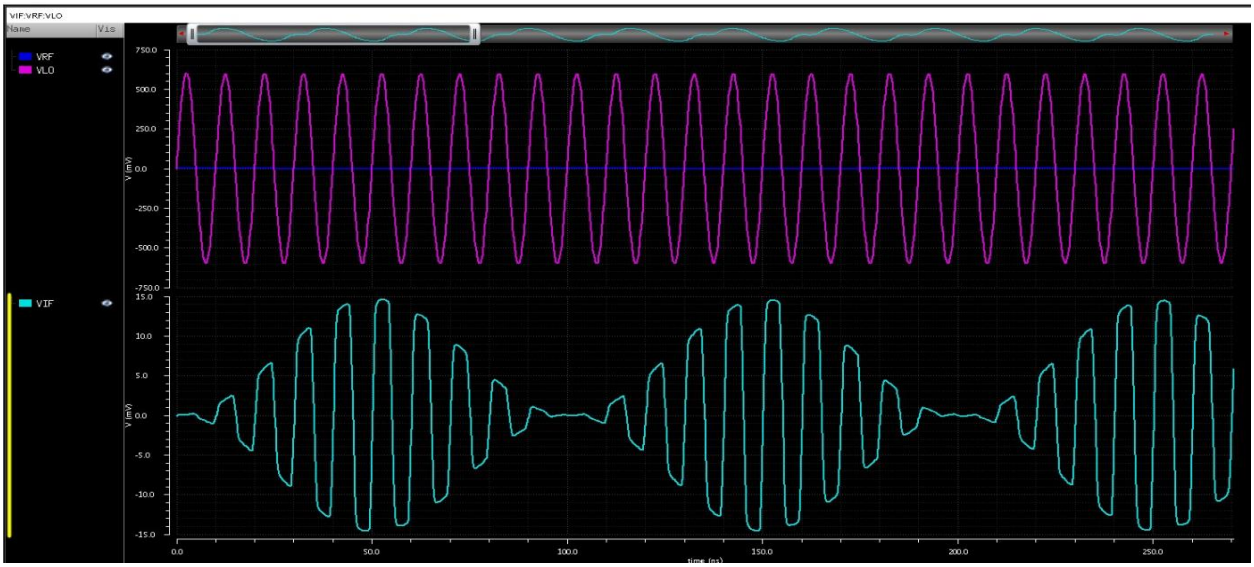


Figure 32

I think I have included enough evidence for the Modulation and I will go on with the Phase Detection.

Phase detection

Phase detection is very important in RF circuits as it is used in the PLL design to match the phase of the output with the input incoming signal. But how is this working on a Gilbert Cell. I should probably emphasize here that the RF and LO signals should be high enough. I have shown 4 cases below for the possibilities that can happen with RF and LO signals. How the output VIF will change for each of the cases. By the red arrows I have shown where there will be current flowing. On the wires where I haven't put arrows, there will ideally be 0 current or very small. With blue arrows I have shown voltage changes. An upward blue arrow means the voltage is high, and a downward arrow means the voltage is low.

RF low, LO low -> VIF low

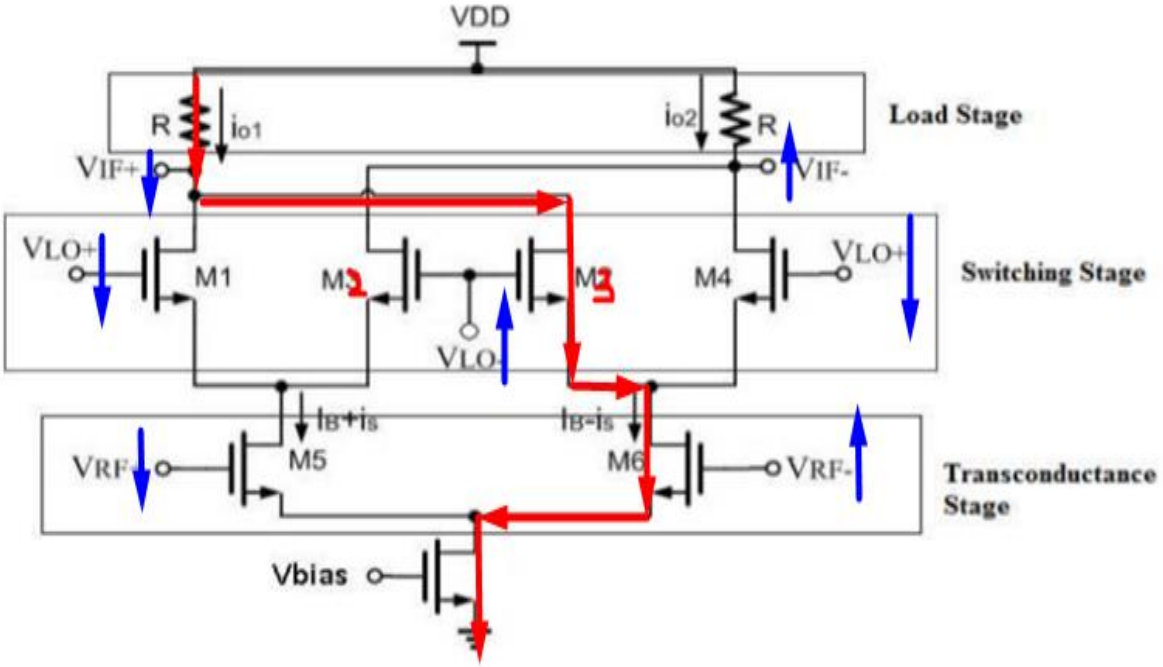


Figure 33

RF high, LO low -> VIF high

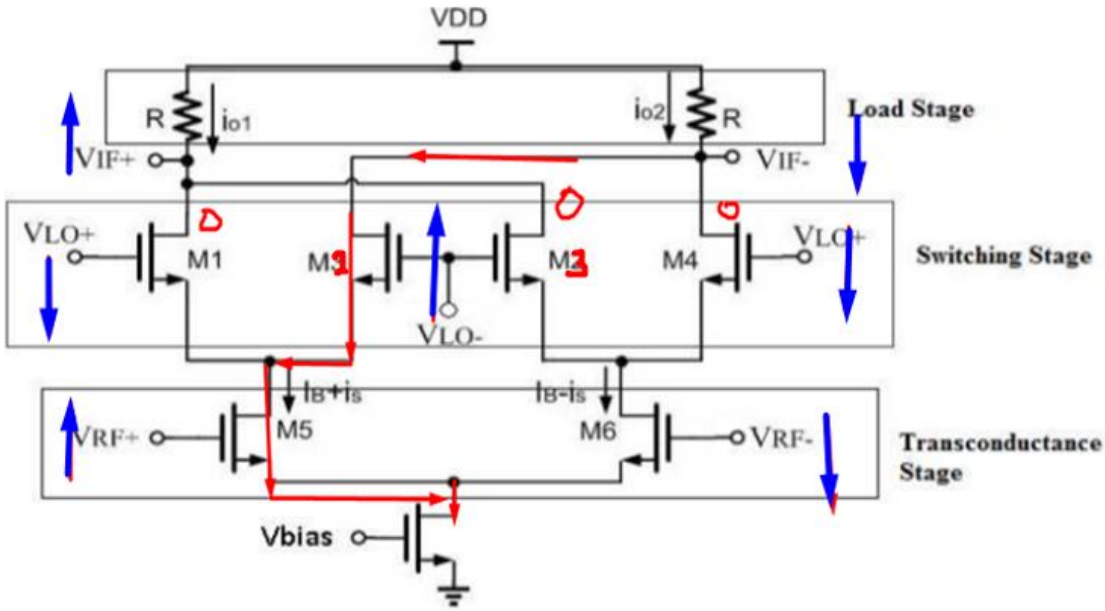


Figure 34

RF low, LO high -> VIF high

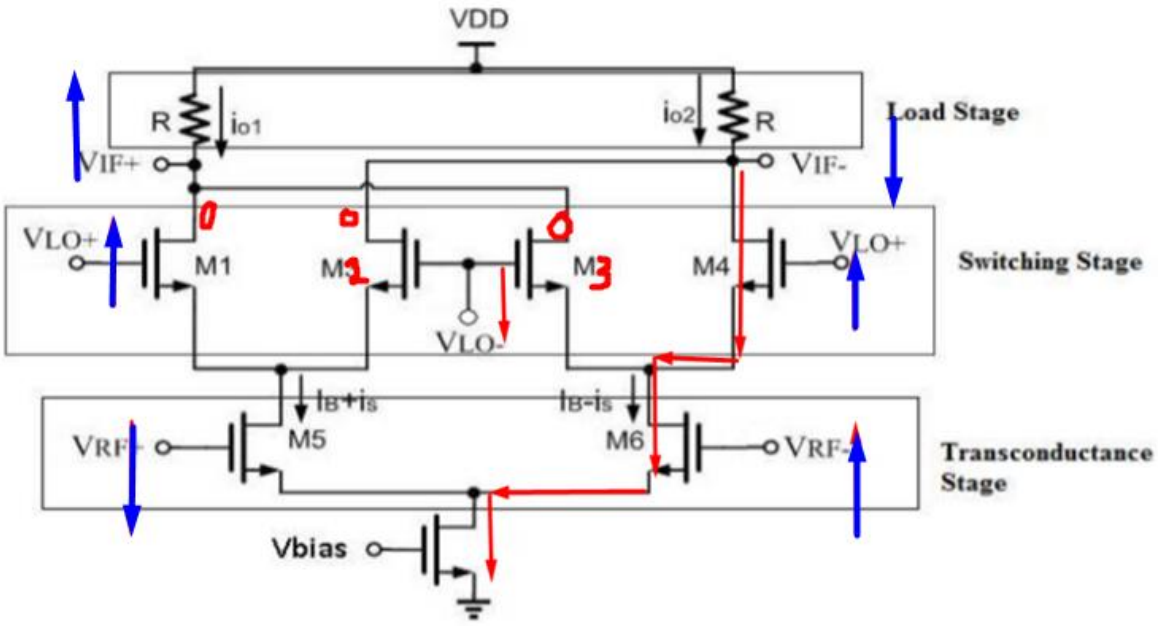


Figure 35

RF high, LO high -> VIF low

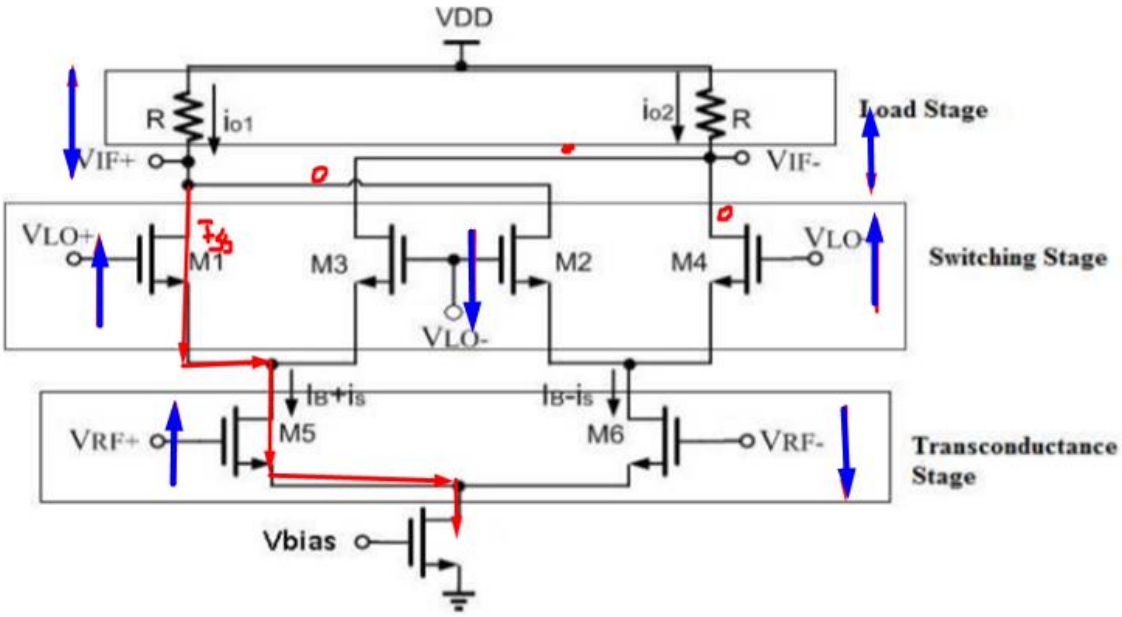


Figure 33

Also, by using cadence and inputting RF and IF signals I was able to test this circuit for a phase detection. In the 4 pictures above, I have shown the mechanism that the circuit is working. Please see how the circuit is correclty predicting the phase change in Figure 37.

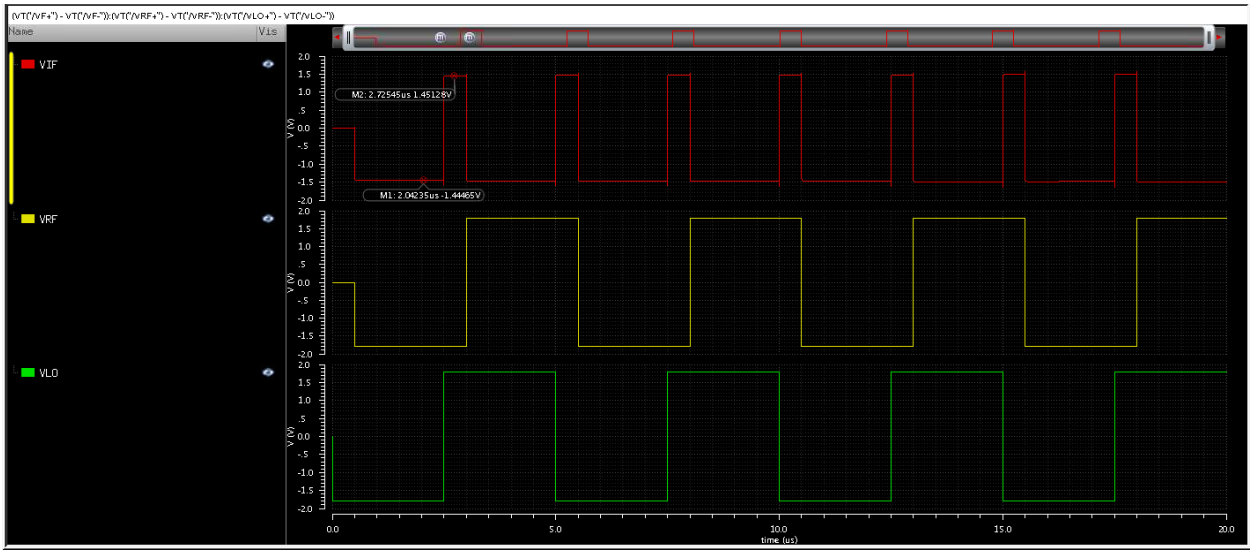


Figure 34

Another thing I would like to point out is the VIF high and low voltages. Please see in Figure 38 that the Iss current for this circuit is 1.92 mA. When one of the cases on Figures 33-36 happens, the whole Iss current will go through one of the ways I have shown on those figures by means of the red arrows. I have selected my RD = 1000. I should have seen a high value of RD*1.92m=1.92V and a low value of -RD*1.92m=-1.92 V but since there can be some residual current going through some of the transistors, the output has decreased to 1.45 V.

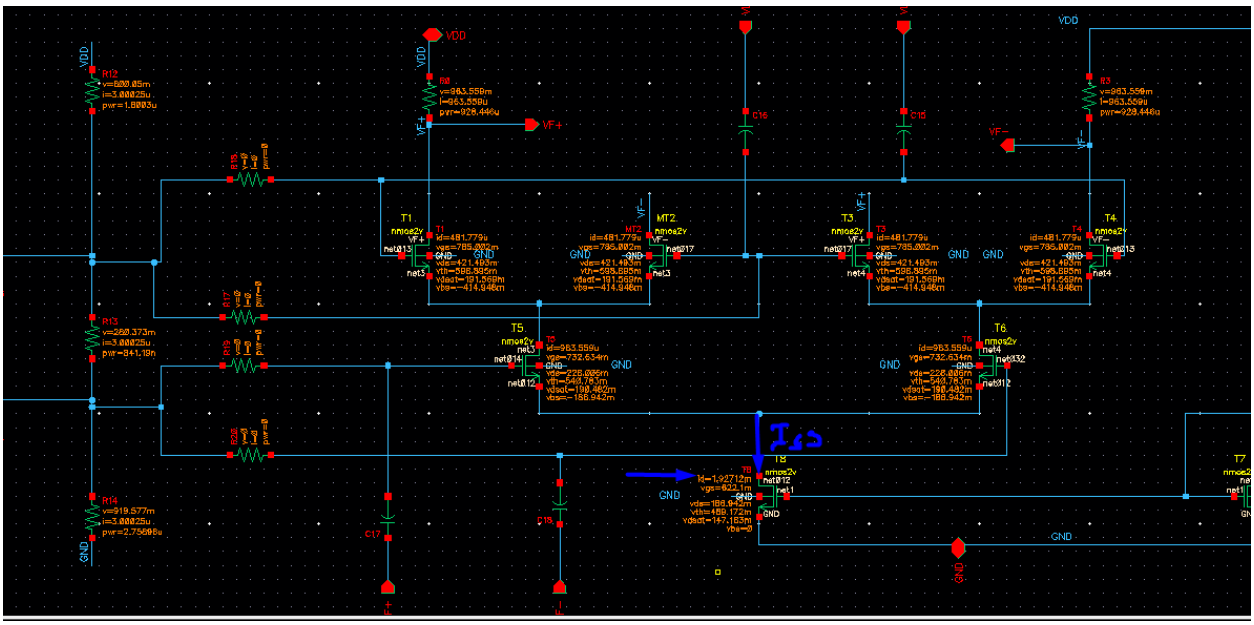


Figure 38

If VRF and VLO have no phase change amongst them, the VIF should be as shown in Figure 39.

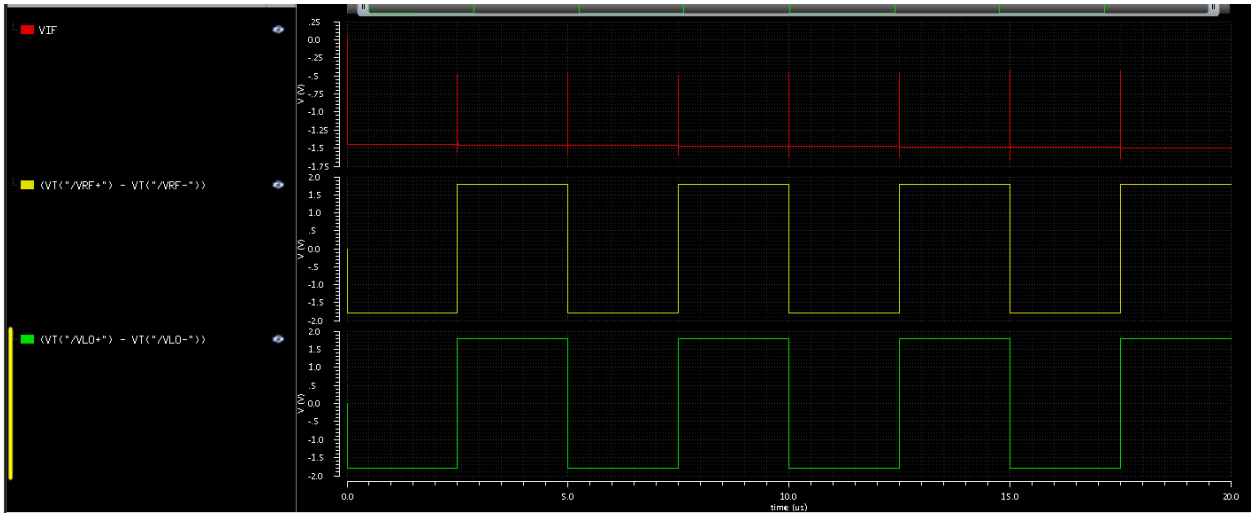


Figure 39

Please see on Figure 39 that the VIF remains low.