Gerald Topalli
040160911

Project 1

For this project, I decided to build an Active LPF called the Sallen-Key Active filter. This filter is a derivation of the other Chebyshev filter which is a very well-known circuit. The general circuit is shown in Figure 1. R_1, R_2, C_1 and C_2 are responsible for creating the cutoff frequency whereas R_3 and R_4 create a 3dB gain which is important in some sort of sense.

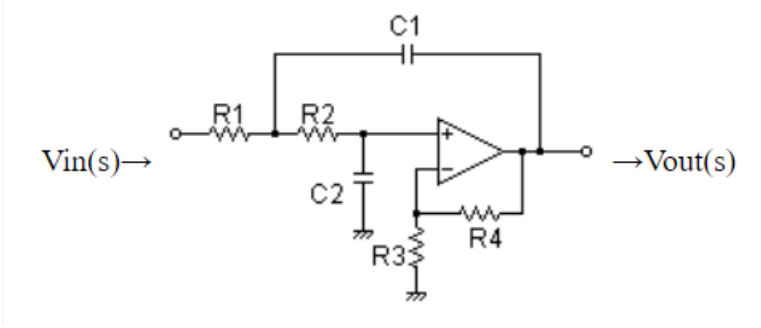

Figure 1

Analyzing the circuit in Figure 1 in the s-domain, we find the transfer function shown in Figure 2. We can see that the transfer function is dependent on the Gain (G) of the schematic. Also note that the DC-gain of this circuit is G also shown in Figure 2. By selecting the R_3 and R_4 properly, I can make the DC-gain to be almost 3dB which is interesting to see because than the -3dB bandwidth of the filter will be the frequency where the filter transfer function equals to 0dB.

$$\frac{vo}{vi} = \frac{\frac{G}{C1C2R1R2}}{s^2 + s\frac{1}{C1R2} + s\frac{1}{C1R1} + s\frac{1}{C2R2}(1-G) + \frac{1}{C1C2R1R2}}$$

$$G = \frac{R3+R4}{R3}$$

Figure 2

In this project I will firstly try to build a CMOS OP-AMP using TSMC 0.18u transistor library in cadence. The OP-AMP will be a 2-stage circuit and the inputs will be taken through PMOS transistors. I will do this because the PMOS transistor exhibit lower Temperature Noise Figures and also it is important to note the DC level biasing of the output node. We need to carefully consider it because the circuit will work on a feedback configuration. Practice has proved that PMOS input OP-AMP are better than NMOS equivalents for this purpose. Of course the circuit will exhibit slightly lower gain values, but I promise the gain will be high enough for our assumptions to be true. In the next couple of pages I will try to explain in detail how I biased the circuit and the results that I obtained. Please let me know if you cannot see the calculations or figures very well. I will try to send you clearer figures.

Op-Amp Design using TSMC 0.18u transistor

I searched in Google regarding this technology and the characteristics that I found are shown in Figure 3.

Parameter	Symbol	N MOS	P MOS	Unit
Maximum supply voltage	$V_{DD,max}$	1.8		V
Zero-bias threshold voltage	V_{th0}	0.50	−0.48	V
Bulk effect parameter	γ	0.42	−0.67	$\sqrt{V}$
Twice Fermi potential	$2\phi_F$	0.87	−0.90	V
Zero-bias sub-threshold slope	n	1.31	−1.29	
Channel length modulation constant	k_λ	0.041	−0.039	μm/V
Current factor	$K' = \mu C_{ox}$	316	−62	$\mu A/V^2$
Gate area capacitance	C_{ox}	8.4	8.4	$fF/\mu m^2$
Gate width overlap capacitance	C_{ov}	0.72	0.68	$fF/\mu m$
Junction area zero-bias capacitance	C_{j0}	1.0	1.2	$fF/\mu m^2$
Junction perimeter zero-bias capacitance	C_{jsw0}	0.25	0.20	$fF/\mu m$
Flicker noise coefficient (not KF)	K_f	$3.3 \cdot 10^{-25}$	$1.6 \cdot 10^{-25}$	J
Minimum channel length	L_{min}	0.18		μm
Typical source/drain length	ℓ_{SD}	0.6		μm
Mosis scalable design rules unit	λ_{SUBM}	0.1		μm
Thermal voltage (kT/q)	V_T	26		mV

Figure 3

I then tested the transistor in cadence and I found slightly different values in cadence, especially for Current Factor. The values I calculated are shown in Figure 4. I found these values by running a DC analysis and printing the Beff of the NMOS and PMOS transistor whose W/L was 10 and their V_{DS} were $V_{DD}/2$.

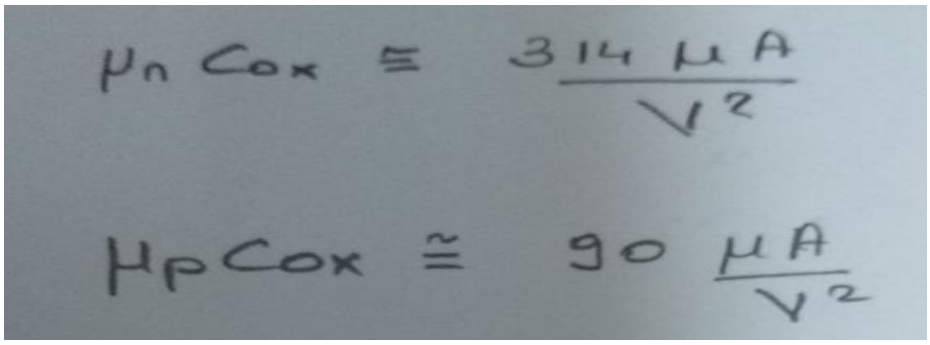

Figure 4

This step is very important because we will be selecting the widths of the transistors by using these equations. I also need to mention that I select V_{dsat} = 0.2 for most of my designs. Assuming the V_{th} = 0.5 for the transistor, I will need at least a V_{gs} greater than 0.7 to have the transistor working in the strong inversion region (which I really like working with) since the transistor's behavior is well known by us students.

The schematic of the Op-Amp is pretty generic. The schematic is shown in Figure 5. I have labeled the transistors the same way we labeled them in the class.

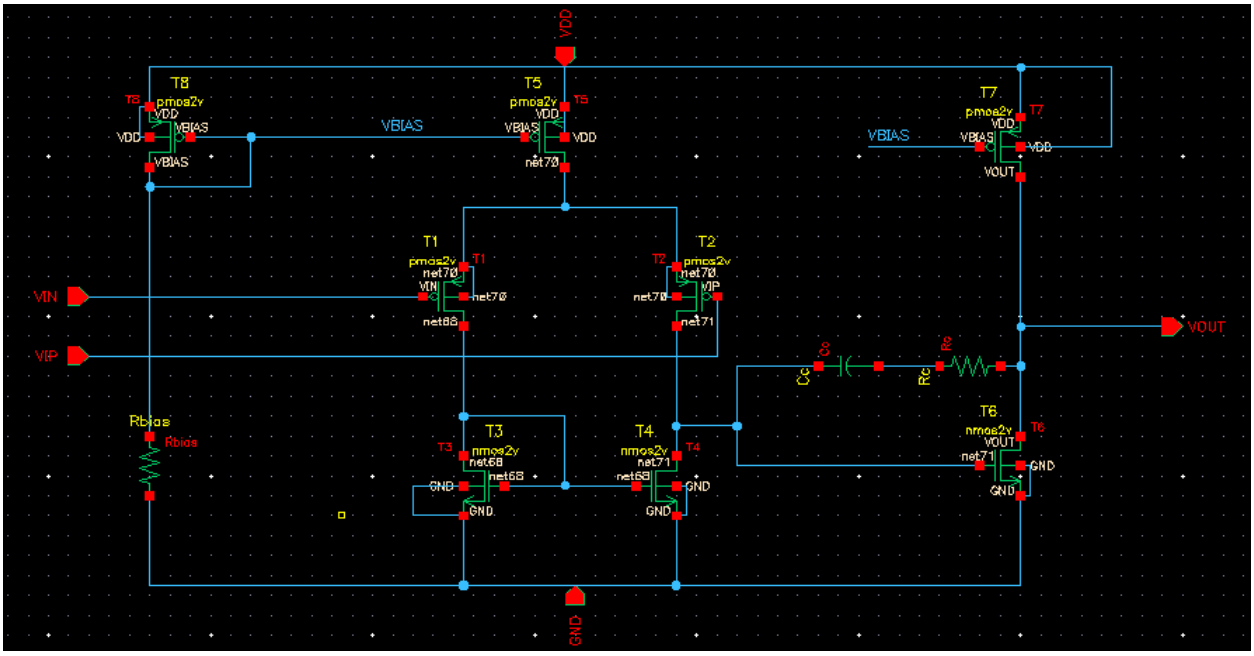

Figure 5

I wanted to have around 100uA flowing through T_1 and T_2, so the tail current which is supplied by T5 should be 200uA. I usually select equal sizes of T_5 and T_8. T_5 and T_8 and the R_{bias} is a very simple current mirror. To produce 200uA at T_8 I showed the calculations in Figure 6.

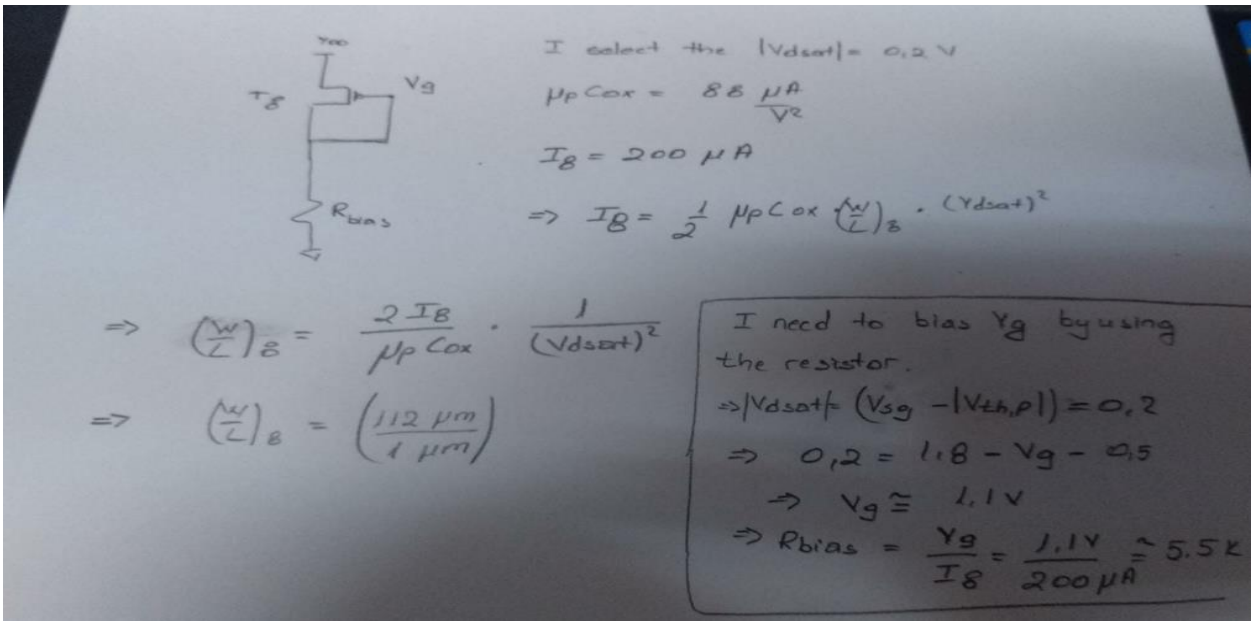

Figure 6

$T_5 = T_8$ are equal and the R_{bias} = 5.5k Ohms. For these values I run a DC test in the circuit and I found a current of 201uA at the T8 and T5. The results are shown in Figure 7. Without much effort, I selected the T_1 and T_2 just by knowing that the current of T_5 will be twice the current in T_1 or T_2, thus I just need to divide the width of T_5 by 2. So $(W/L)_1 = (W/L)_2 = 66 = (W/L)_5/2$

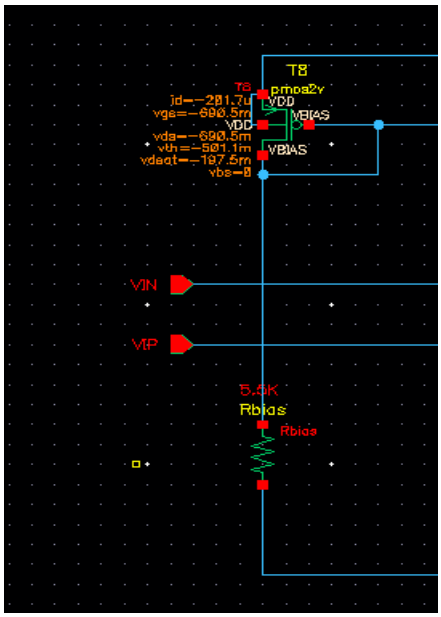

Figure 7

For T_3 and T_4, I need to do an analysis since they are implemented in NMOS. Figure 8 shows the calculation I did to select the widths of T_3 and T_4.

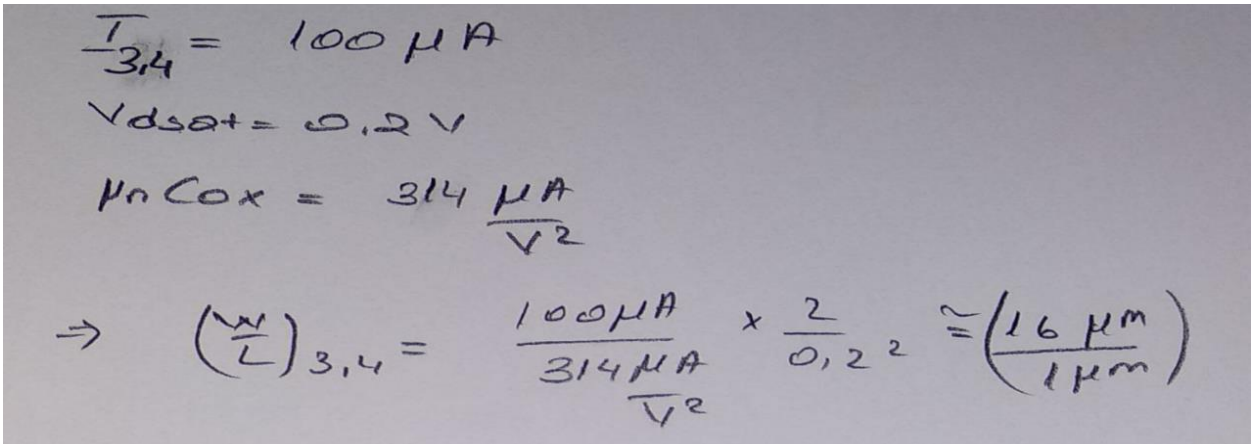

Figure 8

Since there will be another second amplifier stage, whose amplifying transistor will be biased by the differential pair current mirror (T_3 and T_4) I can easily calculate the size of T_6. Same logic applies for the size of T_7 which is being biased by T_8 and R_{bias}. Figure 9 shows how I came up with the sizes of the T_6 and T_7. Note that I used a high current in the second stage since in many of the applications; we need to supply high power from the last stage.

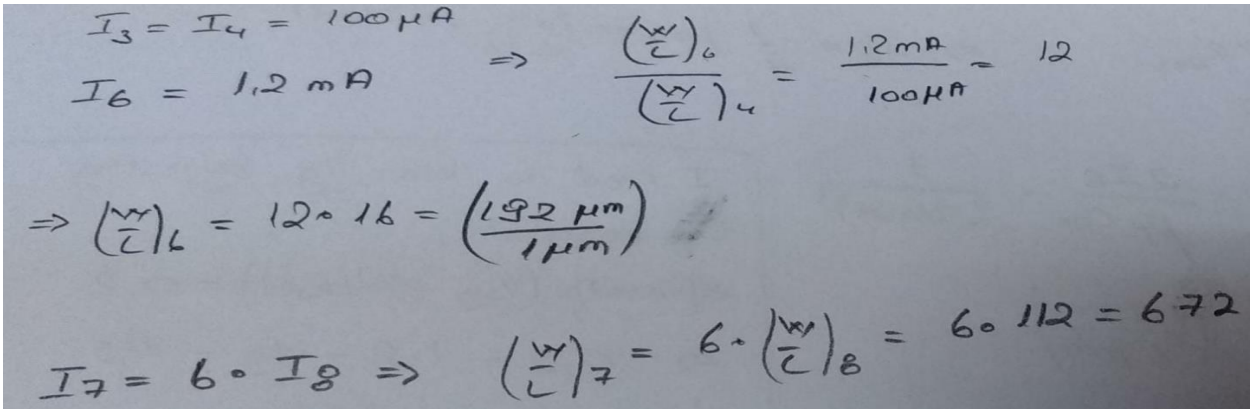

Figure 9

After biasing the V_{IP} and V_{IN} with a common mode voltage of 0.8, DC Operating Point values shown in Figure 10 are observed.

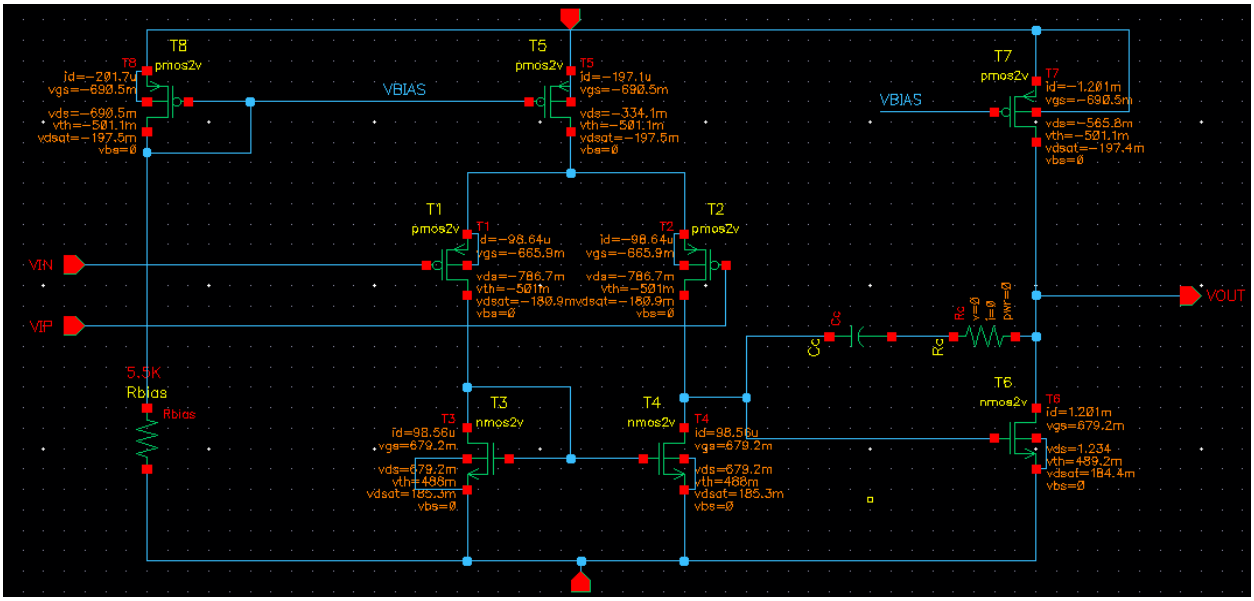

Figure 10

As it seems, the sizing of the transistors has been done in an appropriate way since everything is biased correctly and furthermore the current are very close to the calculated values. Of course there is some error, but those errors come because we have approximated the device equations. In the next few pages I will discuss about Miller Compensation and do some tests to the circuit.

The current in the T_1 and T_2 is approximately 100uA (98.6uA). So the first stage will try to source this current through the capacitance. Here the definition of slew rate comes up. For most circuits, 12V/usec is enough. I am selecting a 4pF capacitance Cc to make this circuit slew rate about 25V/usec. See the calculations in Figure 11.

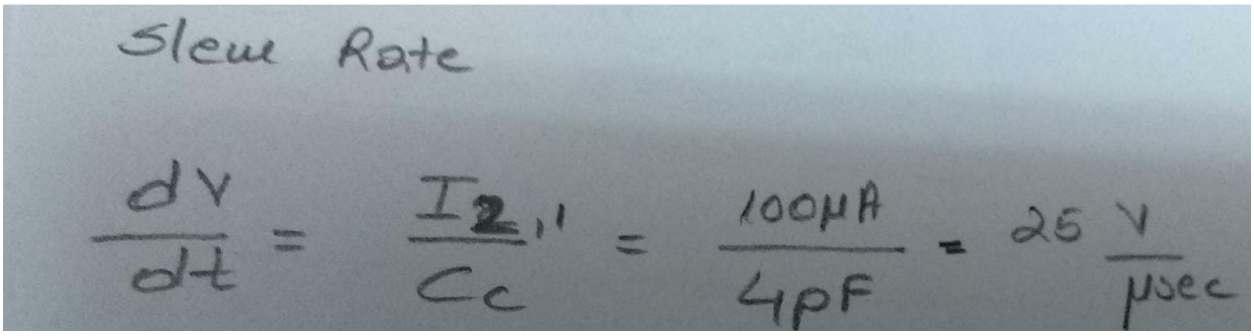

Figure 11

In the class we studied that this circuit has 3 poles and 1 zero. The added R_c in the circuit in Figure 10 can help us make the second pole and first zero cancel each other. For this purpose I will try to find the resistor R_c which will make the circuit behave as a single pole system in a broad range of frequencies. Note that the third pole will occur very far in the frequency domain. For the calculation of R_c, I will approximately find all the capacitances and the gm_6 value. Please find all the simulated values and the calculations I made in Figure 12.

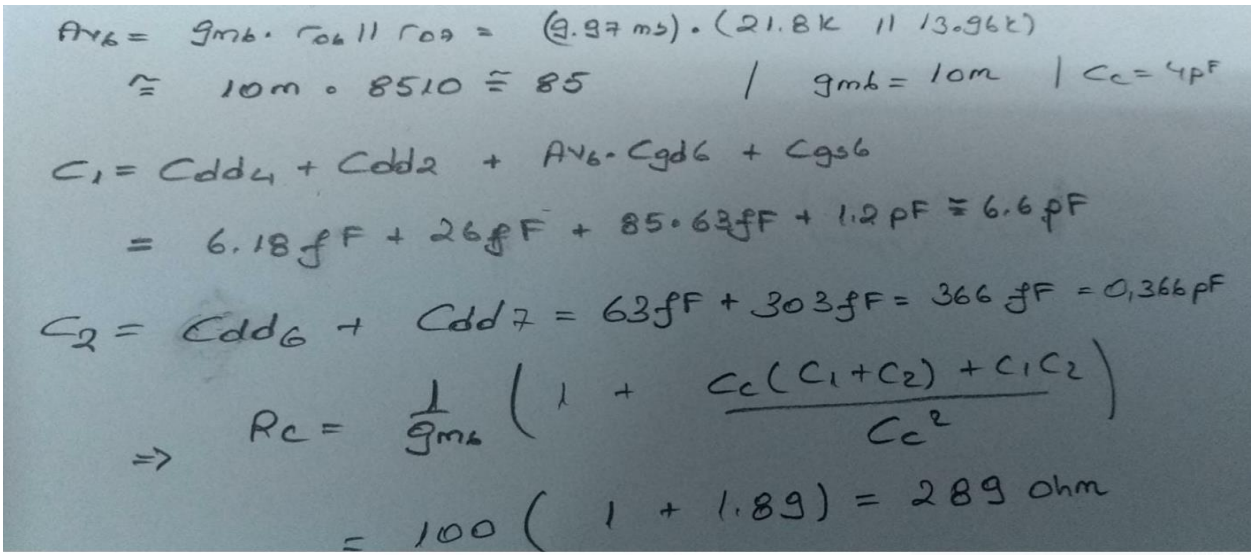

Figure 12

I estimate the R_c to be 289 but that I believe it will contain a lot of error because those are not very accurate calculations. For this purpose I will use a Monte Carlo Analysis (Plot AC magnitude) by sweeping the resistance value from 100 to 300. 100 is the minimum value the R_c can take. The resulting window is shown in Figure 13.

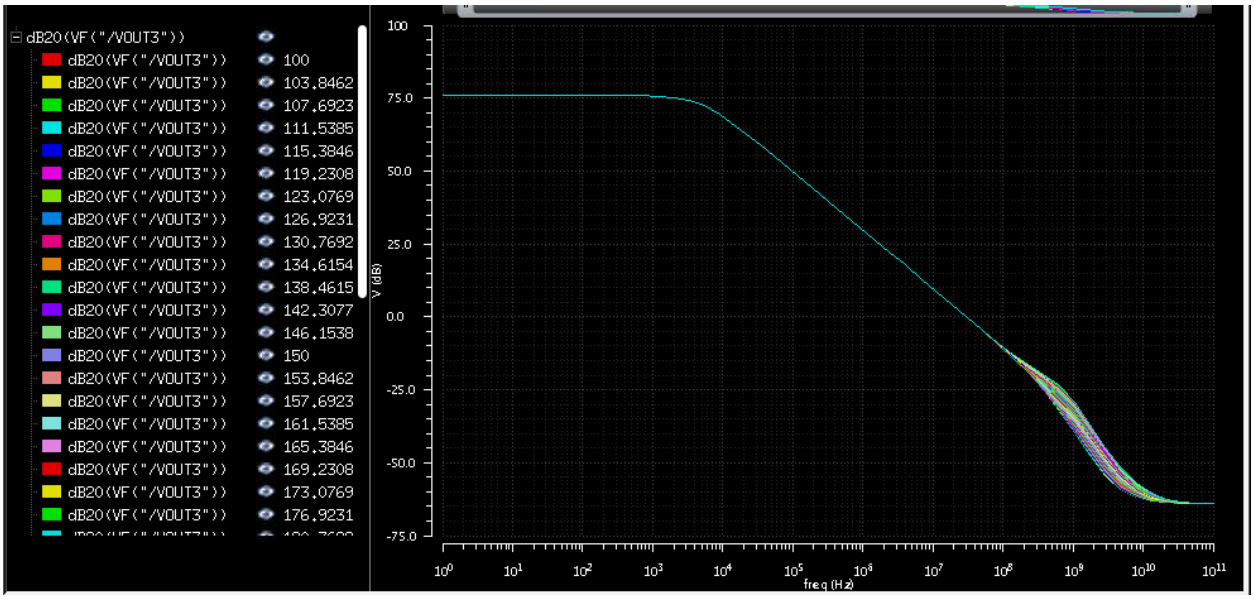

Figure 13

After careful observations, I found out that the best 1-pole representation is retrieved if Rc = 145. I know this is quite a lot of change but the AC analysis always gives these errors. For an R_c of 145 Ohms. Figure 14 shows the AC magnitude of the circuit.

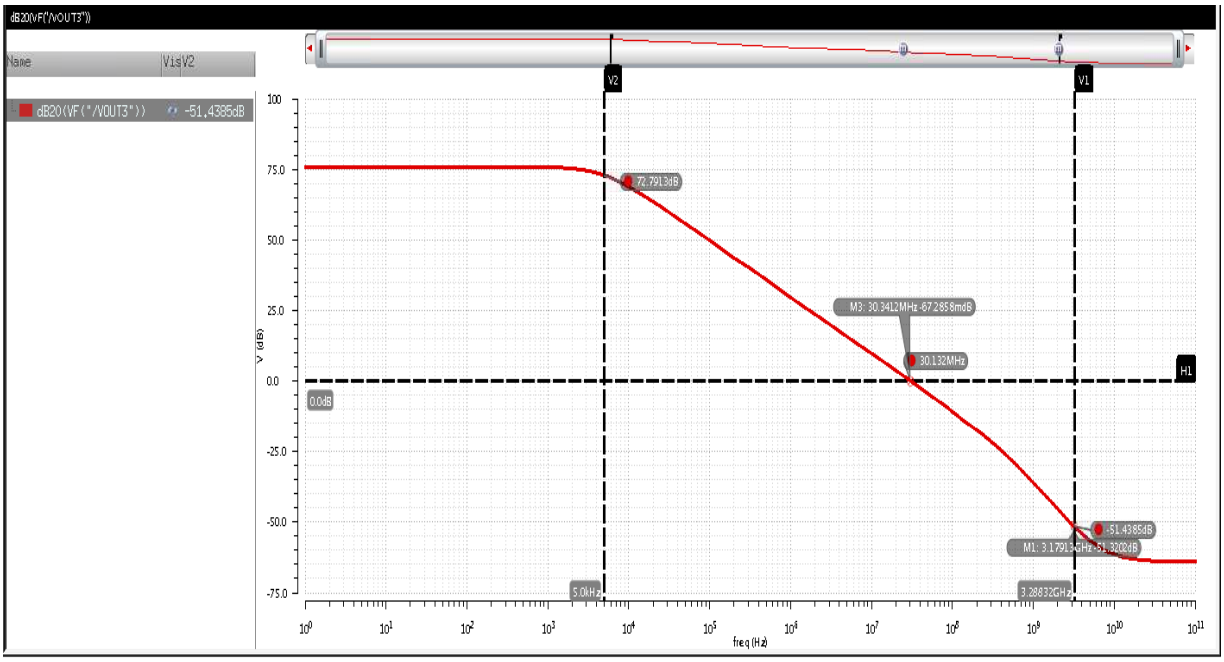

Figure 14

In Figure 14 please see that 1-st pole happens at 5 kHz. The unity gain bandwidth is 30MHz (first pole * DC gain of OpAmp). The circuit continues to have single pole response until f = 3.1GHz, region at which the effect of some zeros is felt because the second stage has huge sizes.

The testbench I used to test this circuit is shown in Figure 15.

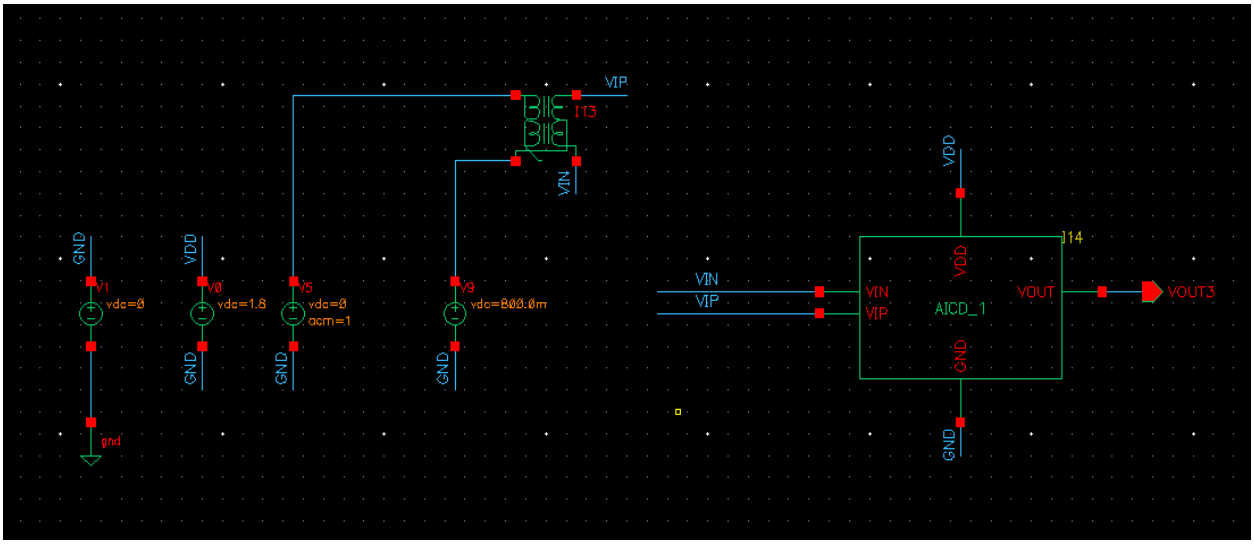

Figure 15

AICD_1 is the Op-Amp circuit. The V_{IC} = 0.8. The ideal balun I used here is to create the VIP and VIN from a DC signal and an AC signal.

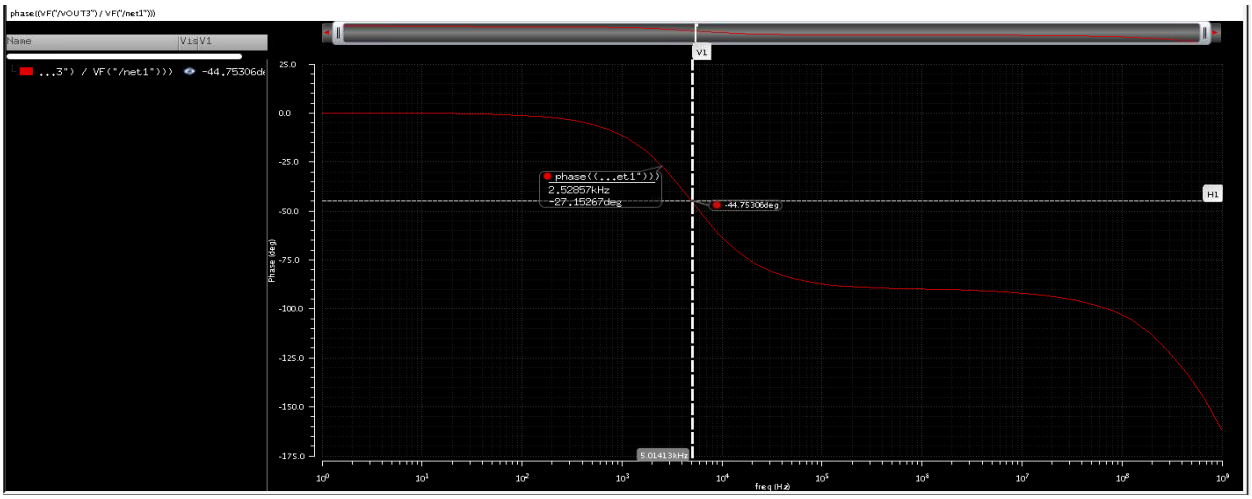

Figure 16

In Figure 16 I have shown the phase response of the output signals with respect to its inputs up to about 330MHz, the phase response is similar to the phase response of a one pole system up to some point.

Sallen-Key Filter design

If the amplifier is working fine, the Sallen-Key Filter should not be very difficult to be designed. For design purposes I am selecting equal $R_{1,2}$ and equal $C_{1,2}$. This will make the poles

of the system occur at the same frequency. The gain of the circuit is shown in Figure 17. For this circuit I can have a gain greater than 0dB. I can make the DC-gain of the circuit to be 3 almost 3dB so that at -3dB cutoff frequency the gain is 0 dB. 3dB = 1.47. Please follow Figure 17 for more explanations regarding the selection of $R_{3,4}$.

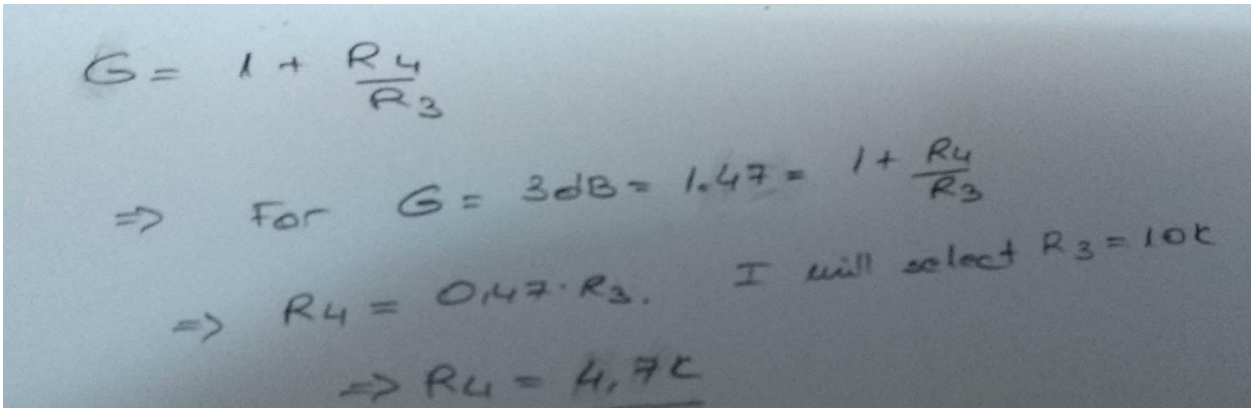

Figure 17

So, in order to have a mid-band gain of 3dB, we have to select the R_3 and R_4 as in Figure 17. Figure 18 shows the complete circuit.

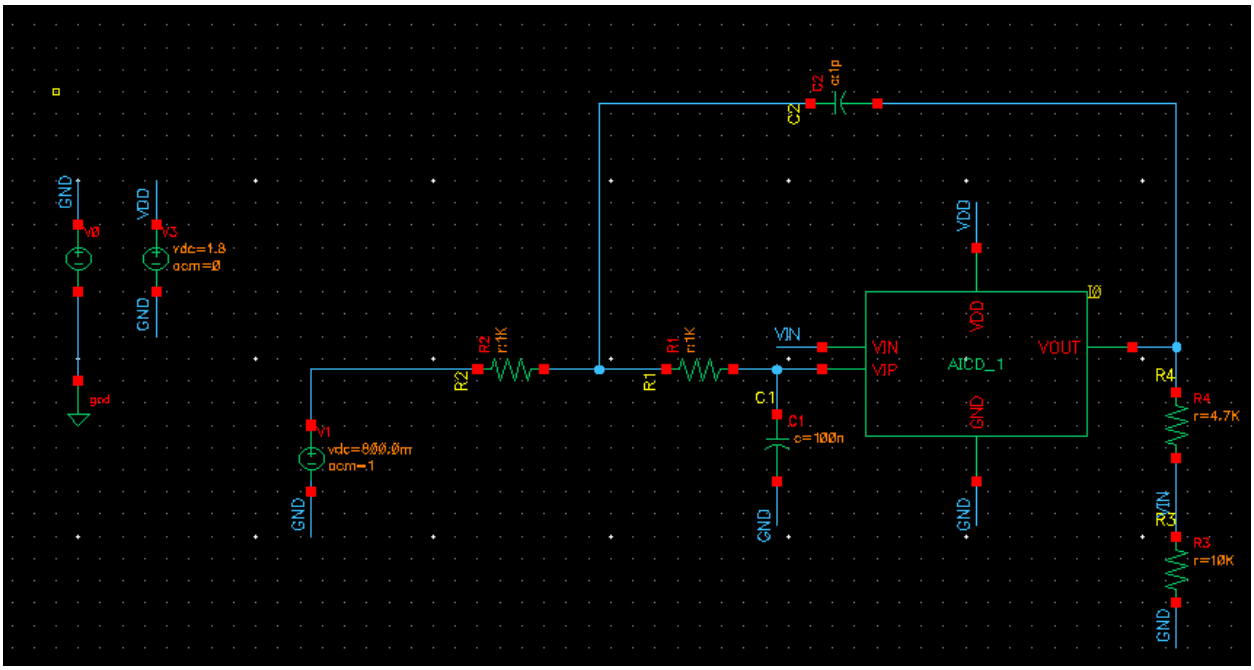

Figure 18

The cutoff frequency for this circuit is: $fc = 1/(2 * pi * R1 * C1)$ EQUATION(1). We can derive this by finding the poles of the transfer function in Figure 2. By using the equations in Figure 2, and one matlab script shown in Figure 19, I found the two poles of the circuit.

```
syms s R1 C1 R2 C2 R3 R4 G
G = (R3+R4)/R3
H = (G/(R1*C1*R2*C2))/(s*s + s*( 1/(R2*C1)+ 1/(R1*C1) + (1-G)/(R2*C2) ) + 1/(R1*C1*R2*C2))
H = simplify(H)
Poles = poles(H,s)
```

Figure 19

Figure 20 shows the output of the matlab code. The poles continue even further than in Figure 20 but I didn't have more space to show them with a screenshot. If I take $R_1 = R_2$ and $C_1 = C_2$, then the poles simplify to the equation (1).

```
G =

(R3 + R4)/R3


H =

(R3 + R4)/(C1*C2*R1*R2*R3*(s^2 + (1/(C1*R1) + 1/(C1*R2) - ((R3 + R4)/R3 - 1)/(C2*R2))*s + 1/(C1*C2*R1*R2)))


H =

(R3 + R4)/(R3 - C1*R1*R4*s + C2*R1*R3*s + C2*R2*R3*s + C1*C2*R1*R2*R3*s^2)


Poles =

  ((C1^2*R1^2*R4^2 - 2*C1*C2*R1^2*R3*R4 - 4*C1*C2*R1*R2*R3^2 - 2*C1*C2*R1*R2*R3*R4 + C2^2*R1^2*R3^2 + 2*C2^2*R1*R2*R3^2 + C2^2*R2^2*R3^2)^(1/2) + C1*R1*R4 - C2*R1*R3 - C2*R2*R3)/(2*C1*C2*
 -((C1^2*R1^2*R4^2 - 2*C1*C2*R1^2*R3*R4 - 4*C1*C2*R1*R2*R3^2 - 2*C1*C2*R1*R2*R3*R4 + C2^2*R1^2*R3^2 + 2*C2^2*R1*R2*R3^2 + C2^2*R2^2*R3^2)^(1/2) - C1*R1*R4 + C2*R1*R3 + C2*R2*R3)/(2*C1*C2*
```

Figure 20

Let's now test the circuit for two different C values. Let's take C = 0.1uF and C = 10nF. These two frequencies should be one decade away from each other. Please refer to calculations in Figure 21.

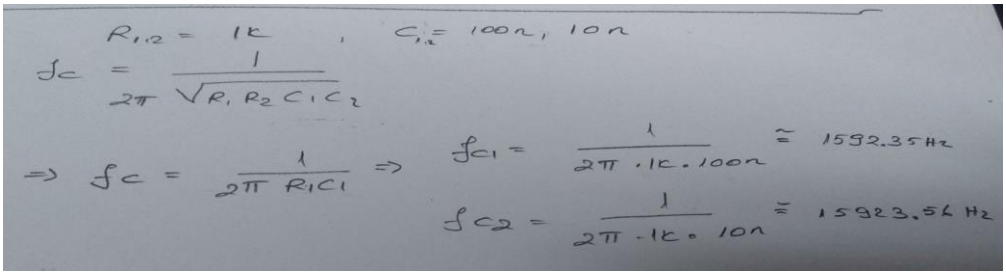

Figure 21

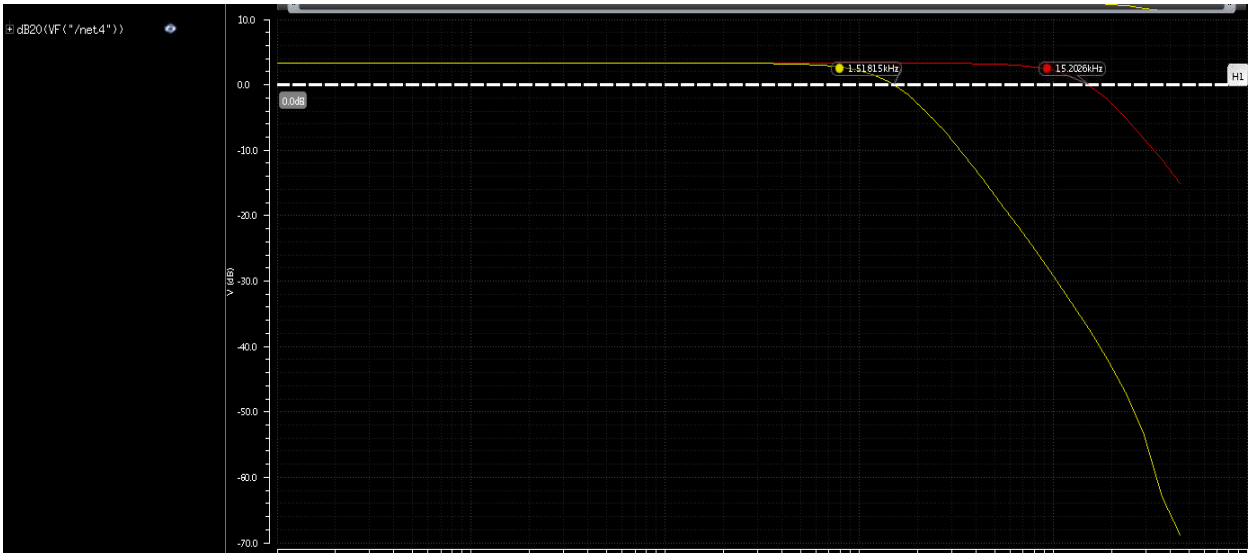

Figure 22

The values calculated in Figure 21 are very close to the simulated values in Figure 22. The mid-band gain is about 3dB as I tried to make sure with the selection of R_3 and R_4. Now I will do some more tests and I will try to build a cutoff frequency vs capacitance table by utilizing matlab as well.

1	1500000	1000000	750000	594000	506000	420000	373000	338000	296000	278000	253000	236000	212430	200000	188793	179000	168000	160000	150700	5970	3000
2	0.1000	0.1500	0.2000	0.2500	0.3000	0.3500	0.4000	0.4500	0.5000	0.5500	0.6000	0.6500	0.7000	0.7500	0.8000	0.8500	0.9000	0.9500	1	25	50

Figure 23

The first row is the cutoff frequency in Hz and the second row is the capacitance value in nanoFarads. I also calculated them by hand and the values are very close to the simulated ones.

Test 1

It would be interesting to see how the circuit filters frequencies higher than the cutoff frequency. I am selecting C = 0.1u. For this value, the magnitude response is shown in Figure 24.

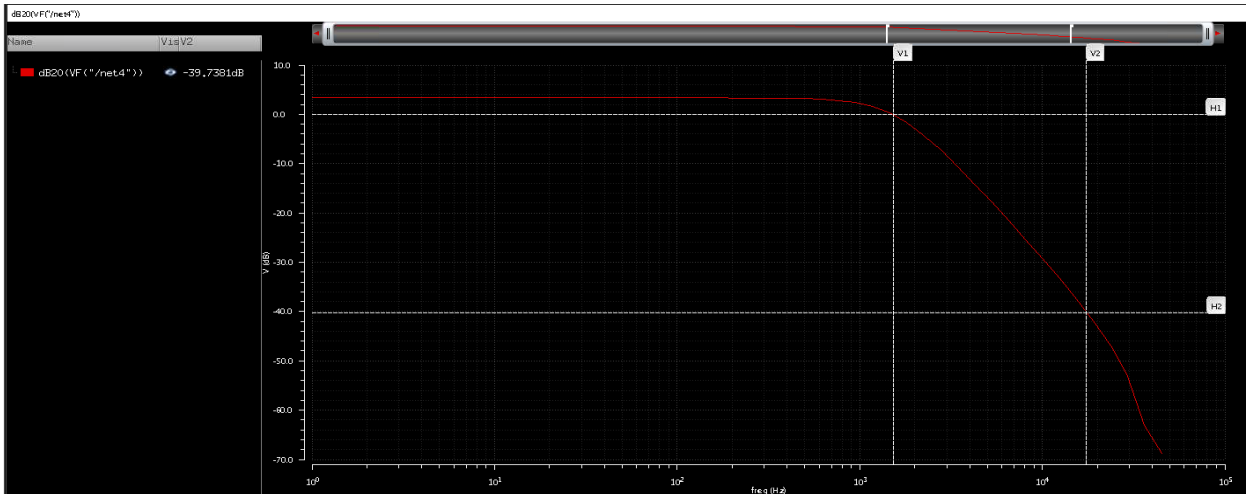

Figure 24

The circuit's mid-band gain is 3dB. Please see carefully that since the poles are at the same frequency, the transfer function decreases with 40dB/dec after the location of poles in the frequency domain. The cutoff frequency is 1.51k. I will input two different harmonics at the input of the circuit. The first harmonic will be 1 kHz and the second harmonic will be 5 kHz. Since the cutoff frequency for this circuit is 1.51 kHz, only the 1 kHz harmonic will be present in the circuit's output. Please refer to the Figure 25 and 26 respectively for the test bench and for the transient response simulation results.

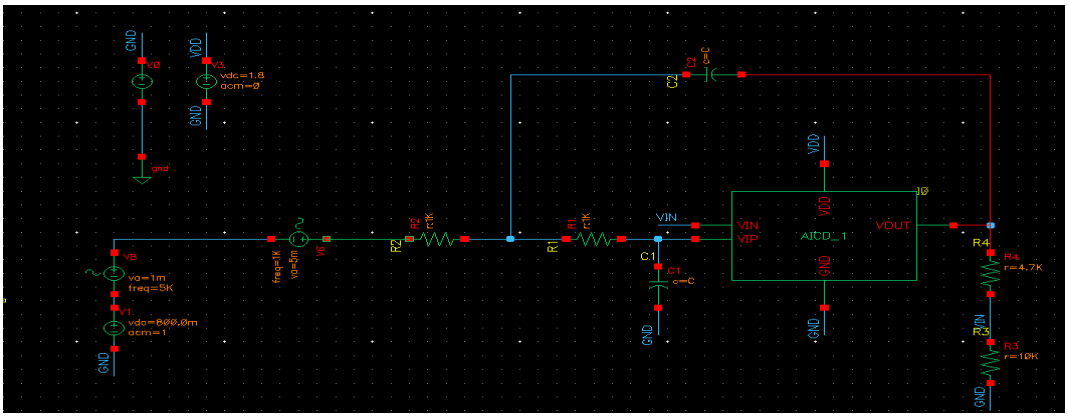

Figure 25

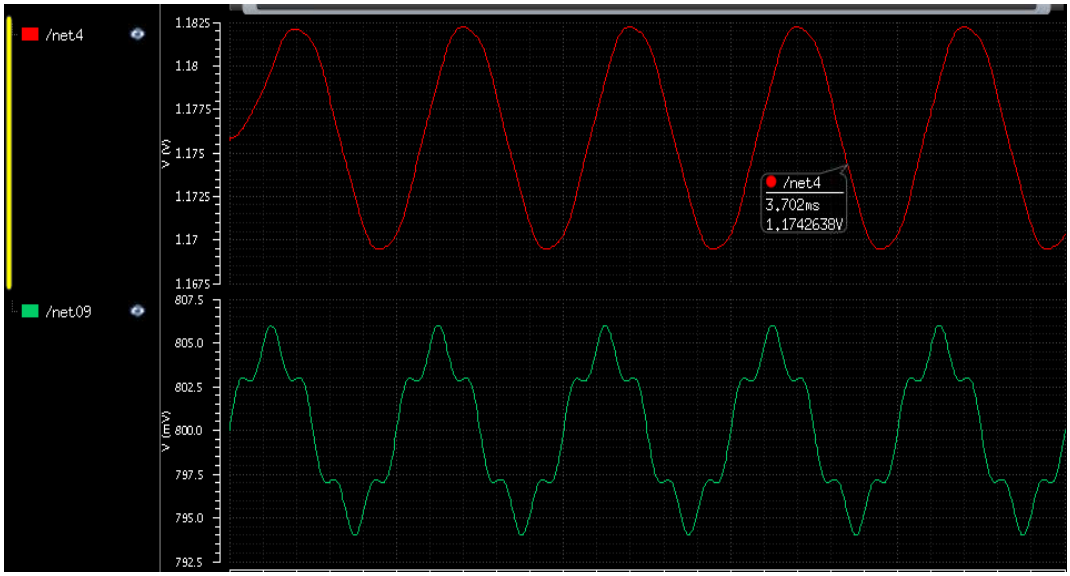

Figure 26

As it seems, the circuit is working nice and good. The circuit is filtering the 5 kHz harmonic and it is allowing only the 1 kHz harmonic to pass to the output. The circuit will work the same way for other selections of C.

Test 2

I will now put a square wave at the input of the circuit. Figure 27 shows the Fourier series of a square wave.

Therefore, *fourier series expression for square wave is*

$$x(t) = \sum_{n=1}^{n=\infty} b_n \sin nw_0 t$$

$$= \frac{4A}{n\Pi} \sum_{n=1}^{n=\infty} \sin nw_0 t$$

$$= \frac{4A}{\Pi} \sin w_0 t + \frac{4A}{3\Pi} \sin 3w_0 t + \frac{4A}{5\Pi} \sin 5w_0 t + \cdots$$

640 x 300

Figure 27

So, if I input a square signal of 1 kHz, there will be harmonics at odd multiples of the input signal frequency. I suspect the filter to filter those out. Let's see what will happen on a transient analysis. Please refer to Figure 28.

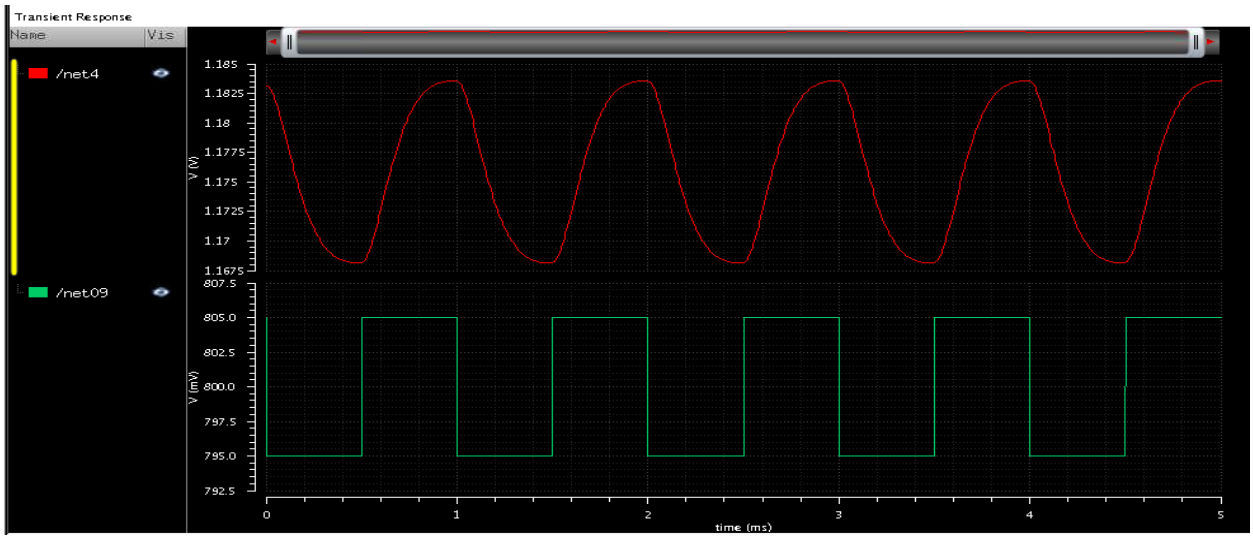

Figure 28

As it seems, the circuit has filtered the other components and the only component remaining is the 1 kHz harmonic since that frequency is smaller than the cutoff frequency. The output waveform is almost a sine function.

Test 3

Now let's test the settling time of this device. I applied a step function with a magnitude of 0.8V and the following is the response.

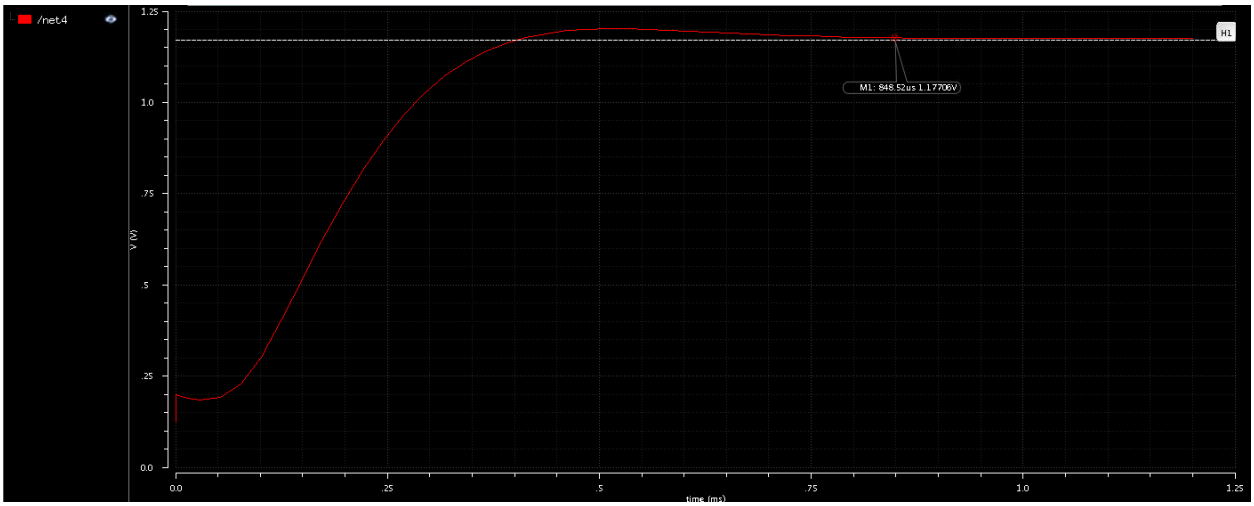

Figure 29

In order to prove that is the correct response, I will write a matlab code which will generate the step response of the circuit given its transfer function. The transfer function of R1= R2 = 1k

and C1 = C2 = 0.1u is shown in Figure 30.

```
sys =

        1.47e08
  --------------------
  s^2 + 15300 s + 1e08

Continuous-time transfer function.
```

Figure 30

I will now multiply the sys function with 0.8 since the step function value will not be 1V but will be 0.8V. The sys transfer function changes to the following:

```
sys =

        1.176e08
  --------------------
  s^2 + 15300 s + 1e08

Continuous-time transfer function.
```

Figure 31

Now I will plot the step response of the circuit. Please refer to Figure 32.

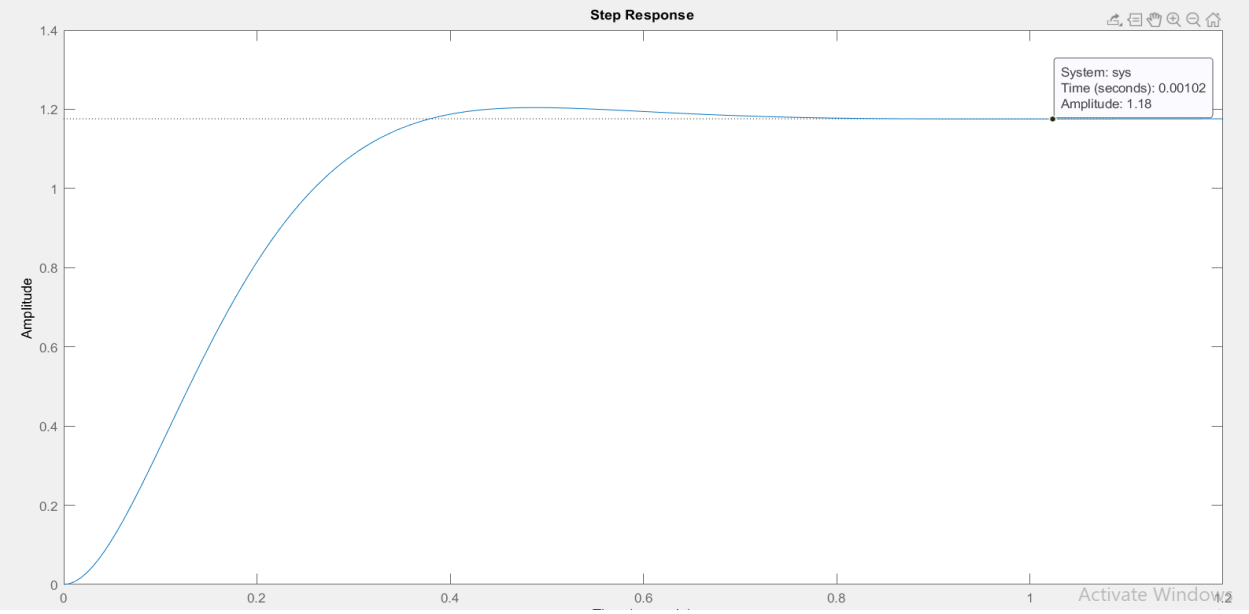

Figure 32

So the simulated response and the calculated response in matlab do not differ by much with some exceptions that come from hardware difficulties.

With this I am finishing this project and I really hope I have explained everything in a clear way.