Manual for the RAM Tester

Objective

This device was specially developed to reliably test a wide range of RAM types from the Commodore series (C64, C128, Amiga 500, 1000, 2000, and some later models). There were already RAM testers on the market, but hardly any supported ZIP (Zig-zag Inline Package) modules.

This device fills this gap and can now test nine different types of RAM chips. As a pure hobby project, the focus is on a simple design with minimal material costs - hence only a single ZIP socket. Additional sockets would have been possible, but on the other hand increased PCB size and wasted sockets. I prefer a minimal HW effort especially PCB for sustainability.

The project has been open source from the beginning. Schematics, board layout, and firmware can be found on GitHub at:

https://github.com/tops4u/ram-tester

Valid for all RAM testers with firmware 2.4.0 and newer

Version: 27.6.2025
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Capabilities

The device can test the following chips:

16 Pin DIP only (Dual Inline Package)

- **4164** - an older chip used in the early C64/C128. Structure: 64K cells (65,535) with one bit each. Totaling 8kB.
- **41256** - a chip from the early Amiga (500/1000/2000) series. Structure: 256K cells (262,144) with one bit each. Totaling 32kB.

18 Pin DIP only

- **4416** - a chip from older computers like the Commodore 16 or Plus. Structure: 16K cells (16,384) with 4 bits each. Totaling 8kB, the same as the 4164, but it writes and reads 4 bits simultaneously.
- **4464** - Was used, for example, in newer C64s and reduced the number of RAM chips from 8 to 2. Organized in 64K cells (65,535) with 4 bits each. Total 32kB.
- **411000** - A somewhat newer chip that was used, for example, in Amiga expansion cards. Organized as 1M cells (1,048,576) with one bit each. Thus, 128kB per chip.

20 Pin DIP or ZIP

- **514256/44256** - A chip used in later Amiga series, sometimes also on expansion cards, e.g., turbo cards. Organized in 256K cells with 4 bits each, totaling 128kB.
- **514258/44258** - Same chip as the 514256/44256 but with the Static Column option - when reading, a CAS strobe is not required for a column change, which saves a small amount of time.
- **514000/441000** - Chip with 1M cells with 4 bits each. Thus, a total storage capacity of 512kB per chip. Was used in later Amigas and in memory expansions.
- **514002/441002** - Same organization as the 514000/441000 but also with the Static Column option (analogous to 514258/44258).

Components of the Tester

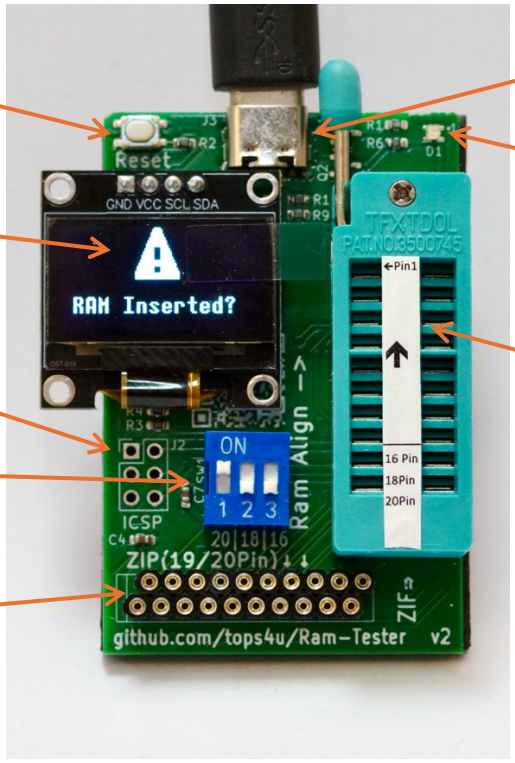
Reset Button, starts the Test.

Display for operations and errors (optional)

ICSP for updates.

DIP Block for PIN count configurations

ZIP socket for ZIP RAM types



Power supply via USB-C

Status LED

ZIF socket for testing DIP RAM. RAM must be inserted with PIN-1 top left!

Test procedure

1. Connect Power

- Connect the device to a 5V power source.
- It is a USB-C device that automatically negotiates 5V with the charger.
- Alternatively, you can use a USB-C to USB-A adapter.

2. Automatic Fuse

- The device has a self-resetting fuse.
- In case of a short circuit or other problems, it switches off for protection.
- Once the fault is resolved, the fuse resets itself after a short time.

3. Warning: Socket Occupancy

- During the test, only one RAM chip may be in one of the two sockets (ZIP or ZIF) - never in both at the same time!

4. Warning: Chip Type

- The 411000 chip may only be used in the ZIF socket (DIP form). Using this chip in the ZIP socket can destroy it!

5. Set the DIP-Switch

- Use the DIP switch to set the number of pins your chip has.
- Only one switch must be in the ON position at any time.
- If none or more than one switch is ON, after a restart, a wrench symbol and "DIP Settings!" will appear on the display. Below this message, you will see the installed firmware version.

Insert the chip to be tested into the appropriate socket. The test is initiated by pressing the «RESET» button.

1. The display starts and shows "RAM-TESTER".
2. The position of the DIP switches is checked. If the combination is invalid, a wrench symbol and the text "DIP Settings!" appear.
3. Depending on the DIP setting, each connection of the RAM chip is checked for a short circuit to ground. If the system finds a short circuit, a lightning bolt symbol is displayed, and the first faulty pin (in ascending order) is shown.
4. The RAM chip is initialized. The device then checks the size of the chip by writing and reading data. If this fails, the warning triangle and the message "RAM inserted?" appear.
5. Once the size has been recognized, the chip designation is shown on the display.
6. Tests of the address lines, the address decoder, and the row and column logic now follow. An error leads to a corresponding error message indicating which address is affected.
7. In the first part of the memory test, all cells are set once to "0" and then to "1". Cells that cannot be switched are detected this way.
8. In the second part, the device writes each row with alternating bit patterns ("01010101..." and "10101010...") and reads it back. If problems occur in step 7 or 8, the message "RAM Faulty" is displayed.
9. In the final test, the device writes random data, immediately performs a RAS-only-refresh, and waits until the minimum guaranteed retention time is reached. Then the complete row is read and compared. If an error occurs here, "Retention Error" appears.

If all steps are completed without errors, the RAM chip is considered OK.

Information: In step 9, a pseudo-random pattern is used. This does not test all cells for their retention period simultaneously. With firmware 2.4.1, new logic was introduced: With each run, the pattern is changed so that all bits are inverted. To cover all cells, you can run the test twice in a row with the same chip.