TOPST AI-G Hardware

User Guide

Rev. 1.01 [G]
2025-07-18

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1 INTRODUCTION

This document is a hardware user guide for the AI-G based on the TCC7501. This document describes system installation, debugging, and detailed information on the overall design and usage of the AI-G.

1.1 Terminology

Terminology	Definition
CPU	Central Processing Unit
FWDN	Firmware Download
GPIO	General Purpose Input Output
HAT	Hardware Attached on Top
TOPS	Tera Operations Per Second
TOPST	Total Open-platform for System development and Training

2 BLOCK DIAGRAM

2.1 System Block Diagram

Figure 2.1 shows the system block diagram of the AI-G.

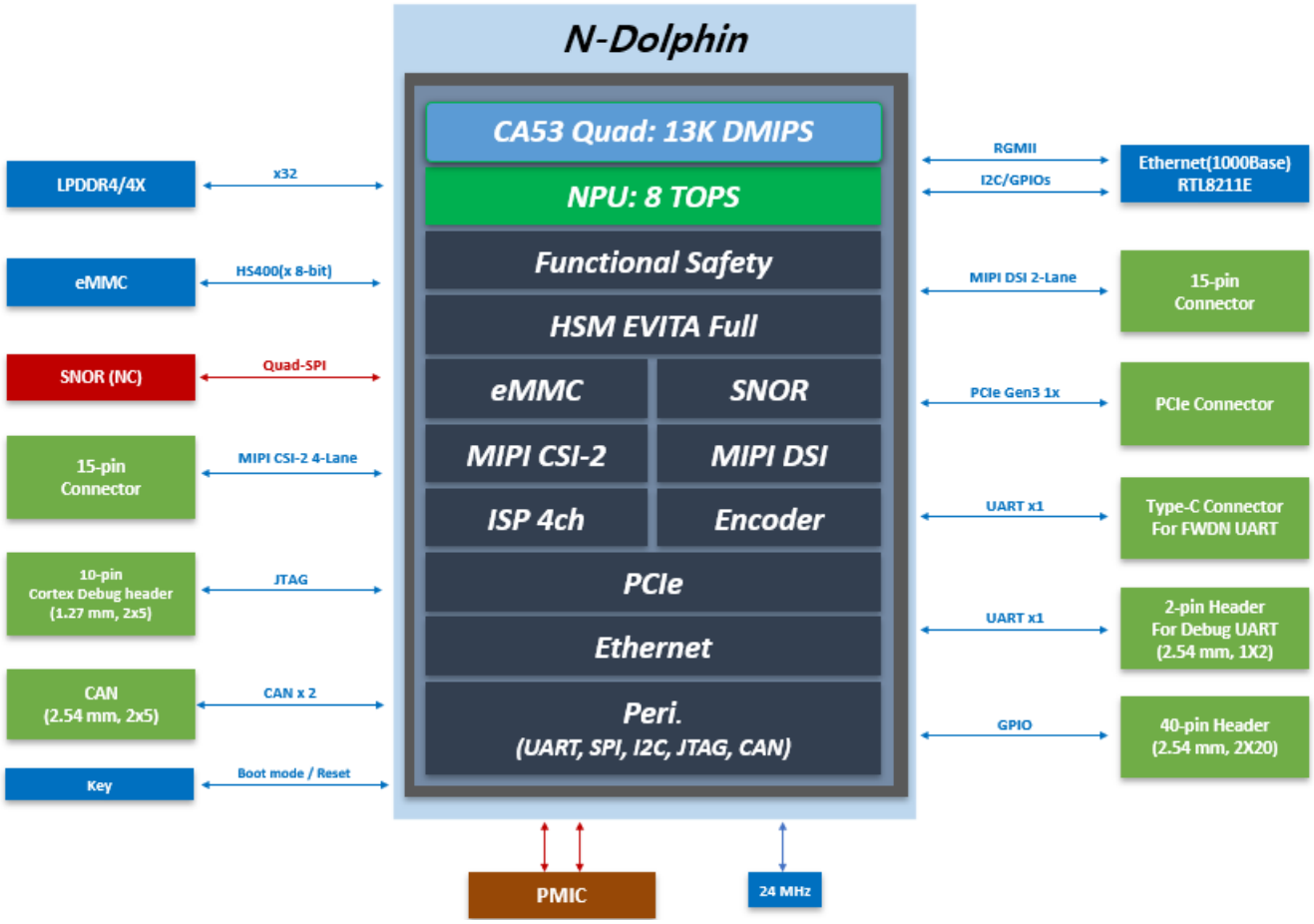

Figure 2.1 System Block Diagram

2.2 Features of AI-G Board

Table 2.1 describes the features of the AI-G board.

Table 2.1 Features of AI-G Board

Function		Description	Note
Processor	TCC7501	Main Processor: Cortex-A53 Quad Neural Processor: 8 TOPS	
Memory	eMMC	eMMC 5.1 Speed: HS200 Density: 8 GB	
	LPDDR4X	Maximum Clock: 2133 MHz Density: 2 GB 32-bit	
Video Out	MIPI DSI	1-channel MIPI DSI-2 2-lane	
Video In	MIPI CSI	1-channel MIPI CSI-2 2-lane	Option: 2-channel MIPI CSI-2 4-lane
Peripheral	CAN	3 CAN Transceivers Vendor: Microchip Part number: MCP2562FD-E/SN	
	Ethernet	Ethernet PHY 1000Base-T Vendor: Realtek Part number: RTL8211E	For Firmware Downloader (***FWDN***)
X-TAL	Main	24 MHz	
Pin Header (Male)	UART	DBG UART 4-pin/2.54 mm Pin Header (Male)	
	CAN	CAN 10-pin/2.54 mm Pin Header (Male) CAN Channel selection: CAN 0 and CAN 1	
	JTAG	JTAG 10-pin/1.27 mm Pin Header (Male) System debugging	
	GPIO	GPIO 40-pin/1.27 mm Pin Header (Male) Provide 28 GPIOs through 40-pin header	
Connector	UART	FWDN UART 1-port ■ USB Type-C Connector	
	MIPI DSI	1.0 mm pitch 15-pin	
	MIPI CSI	0.8 mm pitch 40-pin	
	Peripheral Component Interconnect Express (PCIe)	PCI Express Standard	
	Ethernet	RJ45	
Jack	DC Jack	For power input (5V)	
Switch	Boot Mode	System Boot mode switch	
	Reset	System RESET switch	

Note: For inquiries about the AI-G, contact TOPST. [1]

3 OVERVIEW

3.1 AI-G Board

Figure 3.1 shows the top view of the AI-G board.

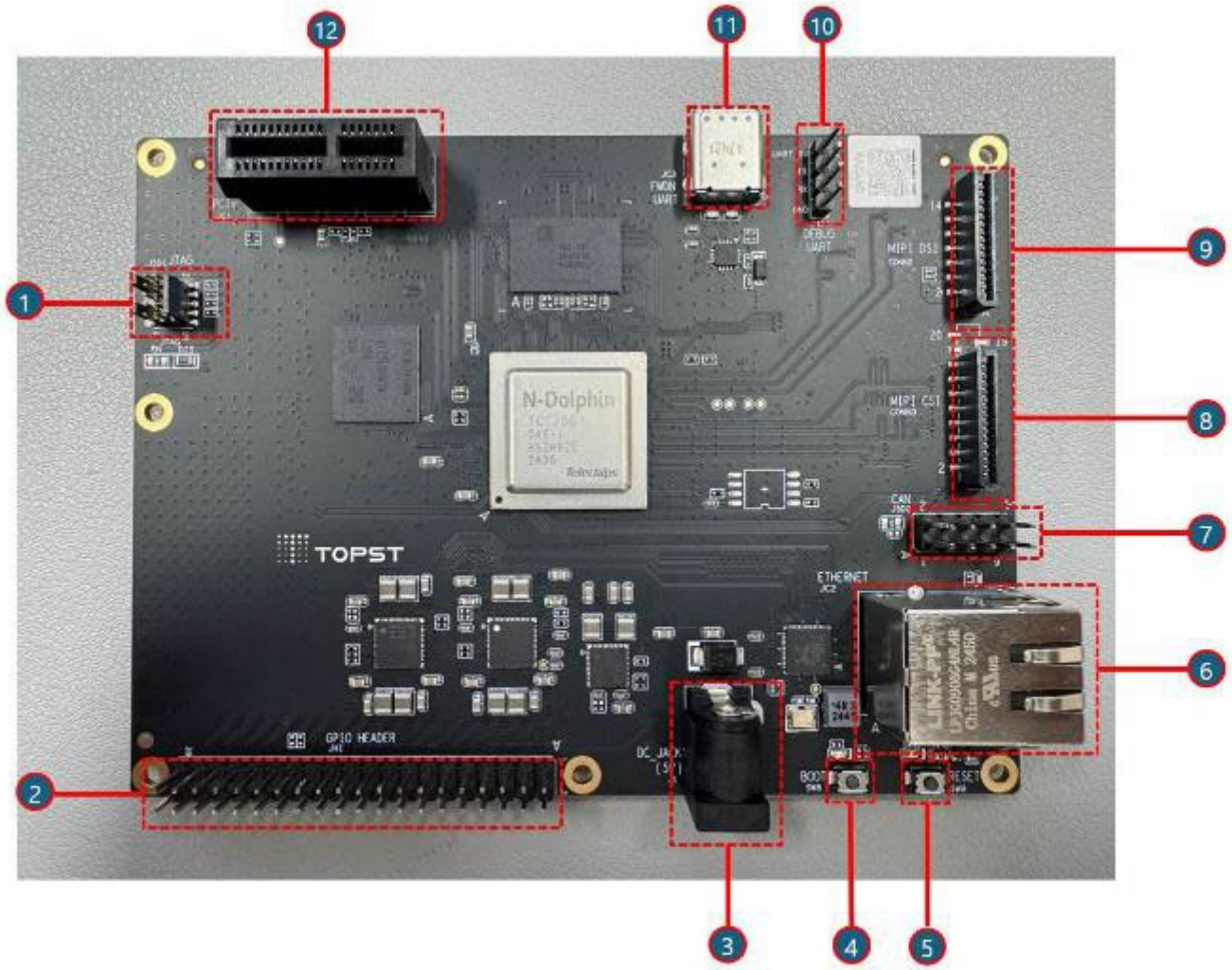

Figure 3.1 AI-G Board (Top View)

Table 3.1 describes the connectors of the AI-G board (top view).

Table 3.1 Description of AI-G Board (Top View)

Number	Reference Number	Name	Description
1	J5D1	JTAG Connector	JTAG Connector for system debugging
2	JH1	GPIO Pin Header (Male)	General Function Interface Header
3	J1	Power Jack	5V Power Jack
4	SW8	Boot Mode Switch	Switch for changing boot mode
5	SW9	RESET Switch	Switch for system reset
6	JC2	RJ45 Connector	Legacy Ethernet port
7	J5D2	10-pin Header (Male)	CAN Header
8	CONN3	MIPI CSI Connector	Connect to the Camera module
9	CONN2	MIPI DSI Connector	Connect to the Display module
10	J4S1	DBG UART Connector	UART Debug Port
11	JC3	USB Type-C Connector	USB 2.0 FWDN connector
12	JC1	PCIe Standard Connector	Connect to the PCIe Device

4 SPECIFICATIONS

4.1 LPDDR4X

The LPDDR4X memory is located on the AI-G board and the information is as follows:

- 32-bit
- Density: 2 GB
- Maximum Clock: 2133 MHz

4.2 eMMC

The eMMC memory is located on the AI-G board and the information is as follows:

- eMMC 5.1
- Density: 8 GB
- Supports up to HS200

4.3 Power Connector (J1)

J1 is a DC 5V external power supply connector with a 2.5 mm x 5.5 mm plug. It is used to supply power to the AI-G board. The power supply current should be at least 5A.

Figure 4.1 shows the power plug size for DC 5V power supply.

Figure 4.1 Plug Size for DC 5V Power Supply

Note: The plug size must be compatible with 2.1 mm to 2.5 mm.

Caution: Compatibility problems may occur if you use an adapter other than the power adapter provided by TOPST.

Figure 4.2 Power Connector (J1)

4.4 JTAG Connector (J5D1)

J5D1 is a standard 10-pin/1.27 mm connector for the JTAG emulator.

Figure 4.3 shows the location of J5D1 on the AI-G board.

Figure 4.3 JTAG Connector (J5D1)

Table 4.1 describes the pins of J5D1.

Table 4.1 J5D1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J5D1	
1	SYS_3P3	-	Power 3.3V
2	TMS	◄	Test Mode State
3	DGND	-	Ground
4	TCK	◄	Test Clock
5	DGND	-	Ground
6	TDO	►	Test Data Output
7	NC	-	Not Connected
8	TDI	◄	Test Data In
9	DGND	-	Ground
10	JTAG_RST#	◄	System Reset

4.5 Boot Mode

The AI-G board supports two boot modes:

- USB Boot Mode (FWDN)
- eMMC Boot Mode (GPIO_SD Group)

The AI-G board is set to eMMC Boot Mode by default. If there is no boot image in the eMMC Device, the boot mode is automatically switched to USB Boot Mode.

4.5.1 USB Boot Mode (FWDN)

Figure 4.4 shows the Boot Mode switch and RESET switch. USB Boot Mode is used for firmware updates. To enter USB boot mode, both the Boot mode switch and RESET switch are required. It is recommended to use this method when uploading the image.

Figure 4.4 Boot Mode Switch and RESET Switch for Entering USB Boot Mode

The following steps describe the switch operation for entering USB Boot Mode.

1. When power is supplied, the LED above the RESET switch turns on.
2. Press and hold the Boot Mode switch. When you press the Boot Mode switch, you can see the red LED above the Boot Mode switch turn on. Keep pressing the switch to keep the LED on.
3. The RESET switch LED is green by default. If you press the RESET switch once, the green LED turns off and then turns on again.
4. Release the Boot Mode switch.

Figure 4.5 shows the operation sequence of the Boot Mode and RESET switches for entering USB Boot Mode (FWDN).

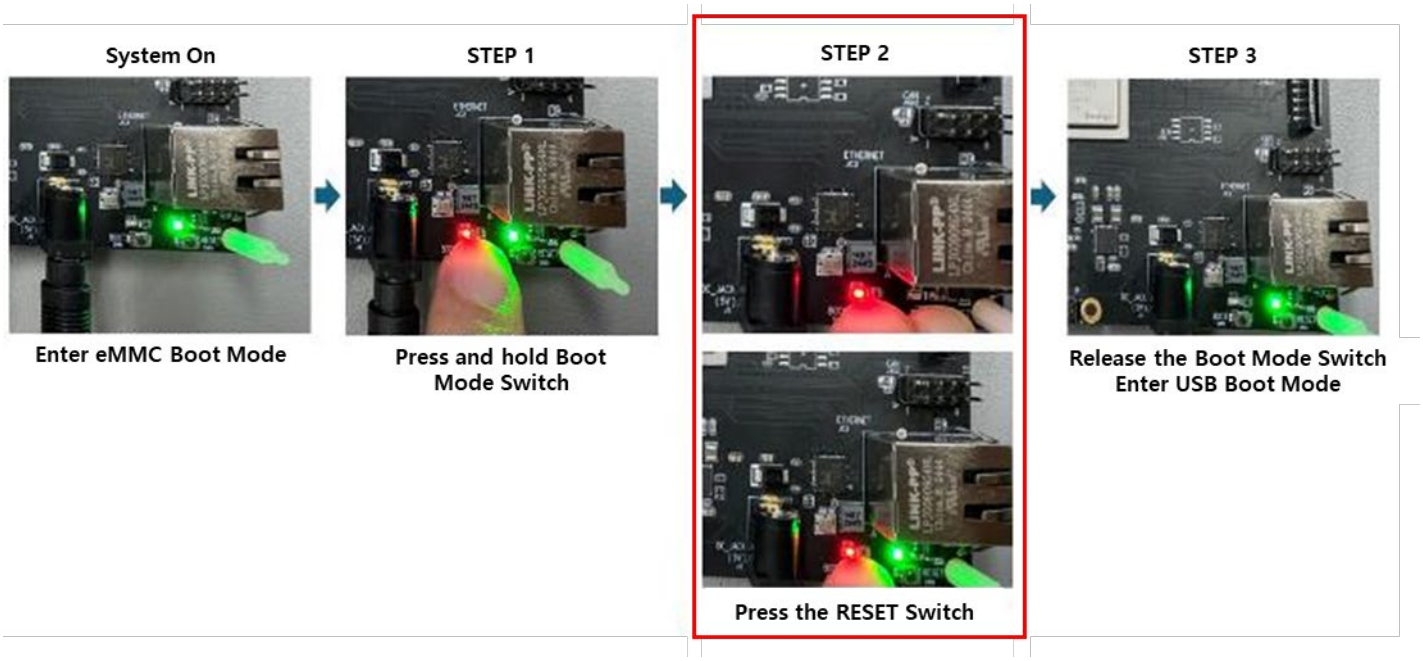

Figure 4.5 Sequence of Entering USB Boot Mode (FWDN)

4.6 PCIe Connector (JC1)

Figure 4.6 shows the PCIe connector that enables the use of the PCIe interface devices on the AI-G board. The AI-G supports PCIe-gen3 x 1-lane.

- PCIe Controller: Supports Gen3, 1-lane operation
- Inbound/Outbound Address Translation Units (iATU): 4 channels available
- PCIe Reference Clock: Internal clock (refclk_type = 0)

Figure 4.6 PCIe Standard Connector (JC1)

Table 4.2 describes the pins of JC1.

Table 4.2 JC1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► JC1	
A1	PCIe_DETECT	◄	PCIe Card Detection
B1	12V_TP	-	Power 12V Test Point
A2	12V_TP	-	Power 12V Test Point
B2	12V_TP	-	Power 12V Test Point
A3	12V_TP	-	Power 12V Test Point
B3	12V_TP	-	Power 12V Test Point
A4	DGND	-	Ground
B4	DGND	-	Ground
A5	NC	-	Not Connected
B5	NC	-	Not Connected
A6	NC	-	Not Connected
B6	NC	-	Not Connected
A7	NC	-	Not Connected
B7	DGND	-	Ground
A8	NC	-	Not Connected
B8	PCIe_3P3	-	Power 3.3V
A9	PCIe_3P3	-	Power 3.3V
B9	NC	-	Not Connected
A10	PCIe_3P3	-	Power 3.3V
B10	PCIe_3P3	-	Power 3.3V
A11	PCIe_RST#	►	PCIe Reset
B11	PCIe_WAKE#	◄	PCIe Wake
A12	DGND	-	Ground
B12	PCIe_CLKREQ#	◄	PCIe Clock Request
A13	PCIe_REFCLKOUT_P	►	PCIe Positive Clock
B13	DGND	-	Ground
A14	PCIe_REFCLKOUT_N	►	PCIe Negative Clock
B14	PCIe_TXP	►	PCIe Transmit Positive Data
A15	DGND	-	Ground
B15	PCIe_TXN	►	PCIe Transmit Negative Data
A16	PCIe_RXP	◄	PCIe Receive Positive Data
B16	DGND	-	Ground
A17	PCIe_RXN	◄	PCIe Receive Negative Data
B17	PCIe_DET#	◄	PCIe Card Detection
A18	DGND	-	Ground

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► JC1	
B18	DGND	-	Ground

4.7 MIPI DSI and MIPI CSI Connectors (CONN2 and CONN3)

Figure 4.7 and Figure 4.8 show the MIPI DSI and MIPI CSI connectors on the AI-G board. The AI-G supports 1 channel of MIPI CSI and MIPI DSI, each configured with 2-lane interface. A 4-lane interface (MIPI CSI) is optional and requires a 20-pin connector instead of a 15-pin connector.

The supported output media through MIPI includes:

- MIPI DSI: Supports resolutions up to 1920 x 1080 at 60 fps

Figure 4.7 MIPI DSI Connector (CONN2)

Table 4.3 describes the pins of CONN2.

Table 4.3 CONN2 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► CONN2	
1	SYS_3P3	-	Power 3.3V
2	SYS_3P3	-	Power 3.3V
3	DGND	-	MIPI0_I2C Clock
4	MIPI_M_SDA	◄►	Serial Data for SerDes IC
5	MIPI_M_SCL	►	Serial Data for SerDes Clock
6	DGND	-	Ground
7	MIPI_M_D0P	►	MIPI DSI-2 Positive Data 0
8	MIPI_M_D0N	►	MIPI DSI-2 Negative Data 0
9	DGND	-	Ground
10	MIPI_M_CLKP	►	MIPI DSI-2 Positive Clock
11	MIPI_M_CLKN	►	MIPI DSI-2 Negative Clock
12	DGND	-	Ground
13	MIPI_M_D1P	►	MIPI DSI-2 Positive Data 1
14	MIPI_M_D1N	►	MIPI DSI-2 Negative Data 1
15	DGND	-	Ground

Figure 4.8 MIPI CSI Connector (CONN3)

Table 4.4 describes the pins of CONN3.

Table 4.4 CONN3 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► CONN3	
1	RPI_CAM_3P3	-	Power 3.3V
2	MIPI_S_SDA	◄►	MIPI0_I2C Data
3	MIPI_S_SCL	►	MIPI0_I2C Clock
4	MIPI_S_GPIO1	◄	General Purpose I/O
5	MIPI_S_PWDN	►	General Purpose I/O
6	GND	-	Ground
7	MIPI_S_CLKP	◄	MIPI CSI-2 Positive Clock
8	MIPI_S_CLKN	◄	MIPI CSI-2 Negative Clock
9	GND	-	Ground
10	MIPI_S_D1P	◄	MIPI CSI-2 Positive Data 1
11	MIPI_S_D1N	◄	MIPI CSI-2 Negative Data 1
12	GND	-	Ground
13	MIPI_S_D0P	◄	MIPI CSI-2 Positive Data 0
14	MIPI_S_D0N	◄	MIPI CSI-2 Negative Data 0
15	GND	-	Ground
16	MIPI_S_D3P	◄	MIPI CSI-2 Positive Data 3
17	MIPI_S_D3N	◄	MIPI CSI-2 Negative Data 3
18	GND	-	Ground
19	MIPI_S_D2P	◄	MIPI CSI-2 Positive Data 2
20	MIPI_S_D2N	◄	MIPI CSI-2 Negative Data 2

4.8 Debug UART Pin Header (Male) (J4S1)

Figure 4.9 shows the debug UART header pin for system debugging. Pin 1 (UART 5V) is a dummy pin and does not provide an output.

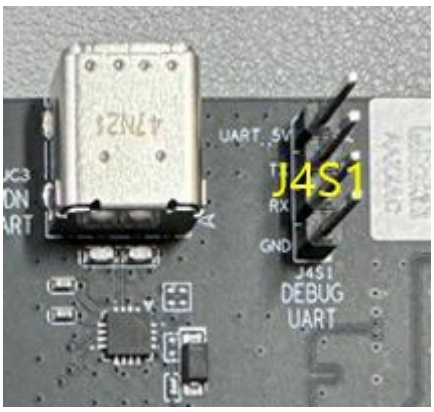

Figure 4.9 Debug UART Pin Header (Male) (J4S1)

Table 4.5 describes the pins of J4S1.

Table 4.5 J4S1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J4S1	
1	USB_5P0	-	Dummy Pin
2	DBG_UT_TX	►	UART Transmit Data
3	DBG_UT_RX	◄	UART Receive Data
4	GND	-	Ground

4.9 Ethernet Connector (JC2)

Figure 4.10 shows the Ethernet connector on the AI-G board. The AI-G board has one Ethernet MAC controller (JC2). JC2 is an RJ45 connector that supports 10 Mbps, 100 Mbps, and 1000 Mbps Ethernet connections.

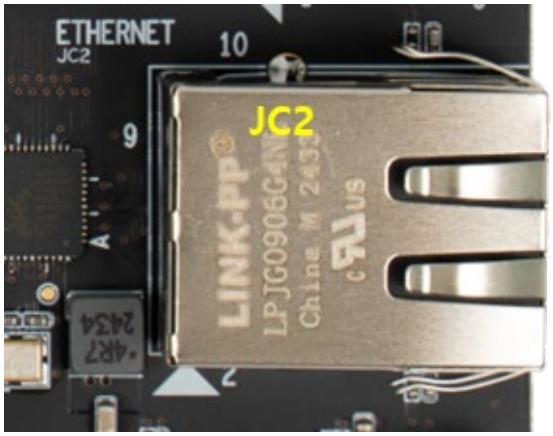

Figure 4.10 Ethernet Connector (JC2)

4.10 CAN Pin Header (Male) (J5D2)

Figure 4.11 shows the CAN pin header (male) on the AI-G board. The AI-G board supports 2-channel CAN.

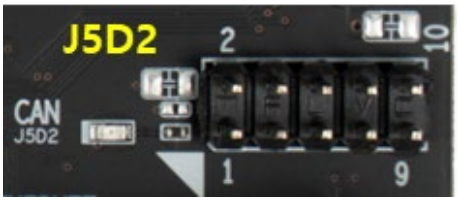

Figure 4.11 CAN Pin Header (Male) (J5D2)

Table 4.6 describes the pins of J5D2.

Table 4.6 J5D2 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J5D2	
1	CAN_3P3	-	Power 3.3V
2	CAN_3P3		Power 3.3V
3	CAN0_TX	►	Transmit Data of CAN0 channel
4	CAN0_RX	◄	Receive Data of CAN0 channel
5	CAN1_TX	►	Transmit Data of CAN1 channel
6	CAN1_RX	◄	Receive Data of CAN1 channel
7	NC	-	Not Connected
8	NC	-	Not Connected
9	DGND	-	Ground
10	DGND	-	Ground

4.11 General Purpose I/O Pin Header (Male) (JH1)

Figure 4.12 shows the general purpose I/O (GPIO) pin header on the AI-G board. The GPIO pin header can be used to connect the Hardware Attached on Top (HAT), which is a Raspberry Pi accessory.

Figure 4.12 General Purpose I/O Pin Header (Male) (JH1)

Table 4.7 describes the pins of JH1.

Table 4.7 JH1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU◄► JH1	
1	SYS_3P3	-	Power 3.3V
2	SYS_5P0	-	Power 5.0V
3	I2C_SDA	◄►	I2C Data
4	SYS_5P0	-	Power 5.0V
5	I2C_SCL	◄►	I2C Clock
6	GND	-	Ground
7	GPIO_D3/MFIO	◄►	General Purpose I/O
8	EXT_TXD	◄►	UART Transmit Data
9	GND	-	Ground
10	EXT_RXD	◄►	UART Receive Data
11	GPIO_D02/MFIO	◄►	General Purpose I/O
12	GPIO_E09	◄►	General Purpose I/O
13	GPIO_D01/MFIO	◄►	General Purpose I/O
14	GND	-	Ground
15	GPIO_D00/MFIO	◄►	General Purpose I/O
16	GPIO_F02	◄►	General Purpose I/O
17	SYS_3P3	-	Power 3.3V
18	GPIO_F03	◄►	General Purpose I/O
19	SPI0_MOSI	◄►	SPI MOSI
20	GND	-	Ground
21	SPI0_MISO	◄►	SPI MISO
22	GPIO_E07		General Purpose I/O
23	SPI0_SCLK	◄►	SPI SCLK
24	SPI0_CS0	◄►	SPI CS
25	GND	-	Ground
26	GPIO_E00	◄►	General Purpose I/O
27	RESERVED0(NC)	-	Not Connection
28	RESERVED1(NC)	-	Not Connection
29	GPIO_F10	◄►	General Purpose I/O
30	GND	-	Ground
31	GPIO_F08	◄►	General Purpose I/O
32	GPIO_E10	◄►	General Purpose I/O
33	GPIO_E08	◄►	General Purpose I/O
34	GND	-	Ground
35	SPI1_MISO	◄►	SPI MISO
36	SPI1_CS0	◄►	SPI CS
37	GPIO_F09	◄►	General Purpose I/O
38	SPI1_MOSI	◄►	SPI MOSI
39	GND	-	Ground
40	SPI1_SCLK	◄►	SPI SCLK

5 REFERENCES

[1] Contact TOPST for more details: topst@topst.ai

Note: Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

6 REVISION HISTORY

Rev. 1.01: 2025-07-18

- Updated
  - Chapter 2.1: Figure 2.1
  - Chapter 2.2:
    - Changed chapter title from "Features of TOPST AI-G Board" to "Features of AI-G Board"
    - Added **Note**
  - Chapter 3.1: Changed chapter title from "TOPST AI-G Board" to "AI-G Board"
  - Chapter 4.3: Added **Caution**
  - Chapter 4.6: Description
  - Chapter 4.7: Description
  - Chapter 4.11: Table 4.7

Rev. 1.00: 2025-02-28

- Official version release

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