# TOPST VCP-G Hardware

## User Guide

**Rev. 1.01 [G]**
**2025-07-18**

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# 1 INTRODUCTION

This document is a hardware user guide for the VCP-G based on the TCC7045. This document describes system installation, debugging, and detailed information on the overall design and usage of the VCP-G.

## 1.1 Terminology

**Table 1.1 Terminology**

| Terminology | Definition |
|---|---|
| ADC | Analog to Digital Converter |
| FWDN | Firmware Download |
| GPIO | General Purpose Input Output |
| MCU | Micro-Controller Unit |
| TOPST | Total Open-Platform for System development and Training |
| VCP | Vehicle Control Processor |

# 2 BLOCK DIAGRAM

## 2.1 System Block Diagram

Figure 2.1 shows the system block diagram of the VCP-G.

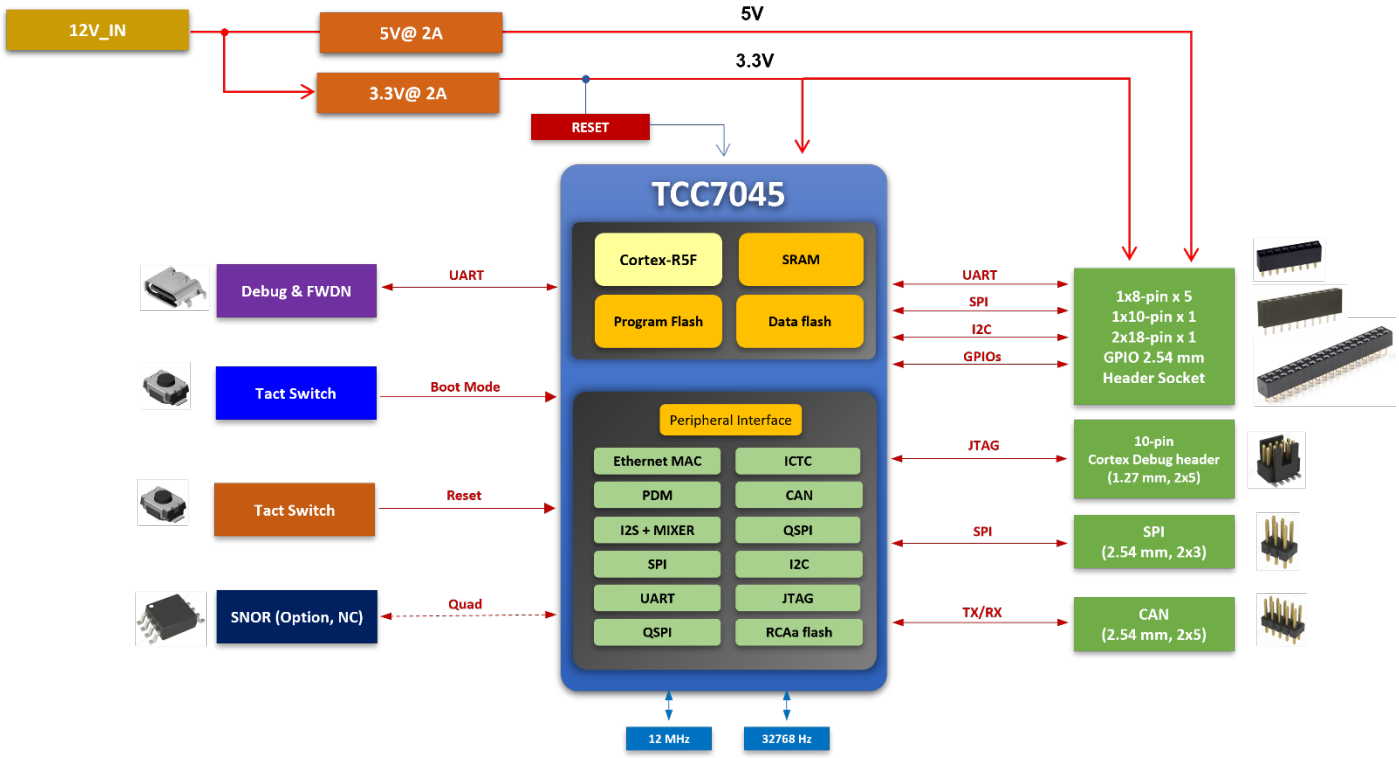


**Figure 2.1 System Block Diagram**

## 2.2 Features of VCP-G Board

Table 2.1 describes the features of the VCP-G board.

**Table 2.1 Features of VCP-G Board**

| | | | |
|---|---|---|---|
| **Part Name** | | | TCC7045 |
| **Package** | | | Package Pin to Pin Compatible FBGA-196pin (12BD) |
| **CPU Frequency** | | | 200 MHz (Up to 300 MHz) |
| **On-chip Memory** | **Program Flash** | | 4 MB |
| | **SRAM** | | 512 KB (Including Retention RAM 16 KB) |
| | **Data Flash** | | 256 KB |
| | **DMA Channel** | | 16-channel |
| **Peripheral** | **Ethernet** | | 1 Gbps with AVB |
| | **CAN/CANFD** | | 3 channels |
| | **Dedicated LIN/UART** | | 3 channels (Maximum 6-channel) |
| | **Dedicated I2C** | | 3 channels (Maximum 6-channel) |
| | **Dedicated GPSB (SPI)** | | 2 channels (Maximum 5-channel) |
| | **MFIO (Allocated UART, I2C, GPSB)** | | 3 channels |
| | **ADC** | **Resolution** | 12-bit SAR type |
| | | **Channels** | 12-channel x 2 groups |
| | | **Input Range** | 3.3V |
| | | **Sample Rate** | Over 1.0 MSPs |
| | **I2S** | | 1-channel |
| | **Serial Flash Interface** | | Quad SPI |
| **Power System** | | | 3.3V single |
| **Temperature** | | | -40 to 105 °C |

# 3 OVERVIEW

## 3.1 VCP-G Board

Figure 3.1 shows the top view of the VCP-G board.

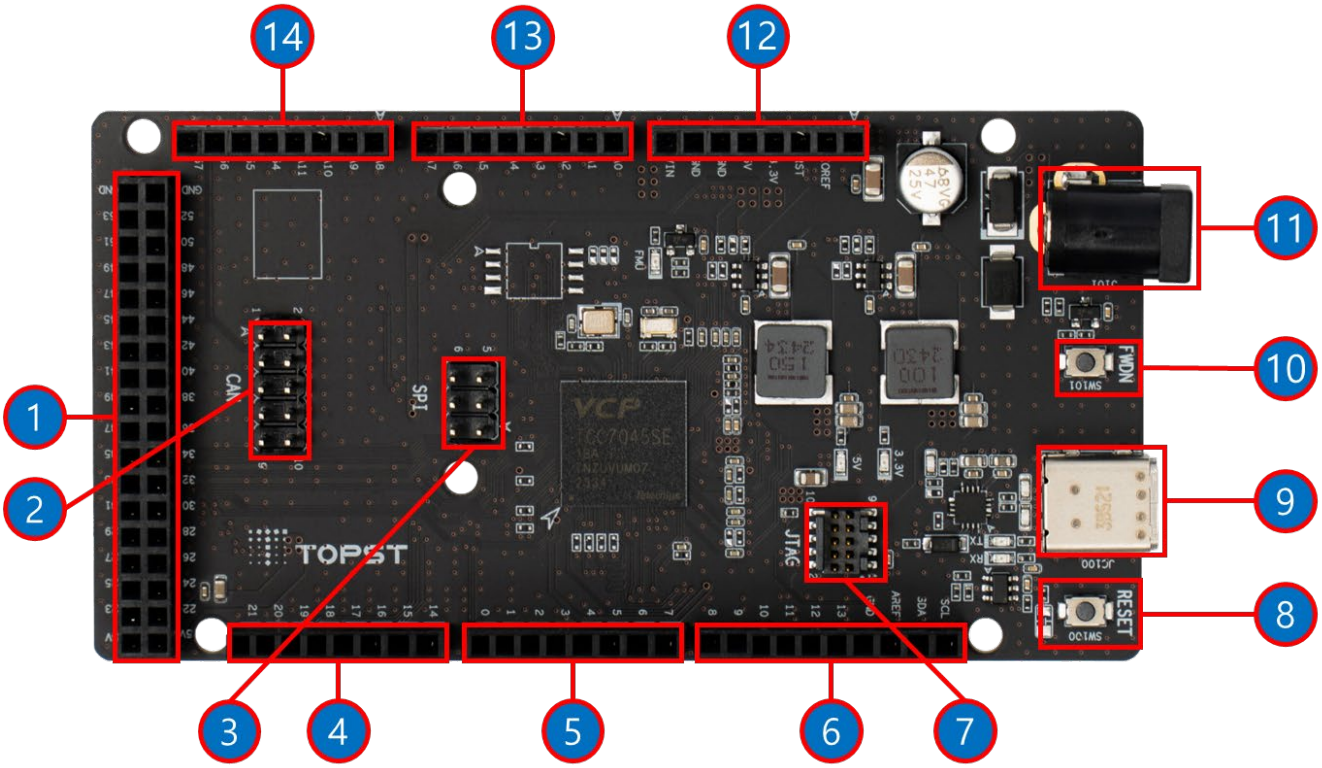


**Figure 3.1 VCP-G Board (Top View)**

Table 3.1 describes the connectors of the VCP-G board (top view).

**Table 3.1 Connectors of VCP-G Board (Top View)**

| Number | Reference Number | Name | Description |
|---|---|---|---|
| 1 | J18D100 | 36-pin Socket Header (Female) | Header for GPIO and ADC |
| 2 | J5D100 | 10-pin Header (Male) | Header for CAN |
| 3 | J3D100 | 6-pin Header (Male) | Header for SPI |
| 4 | J8D104 | 8-pin Socket Header (Female) | Header for GPIO and ADC |
| 5 | J8D102 | 8-pin Socket Header (Female) | Header for GPIO |
| 6 | J10D100 | 10-pin Socket Header (Female) | Header for GPIO and ADC |
| 7 | J100 | 10-pin Header (Male) | Header for JTAG |
| 8 | SW100 | RESET Switch | Switch for system reset |
| 9 | JC100 | USB Type-C Connector | UART for debugging or FWDN port |
| 10 | SW101 | Tact Switch | FWDN: Enter the Firmware download mode of TCC7045 |
| 11 | J101 | Power Jack | 12V Power Jack |
| 12 | J8D100 | 8-pin Socket Header (Female) | Header for Power and Reset |
| 13 | J8D101 | 8-pin Socket Header (Female) | Header for GPIO and ADC |
| 14 | J8D103 | 8-pin Socket Header (Female) | Header for GPIO and ADC |

Figure 3.2 shows the bottom view of the VCP-G board.

**Note:** Figure 3.2 currently shows the VCP-G_V1.1.1 board. This image will be updated to the VCP-G_V2.1.1 board.

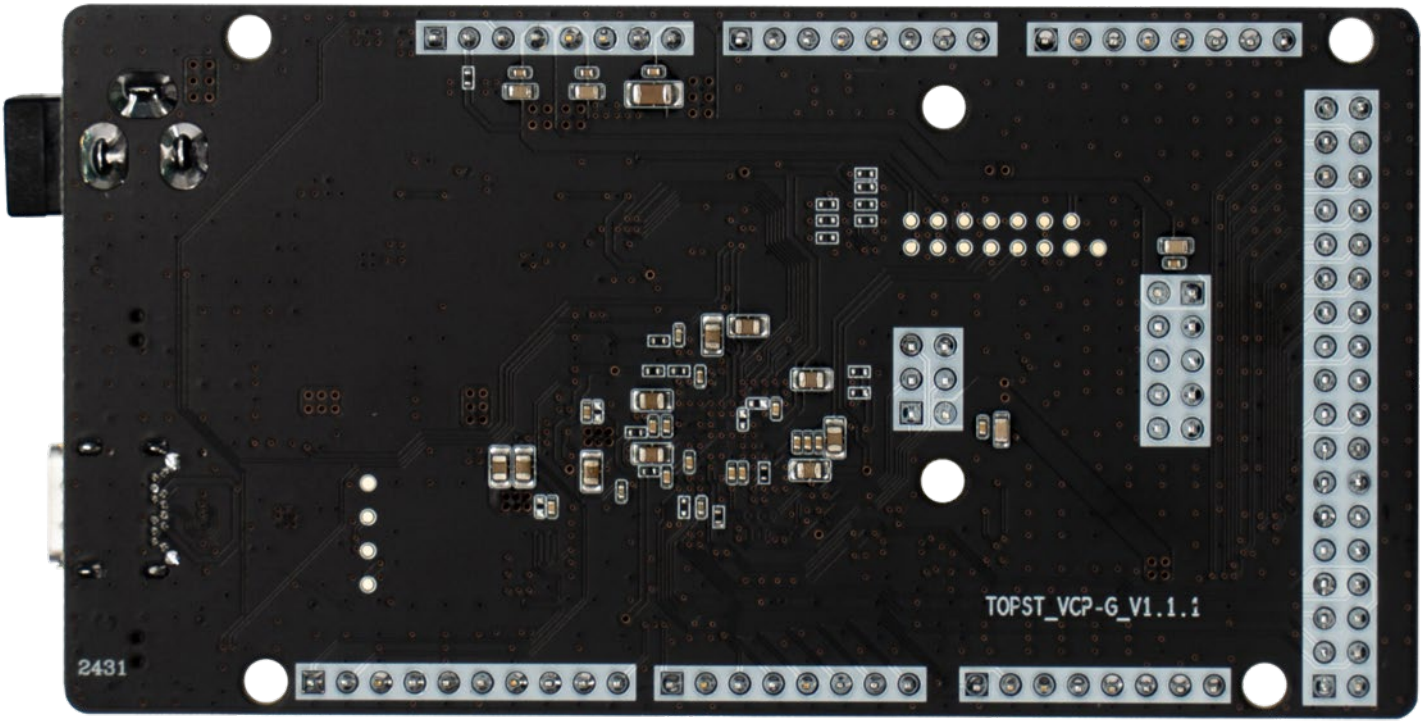


**Figure 3.2 VCP-G Board (Bottom View)**

# 4 SPECIFICATIONS

## 4.1 Serial NOR Flash Memory (U101)

SNOR (Quad SPI type) is located on the VCP-G board and the information is as follows:

- Quad I/O
- Density: 64 Mb

**Note:** Mounted SNOR is provided upon request.

## 4.2 Power Connector (J101)

J101 is a DC 12V external power supply connector with a 2.1 mm x 5.5 mm plug. It is used to power supply to the VCP-G board.

**Note:** The plug size must be compatible with 2.1 mm to 2.5 mm.

**Caution:** Compatibility problems may occur if you use an adapter other than the power adapter provided by TOPST.

Figure 4.1 shows the location of J101 on the VCP-G board.

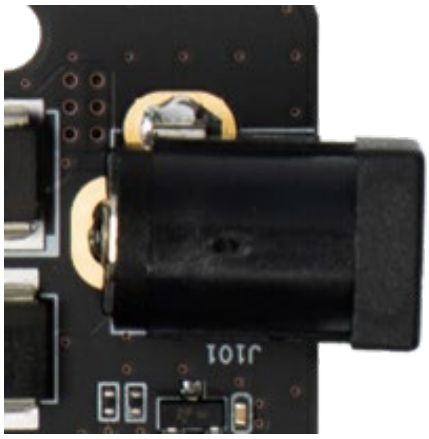


**Figure 4.1 Power Connector (J101)**

## 4.3 JTAG Connector (J100)

J100 is a standard 10-pin/1.27 mm connector for the JTAG emulator.

Figure 4.2 shows the location of J100 on the VCP-G board.

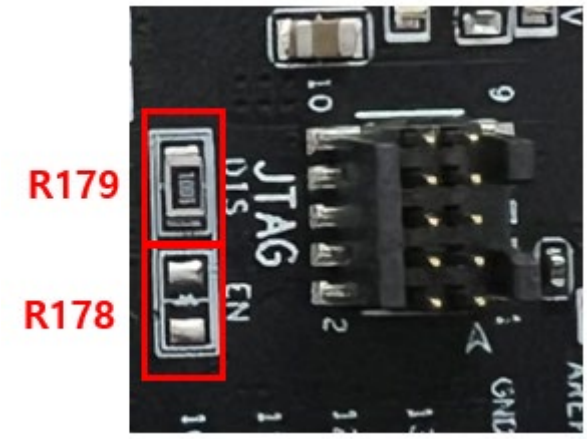


**Figure 4.2 JTAG Connector (J100)**

Table 4.1 describes the pins of J100.

**Table 4.1 J100 Pin Description**

| Pin Number | Schematic Net Name | DIR | Description |
|---|---|---|---|
| | | MCU ◄► J100 | |
| 1 | SW_VDD_3P3 | - | Power 3.3V |
| 2 | TMS | ◄ | Test Mode State |
| 3 | DGND | - | Ground |
| 4 | TCK | ◄ | Test Clock |
| 5 | DGND | - | Ground |
| 6 | TDO | ► | Test Data Output |
| 7 | NC | - | Not Connected |
| 8 | TDI | ◄ | Test Data In |
| 9 | DGND | - | Ground |
| 10 | JTAG_RESETn | ◄ | System Reset |

By default, JTAG is disabled. To enable JTAG, you must change the connections of R178 and R179. If TRSRn is set to high by R178, the MCU enters JTAG mode.

Table 4.2 describes the setting of JTAG Disable/Enable.

**Table 4.2 Setting of JTAG Disable/Enable**

| Mode | TRSTn Value | R178 | R179 |
|---|---|---|---|
| JTAG Disable (Default) | Low (1) | N.C | 1K |
| JTAG Enable (Option) | High (1) | 1K | N.C |

## 4.4 FWDN Switch (SW101)

The VCP-G has one pin for boot configuration using Boot Mode (BM) and supports 2 modes: UART FWDN mode and normal mode. Figure 4.3 shows the location of FWDN tact switch (SW101), which is used to select the boot modes of the VCP-G board.

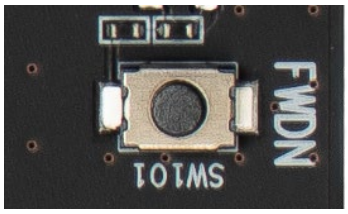


**Figure 4.3 FWDN Tact Switch (SW101)**

Table 4.3 describes the boot mode selection using the FWDN tact switch (SW101).

**Table 4.3 Description of Tact Switch (SW101) for Boot Mode**

| Mode | BM00 Value | SW101 Status |
|---|---|---|
| Normal (Default) | Low (1) | Default |
| FWDN (Optional) | High (1) | Push and supply power |

### 4.4.1 FWDN Mode Method

There are two methods to enter FWDN mode as follows.

#### 4.4.1.1 Method 1

While pressing the FWDN switch (SW101), connect the 12V power supply to turn on the VCP-G board.
The FWDN red indicator turns on when power is applied while the FWDN switch is pressed. After releasing the FWDN switch, the MCU enters FWDN mode.

Figure 4.4 shows how to enter FWDN mode by using method 1.

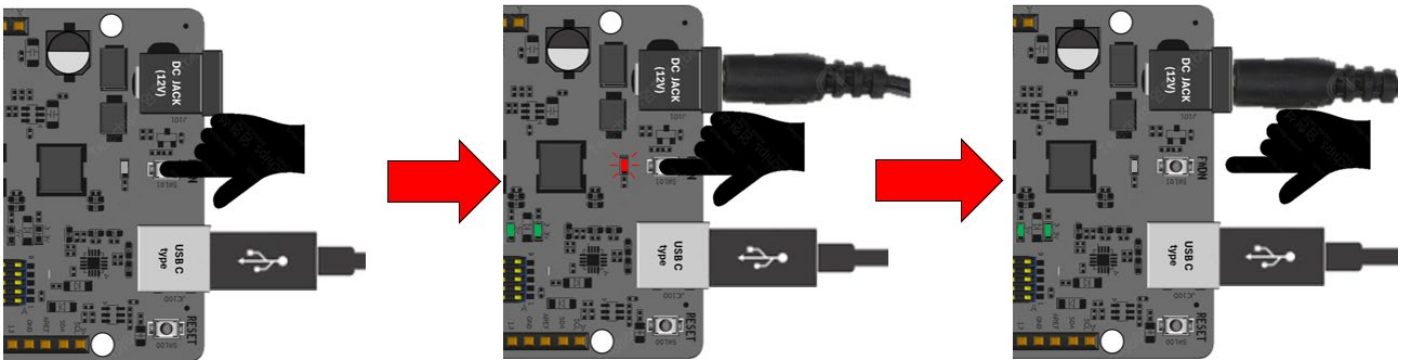


**Figure 4.4 Enter FWDN Mode by using Method 1**

#### 4.4.1.2 Method 2

While connecting the 12V power supply, press the FWDN switch (SW101) and then press the RESET switch (SW100).
The FWDN red indicator turns on when the power is applied while the FWDN switch is pressed. The 3.3V green indicator turns off while the RESET switch is pressed. After releasing the FWDN switch, the MCU enters FWDN mode.

Figure 4.5 shows the FWDN mode by using method 2.

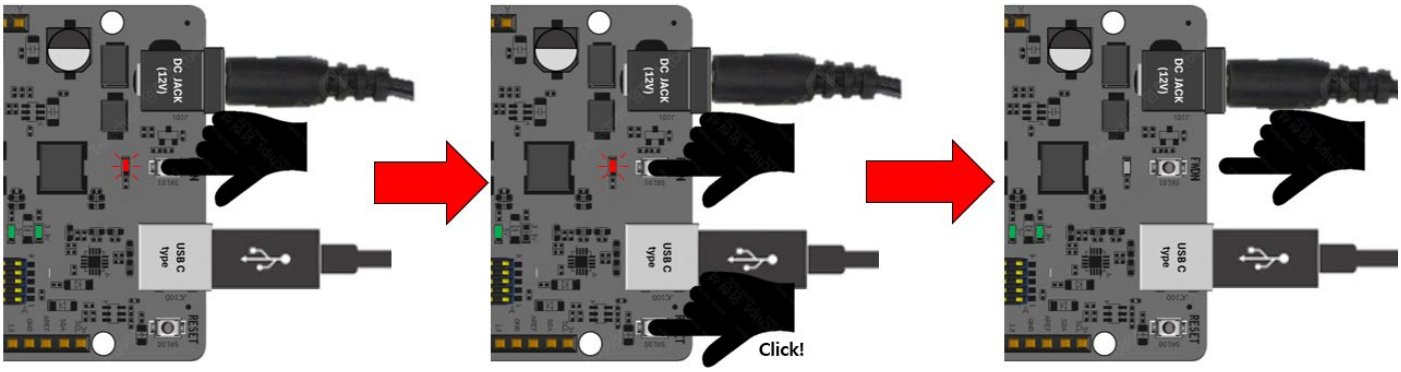


**Figure 4.5 Enter FWDN Mode by using Method 2**

## 4.5 RESET Switch (SW100)

The VCP-G has one RESET switch to perform reset by using the GRESETn pin.

Figure 4.6 shows the RESET switch (SW100) on the VCP-G board.

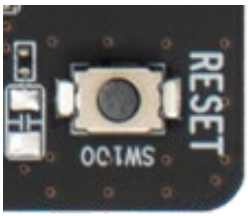


**Figure 4.6 RESET Switch (SW100)**

### 4.5.1 RESET Switch (SW100) Function

SW100 is a tact switch used to reset the power block and system block in TCC7045.
The function of this button is as follows:

- Pressing the tack switch (SW100) while the power is on forces the power block and the system of the VCP-G to reset.

**Important:** Be careful when pressing the tack switch as the power suddenly turns off and data may be corrupted.

## 4.6 Connector for Debugging and FWDN (JC100)

JC100 is a standard USB Type-C connector that is used for debugging or FWDN through UART.

Figure 4.7 shows the location of JC100 on the VCP-G board.

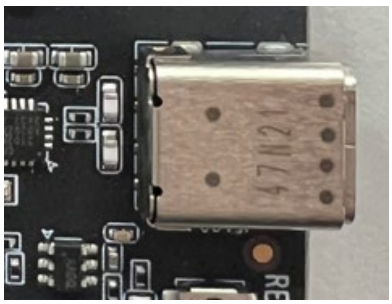

**Figure 4.7 USB Type-C Connector (JC100)**

You can perform FWDN or check debug messages of the VCP-G through JC100.
JC100 on the VCP-G board includes a built-in USB-to-UART bridge controller, so you can directly connect JC100 to PC by using the USB Type-C cable.

## 4.7 Pin Headers for GPIO, ADC, Power, CAN, SPI

The VCP-G board has nine 2.54 mm pin headers for GPIO, ADC, power, CAN, and SPI to connect to other peripherals such as sensor or sub-boards.

Table 4.4 describes the purpose of nine pin headers on the VCP-G board.

**Table 4.4 Pin Headers on VCP-G**

| Number | Reference Number | Name | Description |
|---|---|---|---|
| 1 | J18D100 | 36-pin Socket Header (Female) | Header for GPIO and ADC |
| 2 | J5D100 | 10-pin Header (Male) | Header for CAN |
| 3 | J3D100 | 6-pin Header (Male) | Header for SPI |
| 4 | J8D104 | 8-pin Socket Header (Female) | Header for GPIO and ADC |
| 5 | J8D102 | 8-pin Socket Header (Female) | Header for GPIO |
| 6 | J10D100 | 10-pin Socket Header (Female) | Header for GPIO and ADC |
| 7 | J8D100 | 8-pin Socket Header (Female) | Header for Power and Reset |
| 8 | J8D101 | 8-pin Socket Header (Female) | Header for GPIO and ADC |
| 9 | J8D103 | 8-pin Socket Header (Female) | Header for GPIO and ADC |

Figure 4.8 shows the location of the pin headers on the VCP-G board.

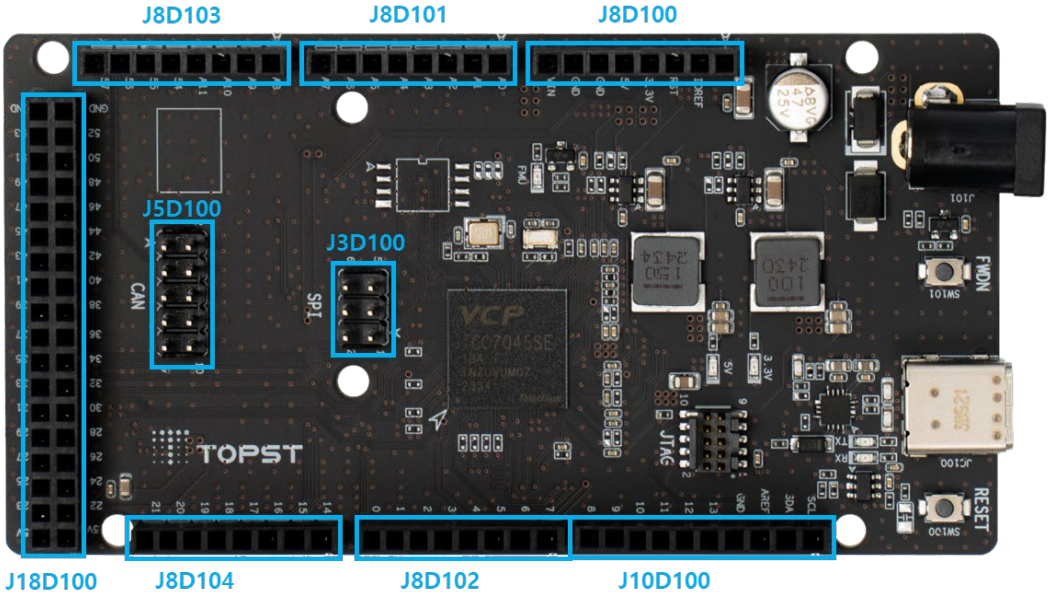


**Figure 4.8 Pin Headers on VCP-G Board**

Table 4.5 shows the pin description of J10D100.

**Table 4.5 J10D100 Pin Description**

| Pin Number | J10D100 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J10D100 | Description |
| 1 | SCL | GPIO_AC07 | ◄► | GPIO or ADC signal |
| 2 | SDA | GPIO_AC06 | ◄► | GPIO or ADC signal |
| 3 | AREF | ADC06 | ◄ | ADC signal |
| 4 | GND | DGND | - | Ground |
| 5 | 13 | GPIO_C12 | ◄► | GPIO signal |
| 6 | 12 | GPIO_C15 | ◄► | GPIO signal |
| 7 | 11 | GPIO_C14 | ◄► | GPIO signal |
| 8 | 10 | GPIO_C13 | ◄► | GPIO signal |
| 9 | 9 | GPIO_A12 | ◄► | GPIO signal |
| 10 | 8 | GPIO_B00 | ◄► | GPIO signal |

Table 4.6 shows the pin description of J8D100.

**Table 4.6 J8D100 Pin Description**

| Pin Number | J8D100 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J8D100 | Description |
| 1 | - | - | - | NC |
| 2 | IOREF | VCP_3P3 | - | Power 3.3V |
| 3 | RST | RESET | ◄ | Reset signal |
| 4 | 3.3V | VCP_3P3 | - | Power 3.3V |
| 5 | 5V | VCP_5P0 | - | Power 5.0V |
| 6 | GND | DGND | - | Ground |
| 7 | GND | DGND | - | Ground |
| 8 | VIN | VIN | - | Voltage input for VCP-G |

Table 4.7 shows the pin description of J8D101.

**Table 4.7 J8D101 Pin Description**

| Pin Number | J8D101 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J8D101 | Description |
| 1 | A0 | ADC03 | ◄ | ADC signal |
| 2 | A1 | ADC04 | ◄ | ADC signal |
| 3 | A2 | GPIO_AC02 | ◄► | GPIO signal |
| 4 | A3 | GPIO_AC03 | ◄► | GPIO signal |
| 5 | A4 | GPIO_AC05 | ◄► | GPIO signal |
| 6 | A5 | GPIO_AC04 | ◄► | GPIO signal |
| 7 | A6 | ADC05 | ◄ | ADC signal |
| 8 | A7 | ADC01 | ◄ | ADC signal |

Table 4.8 shows the pin description of J8D102.

**Table 4.8 J8D102 Pin Description**

| Pin Number | J8D102 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J8D102 | Description |
| 1 | 7 | GPIO_B01 | ◄► | GPIO signal |
| 2 | 6 | GPIO_A13 | ◄► | GPIO signal |
| 3 | 5 | GPIO_B10 | ◄► | GPIO signal |
| 4 | 4 | GPIO_B27 | ◄► | GPIO signal |
| 5 | 3 | GPIO_B11 | ◄► | GPIO signal |
| 6 | 2 | GPIO_B28 | ◄► | GPIO signal |
| 7 | 1 | GPIO_B25 | ◄► | GPIO signal |
| 8 | 0 | GPIO_B26 | ◄► | GPIO signal |

Table 4.9 shows the pin description of J8D103.

**Table 4.9 J8D103 Pin Description**

| Pin Number | J8D103 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J8D103 | Description |
| 1 | A8 | GPIO_AC08 | ◄► | GPIO or ADC signal |
| 2 | A9 | GPIO_AC09 | ◄► | GPIO or ADC signal |
| 3 | A10 | GPIO_AC10 | ◄► | GPIO or ADC signal |
| 4 | A11 | ADC02 | ◄ | ADC signal |
| 5 | 54 | GPIO_K14 | ◄► | GPIO signal |
| 6 | 55 | GPIO_K15 | ◄► | GPIO signal |
| 7 | 56 | GPIO_K01 | ◄ | GPIO signal |
| 8 | 57 | GPIO_K08 | ◄► | GPIO signal |

Table 4.10 shows the pin description of J8D104.

**Table 4.10 J8D104 Pin Description**

| Pin Number | J8D104 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J8D104 | Description |
| 1 | 14 | GPIO_AC00 | ◄► | GPIO or ADC signal |
| 2 | 15 | GPIO_AC01 | ◄► | GPIO or ADC signal |
| 3 | 16 | GPIO_A06 | ◄► | GPIO signal |
| 4 | 17 | GPIO_A07 | ◄► | GPIO signal |
| 5 | 18 | GPIO_A28 | ◄► | GPIO signal |
| 6 | 19 | GPIO_A29 | ◄► | GPIO signal |
| 7 | 20 | GPIO_B03 | ◄► | GPIO signal |
| 8 | 21 | GPIO_B02 | ◄► | GPIO signal |

Table 4.11 shows the pin description of J3D100.

**Table 4.11 J3D100 Pin Description**

| Pin Number | J3D100 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J3D100 | Description |
| 1 | MISO | GPIO_B07 | ◄► | GPIO signal |
| 2 | 5V | VCP_5P0 | - | Power 5.0V |
| 3 | SCK | GPIO_B04 | ◄► | GPIO signal |
| 4 | MOSI | GPIO_B06 | ◄► | GPIO signal |
| 5 | CMD | GPIO_B05 | ◄► | GPIO signal |
| 6 | GND | DGND | - | Ground |

Table 4.12 shows the pin description of J18D100.

**Table 4.12 J18D100 Pin Description**

| Pin Number | J18D100 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J18D100 | Description |
| 1 | 5V | VCP_5P0 | - | Power 5.0V |
| 2 | 5V | VCP_5P0 | - | Power 5.0V |
| 3 | 22 | GPIO_B24 | ◄► | GPIO signal |
| 4 | 23 | GPIO_B23 | ◄► | GPIO signal |
| 5 | 24 | GPIO_B22 | ◄► | GPIO signal |
| 6 | 25 | GPIO_B21 | ◄► | GPIO signal |
| 7 | 26 | GPIO_B20 | ◄► | GPIO signal |
| 8 | 27 | GPIO_B19 | ◄► | GPIO signal |
| 9 | 28 | GPIO_A30 | ◄► | GPIO signal |
| 10 | 29 | GPIO_A27 | ◄► | GPIO signal |
| 11 | 30 | GPIO_A26 | ◄► | GPIO signal |
| 12 | 31 | GPIO_A24 | ◄► | GPIO signal |
| 13 | 32 | GPIO_A25 | ◄► | GPIO signal |
| 14 | 33 | GPIO_A23 | ◄► | GPIO signal |
| 15 | 34 | GPIO_A22 | ◄► | GPIO signal |
| 16 | 35 | GPIO_A21 | ◄► | GPIO signal |
| 17 | 36 | GPIO_A20 | ◄► | GPIO signal |
| 18 | 37 | GPIO_A19 | ◄► | GPIO signal |
| 19 | 38 | GPIO_K13 | ◄► | GPIO signal |
| 20 | 39 | GPIO_K12 | ◄► | GPIO signal |
| 21 | 40 | GPIO_K11 | ◄► | GPIO signal |
| 22 | 41 | GPIO_A18 | ◄► | GPIO signal |
| 23 | 42 | GPIO_A17 | ◄► | GPIO signal |
| 24 | 43 | GPIO_A16 | ◄► | GPIO signal |
| 25 | 44 | GPIO_A11 | ◄► | GPIO signal |
| 26 | 45 | GPIO_A10 | ◄► | GPIO signal |
| 27 | 46 | GPIO_A09 | ◄► | GPIO signal |
| 28 | 47 | GPIO_A08 | ◄► | GPIO signal |
| 29 | 48 | GPIO_A05 | ◄► | GPIO signal |
| 30 | 49 | GPIO_A04 | ◄► | GPIO signal |
| 31 | 50 | GPIO_A03 | ◄► | GPIO signal |
| 32 | 51 | GPIO_A02 | ◄► | GPIO signal |
| 33 | 52 | GPIO_A01 | ◄► | GPIO signal |
| 34 | 53 | GPIO_A00 | ◄► | GPIO signal |
| 35 | GND | DGND | - | Ground |
| 36 | GND | DGND | - | Ground |

Table 4.13 shows the pin description of J5D100.

**Table 4.13 J5D100 Pin Description**

| Pin Number | J5D100 | | | |
|---|---|---|---|---|
| | Port Name | Signal Name | DIR<br>MCU ◄► J5D100 | Description |
| 1 | 3.3V | VCP_3P3 | - | Power 3.3V |
| 2 | 3.3V | VCP_3P3 | - | Power 3.3V |
| 3 | TX0 | GPIO_K08 | ◄► | GPIO signal |
| 4 | RX0 | GPIO_K01 | ◄ | GPIO signal |
| 5 | TX1 | GPIO_K09 | ◄► | GPIO signal |
| 6 | RX1 | GPIO_K02 | ◄ | GPIO signal |
| 7 | TX2 | GPIO_K10 | ◄► | GPIO signal |
| 8 | RX2 | GPIO_K03 | ◄ | GPIO signal |
| 9 | GND | DGND | - | DGND |
| 10 | GND | DGND | - | DGND |

Figure 4.9 shows the total pin assignment of ten pin headers on the VCP-G board.

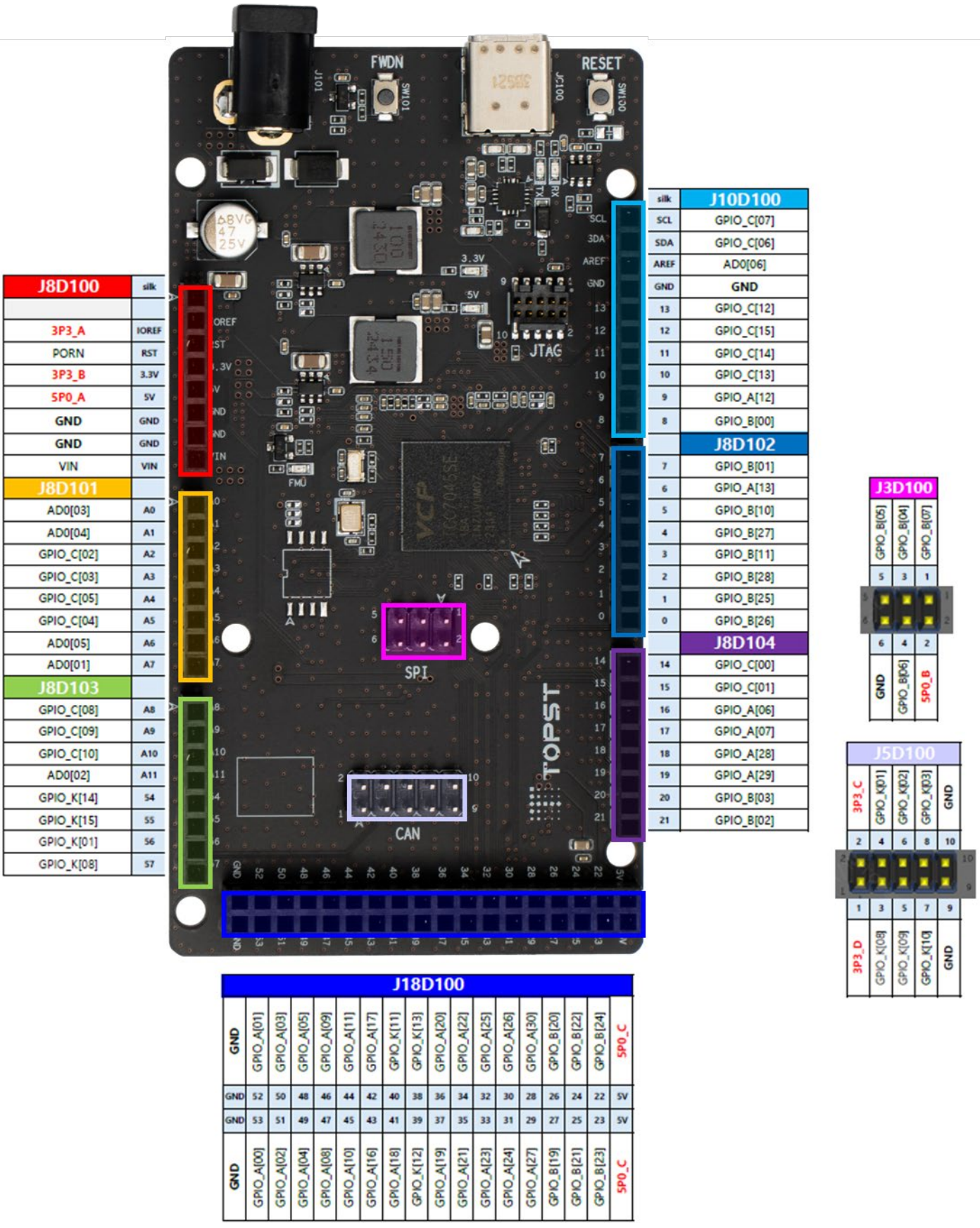


**Figure 4.9 Total Pin Assignment of Pin Headers on VCP-G Board**

# 5 REFERENCES

[1] Contact TOPST for more details: topst@topst.ai

**Note:** Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

# 6 REVISION HISTORY

## Rev. 1.01: 2025-07-18

- Updated
  - Chapter 1: Description
  - Chapter 2.1: Figure 2.1
  - Chapter 3:
    - Changed chapter title from "TOPST VCP-G Overview" to "Overview"
    - Description
    - Table 3.1
  - Chapter 4.1:
    - Changed chapter title from "Quad SPI Flash Memory (U101)" to "Serial NOR Flash Memory (U101)"
    - Description
  - Chapter 4.2: Description
  - Chapter 4.3:
    - Changed chapter title from "Connector for JTAG (J100)" to "JTAG Connector (J100)"
    - Description
  - Chapter 4.5.1: Changed chapter title from "RESET Tact Switch (SW100) Function" to "RESET Switch (SW100) Function"
  - Chapter 4.7:
    - Figure 4.9
    - Table 4.6

- Added
  - Chapter 2.2: Features of VCP-G Board

## Rev. 1.00: 2025-02-28

- Official version release

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