TOPST D3-G Hardware

User Guide

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1 INTRODUCTION

This document is a hardware user guide for the D3-G based on the TCC8050. This document describes system installation, debugging, and detailed information on the overall design and usage of the D3-G.

1.1 Terminology

Terminology	Definition
CPU	Central Processing Unit
D3	Dolphin3
FWDN	Firmware Download
GPIO	General Purpose Input Output
GPU	Graphic Processing Unit
HAT	Hardware Attached on Top
MCU	Micro-Controller Unit
TOPST	Total Open-Platform for System development and Training

2 BLOCK DIAGRAM

2.1 System Block Diagram

Figure 2.1 shows the system block diagram of the D3-G.

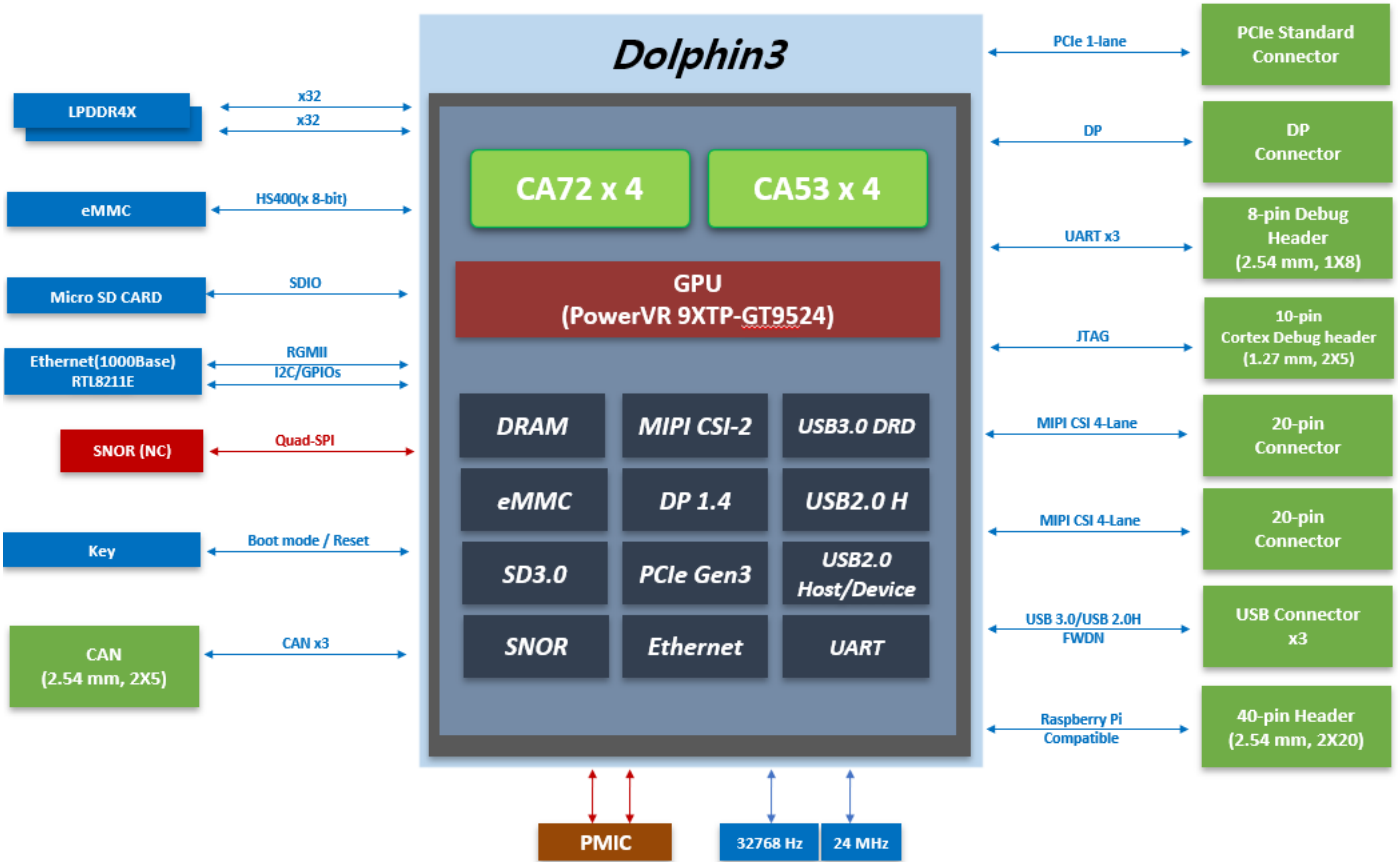

Figure 2.1 System Block Diagram

2.2 Features of D3-G Board

Table 2.1 describes the features of the D3-G board.

Table 2.1 Features of D3-G Board

Function		Description	Note
Application Processor	TCC8050	**TCC8050** Main core: Cortex-A72 Quad Sub-core: Cortex-A53 Quad	
MCU	Built-in TCC8050	Cortex-R5: 600 MHz @ 0.8V	
GPU	Built-in TCC8050	PowerVR 9XTP-GT9524	
Memory	eMMC	eMMC 5.1 Speed: HS400 Density: 32 GB/64 GB	
	LPDDR4X	32-bit x 2 Ch Density: 4 GB/8 GB Maximum Clock: 2133 MHz	
	Serial NOR Flash	Quad I/O Density: 256 Mb	Default: NC
	SD Card	SD Card socket	
Video Out	DP	DP 1.4, 4-lane (8.1 Gbps/lane) Up to 4 displays – Daisy Chain	
Video In	MIPI CSI	2-channel MIPI CSI-2 2-lane	Option: 2-channel MIPI CSI-2 4-lane
Peripheral	USB	USB 3.0 Host – USB Type-A USB 2.0 Host – USB Type-A FWDN – USB Type-C	
	PCIe	1 Ch x PCIe 3.0 (1-lane)	
	CAN	3 channels	Require SNOR to support CAN
	Ethernet	Ethernet PHY 1000Base-T/Legacy	
X-TAL	Main	24 MHz	
	Sub	32768 Hz	
Pin Header (Male)	General Function Interface	Standard 40-pin/2.54 mm Pin Header (Male) ■ Raspberry Pi Compatibility	
	CAN	Standard 10-pin/2.54 mm Pin Header (Male)	
	UART	Standard 8-pin/2.54 mm Pin Header (Male) ■ Debug A72, A53, MC	
Connector	USB3.0 Host	Type-A 9-pin	
	USB2.0 Host	Type-A 4-pin	
	USB2.0 FWDN	Type-C 12-pin	
	DP	DP Connector	
	SD Card	Micro SD Card Slot	
	MIPI CSI	1 mm pitch 15-pin	Option: 20-pin for 4-lane
	Peripheral Component Interconnect Express (PCIe)	PCI Express Standard	
	Ethernet	RJ45	
	JTAG	Standard 10-pin/1.27 mm	
Jack	DC Jack	For power input (5V)	
Switch	Boot mode	System Boot mode switch	
	Reset	System RESET switch	

Note: For inquiries about the D3-G, contact TOPST. [1]

3 OVERVIEW

3.1 D3-G Board

Figure 3.1 shows the top view of the D3-G board.

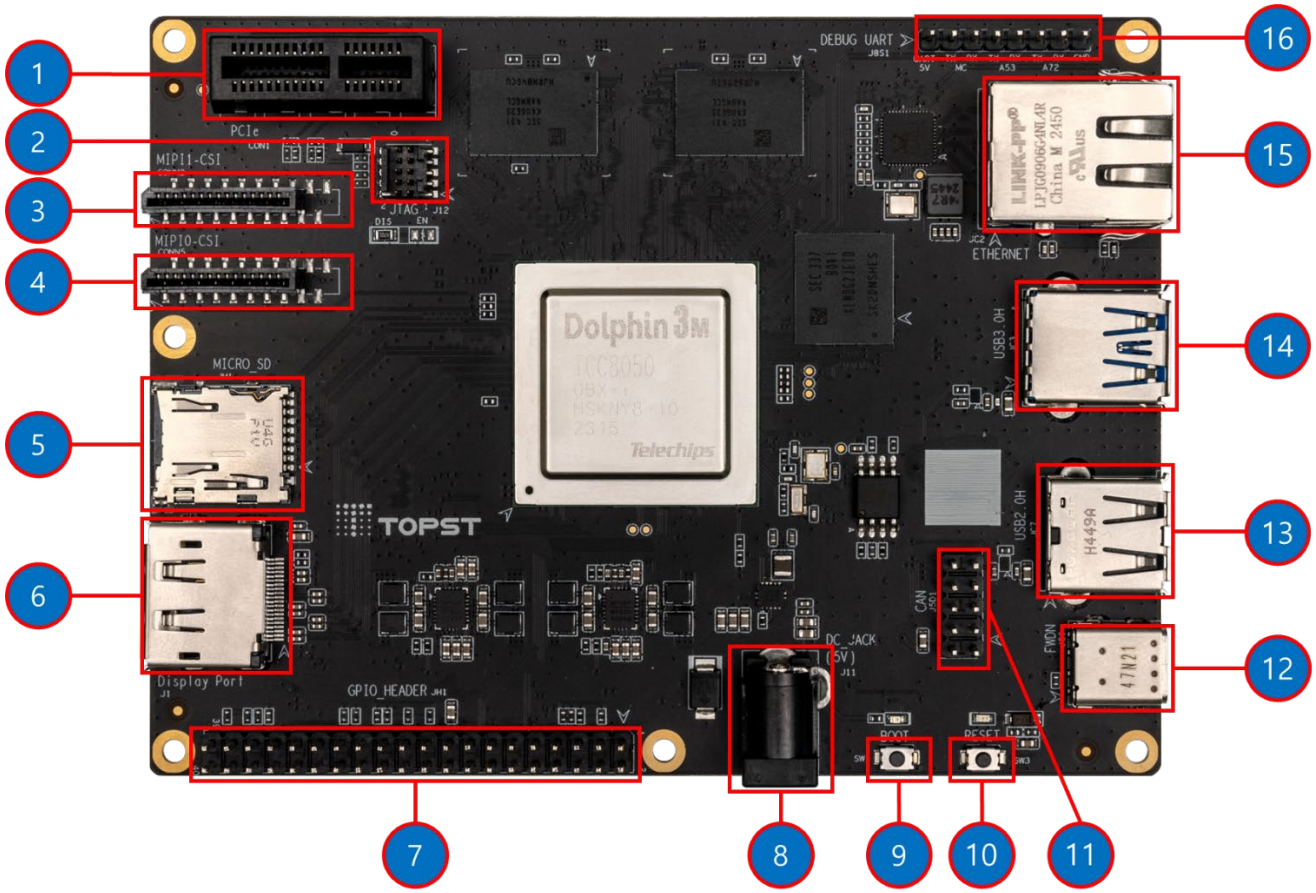

Figure 3.1 D3-G Board (Top View)

Table 3.1 describes the connectors of the D3-G board (top view).

Table 3.1 Description of D3-G Board (Top View)

Number	Reference Number	Name	Description
1	CON1	PCIe Standard Connector	Connect to the PCIe Device
2	J12	JTAG Connector	JTAG connector for system debugging
3	CONN2	MIPI CSI Connector	Connect to the Camera module
4	CONN5	MIPI CSI Connector	Connect to the Camera module
5	JM1	Micro SD Socket	SD memory card socket
6	J1	DP Connector	Connect to the DP interface module
7	JH1	GPIO Header Male	General Function Interface Header
8	J11	Power Jack	5V Power Jack
9	SW1	Boot Mode Switch	Switch for changing boot mode
10	SW3	RESET Switch	Switch for system reset
11	J5D1	10-pin Header (Male)	CAN Header
12	JC6	USB Type-C Connector	USB2.0 FWDN connector
13	JC7	USB Type-A Connector	USB2.0 High speed Host connector
14	JC3	USB Type-A Connector	USB3.0 Super speed connector
15	JC2	RJ45 Connector	Legacy Ethernet port
16	J8S1	8-pin Header (Male)	UART debug Header

4 SPECIFICATIONS

4.1 LPDDR4X

The LPDDR4X memory is located on the D3-G board and the information is as follows:

- 32-bit x 2-channel
- Density: 4 GB/8 GB
- Maximum Clock: 2133 MHz

4.2 eMMC

The eMMC memory is located on the D3-G board and the information is as follows:

- eMMC 5.1
- Density: 32 GB or 64 GB
- Supports up to HS400

4.3 Serial NOR Flash Memory

SNOR (Quad SPI type) is located on the D3-G board and the information is as follows:

- Quad I/O
- Density: 256 Mb

4.4 Power Connector (J11)

J11 is a DC 5V external power supply connector with a 2.5 mm x 5.5 mm plug. It is used to supply power to the D3-G board. The power supply current should be at least 5A.

Figure 4.1 shows the power plug size for DC 5V power supply.

Figure 4.1 Plug Size for DC 5V Power Supply

Note: The plug size must be compatible with 2.1 mm to 2.5 mm.

Caution: Compatibility problems may occur if you use an adapter other than the power adapter provided by TOPST.

Figure 4.2 Power Connector (J11)

4.5 JTAG Connector (J12)

J12 is a standard 10-pin/1.27 mm connector for the JTAG emulator.

Figure 4.3 shows the location of J12 on the D3-G board.

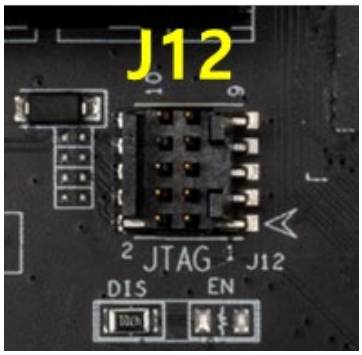

Figure 4.3 JTAG Connector (J12)

Table 4.1 describes the pins of J12.

Table 4.1 J12 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J12	
1	SYS_3P3	-	Power 3.3V
2	TMS	◄	Test Mode State
3	DGND	-	Ground
4	TCK	◄	Test Clock
5	DGND	-	Ground
6	TDO	►	Test Data Output
7	NC	-	Not Connected
8	TDI	◄	Test Data In
9	DGND	-	Ground
10	RESET#	◄	System Reset

4.6 Boot Mode

The D3-G board supports three boot modes:

- USB Boot Mode (FWDN)
- eMMC Boot Mode (GPIO_SD0 Group)
- SNOR and eMMC Boot Mode (Optional)

The resistors are located on the bottom of the board. The D3-G board is set to eMMC Boot Mode by default. If there is no boot image in the eMMC device, the Boot Mode is automatically switched to USB Boot Mode.

Figure 4.4 shows the location of Boot Mode resistors on the D3-G board.

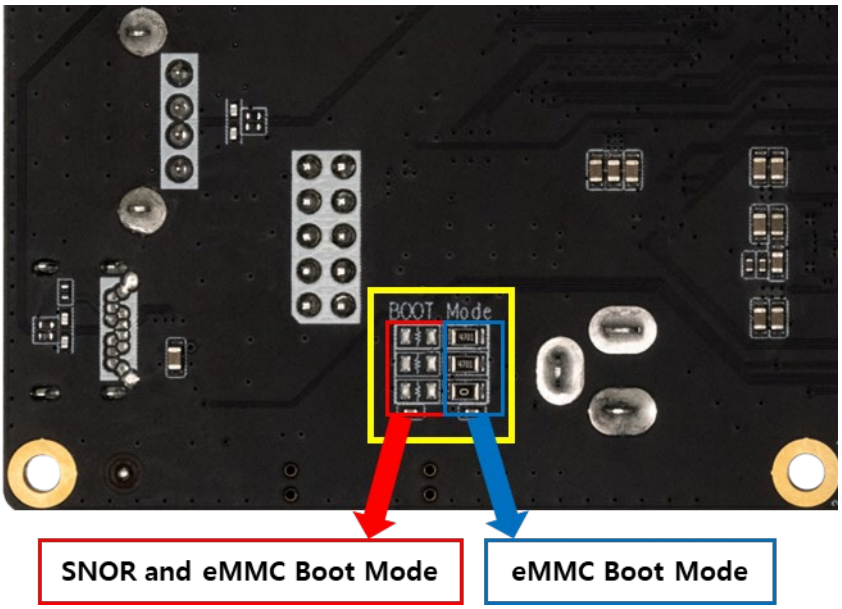

Figure 4.4 Boot Mode-related Resistors

4.6.1 USB Boot Mode (FWDN)

Figure 4.5 shows the Boot Mode switch and RESET switch. USB Boot Mode is used for firmware updates. To enter USB boot mode, both the Boot mode switch and RESET switch are required. It is recommended to use this method when uploading the image.

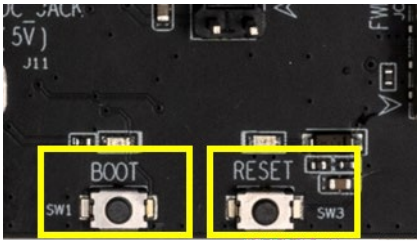

Figure 4.5 Boot Mode Switch and RESET Switch for Entering USB Boot Mode

The following steps describe the switch operation for entering USB Boot Mode.

1. When power is supplied, the LED above the RESET switch turns on.
2. Press and hold the Boot Mode switch. When you press the Boot Mode switch, you can see the red LED above the Boot Mode switch turn on. Keep pressing the switch to keep the LED on.
3. The RESET switch LED is green by default. If you press the RESET switch once, the green LED turns off and then turns on again.
4. Release the Boot Mode switch.

Figure 4.6 shows the operation sequence of the Boot Mode and RESET switches for entering USB Boot Mode (FWDN).

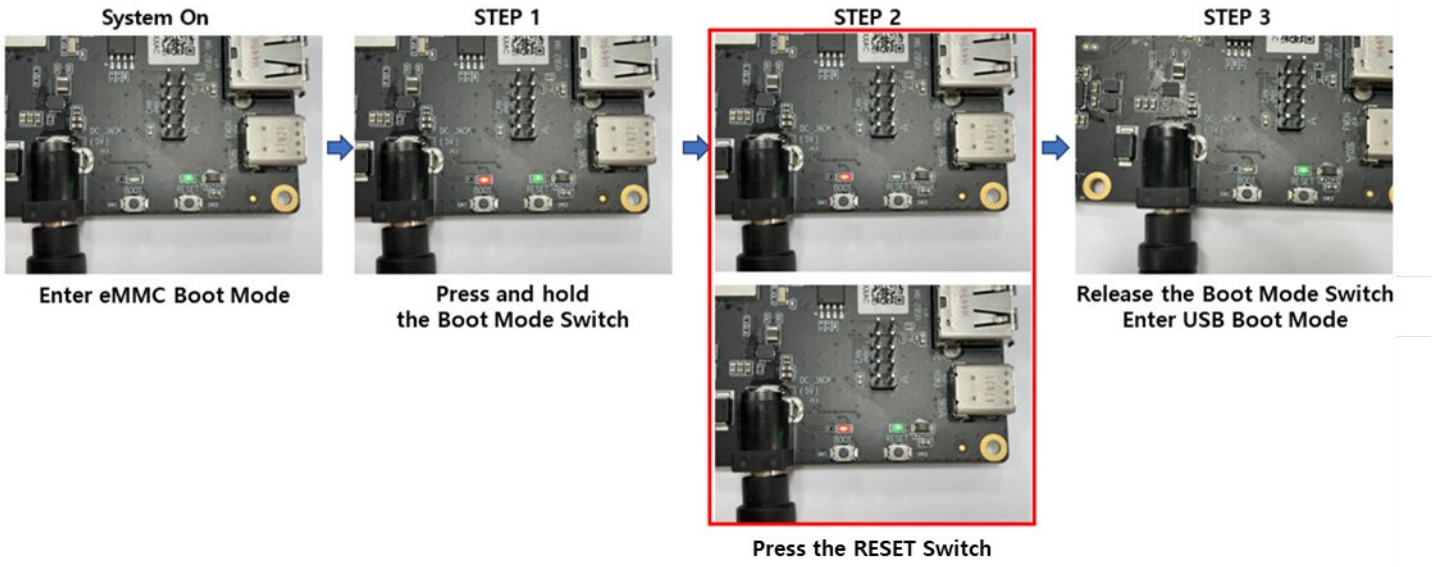

Figure 4.6 Sequence of Entering USB Boot Mode (FWDN)

4.6.2 SNOR and eMMC Boot Mode

SNOR and eMMC Boot Mode are optional. To use this boot mode, the SNOR IC must be mounted on the board, and the surface mount technology (SMT) of boot mode resistors must be changed.

Figure 4.7 shows the required changes for using SNOR and eMMC Boot Mode.

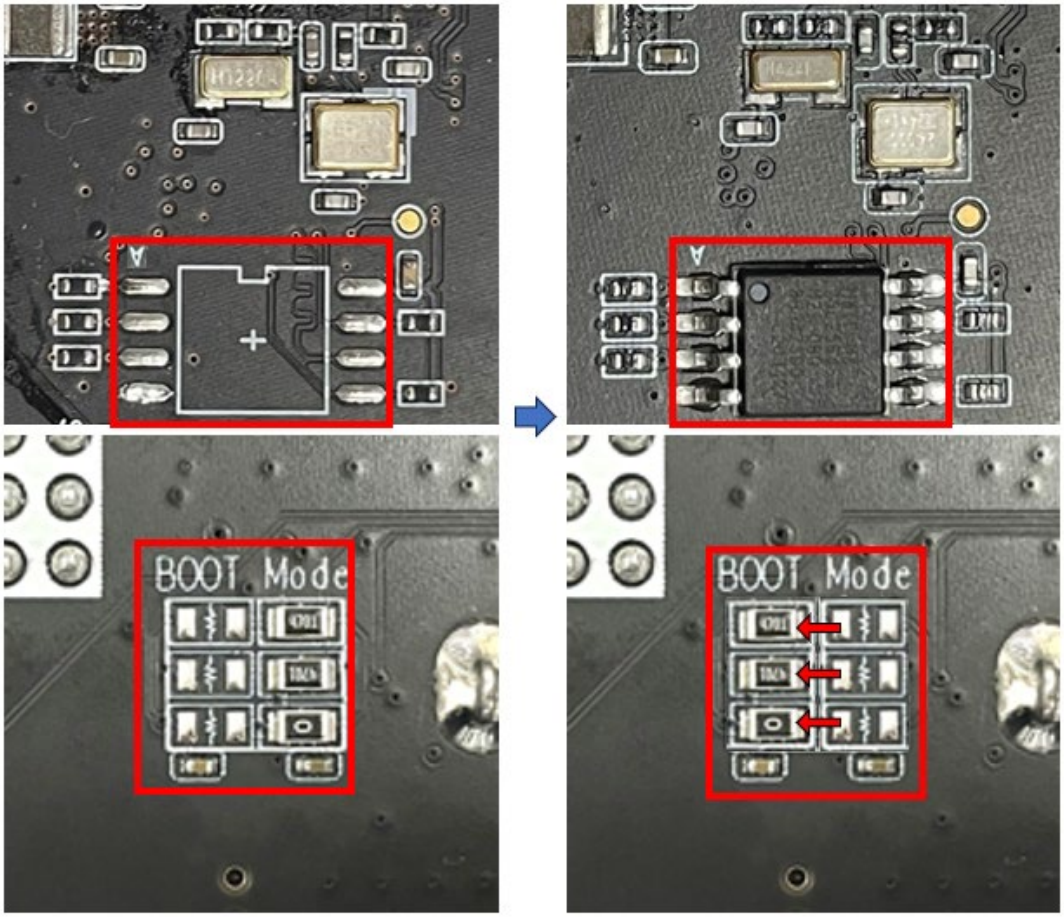

Figure 4.7 Required Changes for Using SNOR and eMMC Boot Mode

4.7 PCIe Connector (CON1)

Figure 4.8 shows the PCIe connector that enables the use of PCIe interface devices on the D3-G board. The D3-G supports PCIe-gen3 x 1-lane.

- PCIe Controller: Supports Gen3, 1-lane operation

Figure 4.8 PCIe Standard Connector (CON1)

Table 4.2 describes the pins of CON1.

Table 4.2 CON1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► CON1	
A1	PCIe_DET#	◄	PCIe Card Detection
B1	12V_TP	-	Power 12V Test Point
A2	12V_TP	-	Power 12V Test Point
B2	12V_TP	-	Power 12V Test Point
A3	12V_TP	-	Power 12V Test Point
B3	12V_TP	-	Power 12V Test Point
A4	DGND	-	Ground
B4	DGND	-	Ground
A5	NC	-	Not Connected
B5	NC	-	Not Connected
A6	NC	-	Not Connected
B6	NC	-	Not Connected
A7	NC	-	Not Connected
B7	DGND	-	Ground
A8	NC	-	Not Connected
B8	PCIe_3P3	-	Power 3.3V
A9	PCIe_3P3	-	Power 3.3V
B9	NC	-	Not Connected
A10	PCIe_3P3	-	Power 3.3V
B10	PCIe_3P3	-	Power 3.3V
A11	PCIe_RST#	►	PCIe Reset
B11	PCIe_WAKE#	◄	PCIe Wake
A12	DGND	-	Ground
B12	PCIe_CLKREQ#	◄	PCIe Clock Request
A13	PCIe_REFCLKOUT_P	►	PCIe Positive Clock
B13	DGND	-	Ground
A14	PCIe_REFCLKOUT_N	►	PCIe Negative Clock
B14	PCIe_TXP	►	PCIe Transmit Positive Data
A15	DGND	-	Ground
B15	PCIe_TXN	►	PCIe Transmit Negative Data
A16	PCIe_RXP	◄	PCIe Receive Positive Data
B16	DGND	-	Ground
A17	PCIe_RXN	◄	PCIe Receive Negative Data
B17	PCIe_DET#	◄	PCIe Card Detection
A18	DGND	-	Ground
B18	DGND	-	Ground

4.8 MIPI CSI Connector (CONN2 and CONN5)

Figure 4.9 shows the MIPI CSI connectors on the D3-G board. The D3-G supports 2 channels of MIPI CSI, each configured with a 2-lane interface. A 4-lane interface is optional and requires a 20-pin connector instead of a 15-pin connector.

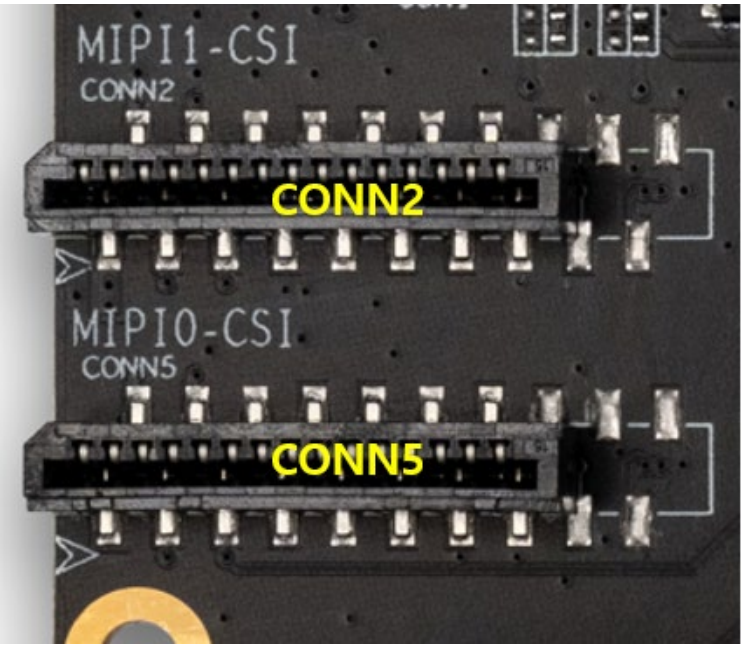

Figure 4.9 MIPI CSI Connectors (CONN2 and CONN5)

Table 4.3 describes the pins of CONN5.

Table 4.3 CONN5 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► CONN5	
1	RPI_CAM_3P3	-	Power 3.3V
2	MIPI0_SDA	◄►	MIPI0_I2C Data
3	MIPI0_SCL	►	MIPI0_I2C Clock
4	MIPI0_GPIO1	◄	General Purpose I/O
5	MIPI0_PD	►	General Purpose I/O
6	GND	-	Ground
7	MIPI0_S_CLKP	◄	MIPI0 CSI-2 Positive Clock
8	MIPI0_S_CLKN	◄	MIPI0 CSI-2 Negative Clock
9	GND	-	Ground
10	MIPI0_S_D1P	◄	MIPI0 CSI-2 Positive Data 1
11	MIPI0_S_D1N	◄	MIPI0 CSI-2 Negative Data 1
12	GND	-	Ground
13	MIPI0_S_D0P	◄	MIPI0 CSI-2 Positive Data 0
14	MIPI0_S_D0N	◄	MIPI0 CSI-2 Negative Data 0
15	GND	-	Ground
16	MIPI0_S_D3P	◄	MIPI0 CSI-2 Positive Data 3
17	MIPI0_S_D3N	◄	MIPI0 CSI-2 Negative Data 3
18	GND	-	Ground
19	MIPI0_S_D2P	◄	MIPI0 CSI-2 Positive Data 2
20	MIPI0_S_D2N	◄	MIPI0 CSI-2 Negative Data 2

Table 4.4 describes the pins of CONN2.

Table 4.4 CONN2 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► CONN2	
1	RPI_CAM_3P3	-	Power 3.3V
2	MIPI1_SDA	◄►	MIPI1_I2C Data
3	MIPI1_SCL	►	MIPI1_I2C Clock
4	MIPI1_GPIO1	◄	General Purpose I/O
5	MIPI1_PD	►	General Purpose I/O
6	GND	-	Ground
7	MIPI1_S_CLKP	◄	MIPI1 CSI2 Positive Clock
8	MIPI1_S_CLKN	◄	MIPI1 CSI2 Negative Clock
9	GND	-	Ground
10	MIPI1_S_D1P	◄	MIPI1 CSI2 Positive Data 1
11	MIPI1_S_D1N	◄	MIPI1 CSI2 Negative Data 1
12	GND	-	Ground
13	MIPI1_S_D0P	◄	MIPI1 CSI2 Positive Data 0
14	MIPI1_S_D0N	◄	MIPI1 CSI2 Negative Data 0
15	GND	-	Ground
16	MIPI1_S_D3P	◄	MIPI1 CSI2 Positive Data 3
17	MIPI1_S_D3N	◄	MIPI1 CSI2 Negative Data 3
18	GND	-	Ground
19	MIPI1_S_D2P	◄	MIPI1 CSI2 Positive Data 2
20	MIPI1_S_D2N	◄	MIPI1 CSI2 Negative Data 2

4.9 Micro SD Card Socket (JM1)

Figure 4.10 shows the micro SD socket. The D3-G supports SD3.0.

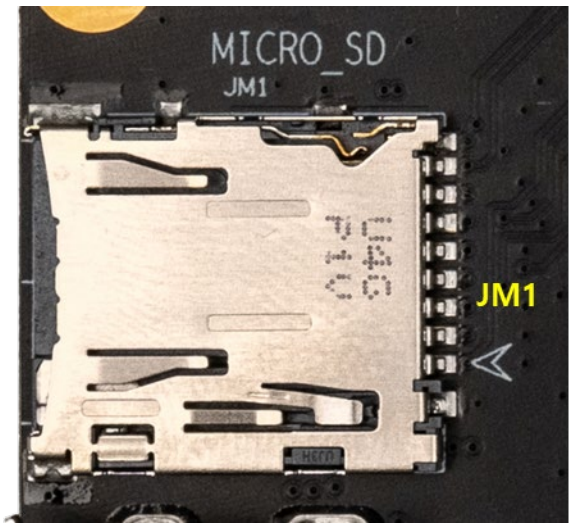

Figure 4.10 Micro SD Socket (JM1)

4.10 DP Connector (J1)

Figure 4.11 shows the DP connector on the D3-G board.

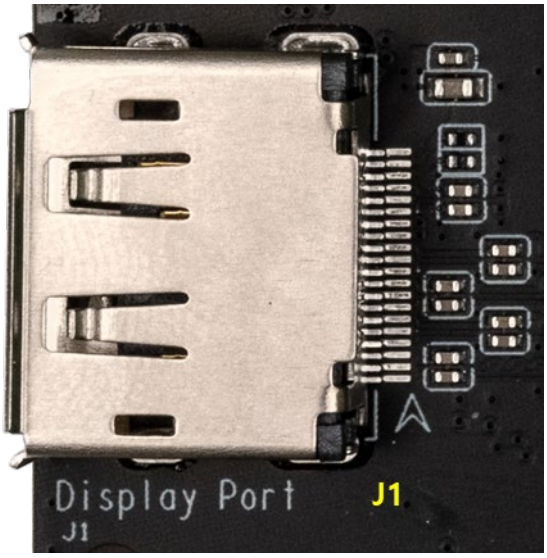

Figure 4.11 DP Connector (J1)

Table 4.5 describes the pins of J1.

Table 4.5 J1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J1	
1	DP_PHY_TX0_P	►	DP output data 0+
2	DGND	-	Ground
3	DP_PHY_TX0_M	►	DP output data 0-
4	DP_PHY_TXRX1_P	►	DP output data 1+
5	DGND	-	Ground
6	DP_PHY_TXRX1_M	►	DP output data 1-
7	DP_PHY_TXRX2_P	►	DP output data 2+
8	DGND	-	Ground
9	DP_PHY_TXRX2_M	►	DP output data 2-
10	DP_PHY_TX3_P	►	DP output data 3+
11	DGND	-	Ground
12	DP_PHY_TX3_M	►	DP output data 3-
13	DP_CFG1	-	Not Connected
14	DP_CFG2	-	Not Connected
15	DP_AUX_P	◄►	DP AUX+
16	DGND	-	Ground
17	DP_AUX_N	◄►	DP AUX-
18	DP_HPD_CON	◄	Hot Plug Detection for DP
19	PDGND	-	Ground
20	DP_CON_3P3	-	DP Power 3.3V
21	DGND	-	Ground
22	DGND	-	Ground
23	DGND	-	Ground
24	DGND	-	Ground

4.11 Debug UART Pin Header (Male) (J8S1)

Figure 4.12 shows the debug UART header pin for system debugging. It consists of 3 UART channels for debugging each CPU core. Pin 1 (UART 5V) is a dummy pin and does not provide an output.

Figure 4.12 Debug UART Pin Header (Male) (J8S1)

Table 4.6 describes the pins of J8S1.

Table 4.6 J8S1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J8S1	
1	UART_5P0	-	Dummy Pin
2	MC_DBG_UT_TXD	►	UART Transmit Data of MCU core (Cortex-R5)
3	MC_DBG_UT_RXD	◄	UART Receive Data of MCU core (Cortex-R5)
4	A53_DBG_UT_TXD	►	UART Transmit Data of sub-core (Cortex-A53)
5	A53_DBG_UT_RXD	◄	UART Receive Data of sub-core (Cortex-A53)
6	A72_DBG_UT_TXD	►	UART Transmit Data of main core (Cortex-A72)
7	A72_DBG_UT_RXD	◄	UART Receive Data of main core (Cortex-A72)
8	GND	-	Ground

4.12 Ethernet Connector (JC2)

Figure 4.13 shows the Ethernet connector on the D3-G board. The D3-G has one Ethernet MAC controller (JC2). JC2 is an RJ45 connector that supports 10 Mbps, 100 Mbps, and 1000 Mbps Ethernet connections.

Figure 4.13 Ethernet Connector (JC2)

4.13 USB Connectors (J3, J6, and JC7)

The D3-G supports three types of USB:

- 1 channel for USB3.0 Host
- 1 channel for USB2.0 Host
- 1 channel for USB2.0 FWDN

Figure 4.14 shows the USB connectors on the D3-G board.

Figure 4.14 USB Connectors (JC3, JC6, and JC7)

Table 4.7 describes the connector for each USB.

Table 4.7 Description of USB Connectors

Reference Number	Function	Description
JC3	USB3.0 Host	USB3.0 Type-A Connector
JC7	USB2.0 Host	USB2.0 Type-A Connector
JC6	USB2.0 FWDN	USB2.0 Type-C Connector

4.13.1 USB3.0 Host Connector (JC3)

JC3 is a USB3.0 Type-A connector for the host port.
USB3.0 supports backward compatibility, so this port can be used for both USB SuperSpeed and USB High-Speed devices.

4.13.2 USB2.0 Host Connector (JC7)

JC7 is a USB2.0 Type-A connector for USB High-Speed host port.

4.13.3 USB2.0 FWDN Connector (JC6)

JC6 only supports USB2.0 FWDN. This connector is used to update software in USB Boot Mode.

4.14 CAN Pin Header (Male) (J5D1)

Figure 4.15 shows the CAN pin header (male) on the D3-G board. The D3-G supports 3-channel CAN.

Figure 4.15 CAN Pin Header (Male) (J5D1)

Table 4.8 describes the pins of J5D1.

Table 4.8 J5D1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU ◄► J5D1	
1	CAN_3P3	-	Power 3.3V
2	CAN_3P3		Power 3.3V
3	CAN0_TX	►	Transmit Data of CAN0 channel
4	CAN0_RX	◄	Receive Data of CAN0 channel
5	CAN1_TX	►	Transmit Data of CAN1 channel
6	CAN1_RX	◄	Receive Data of CAN1 channel
7	CAN2_TX	►	Transmit Data of CAN2 channel
8	CAN2_RX	◄	Receive Data of CAN2 channel
9	DGND	-	Ground
10	DGND	-	Ground

4.15 General Purpose I/O Pin Header (Male) (JH1)

Figure 4.16 shows the general purpose I/O (GPIO) pin header on the D3-G board. The GPIO pin header can be used to connect the Hardware Attached on Top (HAT), which is a Raspberry Pi accessory.

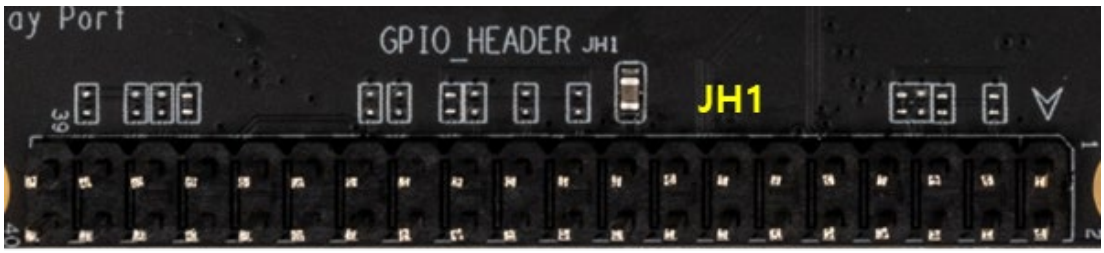

Figure 4.16 General Purpose I/O Pin Header (Male) (JH1)

Table 4.9 describes the pins of JH1.

Table 4.9 JH1 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		CPU◄► JH1	
1	RPI_3P3	-	Power 3.3V
2	RPI_5P0	-	Power 5.0V
3	RPI_GPIO_C21/I2C_SDA	◄►	General Purpose I/O or I2C Data
4	RPI_5P0	-	Power 5.0V
5	RPI_GPIO_C20/I2C_SCL	◄►	General Purpose I/O or I2C Clock
6	GND	-	Ground
7	RPI_GPIO_C22	◄►	General Purpose I/O
8	RPI_GPIO_C26/TX	◄►	General Purpose I/O or UART TX
9	GND	-	Ground
10	RPI_GPIO_C27/RX	◄►	General Purpose I/O or UART RX
11	RPI_GPIO_C23	◄►	General Purpose I/O
12	RPI_GPIO_C28/PWM	◄►	General Purpose I/O or PWM
13	RPI_GPIO_C24	◄►	General Purpose I/O
14	GND	-	Ground
15	RPI_GPIO_C25	◄►	General Purpose I/O
16	RPI_GPIO_C29	◄►	General Purpose I/O
17	RPI_3P3	-	Power 3.3V
18	RPI_GPIO_C04	◄►	General Purpose I/O
19	RPI_GPIO_C02/SPI0_MOSI	◄►	General Purpose I/O or SPI MOSI
20	GND	-	Ground
21	RPI_GPIO_C03/SPI0_MISO	◄►	General Purpose I/O or SPI MISO
22	RPI_GPIO_C05		General Purpose I/O
23	RPI_GPIO_C00/SPI0_SCLK	◄►	General Purpose I/O or SPI SCLK
24	RPI_GPIO_C01/SPI0_CS0	◄►	General Purpose I/O or SPI CS
25	GND	-	Ground
26	RPI_GPIO_C06/SPI0_CS1	◄►	General Purpose I/O or SPI CS
27	RESERVED0 (NC)	-	Not Connected
28	RESERVED1 (NC)	-	Not Connected
29	RPI_GPIO_G01	◄►	General Purpose I/O
30	GND	-	Ground
31	RPI_GPIO_G02	◄►	General Purpose I/O
32	RPI_GPIO_G04/PWM	◄►	General Purpose I/O or PWM
33	RPI_GPIO_G03/PWM	◄►	General Purpose I/O or PWM
34	GND	-	Ground
35	RPI_GPIO_G10/SPI1_MISO	◄►	General Purpose I/O or SPI MISO
36	RPI_GPIO_G08/SPI1_CS0	◄►	General Purpose I/O or SPI CS
37	RPI_GPIO_G06	◄►	General Purpose I/O
38	RPI_GPIO_G09/SPI1_MOSI	◄►	General Purpose I/O or SPI MOSI
39	GND	-	Ground
40	RPI_GPIO_G07/SPI1_SCLK	◄►	General Purpose I/O or SPI SCLK

5 REFERENCES

[1] Contact TOPST for more details: topst@topst.ai

Note: Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

6 REVISION HISTORY

Rev. 1.01: 2025-07-18

- Updated
  - Chapter 2.1: Figure 2.1
  - Chapter 2.2: Table 2.1
  - Chapter 4.1: Updated LPDDR4X density
  - Chapter 4.3: Description
  - Chapter 4.4: Added **Caution**
  - Chapter 4.8: Figure 4.9
  - Chapter 4.15: Table 4.9

Rev. 1.00: 2025-02-28

- Official version release

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