TOPST VCP-G Hardware

User Guide

Rev. 1.1 [G]
2025-01-20

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TABLE OF CONTENTS

Contents

Figures

Tables

1 INTRODUCTION

This document is a hardware user guide for TOPST_VCP based on the TCT7045 application processors. This document describes system installation, debugging, and detailed information on overall design and TOPST_VCP usage.

Table 1.1 describes the features of the TCT7045.

Table 1.1 Features of TCT7045

Part Name			TCT7045
Package			Pin to Pin Compatible FBGA-196pin (12BD)
CPU Frequency			200MHz
On-chip Memory	**Program Flash**		4 MB
	SRAM		512 KB (Including Retention RAM 16 KB)
	Data Flash		256 KB
	DMA Channel		16-channel
Peripheral	**Ethernet**		1 Gbps with AVB
	CAN/CANFD		3-channel
	Dedicated LIN/UART		3-channel (Maximum 6-channel)
	Dedicated I2C		3-channel (Maximum 6-channel)
	Dedicated GPSB (SPI)		2-channel (Maximum 5-channel)
	MFIO (Allocated UART, I2C, GPSB)		3-channel
	ADC	**Resolution**	12-bit SAR type
		Channels	12-channel x 2 groups
		Input Range	3.3V
		Sample Rate	Over 1.0 MSPs
	I2S		1-channel
	Serial Flash Interface		Quad SPI
Power System			3.3V single
Temperature			-40 ~ 105°C

1.1 Terminology

Table 1.2 Terminology

Terminology	Definition
ADC	Analog to Digital Converter
EVB	Evaluation Board
FWDN	Firmware Download
GPIO	General Purpose Input Output
MCU	Micro-Controller Unit
TOPST	Total Open-Platform for System development and Training
VCP	Vehicle Control Processor

2 BLOCK DIAGRAM

2.1 System Block Diagram

Figure 2.1 shows the system block diagram of TOPST VCP-G board.

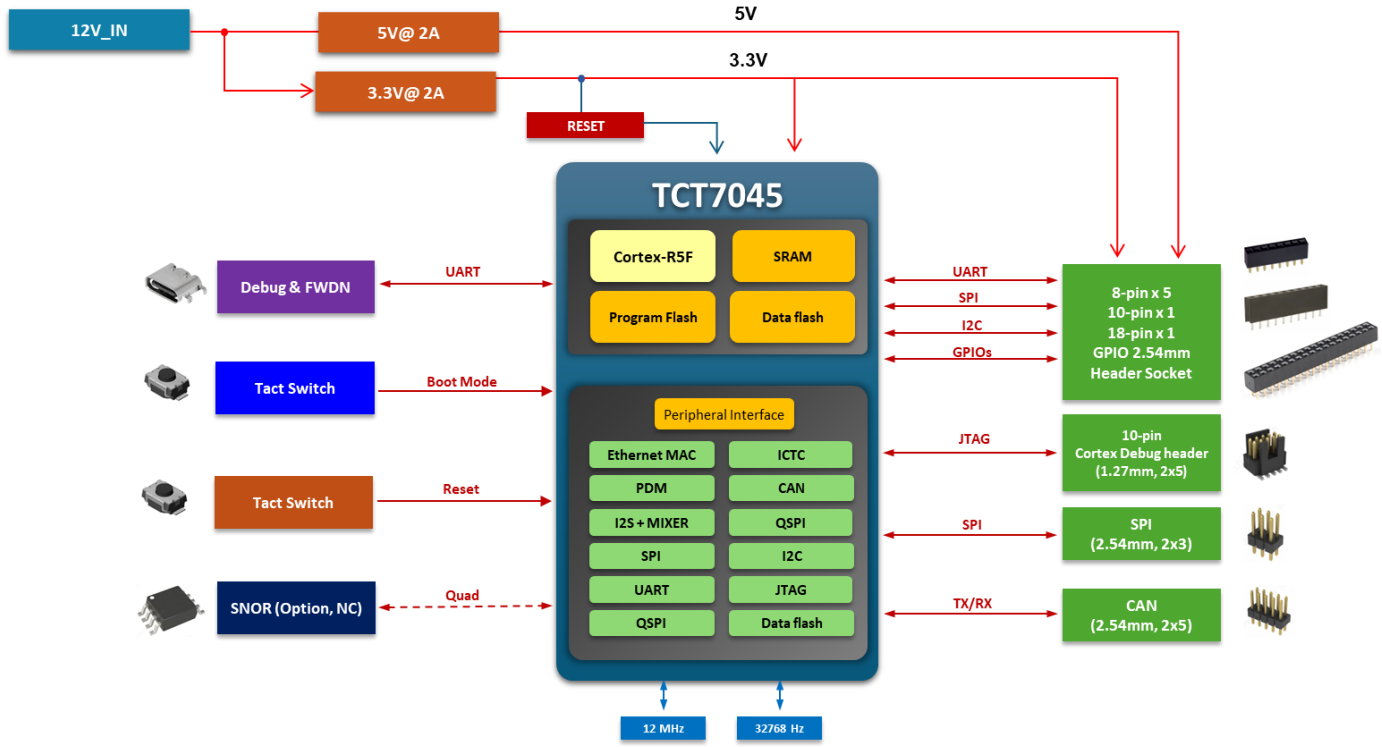

Figure 2.1 System Block Diagram

3 TOPST VCP-G OVERVIEW

The TOPST VCP-G board can used for the following purposes:

- System development
- Training

Table 3.1 describes the default configuration of the TOPST VCP-G board.

Table 3.1 Default Configuration of TOPST VCP-G Board

Board Name	Description
TOPST_VCP_V2.1.1	TCT7045 MCU board for TOPST

3.1 TOPST VCP-G

Figure 3.1 shows the top view of TOPST VCP-G board.

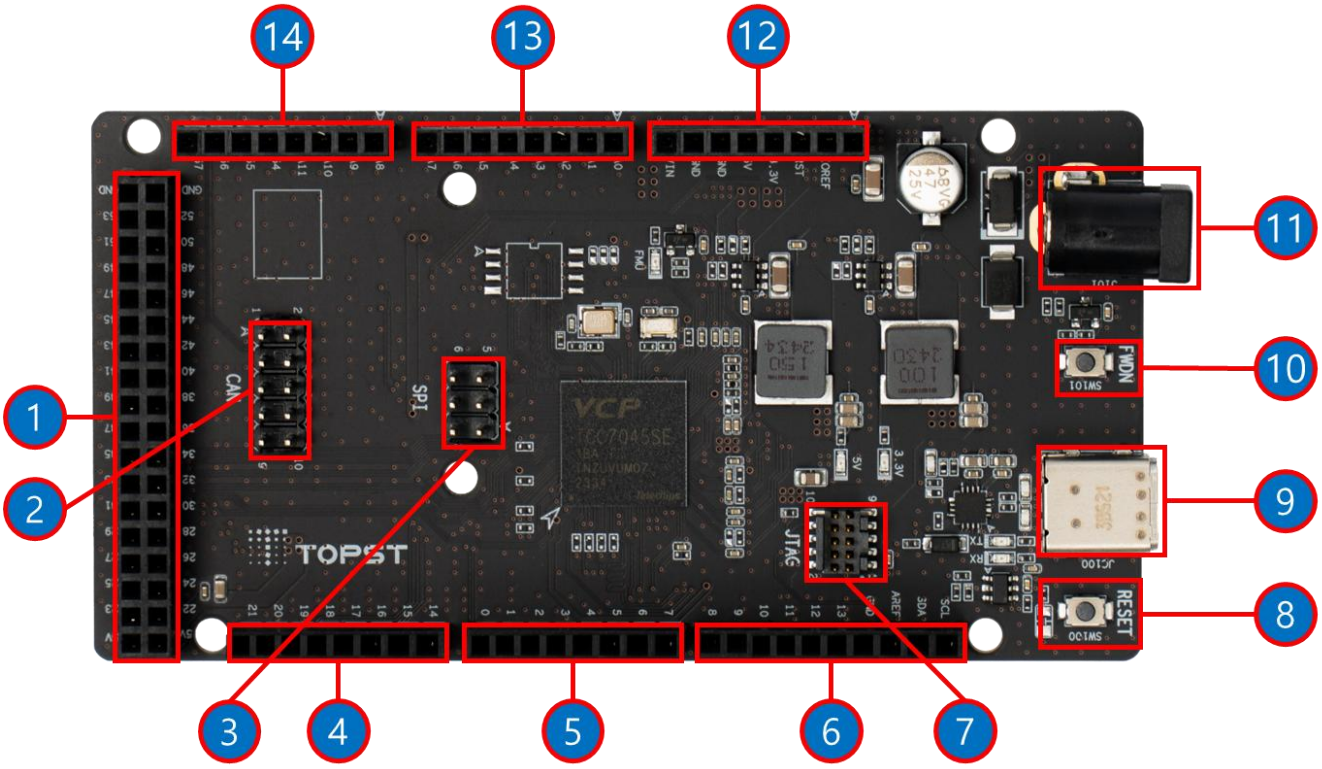

Figure 3.1 TOPST VCP-G Board (Top View)

Table 3.2 describes connectors of TOPST VCP-G board (top view).

Table 3.2 Description of TOPST VCP-G Board (Top View)

Number	Reference Number	Name	Description
1	J18D100	36-Pin Header Female	Header for GPIO & ADC
2	J5D100	10-Pin Header Male	Header for CAN
3	J3D100	6-Pin Header Male	Header for SPI
4	J8D104	8-Pin Header Female	Header for GPIO & ADC
5	J8D102	8-Pin Header Female	Header for GPIO
6	J10D100	10-Pin Header Female	Header for GPIO & ADC
7	J100	10-Pin Header Male	Header for JTAG
8	SW100	Tact Switch	PORN: Initializes the system and the power management of TCT7045
9	JC100	USB Type-C Connector	UART for debugging or FWDN port

Number	Reference Number	Name	Description
10	SW101	Tact Switch	FWDN: Enter the Firmware down mode of TCT7045
11	J101	DC Jack	DC Power Input Jack
12	J8D100	8-Pin Header Female	Header for Power & Reset
13	J8D101	8-Pin Header Female	Header for GPIO & ADC
14	J8D103	8-Pin Header Female	Header for GPIO & ADC

Figure 3.2 shows the bottom view of the TOPST VCP-G board.

Figure 3.2 TOPST VCP-G Board (Bottom View)

4 SPECIFICATIONS

4.1 Quad SPI Flash Memory (U101)

The information on the Quad SPI flash memory is as follows:

- Density : 64 Mb

Note: SNOR is not mounted on the TOPST VCP-G board as default.

4.2 Power In Connector (J101)

DC 12V is supplied to the TOPST VCP-G through the DC jack of J101 from a 12V adaptor.
Figure 4.1 shows the location of J101.

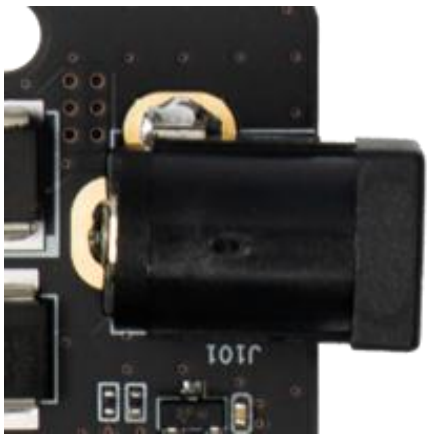

Figure 4.1 Power In Connector (J101)

4.3 Connector for JTAG (J100)

A JTAG emulator can be connected to the TOPST VCP-G through J100 for debugging.Figure 4.2 shows the location of J100.

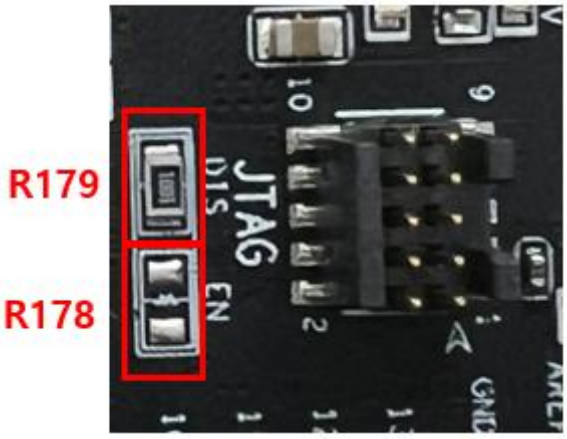

Figure 4.2 Connector for JTAG (J100)

Basically, JTAG is disabled. To enable JTAG, you must change the connections of R178 and R179. If TRSRn is set to high by R178, the MCU enters JTAG mode.
Table 4.1 describes the pins of J100.

Table 4.1 J100 Pin Description

Pin Number	Schematic Net Name	DIR	Description
		MCU ◄► J100	
1	SW_VDD_3P3	-	Power 3.3V
2	TMS	◄	Test Mode State
3	DGND	-	Ground
4	TCK	◄	Test Clock
5	DGND	-	Ground
6	TDO	►	Test Data Output
7	NC	-	Not Connected
8	TDI	◄	Test Data In
9	DGND	-	Ground
10	JTAG_RESETn	◄	System Reset

Table 4.2 describes the setting of JTAG Disable/Enable.

Table 4.2 Setting of JTAG Disable/Enable

Mode	TRSTn Value	R178	R179
JTAG Disable (Default)	Low (1)	N.C	1K
JTAG Enable (Option)	High (1)	1K	N.C

4.4 FWDN Switch (SW101)

The TOPST VCP-G board has one pin for boot configuration using Boot Mode (BM) and supports 2 modes: UART FWDN mode and normal mode.
Figure 4.3 shows the location of FWDN tact switch (SW101) and is used to select the boot modes of the TOPST VCP-G board.

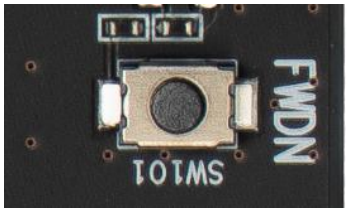

Figure 4.3 FWDN Tact Switch (SW101)

Table 4.3 describes the boot mode selection using the FWDN tact switch (SW101).

Table 4.3 Description of Tact Switch (SW101) for Boot Mode

Mode	BM00 Value	SW101 Status
Normal (Default)	Low (1)	Default
FWDN (Option)	High (1)	Pushed and Power

4.4.1 FWDN Mode Method

There are two methods to enter FWDN mode.

4.4.1.1 Method 1

While pressing the FWDN switch (SW101), connect the 12V power supply to turn on the TOPST VCP-G board.
The FWDN red state light is turned on when power is applied while the FWDN switch is pressed. After releasing FWDN switch (SW101), MCU enters FWDN mode.

Figure 4.4 shows how to enter FWDN mode by using method 1.

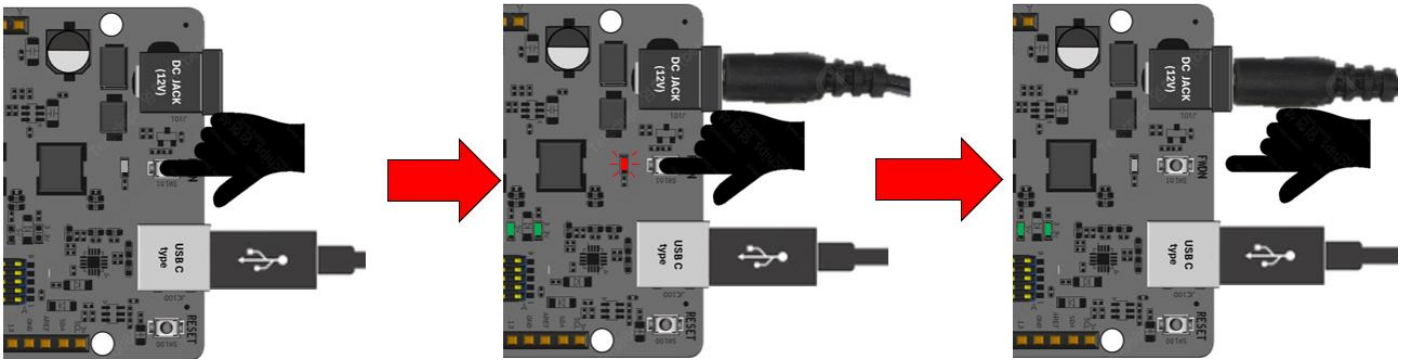

Figure 4.4 Entering FWDN Mode by Using Method 1

4.4.1.2 Method 2

While connecting the 12V power supply, press the FWDN switch (SW101) and then press the RESET switch (SW100).
The FWDN red state light turns on when the power is applied while the FWDN switch is pressed. The 3.3V green light turns off while the RESET switch is pressed. After releasing the FWDN switch (SW101), MCU enters FWDN mode.

Figure 4.5 shows the FWDN mode by using method 2.

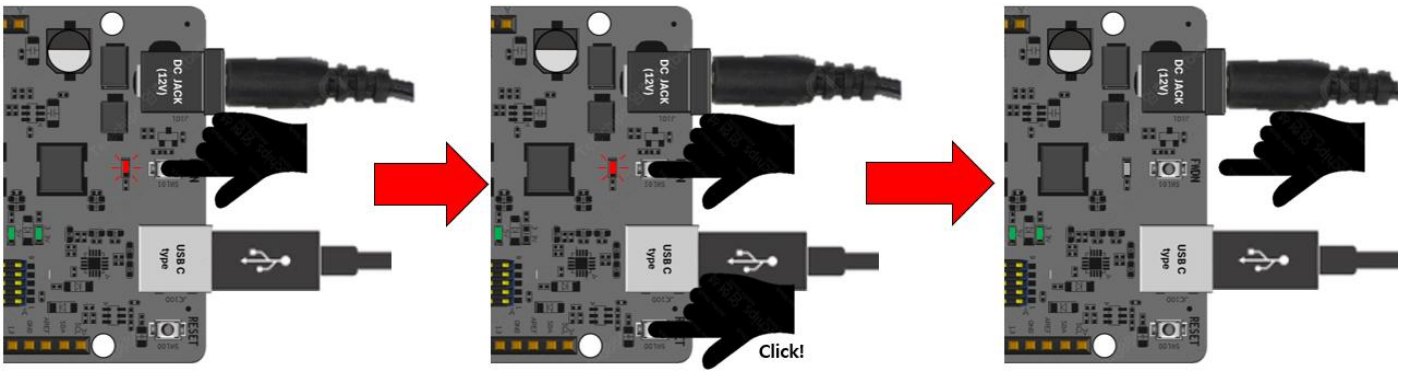

Figure 4.5 Entering FWDN Mode by Using Method 2

4.5 RESET Switch (SW100)

The TOPST VCP-G board has one RESET switch for power of RESET using PORN pin.
Figure 4.6 shows the RESET tact switch (SW100).

Figure 4.6 RESET Tact Switch (SW100)

4.5.1 RESET Tact Switch (SW100) Function

SW100 is a tact switch to reset the power block and system block in TCT7045.
The function of this button is as follows:

- Pressing the tack switch (SW100) while the power is on forces the power block to reset and the system of the TCT7045.

Note: Be careful when pressing the tack switch as the power may suddenly turn off and data may be corrupted.

4.6 Connector for Debugging and FWDN (JC100)

The JC100 is a standard USB Type-C connector. On the TOPST VCP-G board, JC100 is used for debugging or FWDN via UART.
Figure 4.7 shows the location of JC100.

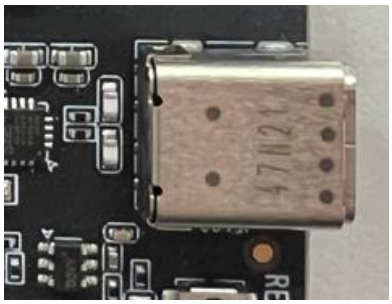

Figure 4.7 USB Type-C Connector (JC100)

You can perform FWDN or check debugging message of the TCT7045 through JC100.
JC100 on the TOPST VCP-G board includes a built-in USB-to-UART bridge controller, so you can directly connect JC100 to PC by using the USB Type-C cable.

4.7 Pin Headers for GPIO, ADC, Power, CAN, SPI

The TOPST VCP-G board have nine 2.54mm pin headers for power, GPIO, ADC, CAN, and SPI to connect others.
Table 4.3 describes purpose of nine pin headers on the TOPST VCP-G board.

Table 4.4 Pin Headers on TOPST VCP-G Board

Number	Reference Number	Name	Description
1	J18D100	36-Pin Header Female	Header for GPIO & ADC
2	J5D100	10-Pin Header Male	Header for CAN
3	J3D100	6-Pin Header Male	Header for SPI
4	J8D104	8-Pin Header Female	Header for GPIO & ADC
5	J8D102	8-Pin Header Female	Header for GPIO
6	J10D100	10-Pin Header Female	Header for GPIO & ADC
7	J8D100	8-Pin Header Female	Header for Power & Reset
8	J8D101	8-Pin Header Female	Header for GPIO & ADC
9	J8D103	8-Pin Header Female	Header for GPIO & ADC

Figure 4.8 shows the location of pin headers on the TOPST VCP-G board.

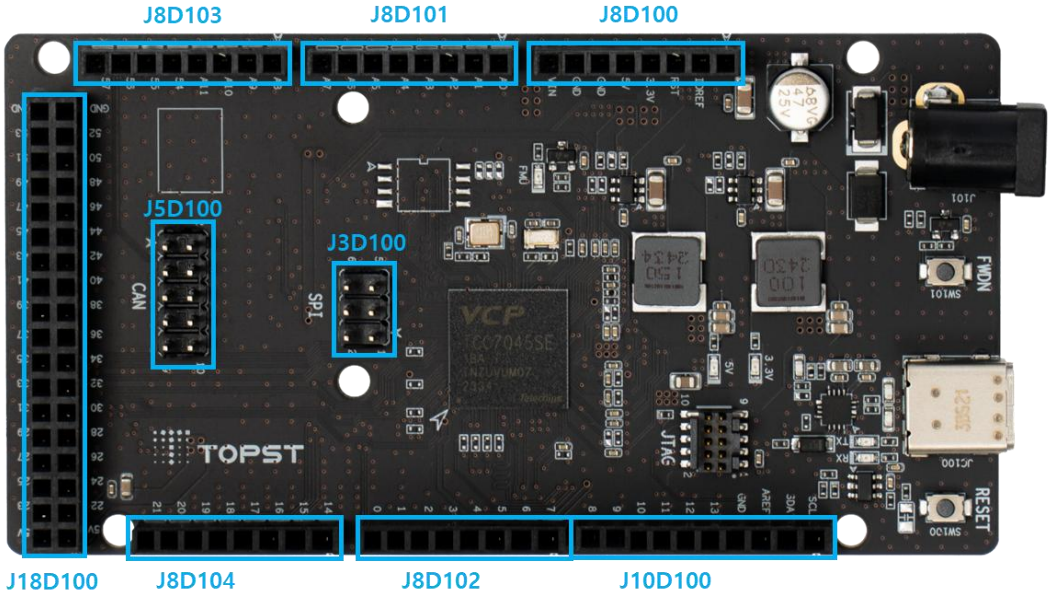

Figure 4.8 Pin Headers on TOPST VCP-G Board

Table 4.4 shows the pin description of J10D100.

Table 4.6 J10D100 Pin Description

Pin Number	J10D100			
	Port Name	Signal Name	DIR MCU ◄► J10D100	Description
1	SCL	GPIO_AC07	◄►	GPIO or ADC signal
2	SDA	GPIO_AC06	◄►	GPIO or ADC signal
3	AREF	ADC06	◄	ADC signal
4	GND	DGND	-	Ground
5	13	GPIO_C12	◄►	GPIO signal
6	12	GPIO_C15	◄►	GPIO signal
7	11	GPIO_C14	◄►	GPIO signal
8	10	GPIO_C13	◄►	GPIO signal
9	9	GPIO_A12	◄►	GPIO signal
10	8	GPIO_B00	◄►	GPIO signal

Table 4.5 shows the pin description of J8D100.

Table 4.7 J8D100 Pin Description

Pin Number	J8D100			
	Port Name	Signal Name	DIR MCU ◄► J8D100	Description
1	-	-	-	
2	IOREF	VCP_3P3	-	Power 3.3V
3	RST	RESET	◄	Reset signal
4	3.3V	VCP_3P3	-	Power 3.3V
5	5V	VCP_5P0	-	Power 5.0V
6	GND	DGND	-	Ground
7	GND	DGND	-	Ground
8	VIN	VIN	-	Voltage input for TOPST VCP-G

Table 4.6 shows the pin description of J8D101.

Table 4.8 J8D101 Pin Description

Pin Number	J8D101			
	Port Name	Signal Name	DIR MCU ◄► J8D101	Description
1	A0	ADC03	◄	ADC signal
2	A1	ADC04	◄	ADC signal
3	A2	GPIO_AC02	◄►	GPIO signal
4	A3	GPIO_AC03	◄►	GPIO signal
5	A4	GPIO_AC05	◄►	GPIO signal
6	A5	GPIO_AC04	◄►	GPIO signal
7	A6	ADC05	◄	ADC signal
8	A7	ADC01	◄	ADC signal

Table 4.7 shows the pin description of J8D102.

Table 4.9 J8D102 Pin Description

Pin Number	J8D102			
	Port Name	Signal Name	DIR MCU ◄► J8D102	Description
1	7	GPIO_B01	◄►	GPIO signal
2	6	GPIO_A13	◄►	GPIO signal
3	5	GPIO_B10	◄►	GPIO signal
4	4	GPIO_B27	◄►	GPIO signal
5	3	GPIO_B11	◄►	GPIO signal
6	2	GPIO_B28	◄►	GPIO signal
7	1	GPIO_B25	◄►	GPIO signal
8	0	GPIO_B26	◄►	GPIO signal

Table 4.8 shows the pin description of J8D103.

Table 4.10 J8D103 Pin Description

Pin Number	J8D103			
	Port Name	Signal Name	DIR MCU ◄► J8D103	Description
1	A8	GPIO_AC08	◄►	GPIO or ADC signal
2	A9	GPIO_AC09	◄►	GPIO or ADC signal
3	A10	GPIO_AC10	◄►	GPIO or ADC signal
4	A11	ADC02	◄	ADC signal
5	54	GPIO_K14	◄►	GPIO signal
6	55	GPIO_K15	◄►	GPIO signal
7	56	GPIO_K01	◄	GPIO signal
8	57	GPIO_K08	◄►	GPIO signal

Table 4.9 shows the pin description of J8D104.

Table 4.11 J8D104 Pin Description

Pin Number	J8D104			
	Port Name	Signal Name	DIR MCU ◄► J8D104	Description
1	14	GPIO_AC00	◄►	GPIO or ADC signal
2	15	GPIO_AC01	◄►	GPIO or ADC signal
3	16	GPIO_A06	◄►	GPIO signal
4	17	GPIO_A07	◄►	GPIO signal
5	18	GPIO_A28	◄►	GPIO signal
6	19	GPIO_A29	◄►	GPIO signal
7	20	GPIO_B03	◄►	GPIO signal
8	21	GPIO_B02	◄►	GPIO signal

Table 4.10 shows the pin description of J3D100.

Table 4.12 J3D100 Pin Description

Pin Number	J3D100			
	Port Name	Signal Name	DIR MCU ◄► J3D100	Description
1	MISO	GPIO_B07	◄►	GPIO signal
2	5V	VCP_5P0	-	Power 5.0V
3	SCK	GPIO_B04	◄►	GPIO signal
4	MOSI	GPIO_B06	◄►	GPIO signal
5	CMD	GPIO_B05	◄►	GPIO signal
6	GND	DGND	-	Ground

Table 4.12 shows the pin description of J18D100.

Table 4.13 J18D100 Pin Description

Pin Number	J18D100			
	Port Name	Signal Name	DIR MCU ◄► J18D100	Description
1	5V	VCP_5P0	-	Power 5.0V
2	5V	VCP_5P0	-	Power 5.0V
3	22	GPIO_B24	◄►	GPIO signal
4	23	GPIO_B23	◄►	GPIO signal
5	24	GPIO_B22	◄►	GPIO signal
6	25	GPIO_B21	◄►	GPIO signal
7	26	GPIO_B20	◄►	GPIO signal
8	27	GPIO_B19	◄►	GPIO signal
9	28	GPIO_A30	◄►	GPIO signal
10	29	GPIO_A27	◄►	GPIO signal
11	30	GPIO_A26	◄►	GPIO signal
12	31	GPIO_A24	◄►	GPIO signal
13	32	GPIO_A25	◄►	GPIO signal
14	33	GPIO_A23	◄►	GPIO signal
15	34	GPIO_A22	◄►	GPIO signal
16	35	GPIO_A21	◄►	GPIO signal
17	36	GPIO_A20	◄►	GPIO signal
18	37	GPIO_A19	◄►	GPIO signal
19	38	GPIO_K13	◄►	GPIO signal
20	39	GPIO_K12	◄►	GPIO signal
21	40	GPIO_K11	◄►	GPIO signal
22	41	GPIO_A18	◄►	GPIO signal
23	42	GPIO_A17	◄►	GPIO signal
24	43	GPIO_A16	◄►	GPIO signal
25	44	GPIO_A11	◄►	GPIO signal
26	45	GPIO_A10	◄►	GPIO signal
27	46	GPIO_A09	◄►	GPIO signal
28	47	GPIO_A08	◄►	GPIO signal
29	48	GPIO_A05	◄►	GPIO signal
30	49	GPIO_A04	◄►	GPIO signal
31	50	GPIO_A03	◄►	GPIO signal
32	51	GPIO_A02	◄►	GPIO signal
33	52	GPIO_A01	◄►	GPIO signal
34	53	GPIO_A00	◄►	GPIO signal
35	GND	DGND	-	Ground
36	GND	DGND	-	Ground

Table 4.13 shows the pin description of J5D100.

Table 4.14 J5D100 Pin Description

Pin Number	J5D100			
	Port Name	Signal Name	DIR MCU ◄► J5D100	Description
1	3.3V	VCP_3P3	-	Power 3.3V
2	3.3V	VCP_3P3	-	Power 3.3V
3	TX0	GPIO_K08	◄►	GPIO signal
4	RX0	GPIO_K01	◄	GPIO signal
5	TX1	GPIO_K09	◄►	GPIO signal
6	RX1	GPIO_K02	◄	GPIO signal
7	TX2	GPIO_K10	◄►	GPIO signal
8	RX2	GPIO_K03	◄	GPIO signal
9	GND	DGND	-	DGND
10	GND	DGND	-	DGND

Figure 4.9 shows the total pin assignment of ten pin headers on the TOPST VCP-G.

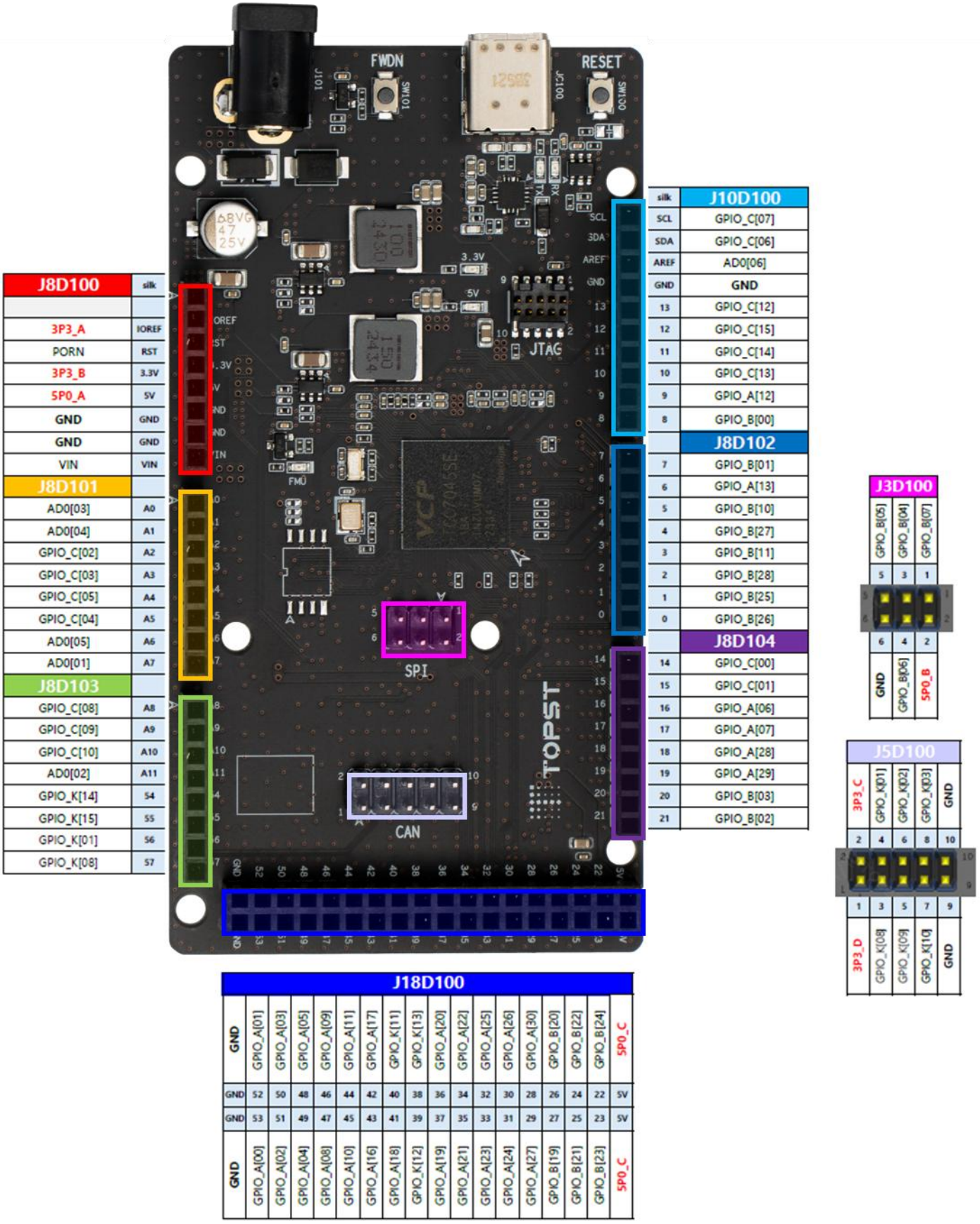

Figure 4.9 Total Pin Assignment of Pin Headers on TOPST VCP-G Board

5 REFERENCES

[1] Contact TOPST for more details: topst@topst.ai

Note: Reference documents can be provided whenever available, depending on the terms of a contract. If the reference documents are unavailable, the contents directly related to your development can be guided.

6 REVISION HISTORY

Rev. 1.00: 2025-01-13

- First version release

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