Got it! Let's go deeper into the **working principle of the 7T SRAM cell** — not just its advantages and modifications.

7T SRAM Cell – Working Principle

The **7T SRAM cell** is an improvement over the conventional 6T SRAM cell, designed mainly to reduce power consumption during the read cycle and improve stability.

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1. Structure & Key Difference

- **Base Structure:** It still uses two cross-coupled inverters (like 6T SRAM) to store data.
- **Additional Transistor (M7):**
  - Connected as a **feedback control transistor** between the first and second inverter.
  - Can disconnect feedback during write operation to make writing easier and more stable.
- **NM4 (Access Transistor):**
  - **Turned OFF** during write operation to break the feedback loop.
  - **Turned ON** during read operation to allow feedback and maintain stability.

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2. Working Phases

A. Write Operation

- **Step 1:** Word line is asserted to enable access transistors.
- **Step 2:** NM4 is **turned OFF** to **disconnect the feedback path** temporarily.
- **Step 3:** Input data is driven directly into the storage node through bit lines.
- **Effect:**
  - With feedback disconnected, there is no contention from the previous stored value.
  - This makes **writing faster** and **less power-hungry** compared to fighting against the existing stored state.

B. Read Operation

- **Step 1:** NM4 is **turned ON**, reconnecting the feedback path.
- **Step 2:** Word line is asserted; bit lines are precharged.
- **Step 3:** Depending on stored value, one of the bit lines starts discharging.

- **Effect:**
  - Feedback keeps storage nodes strongly latched.
  - Prevents accidental flipping of data during read (improving stability).

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3. Power & Delay Behavior

- **Read Power:** Reduced because the extra transistor isolates switching activity and avoids unnecessary current paths.
- **Write Power:** Higher compared to 6T SRAM, because additional transistor switching introduces extra dynamic power consumption.
- **Read Delay:** Slightly higher than 6T because feedback adds extra transistor path resistance.

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4. Summary Table

Operation	NM4 State	M7 Role	Effect
Write	OFF	Disconnects feedback	Easier write, no contention
Read	ON	Maintains feedback	Improves read stability

Key Insight

The **7T SRAM cell's working principle** revolves around **selectively controlling the feedback path**:

- Break feedback during **write** for easier bit flipping.
- Reconnect feedback during **read** for higher **read stability** and lower power dissipation.

Would you like me to **draw a labeled diagram of the 7T SRAM cell and mark the current flow paths** for read and write operations? This could make the working principle much easier to visualize.

Absolutely! Here's a **clear breakdown of the Advantages and Disadvantages of the 7T SRAM Cell** based on its design and working principle:

Advantages of 7T SRAM Cell

1. **Lower Read Power Dissipation**
    - Since the feedback transistor (M7) helps isolate the storage nodes during read, there is less short-circuit current and hence reduced power consumption compared to conventional 6T SRAM.
    - Simulation results in the paper show **30.65% lower read power** than 6T SRAM.
2. **Improved Read Stability**
    - The feedback mechanism strengthens the stored data during read operations, reducing the probability of accidental bit flipping (read disturb issue).
3. **Better Noise Immunity during Read**
    - Reconnecting feedback during read helps maintain the state, making the cell more robust against noise and supply fluctuations.
4. **Enhanced Read Cycle Performance**
    - Due to the improved stability, the read cycle is more reliable, even under process variations.
5. **Reduced Risk of Write-Read Conflict**
    - By turning off NM4 during writes, the previous stored data does not oppose the incoming data, ensuring a successful write.

Disadvantages of 7T SRAM Cell

1. **Increased Write Power Consumption**
    - Disabling feedback and toggling the extra transistor during each write introduces extra dynamic power overhead.
    - Simulation results show **26.18% higher write power** compared to 6T SRAM.
2. **Larger Area Overhead**
    - The extra transistor increases the area of each cell, reducing memory density compared to 6T SRAM.
3. **Longer Read Delay**
    - The additional series transistor adds resistance in the read path, resulting in higher read delay (about **1.3× higher** than 6T SRAM).
4. **More Complex Control Signals**
    - Requires additional control to turn NM4 OFF during write and ON during read, slightly complicating peripheral circuitry.

Summary Table

Aspect	Advantage	Disadvantage
Read Power	30–35% lower than 6T → energy-efficient read	–
Read Stability	Higher, due to feedback reconnection	Slightly higher read delay

Aspect	Advantage	Disadvantage
Write Operation	Easier write (feedback disconnected)	Write power increases (~26% more)
Area	–	Larger area (less density)
Control Logic	–	Requires extra signal for M7/NM4

☑ **Conclusion:**
The 7T SRAM cell is **ideal when read power efficiency and read stability are top priorities**, but it comes with **higher write power, more area, and slightly slower read speed**.

Would you like me to create a **side-by-side comparison table** of **6T, 7T, 8T, and 9T SRAM cells** summarizing their **advantages and disadvantages** in one place for easy reference?

Great question — the **extra transistor (the 7th transistor)** in a 7T SRAM cell is not random — it is **added with a very specific purpose** to improve the cell's reliability and power behavior.

Let's break it down clearly:

Purpose of the Extra Transistor in 7T SRAM Cell

1. Feedback Control (Main Purpose)

- The extra transistor (often called **M7** or **feedback-cut transistor**) is placed in the **feedback loop** of the two cross-coupled inverters.
- **During write operation:**
  - M7 is turned **OFF**.
  - This **disconnects the feedback path** between the two inverters.
  - Without feedback, the previously stored value does not fight the incoming data, making it **much easier to flip the cell**.
- **During read operation:**
  - M7 is turned **ON** again.
  - This reconnects the feedback, which keeps the data **strongly latched**, improving **read stability**.

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2. Reduction of Read Power

- By controlling feedback and the path of current, the 7T design **reduces short-circuit current** during the read cycle.
- This leads to **30–35% lower read power dissipation** compared to the conventional 6T SRAM cell.

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3. Prevention of Read Disturb

- In a 6T cell, reading can disturb the stored data because the access transistor connects the storage node to the bitlines directly.
- In 7T, the extra transistor ensures the storage nodes remain strong (better noise margin) during read, preventing accidental flipping of bits.

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4. Improved Stability under Process Variations

- The added transistor helps control leakage and improves **read static noise margin (RSNM)** compared to 6T under certain conditions, making the cell more robust in scaled technology nodes.

Summary of Why the Extra Transistor Is Used

Reason	Effect / Benefit
Feedback disconnection during write	Easier write (no fight from old state) → faster & more reliable write
Feedback reconnection during read	Stronger data holding → improved read stability
Controlled current path	Reduced read power dissipation
Better noise immunity	Less risk of read disturb and bit flips

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☑ **In short:**
The extra transistor in 7T SRAM is proposed to selectively break and restore the feedback path — making **write easier** and **read more stable** while lowering **read power consumption**.

Would you like me to **draw a labeled diagram** of the 7T SRAM cell and show **where this extra transistor is placed** and **how current flows during read/write**? This would make it very clear visually.