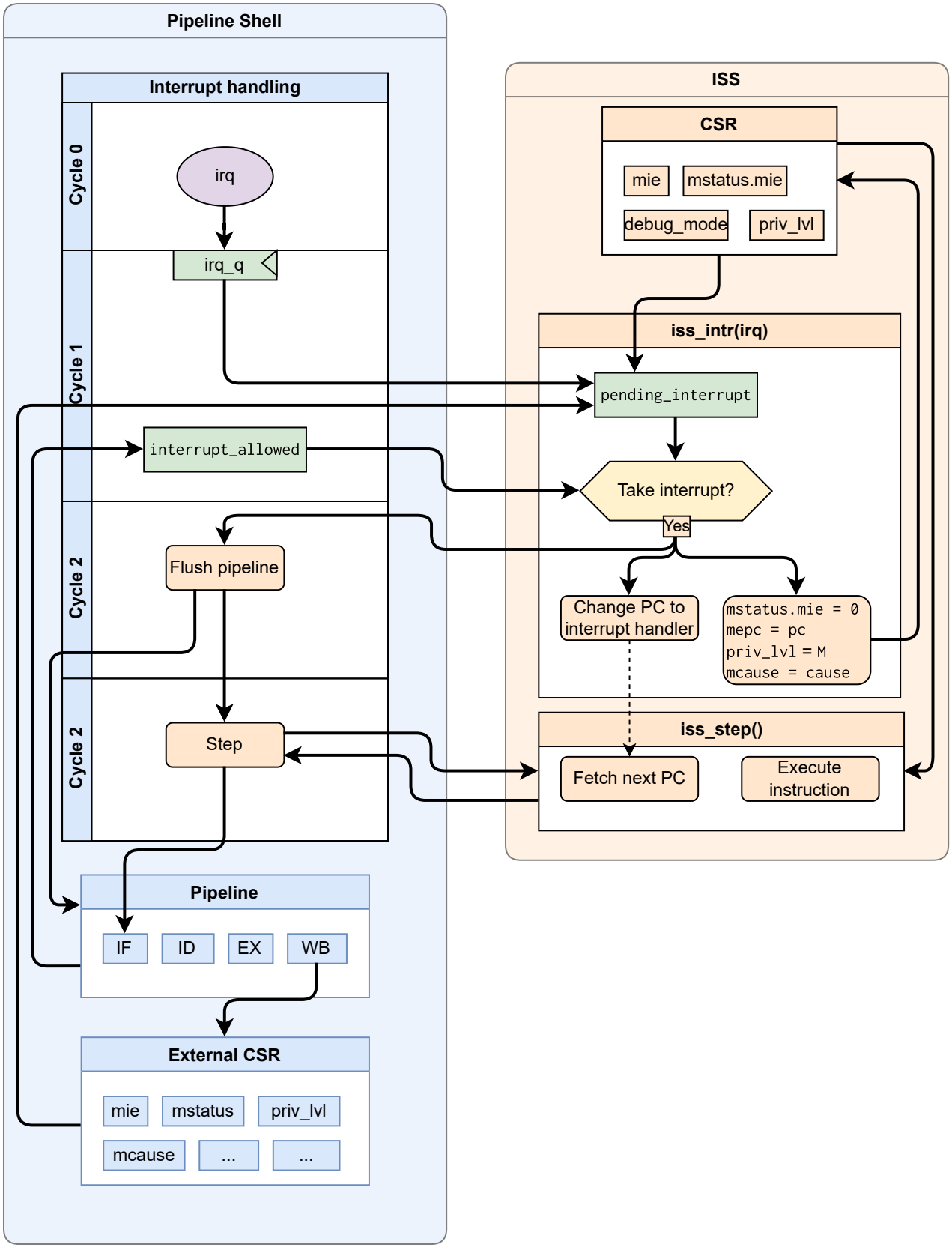
Pipeline Shell
Interrupt handling
Cycle 0
irq
Cycle 1
irq_q
interrupt_allowed
Cycle 2
Flush pipeline
Cycle 2
Step
Pipeline
IF
ID
EX
WB
External CSR
mie
mstatus
priv_lvl
mcause
...
...
ISS
CSR
mie
mstatus.mie
debug_mode
priv_lvl
iss_intr(irq)
pending_interrupt
Take interrupt?
Yes
Change PC to interrupt handler
mstatus.mie = 0
mepc = pc
priv_lvl = M
mcause = cause
iss_step()
Fetch next PC
Execute instruction