INF4420

8-Bit D/A Converter

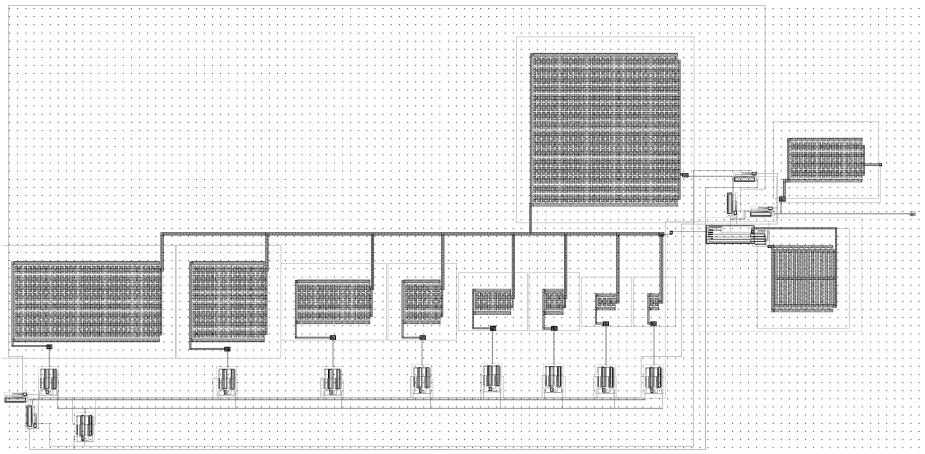

Figure 1: 8-Bit DAC Layout

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Abstract

The main task of this project is to understand and design binary-weighed D/A converters. We start of by looking at at specific type of amplifier, namely the two-stage operational amplifier with a cascoded differential input. This amplifier is designed specifically to operate as the hearth of the D/A converters. After, we dive into the main task where we design a charge-redistribution D/A converter. Here we show the design at a schematic and layout level, of the DAC itself and its components. Finally, we exchange the programmable capacitor array for a resistor network, thereby creating a resistor-bases D/A converter.

We feel the workload has been split fairly equally among the two of us. We designed the schematic level of all components together, while the layout was split where one did the operational amplifier, while the other did the transmission gate, the multiplexer, and the DAC. The report as a whole is cooperated effort. We've worked almost exclusively together in the same room at all times.

1 The function of a Binary-array Charge-redistribution DAC

1.1 DAC architecture description and Operation

This DAC is basically a Switched Capacitor Capacitive-Reset Gain circuit, with a programmable input capacitance. The circuit works in two phases, sample $\phi_{(1)}$ and reset $\phi_{(2)}$. During the sampling phase the output is given by

$$-\frac{C_{Input}}{C_{Feedback}}V_{in}(n)$$

while during the reset phase the output remains near the previous output level

$$V_{out}(n-1)+V_{off}$$

The reason behind the "hold" capacitor, is to stop the op-amp's output from slewing to approximatly 0 during the reset phase. It is important that this capacitance is atleast as large as the highest possible C_{Input}.Now, since the capacitor holds the previously outputted charge, the only thing that will change the output of the op-amp is the op-amps offset voltage between clock phases. Therefore, as the circuit is now insensitive to the opamp's input offset voltage, the effect of the opamp's 1/f noise is greatly reduced.

The capacitor array is programmed by changing which capacitors are charged by the reference voltage. This is controlled by the switches, which in turn is controlled by the binary input word. As the MSBs will cause charge to flow through the higher capacitances, the total C_{Input} will increase, thereby increasing the output as shown from the transfer function above. Note that for the circuit to remain monotonic, the feedback capacitance has to be at least as large as the highest total C_{Input}.

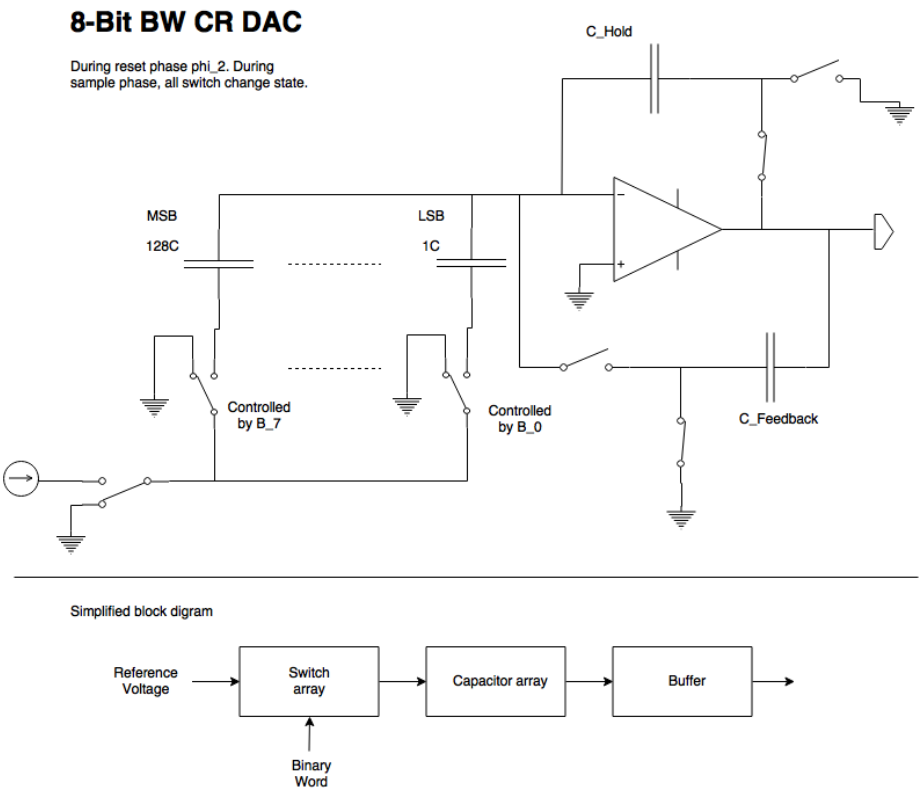


Figure 2: Block diagram of 8-bit DAC

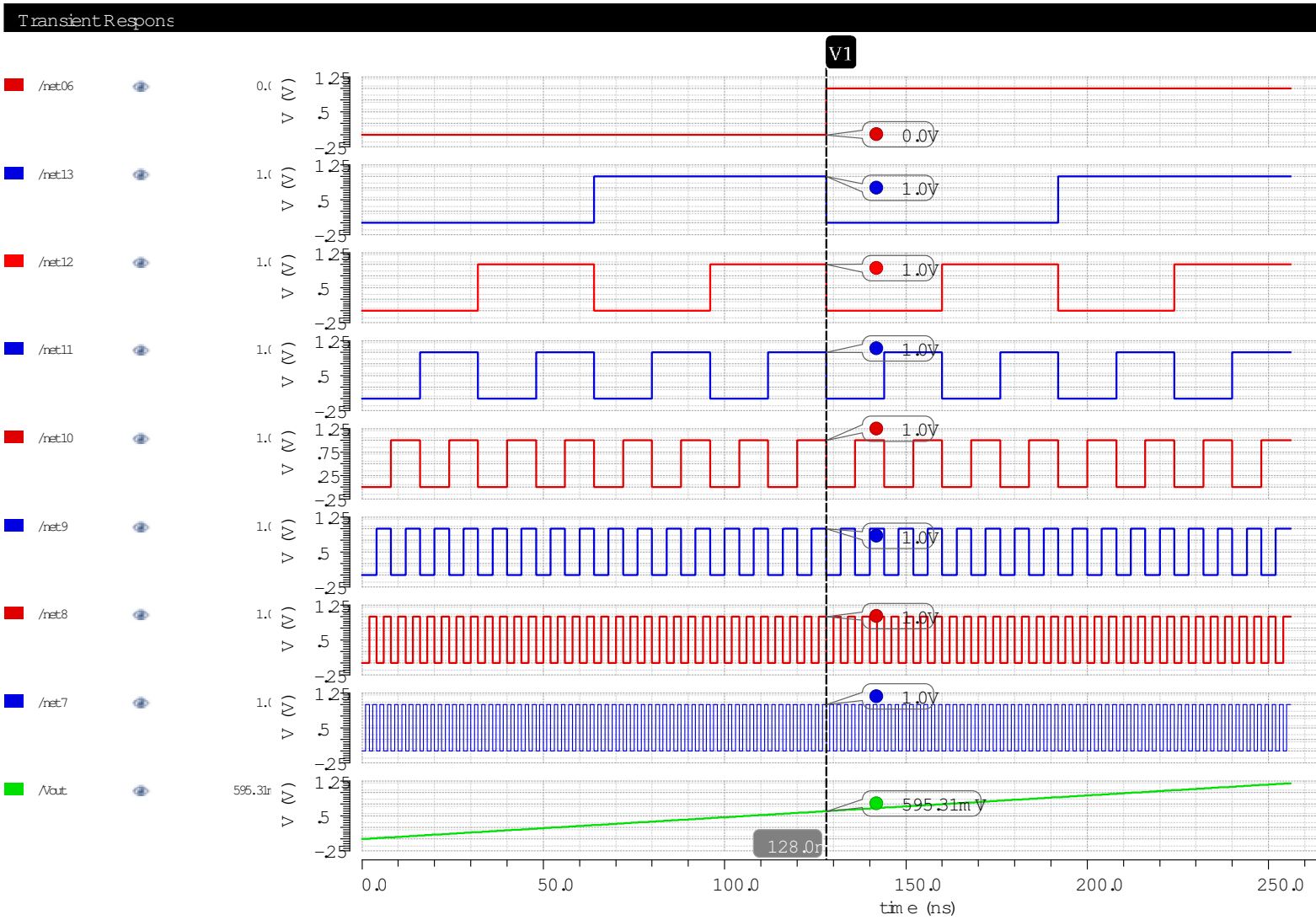


Figure 3: Waveforms at different nodes in the circuit

1.2 Characteristics comparison

	R-2R Resistor Network	Binary-Weighted Resistor Network	Binary-Weighted Charge-Redistribution	Delta-Sigma
Conversion speed	Fast, but slower than Binary-Weigthed due to parasitic capacitance	Binary weigthed has fastest possible convertion speed at the expense of lower accuracy	About same as resistor counterpart, but does have an extra step while converting	Slower, at the expense of very high accuracy
Power Consumption	Approximatly same as Binary-Weigthed resistor network	Minimal decoding circuit and number of switches, therefore low power consumption	Lower, same reason as resistor network. Also, lower because only a certain charge needs to be transferred at any given time.	Low power
Accuracy	Better than Binary-Weighted. Can be non-monotonic at major crossings. Resistors hard to match with a high number of bits. For a 10-bit converter, even using 0.1% precision resistors would not guarantee monotonicity. Can laser-trim down to approx 0.01% presicion.	Not inherently monotonic. Hard to match temperature coefficients of all the resistors	Hard to match capacitors at higher resolution	Very high accuracy
Resolution	Typically 8 bits or fewer, may be pushed to 14 or even more	Usually limited to 8 bits	Limited by capacitor mismatch, usually limited to 8 bits	Very high, upwards of 24 bits
Linearity	Hard to keep linear with higher number of bits.	Limited by nonlinear resistors, and linearity of output buffer	Limited by same reasons as its resistor counterparts, but somewhat better as less mismatch prone	Inherently linear
Area	Relativly few components used, small area	Very small	Small, bit larger than resitor network	Small digital circuit, simple amplification stage
Noise performance	Prone to mismatch and noise at higher resolution	Even more mismatch prone	Less mismatch prone as capacitances are easier to make accurate	Can achieve very high resolution without significant noise, know as a low noise device
Circuit complexity	Simple design	Simplest	A bit more complicated than resistor based DACs	Very simple in contrast to other multi-bit DACs
Cost	Easy and inexpensive at low resolution. Can trade cost for higher accuarcy.	Conceptually the smallest device cost and die area. Can be expensive, therefore limited to 8-bit size	Cheap at lower resolution, more expensive at 10+ bits	Inexpensive relative to the high accuracy
Typical applications	Instrustrial control, mobile, space, video, instrument	Industrial control, mobile	Industrial control, video, mobile, instrument, space	Audio

2 Amplifier design

2.1 Design

We designed the operational amplifier mostly with regard to gain, phase, and bandwidth, as we saw these characteristics as the most important aspects. We where after a gain of >60dB, phase of $>60^0$, and a Unity-Gain-Bandwidth of >4.5MHz. After trying out a few different designs, we ended up with a simple two-stage amplifier with a cascoded differential stage. This way we drastically increased the gain of the first stage, while maintaining a decent gain at the second stage. This way we have fewer transistors at the output, and thereby we can increase the output swing to be approximately rail-to-rail. We could also have created a folded-cascode second stage, but as to save time, we decided that the amplifier matched the set criteria.

The amplifier consists of two stages, and a current-mirror load. The first stage, being the differential input stage, has four p-type transistors as the input transistors and four n-type transistors working as a load to bias the input transistors. This stage is fully symmetrical. Transistor M1b is chosen to have a higher W/L ratio than M1b, such that M1b will operate in strong inversion, while M1a will operate in the weak inversion region. This increases the gain, but somewhat lowers the bandwidth due to extra transistors. The second stage is a basic nmos-pmos common-amplifier. Here the nmos is used for input while the pmos (part of the current mirror) biases the nmos. To increase the gain further, one can cascode the transistors, either in series, or by using a folded topology.

The current mirror biases the differential input transistors, as well as the nmos in the second stage. It uses an external reference current of 29 μA. This current can be generated internally with a CMOS current source circuit such as that shown in figure 5.

One thing we noticed too late was that our slew rate was lacking drastically, as the current flowing from the first stage into the second stage is drastically lower than expected. The slew rate can be made better by increase the size of transistors M1a and M2a, which will move the transistors closer to triode region. In the triode region, the mosfet can supply more increased current, on the cost of lowering the transconductance. This lowered transconductance will lower to gain below what is needed. To get the slew rate to be just barely within the required rate ($\frac{1.2V}{1\mu s} = 2.4\frac{V}{\mu s}$), we have to increase the widths by about 50%, which lowers the gain by 60%. Therefore, a more complex second stage is needed to make up for this lost gain. The lowered gain does however increase the bandwidth by almost 20%.

In addition to slew rate, we have a UGB that is somewhat lower than expected. One way to increase the unity-gain-bandwith is by adding a compensation resistor in with the compensation capacitor, or by increasing the size of the compensating capacitor.

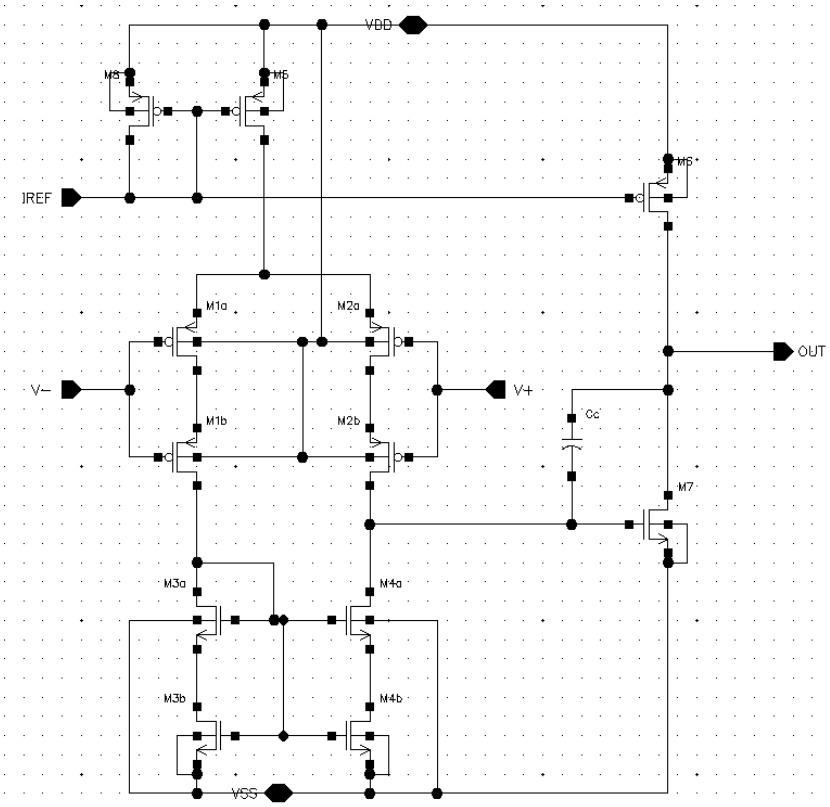


Figure 4: Two-Stage cascoded input operational amplifier

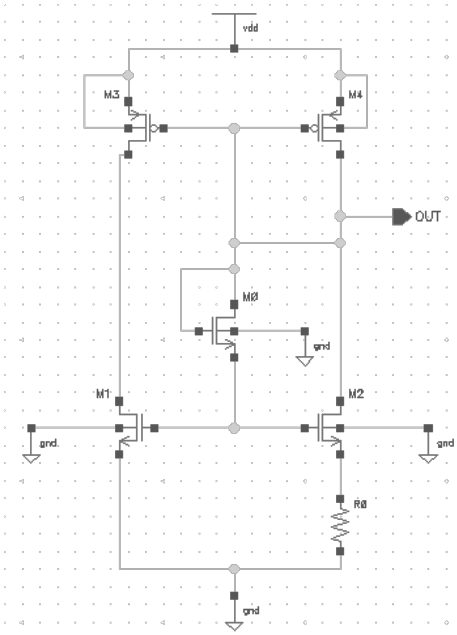


Figure 5: CMOS current generator which can be dimensioned to supply I_{REF}

2.2 Transistor Sizes

	Length (nm)	Total width (μm)	Fingers
M1a	300	3	6
M1b	300	36	60
M2a	300	3	6
M2b	300	36	60
M3a	300	6	10
M3b	600	0.6	1
M4a	300	6	10
M4b	600	0.6	1
M6	300	3.815	7
M7	300	6	10
M5	300	1.74	3
M8	300	1.74	3

Table 1: Transistor values in Transmission Gate

2.3 Characteristics

	Schematic	Layout
Open-Loop Gain (dB)	62.88	64.29
Phase Margin (^{o})	65.06	64.35
UGB (MHz)	3.78	3.85
SR, +/- (V/us)	3.09/1.97	2.7/2
ICMR (V)	0.368 - 1.1	0.36 - 1.06
Output Swing (V)	0.0309 - 1.2	0.0337 - 1.2
Offset (μV)	136.2	1.3
Switching Power, +/- (mW)	40.5/55.3	10.4/9.24

Table 2: Characteristics comparison between schematic & layout

2.4 Layout

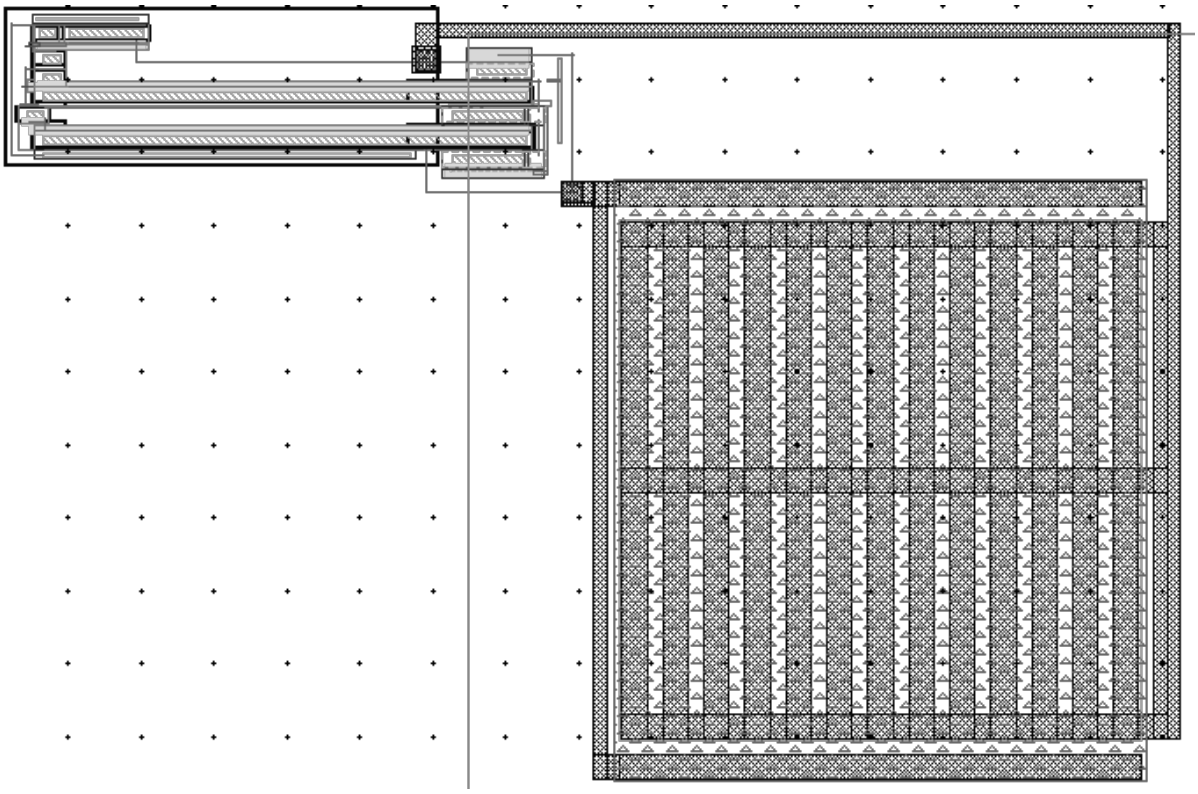
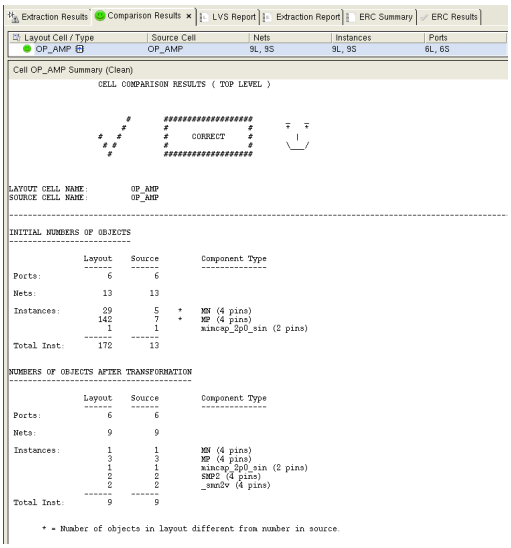


Figure 6: Layout of Operational Amplifier



Extraction Results | Comparison Results | LVS Report | Extraction Report | ERC Summary | ERC Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
OP_AMP	OP_AMP	9L, 9S	9L, 9S	6L, 6S

Cell OP_AMP Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

CORRECT

LAYOUT CELL NAME: OP_AMP
SOURCE CELL NAME: OP_AMP

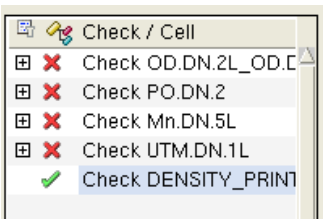
INITIAL NUMBERS OF OBJECTS

	Layout	Source		Component Type
Ports:	6	6		
Nets:	13	13		
Instances:	29	5	*	MN (4 pins)
	142	7	*	MP (4 pins)
	1	1		mimcap_2p0_sin (2 pins)
Total Inst:	172	13		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	6	6	
Nets:	9	9	
Instances:	1	1	MN (4 pins)
	3	3	MP (4 pins)
	1	1	mimcap_2p0_sin (2 pins)
	2	2	SMP2 (4 pins)
	2	2	_smn2v (4 pins)
Total Inst:	9	9	

* = Number of objects in layout different from number in source.



(a) Amplifier LVS-result **(b)** Amplifier DRC-result

Figure 7: Layout reports for amplifier

3 Binary-Array Charge-Redistribution DAC

3.1 Components

3.1.1 Transmission Gate

The transmission gate is put in place instead of single transistors, to limit the effects of the non-idealities on the rest of the circuit. By giving the transistors a high W/L-ratio, the gates will be able to switch faster, as more current will be able to flow through the channel at a given time.

3.1.1.1 Schematic

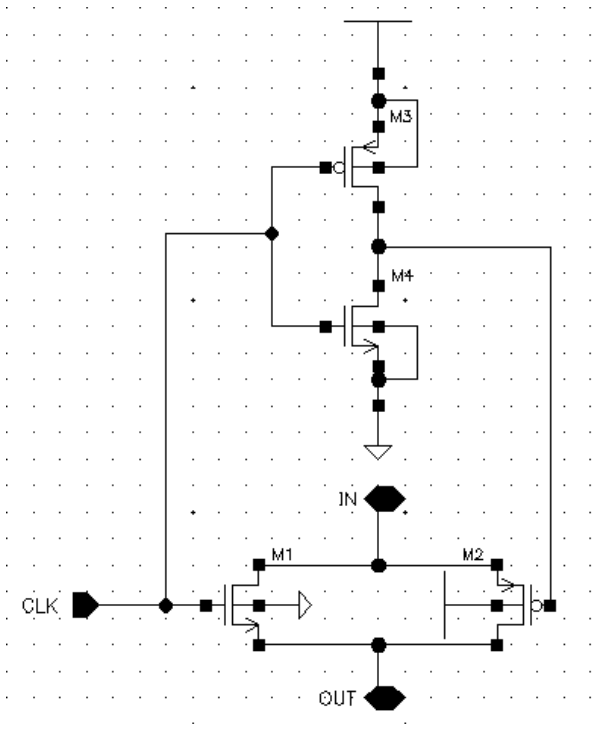


Figure 8: Transmission Gate Schematic

	Length (nm)	Total width (μm)	Fingers
M1	300	3	10
M2	300	6	20
M3	300	0.6	2
M4	300	0.3	1

Table 3: Transistor values in Transmission Gate

3.1.1.2 Layout

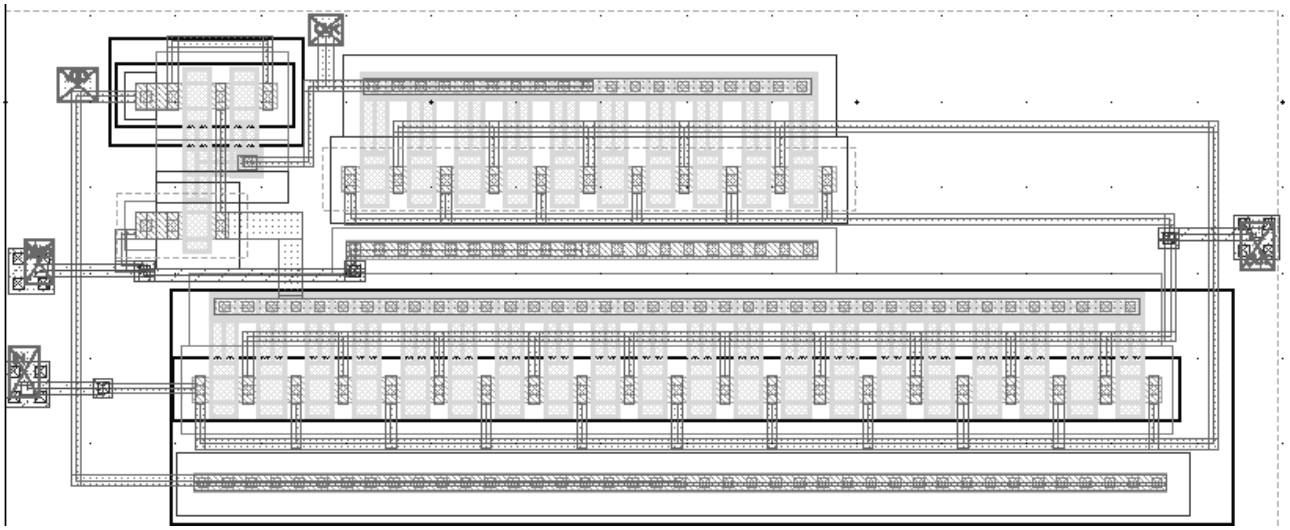
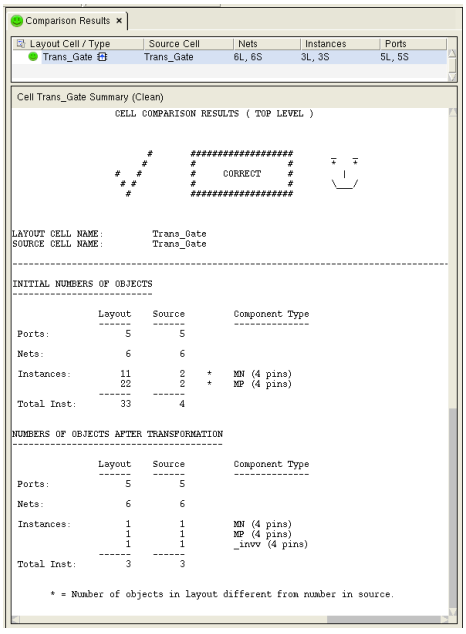
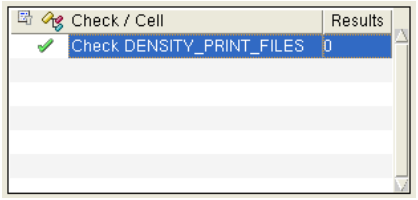


Figure 9: Transmission Gate Layout



(a) Transmission Gate LVS-result



(b) Transmission Gate DRC-result

Figure 10: Layout reports for DAC

3.1.2 2:1 MUX

3.1.2.1 Schematic

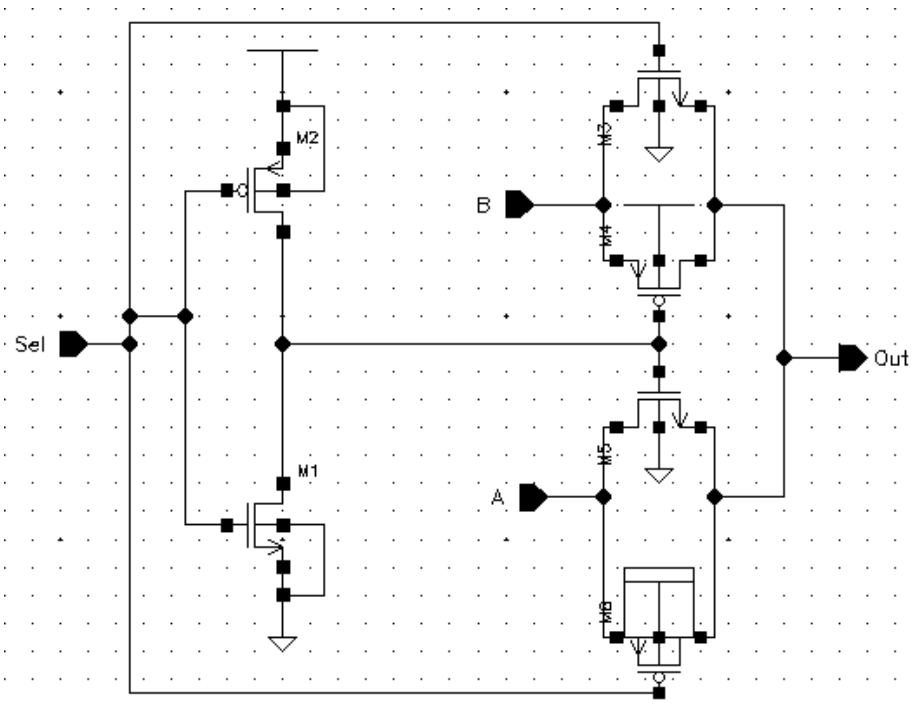


Figure 11: 2:1 MUX Schematic

The 2:1 mux is made out of two transmission gates and one inverter. In this case the inverter will only invert the signal to the transmission gates and the current through the inverter is small. The transistors in the gates have to carry all the current from input A and B to the output. I order to handle this current we scaled up the width in the transmission gates so they could handle higher current. The values we selected is listed in the table under.

	Length (nm)	Total width (μm)	Fingers
M1	300	0.3	1
M2	300	0.6	2
M3	300	3	10
M4	300	6	20
M5	300	3	10
M6	300	6	20

Table 4: Transistor values in 2:1 MUX

3.1.2.2 Layout

In order to make it easier to work with the layout, we placed the pins similar to the schematic of the mux. Select-pin is located on the left side and output on the right. At the top of the layout we placed input B and the vdd. At the bottom we placed input A and gnd.

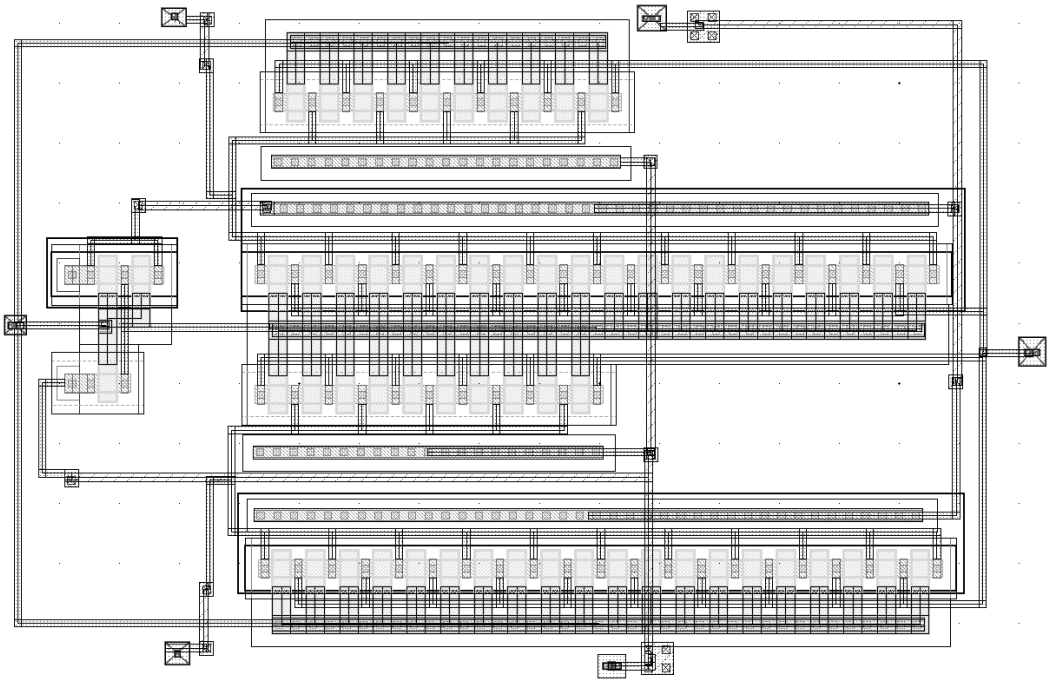
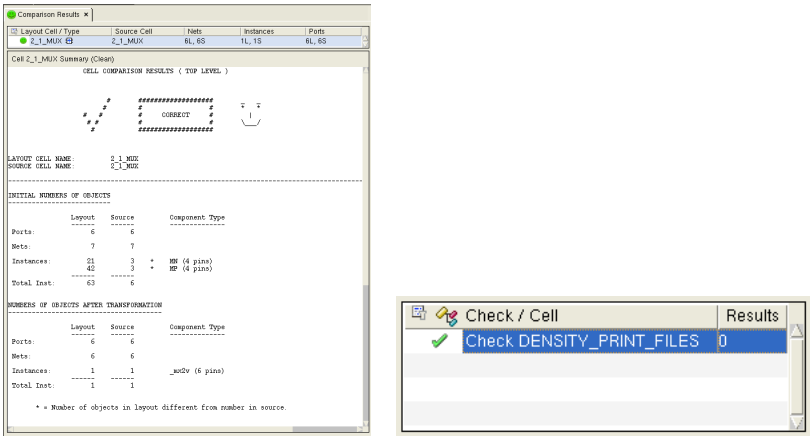


Figure 12: 2:1 MUX Layout



(a) 2:1 MUX LVS-result **(b)** 2:1 MUX DRC-result

Figure 13: Layout reports for DAC

3.2 Design

This circuit works a lot like a switch-capacitor gain circuit as mentioned above; The differences being the programmable capacitor array, the sampling capacitor, and changing reference voltages.

In order to utilize the full voltage range, the bits and clock decide together which reference voltage should be passed through to charge a given capacitor. While PHI1 is active (reset phase), all capacitors should be charged to the common-mode voltage (power ground, 600mV) independent of the bit values. However, when PHI2 is active (sample phase), the capacitors charge is dependent on the corresponding bit value. When the bit value is high, the capacitor will be charged with the high reference voltage (in our case 800mV). Meanwhile, if the bit value is low, the corresponding capacitor will be charged to the low reference voltage (in our case 0V, ground). The output equation of the DAC can be derived from the output equation of a standard SC-gain circuit, with the reference voltage changing upon a word value:

$$V_{Out} = -\frac{C_{Total}}{C_{Feedback}} \cdot V_{Ref} \tag{1}$$

, where $C_{Feedback} = 12.8pF$, and

$$C_{Total} = 50pF \cdot (B_0 + 2 \cdot B_1 + 4 \cdot B_2 + 8 \cdot B_3 + 16 \cdot B_4 + 32 \cdot B_5 + 64 \cdot B_6 + 128 \cdot B_7) \tag{2}$$

The reason that we opted for a sampling capacitor at the output of the amplifier, was for two main reasons. The first being that the sampling capacitor was now no longer dependent on the advanced clock signals PHI1a and PHI2a. Secondly, a feedback hold capacitor caused the DACs output to be unstable for the first ≈100 clock signals. This problem could however have been solved by pre-charging the hold capacitor to be V_{CM}. Sampling the output without feedback fixed both these problems, on the expense of less output voltage swing range. However, after completing and simulating the layout, we noticed that the sampling clock generated a glitch too large to ignore in the output. This glitch did however only last a few nanoseconds. Therefore, when calculating the different characteristics, we chose to ignore the glitches. By creating a more robust transmission gate for the sample clock, this clock feed-through could be mitigated.

We stated above that our choice of hold-circuitry removed the dependencies of two clock signals. However, as you might have noticed, this introduced the need for a new clock signal we called SAMPLE_CLK. This clock is high for a short while near the end of PHI2, as this is when the output is the most stable. We chose to take this clock as an external input, but there are ways to generate this clock from the already present PHI2. One of the better analog methods to do this is so use a voltage-controlled oscillator, a phase-locked-loop, and a binary counter on the VCO to implement the desired delay and duty-cycle.

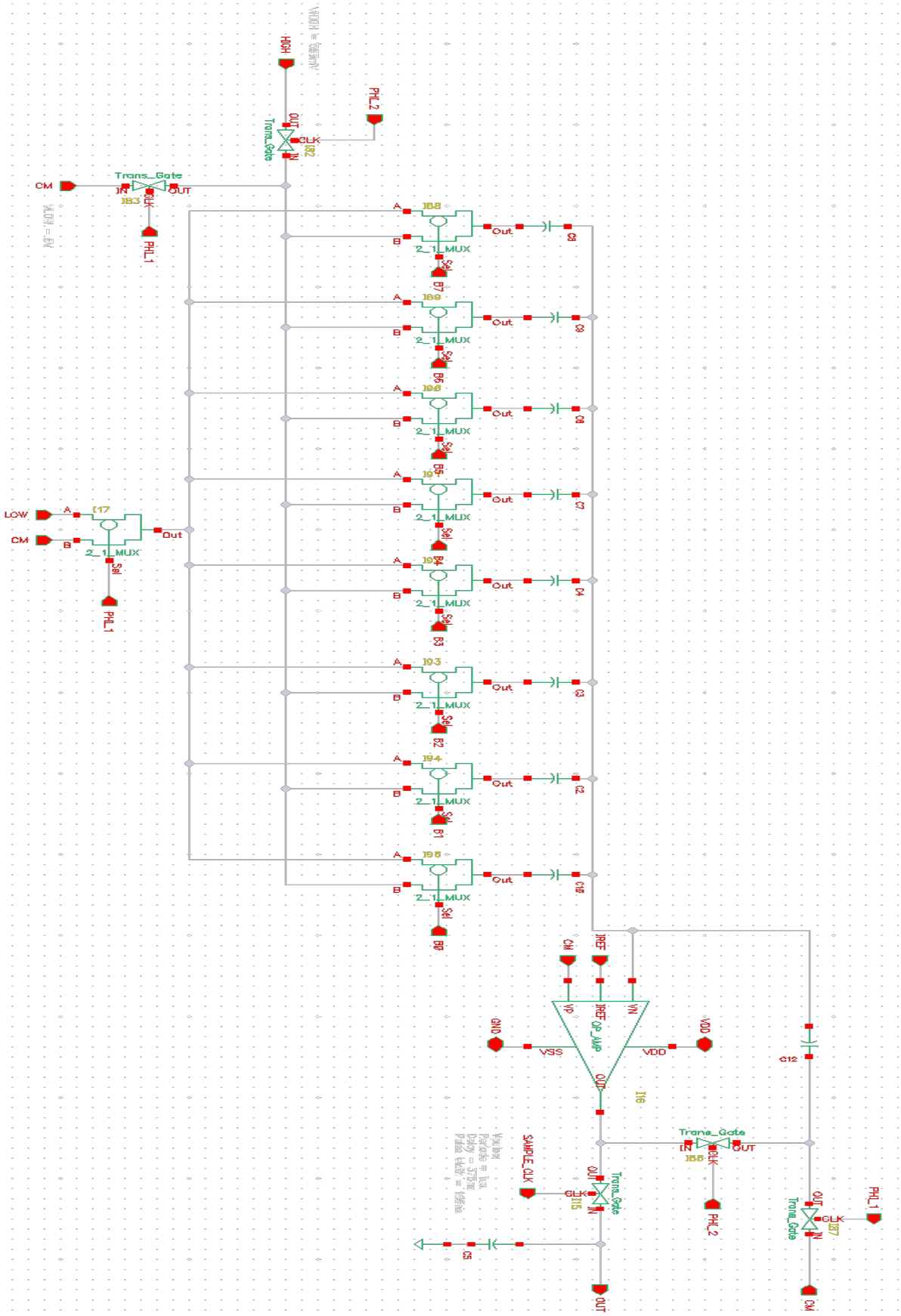


Figure 14: 8-Bit Binary-Weighed Switched-Capacitors D/A Schematic

3.3 Layout

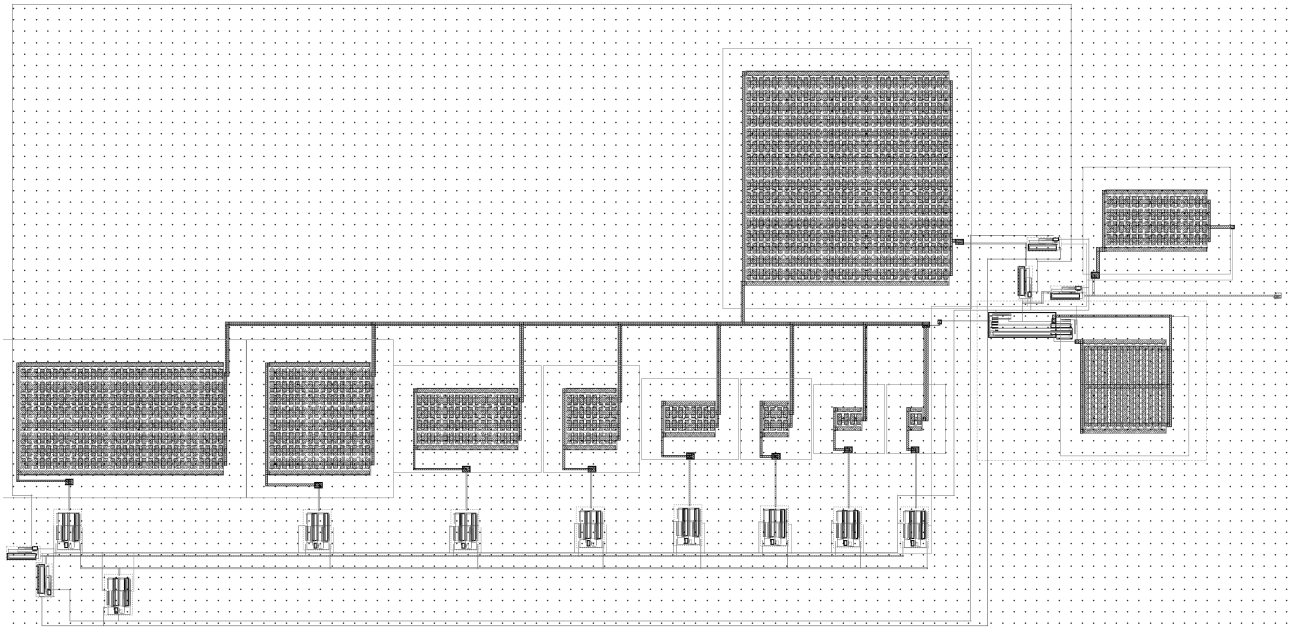
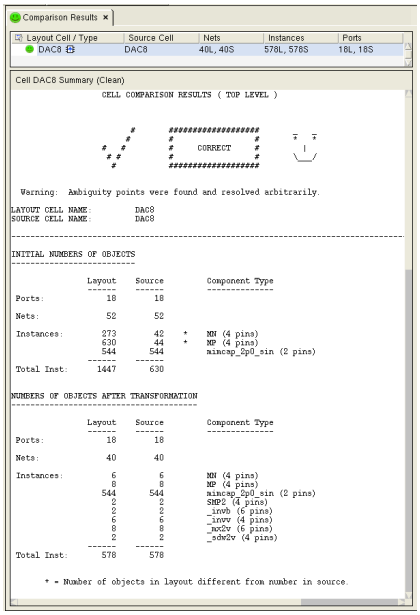
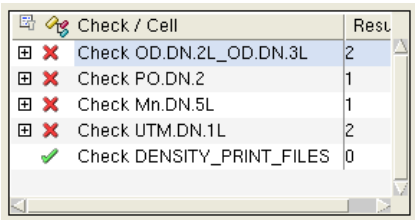


Figure 15: 8-Bit DAC Layout



(a) 8-Bit DAC LVS-result



(b) 8-Bit DAC DRC-result

Figure 16: Layout reports for DAC

4 Binary-Weighted Resistor DAC

The binary-weighted resistor DAC is similar to the charge-redistribution DAC; the big change being that the capacitors are exchanged for resistors. The transfer function is also similar, with a few key differences.

$$V_{Out} = \frac{R_{Feedback}}{R_{Total}} \cdot V_{Ref} \tag{3}$$

, where $R_{Feedback} = R$ and

$$R_{Total} = \frac{B0}{256R} + \frac{B1}{128R} + \frac{B2}{64R} + \frac{B3}{32R} + \frac{B4}{16R} + \frac{B5}{8R} + \frac{B6}{4R} + \frac{B7}{2R} \tag{4}$$

for $B0...B7 \in \{0, 1\}$.

Also, as our power ground is 600mV, the reference voltage (V_{In}) through every transistor is decided by each bit. If the bit is off 1.15V flows through the resistor. On the other hand, if the bit is high, 50mV will flow through the resistor. This way we get the full output range, and a non-inverted signal. If you switch the conditions of the two reference voltages, the signal will then be inverted.

The power consumption is not constant in the resistor DAC. The DAC uses most power when when the input bits are at a low value. This is because the reference voltage over the resistor is relatively high (1.15V). When the bit goes high, the reference voltage over the resistor is set to 50 mV and the current needed is lower. When we plot the current in the DAC we also get some small spikes of higher current when the bit is changing.

The architecture of the resistor DAC is made so that the output only is dependent on the input bit. This is the reason we don't need to sample the output in order to get a stable output.

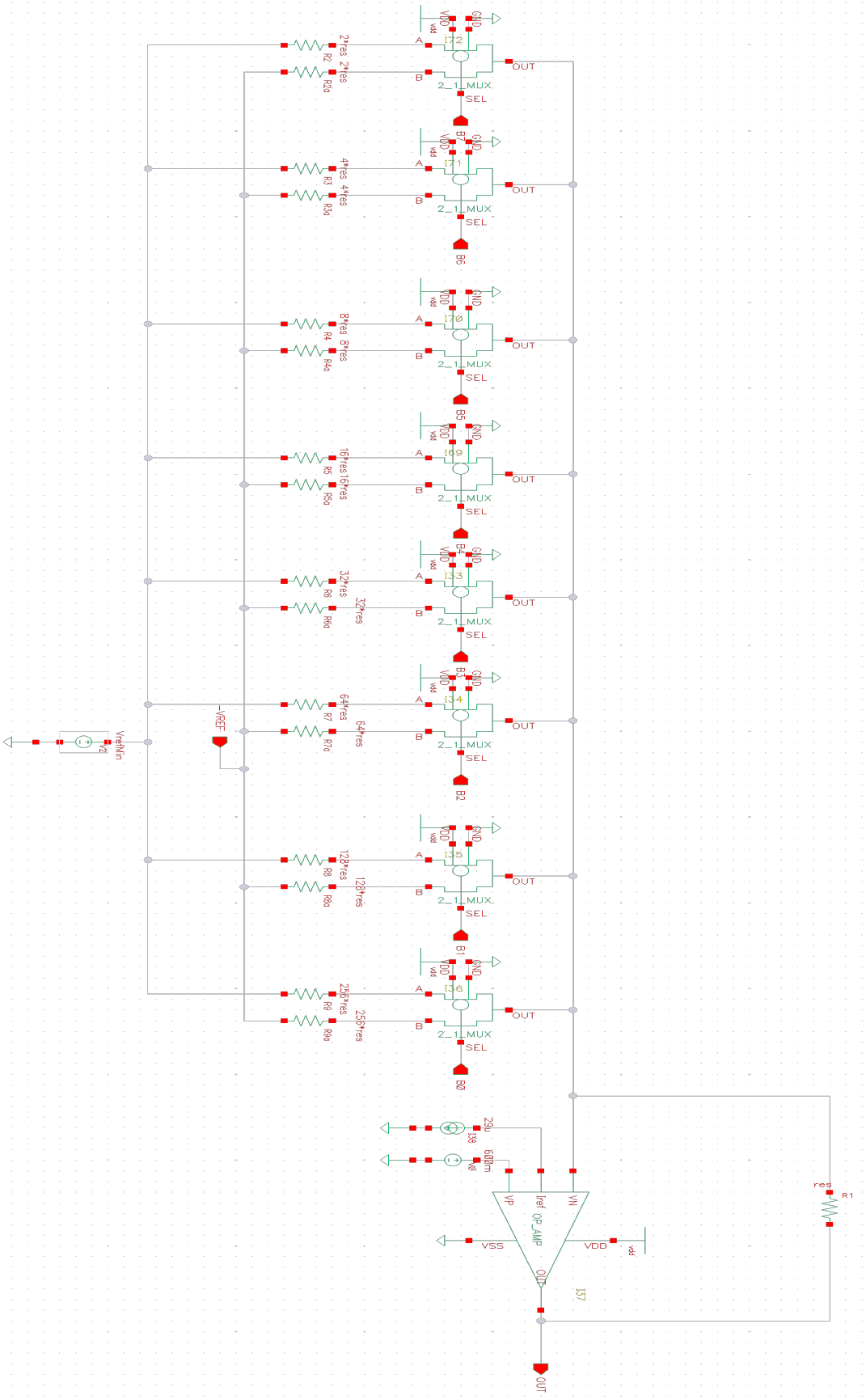


Figure 17: 8-Bit Resistor-DAC Schematic

5 Comparison of DAC results

	Schematic	Layout	Resistor DAC
Offset error	$-48.08mV$	$-11.7mV$	$0.089mV$
Full-scale error	2.41%	1.32%	0.92%
INL	$2.272\mu V$	$1.21\mu V$	$0.152\mu V$
DNL	$1.3mV$	$2.8mV$	$3.5mV$
ENOB	3.3	-	6.7
SNR (dB)	42	-	42.7
Dynamic range (dB)	21.46	-	42.26
THD (dB)	-21.5	-	-52.4
Operating voltage range (mV)	955.35 -134.6 $= 820.8$	1007.5 -179.1 $= 828.4$	1141 -60.61 $= 1080.36$
Maximum conversion speed	Risetime: 49ns Falltime: 10ns Maximum speed: 10MHz	-	-
Power consumtion (W)	Hold: 187.2μ Switch: 512μ Sample: $4.38m$	Hold: 168μ Switch: $6.67m$ Sample: 876μ	Hold: 174μ Switch: 264μ

Table 5: DAC comparsion table

NOTE: We figured out how to use the spectrum analyzer in Cadence after doing the measurements the hard way. We talk about this in the next section.

Offset error is the output of the DAC when the input signal is power ground. In our case, this is when MSB is 1, while other bits are 0. In this case we expected the output to be halfway between VSS and VDD; our power ground 600mV. Instead, as there is some offset error, the output was approximately 552 mV.

The full-scale error is the maximum distance between the bits of our DACs output and a straight, ideal line. We calculated this error by taking the output voltage at every sample, and subtracting the voltage of the ideal line at the same x-value. We then found the highest differnce to be 19.8 mV, which equals to 2.41% of our operating voltage range of 820mV.

There are two standard ways of testing the INL errors: best-fit and endpoint. As our endpoints are "where they should be", while the curve is obviously not perfectly linear, we opted for the endpoint INL as this would give a more honest result. We calculated the INL by taking the integral of our DACs output, while substracting the integral of the straight line between endpoints.

In an ideal DAC, every bit is exactly 1 LSB away from the next (or previous) bit. Therefore, we calculated the difference between every bit, both in the rising and falling direction. Most bits where perfectly 1 LSB away from eachother ($\pm$1mV). However, as can be seen on the waveform, there is a series of bits that has a DNL $>$1 LSB. This causes the non-linearity seen in the plot. The highest DNL error was found to be approximatly 2.3mV, which is close to

0.67LSB.

The effective number of bits is calculated from the SNDR as follows:

$$N_{eff} = \frac{SNDR - 1.76dB}{6.02dB} \tag{5}$$

Signal-to-Noise Ratio is the ratio of the signal power to the power of the noise present in the signal. We found this by running a sine wave through an ideal ADC, taking the ADC output into our DAC, and then substracting the sine wave from the DACs output. We where then left with only the noise. Then, by taking the RMS value of the sine wave and the noise, we can calculate the SNR from the formula:

$$SNR = 20\log\frac{P_{Signal}}{P_{Noise}} = 20\log\left(\frac{A_{rms|_{signal}}}{A_{rms|_{noise}}}\right)^2 \tag{6}$$

There are a few ways to increase the SNR. One can either increase the full scale range of the signal power, or decrease the noise power by deceasing the quantization noise, clock jitter, aperture jitter, and thermal noise.
The total SNR can be calculated as the sum of mentioned individual noise sources, where the theoretical maximum SNR ignores everything but the quantization error. The theoretical maximum can be express as

$$SNR_{Quantization} = 6.02 \cdot N + 1.76 = 6.02 \cdot 8 + 1.76 = 49.92dB \tag{7}$$

Dynamic range is often quantifies by the maximum achievable SNDR (Signal-to-noise and distortion ratio; often referred to as SINAD, signal-to-noise-and-distortions). The SNDR can be calculated from the SNR and the THD

$$SNDR = 20\log_{10}\sqrt{(10^{-SNR/20})^2 + (10^{-THD/20})^2} \tag{8}$$

Total harmonic distortion is the distortion caused by harmonics in the output signal. Can either be expressed in percentage or in dB. We found the THD by doing a discrete fourier transform on the output, when the input was a 1kHz sine wave with $V_{pp} = 1.2V - 0V$. We then added together the absolute value of the 10 first harmonics (as specified by IEEE), before dividing by the fundamental RMS value (as described in equation 9). We then multiplied by 100 to get it in percentage.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_rms}^2}}{V_{fund\_rms}} \tag{9}$$

The input voltages to the DAC is limited by the reference voltages, such that the DACs can produce readable bits even the the input word is "black" (all bits

high) or "white" (all bits low). The DAC is monotonic all the way from ground at the lowest reference voltages, to a bit over around 850 mV as the highest output voltage. To stay safe, the reference voltage is limited to 800 mV in this case. These reference voltages causes the DAC to swing from 955mV down to 134.6 mV, causing the operating voltage range to be 820.4 mV.

The maximum conversion speed is found by checking the rise- and falltime of the DAC when switching from all bits high to all bits low, and vice versa. The highest possible clock rate can then be calculated from these switching times. On the SC DAC schematic, the risetime was the limiting factor. As the DAC has to be able to go from high to low in a matter of half a period, the highest possible conversion speed with a risetime of 49ns is a period of 98ns, which equals a frequency of around 10MHz.

Power consumption is measured as the supply voltage multiplied by the current the DAC draws from VDD during three different situations: while holding, switching, and sampling.

6 Conclusion and Discussion

As stated in the beginning of the previous section, we figured out how to use the spectrum analyzer on deadline day. This gave us some better results. We chose to keep the "hand-calculated" values in the above section, while below you can see the more accurate results from Cadence. We believe the reason that our first values are worse, is because of the input frequency we used while testing. We chose an arbitrary frequency of 1kHz, which caused more harmonics to distort the signal. When choosing a frequency based on the equation

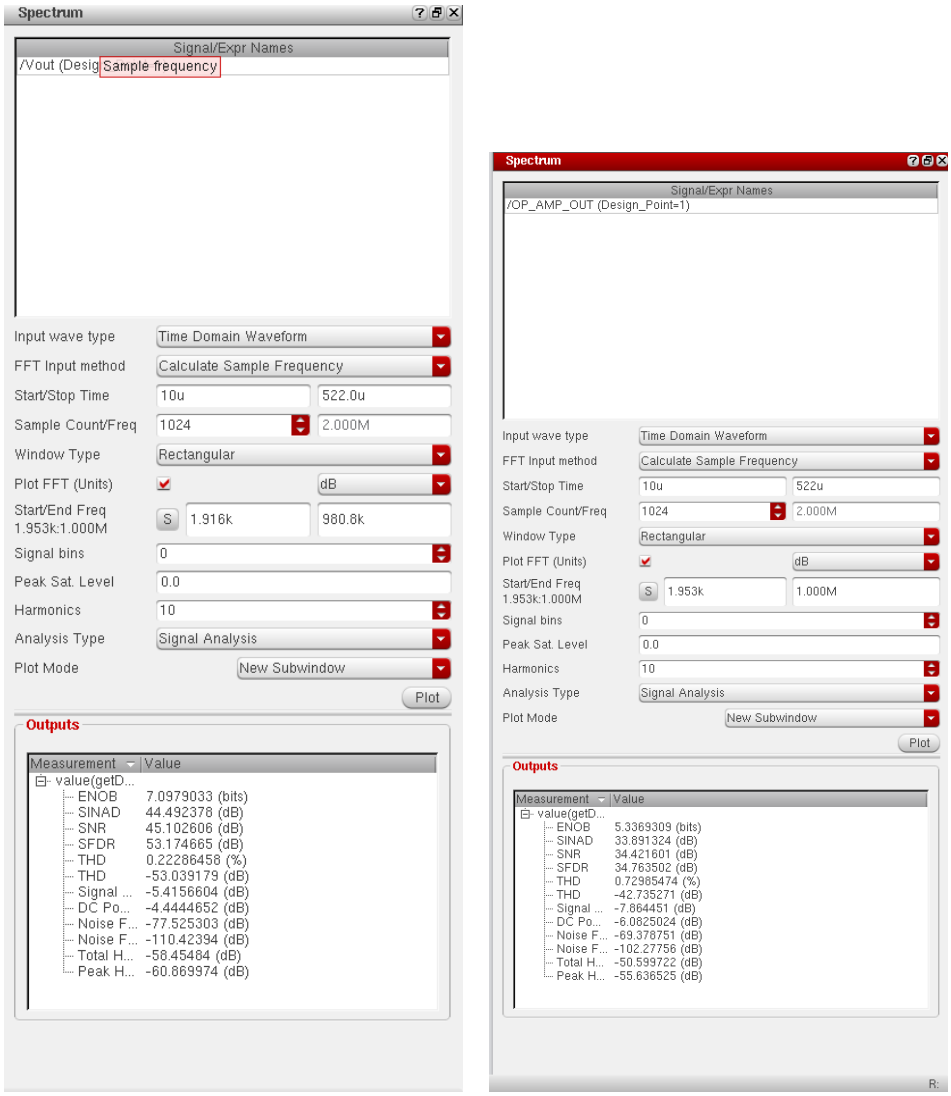
$$F_{In} = \frac{D \cdot F_s}{2^N} = \frac{3 \cdot 1MHz}{256} = 11.71895kHz \tag{10}$$

we get an un-harmonic frequency, which will cause a lot less harmonic distortion. This can be seen on the following page.

The reason we have not given some of the values of the post-layout simulation, is that we did not have time to simulate the netlist with all the parasitics. Even if time was not an issue, the sampling noise at the output would give values that would not accurately describe the DACs behaviour. This is based on the observation that if the sampling noise is removed, the output looks very linear and smooth. As stated earlier, the glitching is most likely charge injection from the transmission gate, as well as clock feed-through from the clock to the hold capacitor.

If you look at the output of the SC DAC schematic, you may notice that the signal becomes more distorted at the higher bits. This is most likely due to some transistors nearing the triode region of operation, thereby the causing the drain current to become less linear.

When it comes to the resistor-based DAC, there are some distinct non-linearities that occur at given times. These glitches comes when the DAC is switching its higher bits, as can be seen that the largest spikes are when the MSB switches.



(a) Resistor DAC spectrum analyzer results

(b) Schemtic SC DAC spectrum analyzer results

Figure 18: Spectrum analyzer results

7 Waveforms

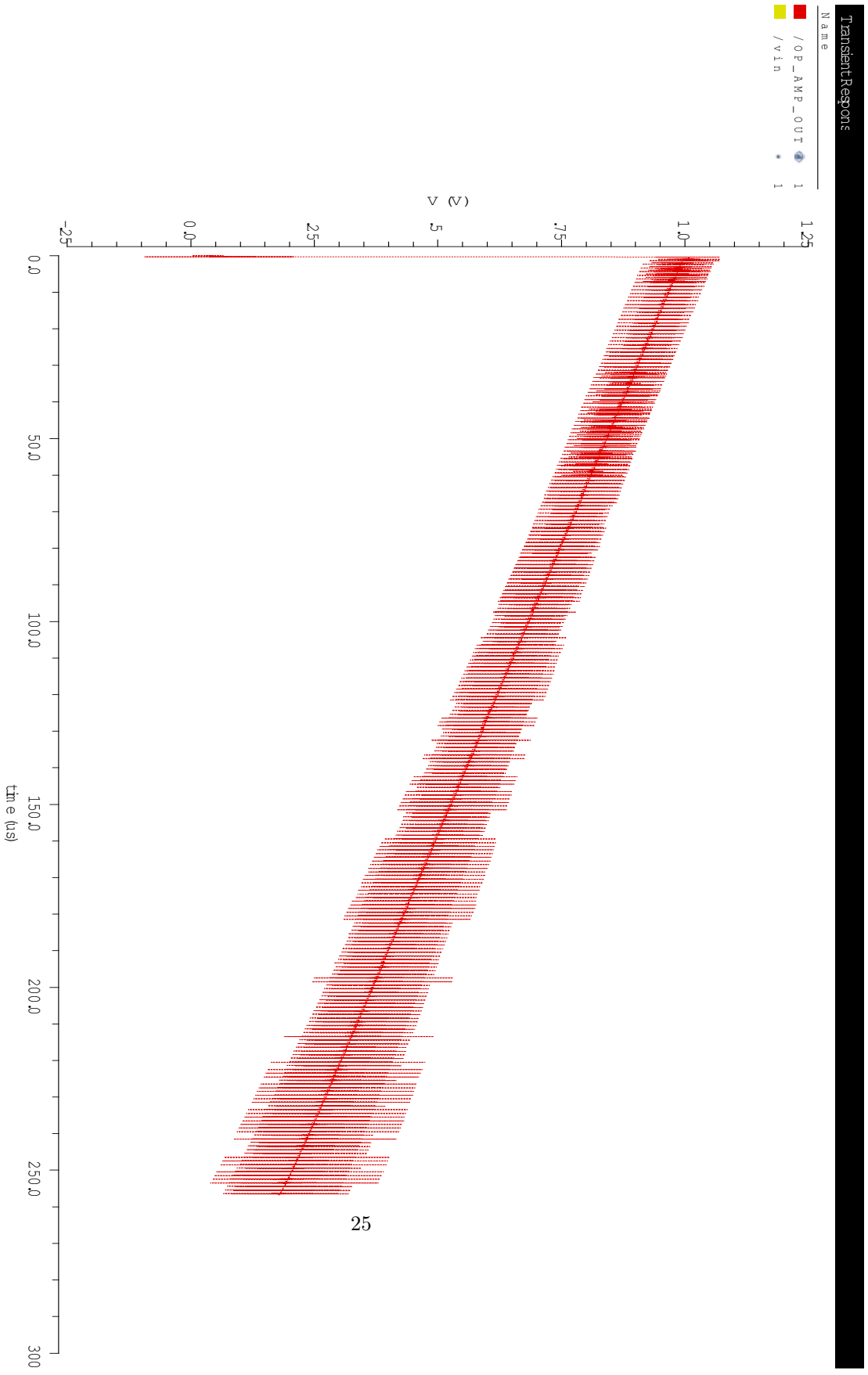


Figure 19: DAC SC post layout simulation, falling direction, with sampling noise

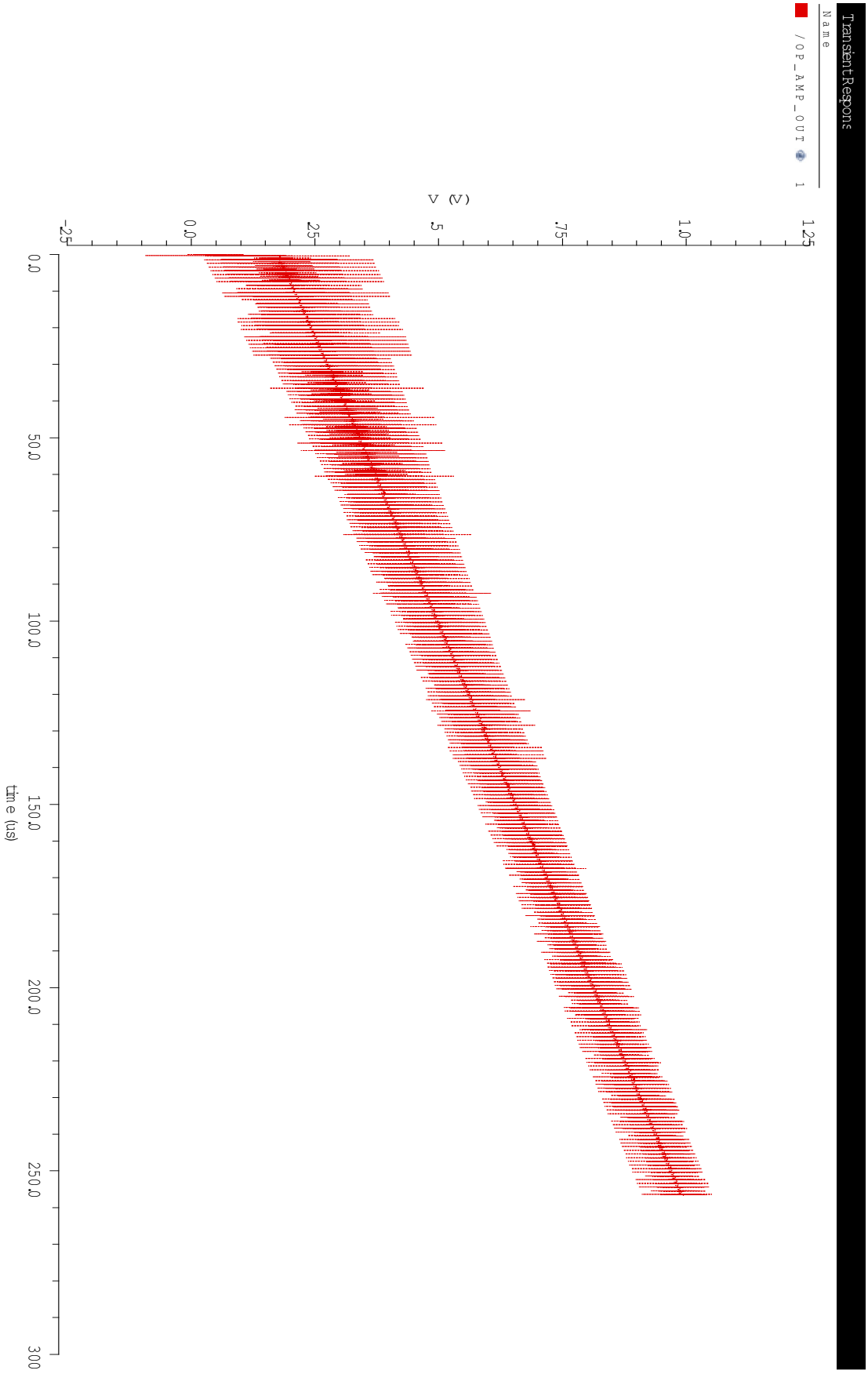


Figure 20: DAC SC post layout simulation, rising direction, with sampling noise

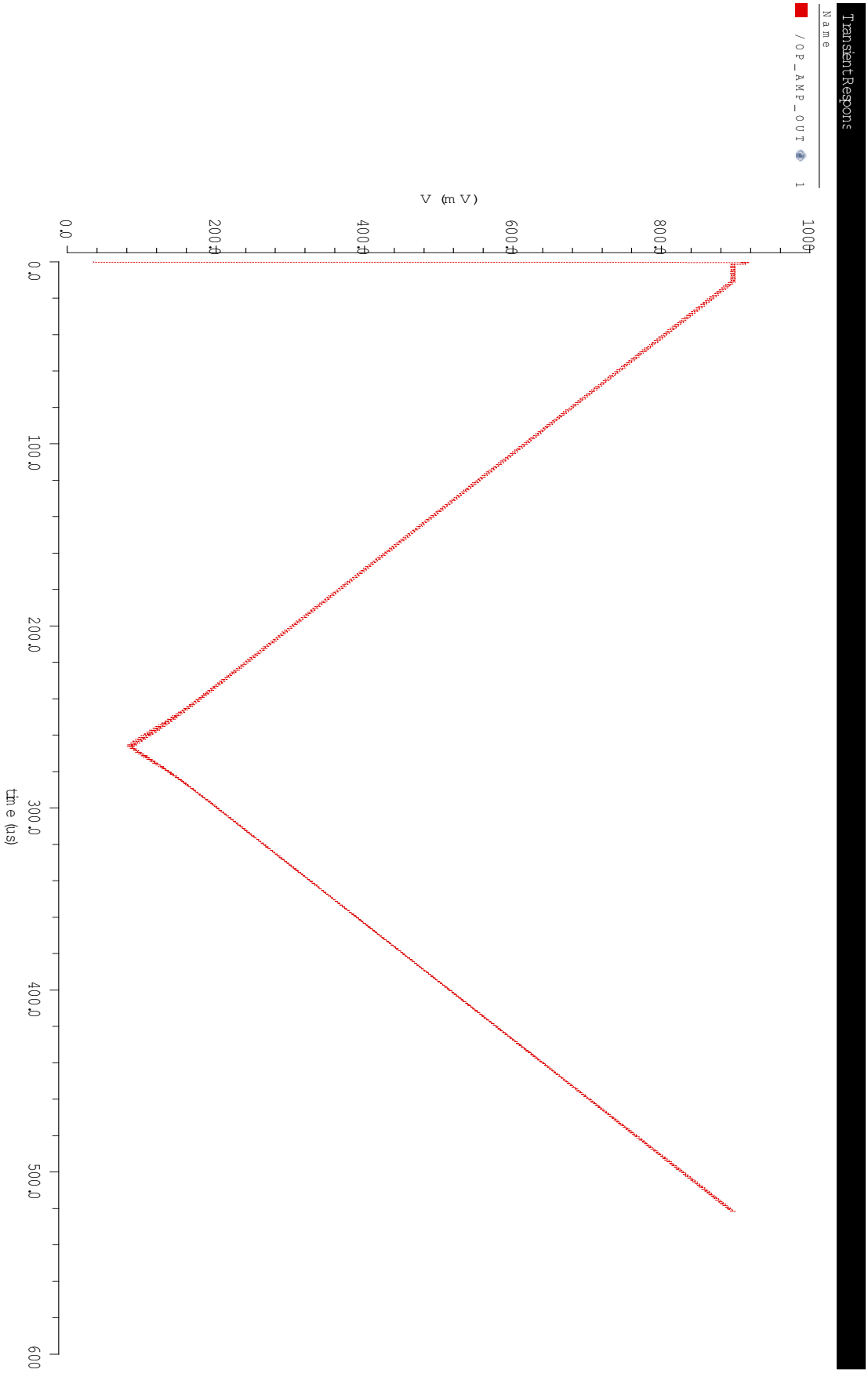


Figure 21: DAC SC schematic simulation

Figure 22: DAC Resistor-Network schematic simulation

8 Sources

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