Digital-to-Analog Converter (DAC)

INF4420 Spring 2018

1 Introduction

Data converters are one of the fundamental building blocks in integrated circuit design. Their purpose is to interface the analog and digital domains. Data converters can be realized in different ways and may be found in a variety of applications. One of them is a **Binary-array Charge-redistribution Digital-to-Analog Converter (DAC)**, shown in Figure 1. This topology uses an Op-amp and a capacitor network to convert a digital signal into an analog signal.

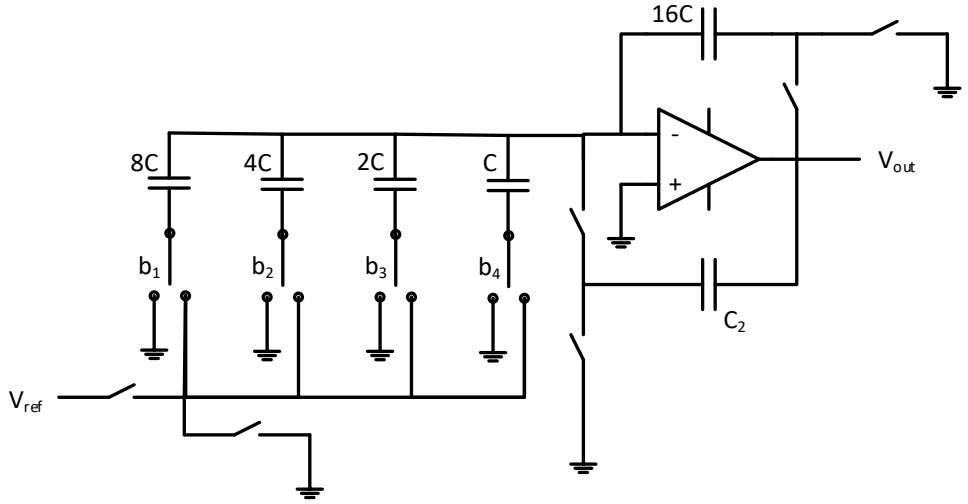

Figure 1: Binary-array Charge-redistribution DAC

2 Project requirements

The main purpose of this project is to design and simulate a Binary-array Charge-redistribution DAC, which meets the specifications outlined in section 3. Other than these specifications, the students have the freedom to choose the methods used to implement the system. The students can work in a group of two as the workload in this project is intended for two students. The group members must read this document completely and carefully assess the task. The work must be distributed almost equally among the members of the group and the same must be mentioned in the final report. PhD students have a slightly requirements, which are explicitly mentioned.

(a) A full schematic for the system and its sub-modules must be drawn. Separate symbol for all sub-modules must be made. The top-level representation should include these sub-modules in a well-organized hierarchical design.

(b) For all modules qualified through schematics simulations, a full physical layout should be made. The sub-modules must be combined into a well-organized layout of the entire system.

It is important to identify and focus the effort on the most critical sub-modules that are most likely to limit the overall system performance.

(c) When combining both analog and digital electronics on a single small CMOS die, the different challenges and potential noise sources must be identified. Based on the assessment of the potential risks, the necessary mitigation must be implemented. The strategies used should be explained in the final report.

(d) Design Rule Checking (DRC) and Layout Versus Schematic (LVS) for sub-modules and the total system must be completed. These checks have to be free of errors. The reports should be enclosed in the final report.

(e) When the layout is ready for sub-modules and system, back annotation of all parasitic components into the schematic must be performed. The full schematic including back annotated parasitic elements must be simulated and the results compared with the simulation without parasitic elements. Comment and explain the results in the final report.

3 Specifications

Assume any other specifications that are not given below.

1. **Binary-array Charge-redistribution DAC**
   1.1. Resolution: 8 bits parallel (**10 bits for PhD students**)
   1.2. Minimum conversion rate: 1 Mega samples/sec
   1.3. Supply voltage: V_{DD} = 1.2 V, V_{SS} = 0 V
   1.4. Minimum Output voltage swing = 0.7 V
   1.5. Maximum DNL = ±1LSB
   1.6. Monotonic

4 Assignments

4.1 Study and understand the functioning of a Binary-array Charge-redistribution DAC

Write a small report (about 2-3 pages) about the Binary-array Charge-redistribution DAC architecture and include the following in your report:

(a) Typical Binary-array Charge-redistribution DAC architecture description and its operation, with a block diagram and waveforms at different nodes in the circuit.

(b) Compare different DAC architectures with respect to their performance, merits and demerits and fill in Table 1.

Table 1: DAC Architecture comparison

DAC types / Attributes	R-2R Resistor network	Binary-weighted Resistor network	Binary-weighted Charge-redistribution	Delta-Sigma
Conversion speed				
Power consumption				
Accuracy				
Resolution				
Linearity				
Area				
Noise performance				
Circuit complexity				
Cost				
Typical applications				

4.2 Design an Amplifier

Use the knowledge gained in Analog Microelectronics course to design and construct an amplifier. Design a test bench to test the amplifier.

4.3 Design of the Binary-array Charge-redistribution DAC

Design a complete Binary-array Charge-redistribution DAC. Design all the required input and output signal lines on the chip, so that your device can be interfaced with the external circuit to build a useful system. Draw the complete schematic diagram.

Assign different digital values to the DAC input and verify that the corresponding analog signals at the DAC output are obtained. Include these observations in the report.

Run the simulations to find the following parameters and include the results in the report.

1) Offset error
2) Full-scale error
3) Integral Non-linearity (INL)
4) Differential Non-linearity (DNL)
5) Effective Number of Bits (ENOB)
6) Signal-to-Noise Ratio (SNR)

7) Dynamic range
8) Total Harmonic Distortion (THD)
9) Operating voltage range
10) Maximum conversion speed
11) Power consumption

4.4 Design of the Binary-weighted Resistor DAC

Design a Binary-weighted Resistor DAC by replacing the capacitor network with a resistor network. Make required changes to the circuit. Run all the simulations that were executed on a Binary-array Charge-redistribution DAC. Tabulate the results and compare their performance.

4.5 Physical layout for Binary-array Charge-redistribution DAC

Make a physical layout for the Binary-array Charge-redistribution DAC. **Please DO NOT make layout for the Binary-weighted Resistor DAC.** Run all the simulations that you executed on the schematic and compare the post layout performance with that of the schematic. Identify the difference in performance and write a report based on your observations.

5 Report requirements

The report should be prepared using LATEX, MS Word or a similar word processor and must document all the different phases of the project. Plots of schematics, layout and simulated results for sub-modules and total system must be included in additions to LVS reports. You must also explain and justify the different choices made for matching, dimensions, implementation of active/passive devices and noise mitigating techniques. The organization of the project and the distribution of responsibility within the group must also be included. In addition, the location of all design files should be listed. Please remember that the report must be considered a stand-alone document that should give the reader a complete view of what you have done. This is important to make sure that the entire picture is included in the final assessment and grading of the project. Please remember to include the references that you used to prepare the report.

Note: DO NOT use “Print screen” to capture the waveforms. Cadence provides a way to capture nice waveforms. In the “Virtuoso Visualization & Analysis” window, select “Graph → Major and Minor Grids” and toggle to disable the grids. This captures a clear waveform. Next, select “File → Print”. In the Print window, select the name of the printer as “Print to File (PDF)”, select the output file path and then select “Options”. In the “Qt-subapplication” window, select “A4” as the Paper and “Landscape” as the orientation. Adjust the margins if you like. Click “OK” to exit window. Finally, select “Print” to print the waveform.

6 Assessment

This project counts 40% towards the final grade.

7 Milestones and deadline

To ensure a good progress during the project period and that all groups completes the project within the deadline certain milestones must be met. The students are responsible to meet the deadlines and to get the necessary approval. The milestones are:

08.03.2018 - A short description (2-3 pages) on how you understand this assignment and how you plan to solve it. Include a detailed block diagram and the input and output waveforms of the complete ADC (Task 4.1).

03.05.2018 - Design and simulations for the entire circuit should be completed for both schematic and layout. The system performance should be demonstrated with simulations and approved by the lab teacher (Tasks 4.2 – 4.5).

11.05.2018 - The project should be completed and the final report submitted.

8 Resources

8.1 Books

(a) The Data Conversion Handbook by Walt Kester (http://www.analog.com/en/education/education-library/data-conversion-handbook.html)
(b) Mixed Signal and DSP Design Techniques by Walt Kester (http://www.analog.com/en/education/education-library/mixed_signal_dsp_design_book.html)
(c) Data Converters by Franco Maloberti
(d) CMOS: Mixed-Signal Circuit Design, 2nd Edition by R. Jacob Baker
(e) CMOS Circuit Design, Layout, and Simulation, 3rd Edition by R. Jacob Baker
(f) Analysis and Design of Analog Integrated Circuits, 5th Edition by Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer
(g) Design of Analog CMOS Integrated Circuits by Behzad Razavi
(h) CMOS Analog Circuit Design, 3rd Edition by Phillip E. Allen, Douglas R. Holberg

8.2 Application notes, White papers & Data sheets

(a) www.analog.com
(b) www.maximintegrated.com
(c) www.ti.com

(d) www.nxp.com

(e) www.st.com

8.3 Research papers

(a) ieeexplore.ieee.org

(b) www.sciencedirect.com

Wish you all the best :)