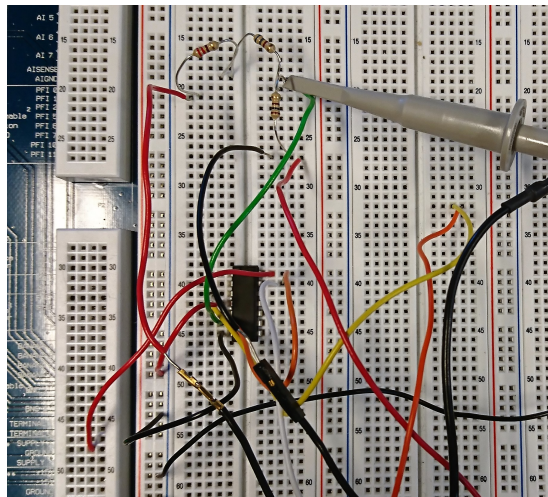


INF3410

Common source amplifier

LAB 2
HENRIKTK
HENRIKLG
SEANAH



Henrik Torland Klev
henriktk@student.matnat.uio.no

Sean Andre Hansen
seanah@student.matnat.uio.no

Henrik Løland Gjestang
henriklg@student.matnat.uio.no

Dato: October 16, 2017

Contents

1	Single PMOS versus common source amplifier	2
2	Input voltage sweep with constant V_{NBias}	3
3	Bias voltage sweep with constant input	6
4	Amplifier frequency dependency	10
5	Formulas used	15

1 Single PMOS versus common source amplifier

The intrinsic gain of a PMOSFET is given by

$$A_o = -g_m r_o$$

Whereas the transconductance is given as

$$g_m = \frac{2I_D}{|V_{OV}|}$$

and the output resistance is

$$r_o = \frac{V_A}{I_D}$$

The gain, A_v , that we expect in this task can be found by calculating

$$A_v = -g_m(r_{o1} || r_{o2})$$

and since the output resistance is assumed to be equal for the PFET and NFET, the equation can be simplified to

$$A_v = \frac{-g_m r_o}{2}$$

These functions will result in A_v being half of the intrinsic gain. Since A_v is half, we expect a gain plot of A_v similar to the gain plot of A_o .

We could have found an approximation of the relationship between A_v and A_o if we had close to the correct values of $k_{n/p}$, but as this parameter is largely dependent on the fabrication process, it is difficult to produce multiple transistors with the same $k_{n/p}$ values.

2 Input voltage sweep with constant V_{NBias}

In this part of the exercises we are using a common source amplifier to find the gain in a range around the linear region. We will be using a bias current I_D of $5\mu A$ supplied by the NMOSFET, then sweep the input voltage from gnd to V_{dd} and plot the output curve. From the linear region of this plot we can calculate the maximum gain A_V (equation 1 in formulas), both as a linear number and in dB (equation 2), by finding the approximation of the biggest derivation of the graph.

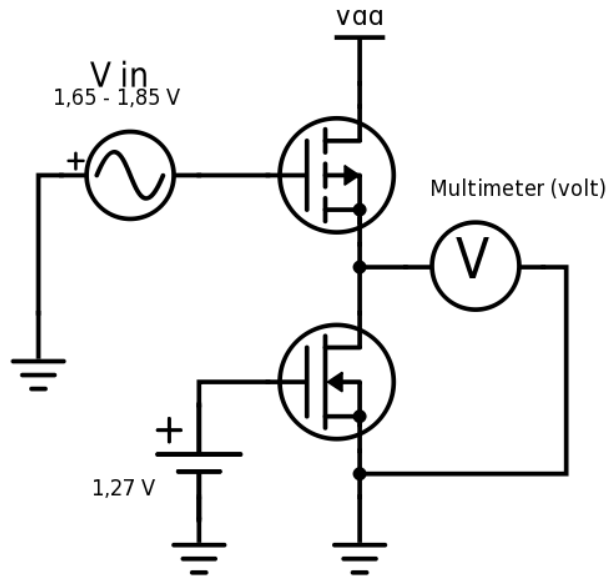


Figure 1: The circuit we used for sweeping the gate of the PMOS

By using the graph of different I_D given an input V_{NBias} we found that $I_D = 5\mu A$ when $V_{NBias} = 1.27V$. By setting a $V_{DD} = 3.3V$ and $V_{SS} = gnd$ we could then sweep the gate of the PMOS from 0V to 3.3V. After sweeping the region from 0V to 3.3V, we noticed that the linear change was happening within the region of 1.65V to 1.85V. To achieve good resolution of our plot, and to get several measurement points in the linear region, we used steps of 1.0 mV for the input voltage.

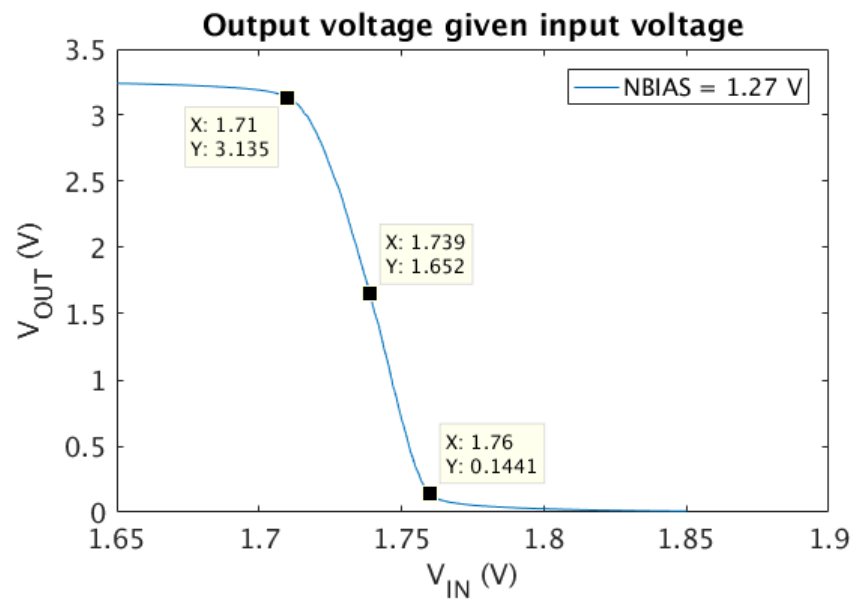


Figure 2: Output (V) given Input (V)

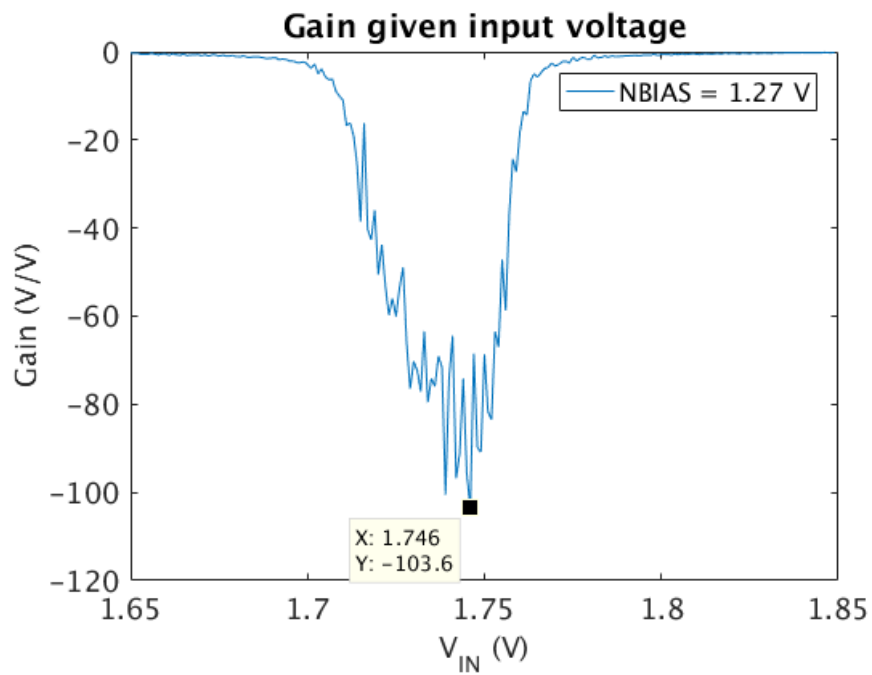


Figure 3: Gain given Input (V)

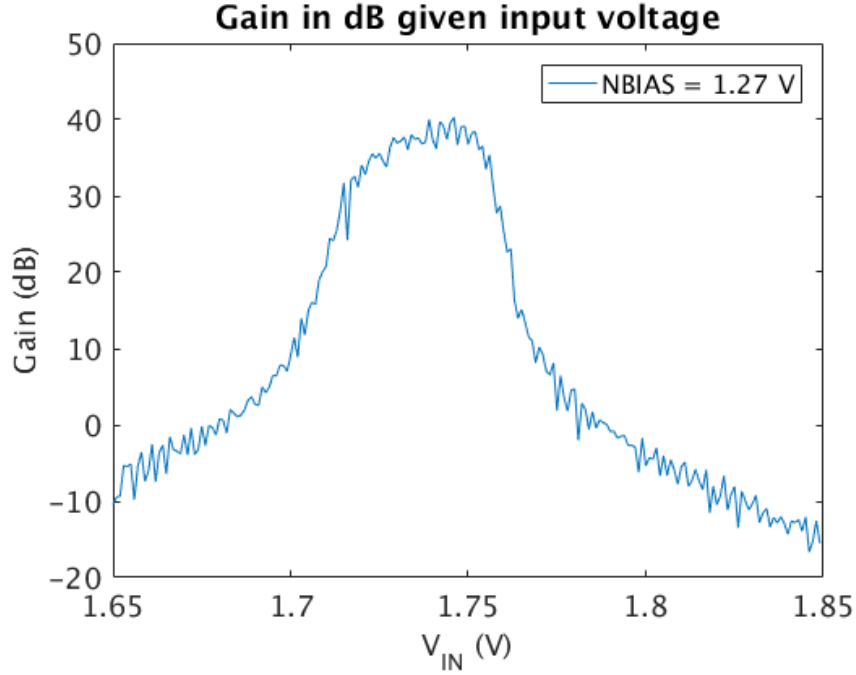


Figure 4: Gain in decibel given Input (V)

As we can see from the plot, we did not need to use a resistive divider to generate the plot around the linear region, as the voltage source gave us sufficient voltage steps. When using a MOSFET as an amplifier, there are 3 important points to consider, which are referred to as A, B, and Q. The MOSFET is operating the active mode/linear region between points A and B, while point Q, the quiescent/bias point, marks where highest possible gain is achieved.

In figure 2 we have marked three points: A (left-most), Q (middle), and B (right-most). Point Q is in the middle of the linear region at approximately $V_{OUT} = \frac{V_{DD}}{2}$. This is the location in which the gain should be at its highest value. When calculating the derived (equation 1) graph in figure 3 we see that the gain is higher in a different point. This is most likely due to our choice of V_{in} . We would have achieved a more accurate representation by using smaller intervals, which could have been obtained by incorporating a voltage divider on the input. We could also have used a higher V_{DD} . This would have ensured a greater change from V_{DD} to ground, and, in turn, would achieve a larger interval for measurements.

3 Bias voltage sweep with constant input

To ensure we are able measure data points from both weak and strong inversion of the NFET, we regulate the V_{NBias} to be in range 0V-2V. Then, by regulating the voltage on the gate of the PFET from 0V-3.3V, we will be able to observe how the linear range change for different V_{NBias} (figure 6). If we then derive (equation 1) the output voltage, we will achieve the gain from each of the different V_{NBias} , shown in figure 7. By then plotting the gain for the different V_{NBias} , against the I_D in each of these points, we will get the plot of figure 8 that shows the operational region of the circuit.

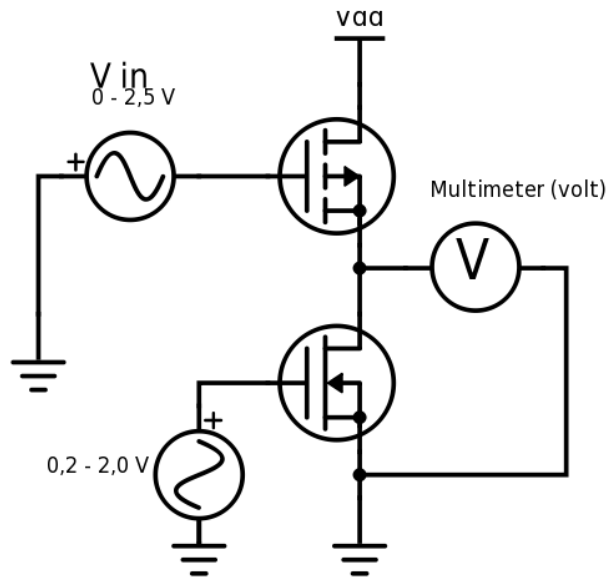


Figure 5: The circuit we used for sweeping the PMOS and NMOS gates

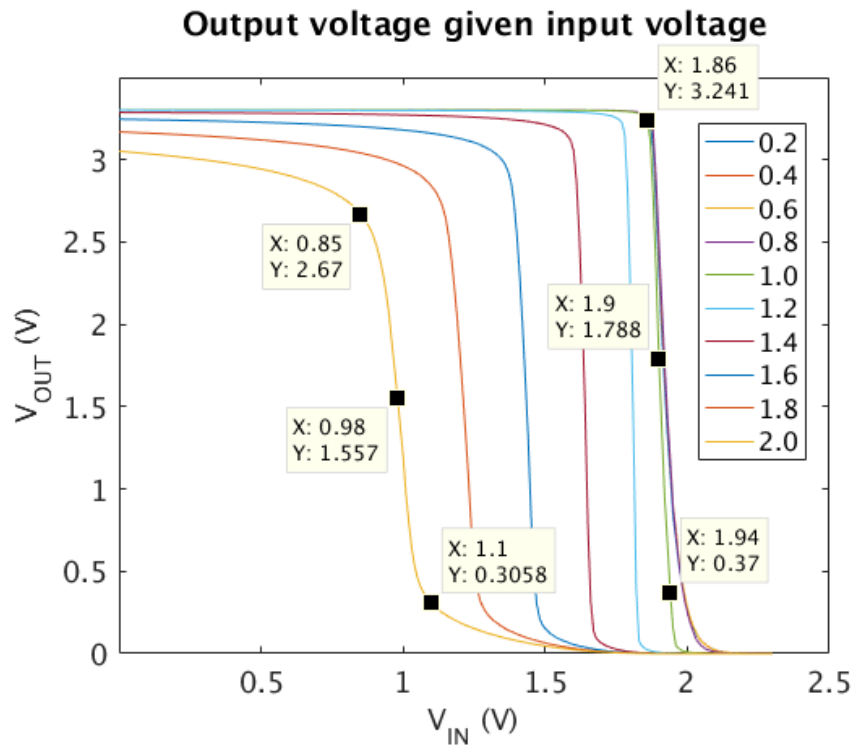


Figure 6: Output voltages for different values of V_{NBIAS} , where the V_{NBIAS} varies by 0.2V for each loop of V_{in}

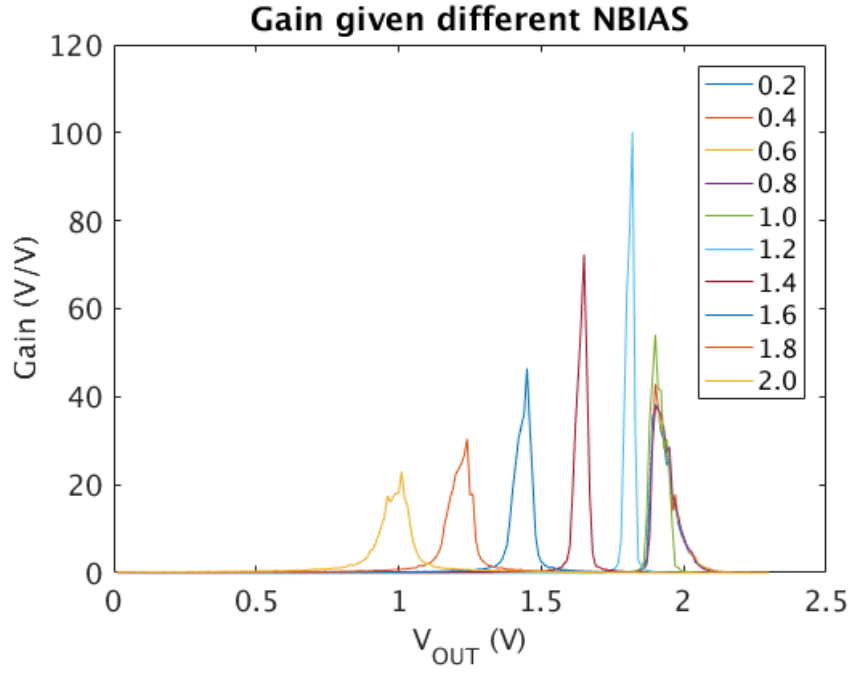


Figure 7: The gain achieved by deriving (equation 1) the results from figure 6. Each graph is a different V_{NBIAS} given in volts, with respect to legend.

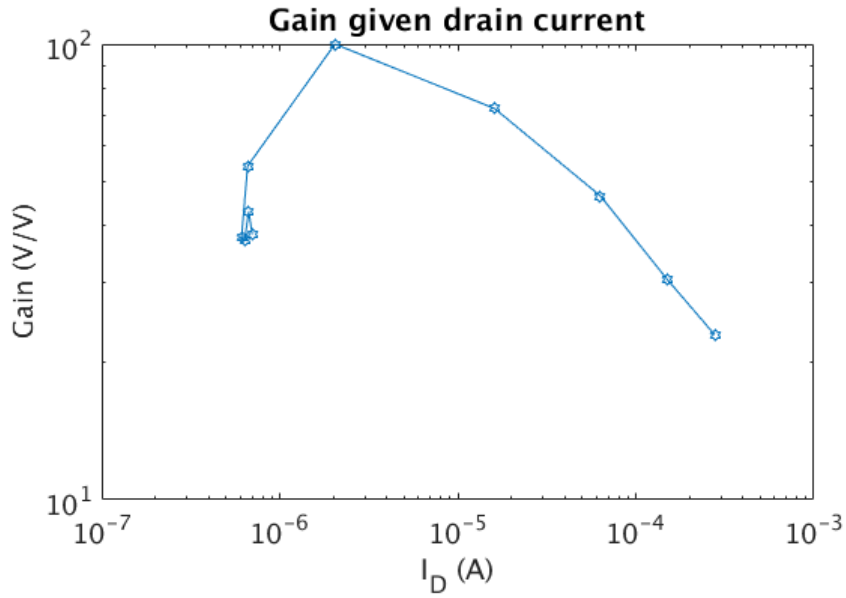


Figure 8: The gain from figure 7 versus the I_D for each V_{NBIAS}

We have in total 10 different measurements of V_{NBIAS} , of which 5 are in weak

inversion, below threshold voltage of 1.02V, and the other 5 in strong inversion, above V_{tn} . In figure 7 we see that the highest maximum gain is achieved with V_{NBias} of 1.2V, but this is likely due to our choice of steps being too large because of time constraints. By observing figure 8, we notice that our curve resembles the curve given in the task for the values above the cut-off. The values below the cut-off vary from the given curve. We could have achieved a closer resemblance if we had chosen a smaller step, but did not have enough time to use a smaller step size. We could also have applied a larger range of V_{NBias} to create a more accurate representation.

The gain of the circuit is affected by a couple of factors. One of the key factors, is the positioning of the measured points; a large difference in points equates to a smaller max gain. Another factor is the choice of V_{NBias} . By choosing a V_{NBias} in the weak inversion region, we achieve a large gain; choosing a V_{NBias} closer to V_{DD} achieves a smaller gain. If we had chosen a larger V_{DD} , we would have achieved a more exact gain. This is due to the gain occurring over a larger interval. We could have achieved a better representation of the gain compared to the I_D , by choosing more V_{NBias} . By choosing more V_{NBias} values, we could also achieve the gain of the amplifier to be at a value closer to V_{tn} . Choosing V_{NBias} closer to 0 could result to a cut-off in the NFET. This could lead to an error in the gain, due to the signal using more time to move from V_{DD} to gnd. Since the equipment would show varying results for a single measurement of V_{NBias} , we could not be certain that the values read were the exact values. The intrinsic gain varies based on the amplifiers transconductance parameter K_n , meaning the gain will vary between transistors. Since the gain is not equal for each transistor, we achieve a lower or higher gain depending on the transistors we choose.

4 Amplifier frequency dependency

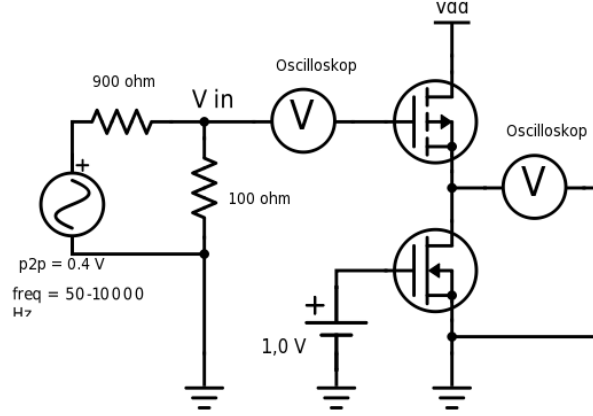


Figure 9: The circuit used for finding frequency threshold, this time with a resistive divider to provide more fine-grained input to the amplifier.

By analyzing the graph for I_D given a V_{NBIAS} , we can find the V_{tn} to be approximately 1.02V. Since our V_{NBIAS} varied between 0.2V and 2V in task 3, we will be using the graph for $V_{NBIAS} = 1.0V$ for this area. In figure 6 we observe that the linear range is between 1.86V - 1.94V, while the midpoint of the linear region is 1.9V. By sweeping the input V_{in} in this region, we can measure the V_{p2p} difference between the signal input and the signal output. The difference in input and output peak-to-peak will be equal to the gain in this region. To get the phase shift of the signals, we can check the shift in signals using a point on the input signal, and a point on the output signal.

When applying a sine wave with $V_{p2p} = 400mV$ to the input, the noise from the voltage divider distorts the signal. This causes the oscilloscope to read the input wave as having $V_{p2p} \approx 300mV$. Ideally the setup of the voltage divider should be dividing the input signal by a factor of 10, so $V_{inp2p} = \frac{V_{p2p}}{10} \implies V_{inp2p} = 40mV$. The noise could be reduced by adding a small capacitor that's connected between v_{IN} and ground. We can also remove the noise on the Oscilloscope by using the average function which is built in.

When measuring phase shift, we first tried to automate the process by controlling the oscilloscope through matlab. This did not work out the way we expected, as the oscilloscope was unable to measure phase shift for several of the frequencies, most likely due to distortion in the signal and/or noise as seen in figure 11. To get a more correct result, we decided to embrace a more manual approach. This process involved setting the frequency of the input signal to different values using Matlab, starting low before increasing. Then, for every frequency, use the oscilloscope to calculate the phase-shift of the average signal value as seen in figure 12. The frequencies used can be seen in figure 14.

We have chosen the frequency base of $2.6 * 10^n$ due to the cut-off frequency

of -3db (equation 2) being at 2600Hz. This indicates that the phase shift would be changing from 260Hz to 26kHz, as the output signal is an inverted signal compared to the input. The phase shift is supposed to lie at approximately -180° at any frequency below 260Hz. Since we only have one breakpoint, we can also assume that the phase shift will be 90° . Looking at the graph in figure 14 we can see the phase vary from -166 to -77. This gives us a phase shift of 89° , which is relatively close to 90° . Some of the possible errors in this task could be contributed to the factors discussed in task 3.

We can conclude task 4 by specifically answer the questions stated.

Is the output amplitude indeed A_V times bigger than the input?

This answer is yes when you take the average of the input signal, thereby reducing noise. This can be seen in figure 12. When you observe the noisy signal in figure 11, we see that the oscilloscope has trouble calculating V_{p2p} . This causes the output to be about 4 times larger than the input, instead of the expected 20 (found from figure 13).

Can you detect the frequency at which the output starts to become smaller?

This answer can be seen from the figure 13, where we see the gain starts to become smaller at around 960 Hz.

At what frequency do you observe a -3dB decrease in the original output swing?

Figure 13 shows this point is at 2600 Hz. The formula used to calculate this number is used seen in equation 2 at the last page.

What's the phase of the output relative to the input?

Figure 14 shows the phase-shift in the output relative to the input for a given frequency.

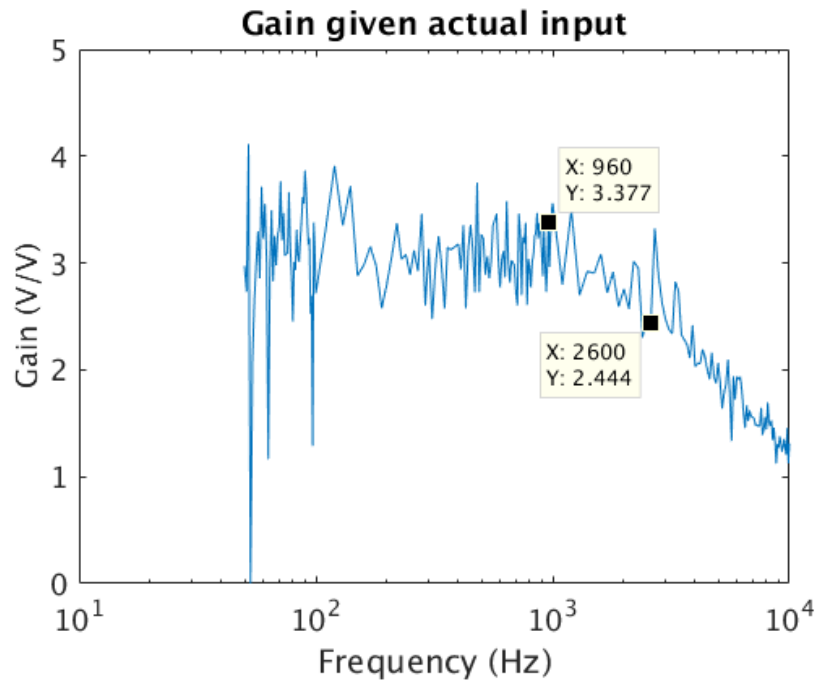


Figure 10: Gain measured when comparing the V_{p2p} of the input and output signals

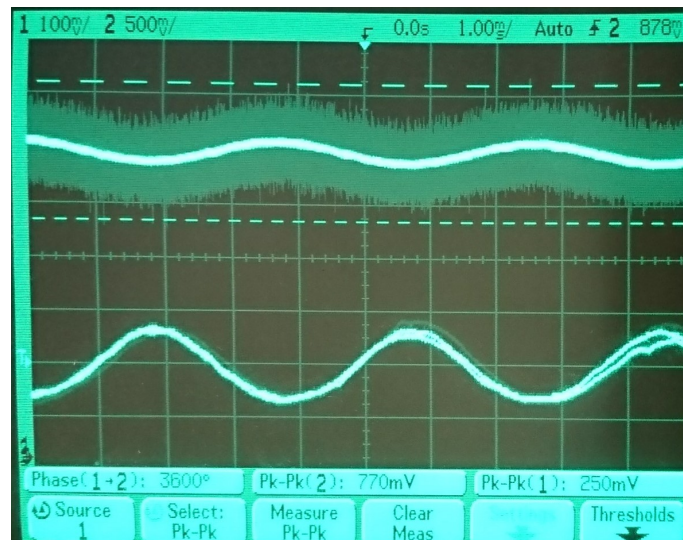


Figure 11: Picture of oscilloscope with V_{in} at channel 1 (above) and V_{out} as channel 2 (below), with ambient noise/distortions in signals.

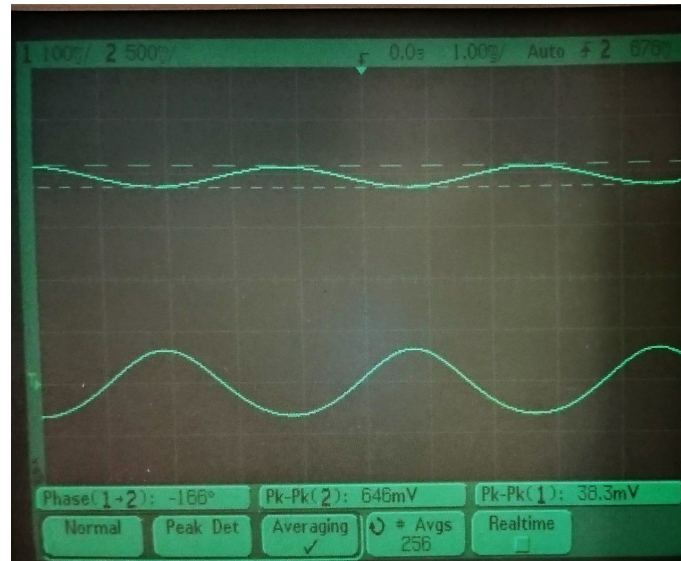


Figure 12: Picture of oscilloscope with V_{in} at channel 1 (above) and V_{out} as channel 2 (below), using the oscilloscope's 'average' function.

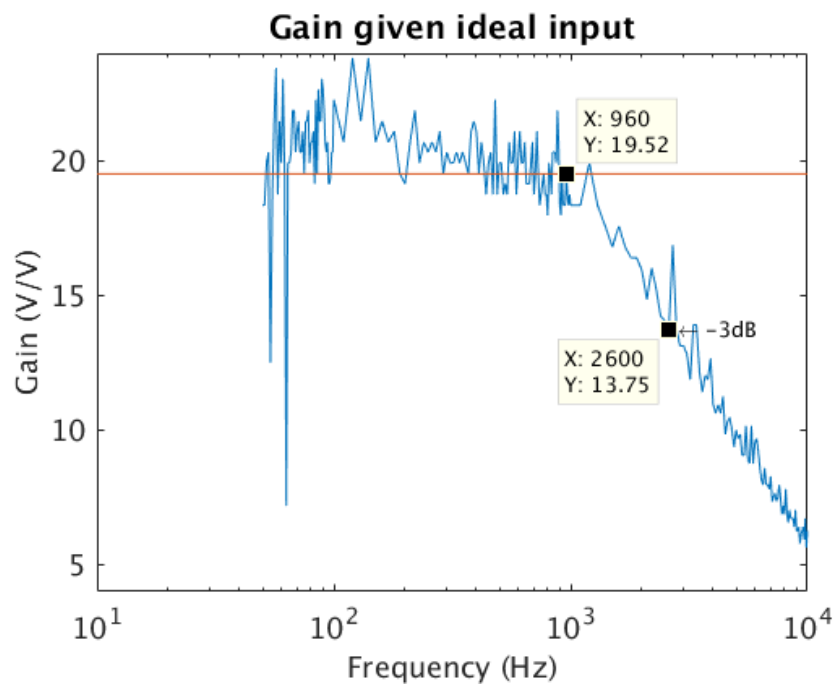


Figure 13: Gain calculated when assuming the $V_{p2p} = 40mV$ on the input

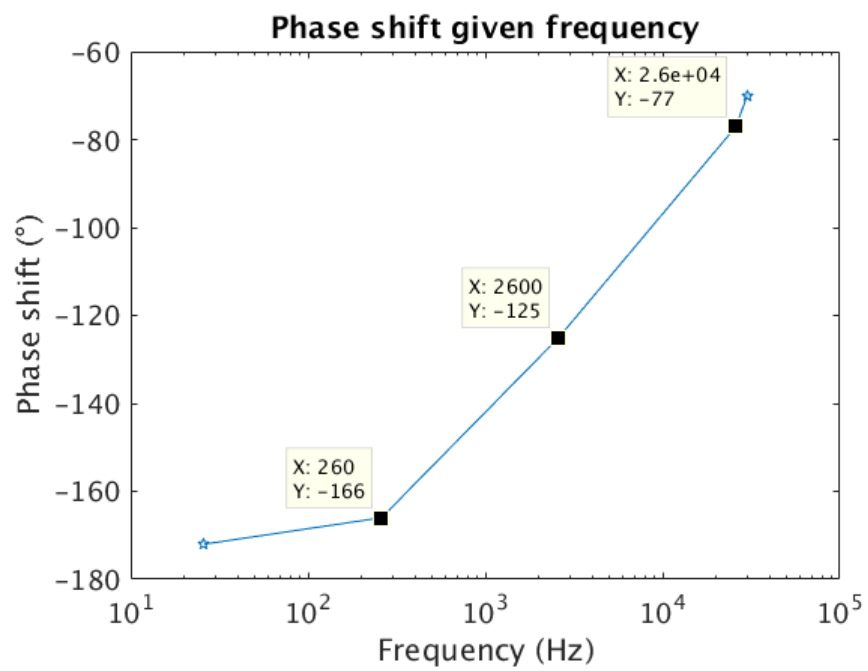


Figure 14: Phase shift of the input vs. the output signal

5 Formulas used

Formula for finding derivative:

$$A_v = \frac{\Delta y}{\Delta x} = \frac{y(i) - y(i+1)}{x(i) - x(i+1)} \quad (1)$$

Formula for decibel conversion

$$A_v dB = 20 \cdot \log(A_v) \quad (2)$$