INF3410, fall 2017, mandatory labratory exercise 3: The Miller Effect (deadline 07-Nov-2017, 10:00!)

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Abstract

This third lab task is meant to give hands-on experience with an important limitation to bandwidth in analog amplifiers and speed in digital gates: the Miller Effect.

Please refer to lab 1 for **Safty Rules** and general rules of conduct in the lab!

1 Graded Mandatory Group Assignments

Note that this is part of the courses exam and strict rules apply as described in the document http://www.mn.uio.no/ifi/english/studies/admin/mandatory-assignments/index.html. The page explains the significance of mandatory assignments in a course and in particular group assignments. It also specifies your responsibility to not plagiarize anybody else's work and that you are required to conduct and understand your own experiments and obtain your own results, while you are still allowed and encouraged to exchange advice and experiences also between groups.

Each group must deliver a written lab report using the Devilry online submission system **before** the **hard** deadline indicated in the title. Note that you can submitt multiple times and the last submission before the deadline will be graded, so it might be a good idea to plan to submit preliminary versions well before the deadline. The points given for this lab assignment will be weighted as 20% of the total score of the course. Together with the mandatory lab exercise 3 this score will cont 40% towards your final grade.

Each task is labeled with how many points it will contribute towards the score.

2 Requirements for the Lab Report (read carefully!)

You are required to execute the tasks and answer all the questions posed below and to submit a report on your work. The report needs to be explaining clearly what you have done, how you have done it, what the results were and what you conclude from them. Make sure to answer all questions! Supply the report with drawings of the circuits (including the values of the components and parameters you used where appropriate, e.g. bias voltages/currents, component sizes etc.) and measurement setups, and show your measurements in graphs! Use labels in the schematics that you draw, such as M_1, M_2 (M is often used fro labelling CMOS transistors), $opamp_1$, I_1, V_1 etc. You should then use those labels in your text, since it is much easier to write: 'transistor M_1 in figure 1' than 'the transistor third from the top and second from the left in the righthand side circuit in figure 1'. **MANDATORY**: Include a photograph of your circuit into the report!

3 Introduction

Bandwith and gate delay are related performance concepts from the analog and digital circuits world respectively. They are both affected by limits in current magnitude and capacitive loads. While parasitic capacitances towards DC potentials all over integrated circuits are bad for the the performance, it is capacitance not to DC potentials but those between nodes that are driven in opposite directions that can be make even small capacitances into a real problem.

In our lab we must be very careful when setting up and carrying out our measurements! Be sure to follow the safety instructions indicated in lab 1!

4 Tools

- **Capacitors**
  In the lab there are only ceramic capacitors available, so please use only those. In contrast to tantal capacitors, ceramic capacitors can be operated at any voltage polarity accoss them. You are NOT allowed to bring in tantal capacitors or use anything else but the ceramic capacitors available in the lab. A huge negative voltage over a tantal capacitor can burst the capacitor physically and endanger eyes and skin of people nearby.

Please refer to labs 1 and 2 for indtroductions to the other previously introduced instruments and tools:

- **The NI-ELVIS bord and plug-in bread bord**

- **MATLAB**
- **GPIB interface**
- **Voltage sources**
- **Multimeters**
- **Oscilloscope HP54622D**
- **An Agilent 33250A wave form generator**
- **CMOS transistors**
- **Potentiometer operated as tweakable voltage source**

Always clean up the lab after your time slot, such that the next group can use the equipment!

5 General Advice

- Draw a schematic before you start assembling components on the PCB! Label pins on the PCB and in the schematics (!) clearly in order to keep your overview. Debuging will be much, *much* easier that way!
- Come to the lab with a work plan: Read the entire lab task beforehand and make a plan how to proceed. Put yourself a goal for a lab session. Read the relevant book chapters in order to understand the entire lab. Be ready with questions already before the lab if there are still things unclear.

6 Miller Effect in CS Amp

Task 1 (2p): The first experiment shall be almost the same as you have already performed in lab 2. Before we get to implement the circuit in figure 1 B) we shall modify the CS amplifier of lab 2 by first placing the capacitor C_{MILLER} NOT LIKE IN THE FIGURE, but between output v_O and Gnd in parallel with the scope probe capacitance C_{SCOPE}. However, you should already add the resistor R_S in series at the input between your waveform generator and the PFET. However, in order to get small enough swing of v_G you need to employ the same resistive division as in lab2 (1 A)) to implement the equivalent Thévenin circuit (v_I with R_S in 1 B)). Can you choose the correct magnitude of resistors R_1 and R_2 in the resistive divider to get the desired Thévenin output resistance $R_S = 10\text{k}\Omega$? What is the relationship between v_I' and v_I and what will be the relationship between the small signals v_i' and v_i (compare lab 2)? Choose $C_{MILLER} = 15pF$, i.e. about the same as C_{SCOPE}. Use the same bias

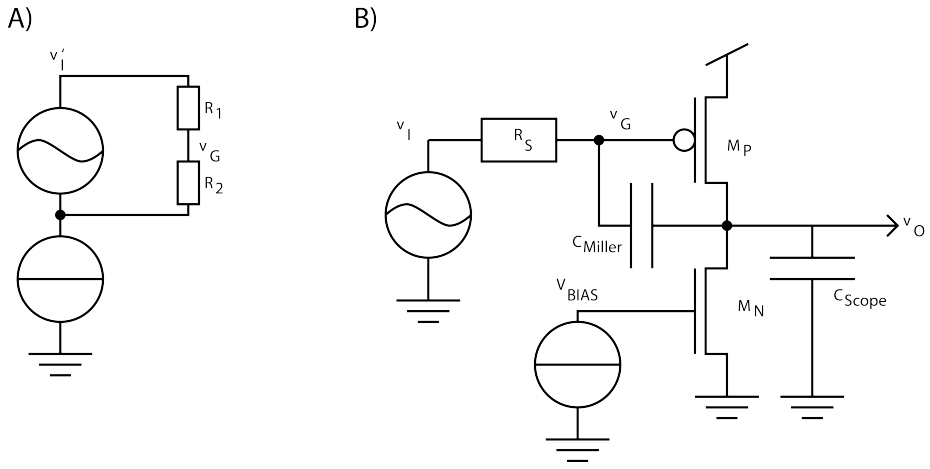

Figure 1: A) resistive divider (like in lab 2) for generating v_g with appropriate Thévenin resistance R_S. B) CS amp with explicit Miller capacitor and series resistance emulating a source resistance from the waveform generator.

setting for V_{BIAS} as for Task 4 in lab 2. As a sanity check produce a plot like in task 2 of lab 2 for v_O by sweeping v_I. The DC gain that you can measure this way should still be the same as in lab 2, right? Please write down the measured gain A_V once again.

Task 2 (2p): With the setup in task 1, also produce a Bode-plot and determine the -3dB frequency, i.e. bandwidth (BW). It should be smaller than the one measured in lab 2 because of the added capacitance. Please verify and document this. NOTE: we are now interested in the relationship $\frac{v_o}{v_i}$ for the bode plot, but you cannot measure v_i at node v_G. Instead you need to observe v_I' and use the relationship to v_i that you deduced in task 1.

Task 3 (4p): Now move C_{MILLER} to actually be a Miller capacitance between v_G and the output node v_O. Repeat both: your plot where you sweep v_I and the Bode plot. You should observe a significant reduction in BW, even though the total capacitance and resistance in the circuit is still the same. Can you use C_{MILLER} and A_V to express how much reduction in BW you actually expect and compare this with your measurment results?