INF3410

The Miller Effect in CS amplifier

LAB 3

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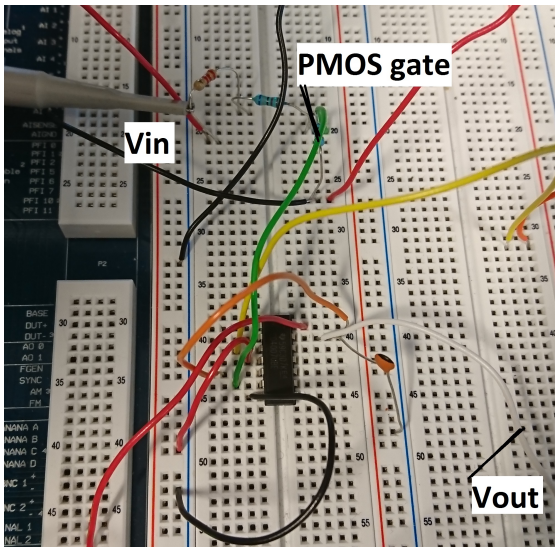
SEANAH



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1 Comparing results with previous lab

We have throughout this lab chosen to keep V_{DD} at 3.3 volts to be able to compare results with previous lab exercises, although at the cost of having less accurate results. We changed the resistive divider (R_S) from Lab 2, to achieve the same relationship between V_I' and V_I (1:10) while making R_S 10kΩ. This was done by choosing resistors equal to the ones in figure 1, which is the setup for this task. First we did a DC sweep at the PMOS gate, while VBIAS was set to 1.0V (the equivalent of the chosen VBIAS in lab 2). According to the task we were supposed to achieve the same results, with respect to DC gain, as from Lab 2. However, we expect the max gain to be different in some aspect, as the added capacitance C_W will affect the output (As seen in figure 4 and 5). We found that, with and without, the capacitance C_W the DC gain was at approximately A_v = -24 (V/V) as seen in figure 3.

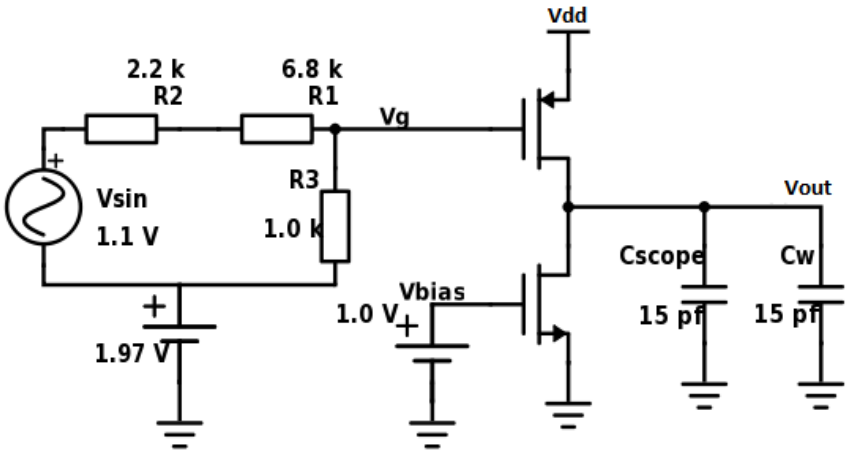

Figure 1: Circuit setup for task 1 and task 2

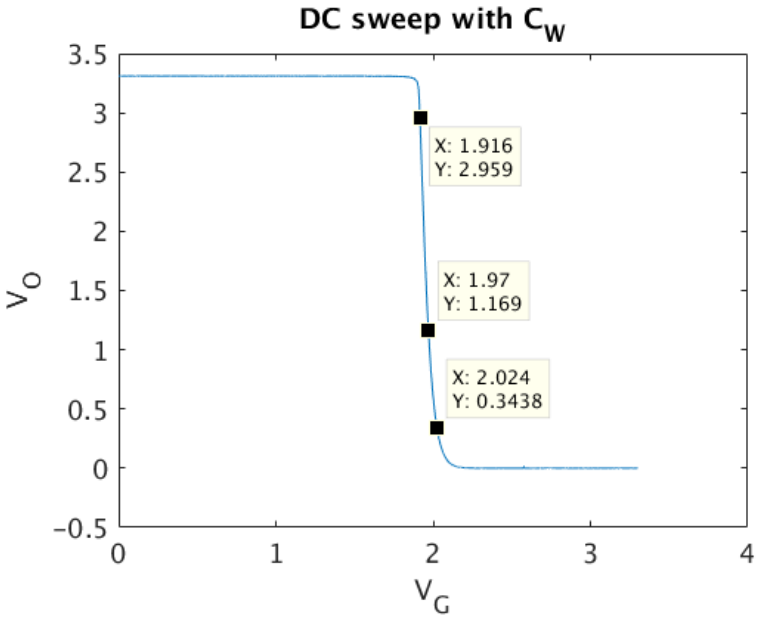

Figure 2: DC sweep at PMOS gate with added capacitance (measured). V_{BIAS}=1.0 V

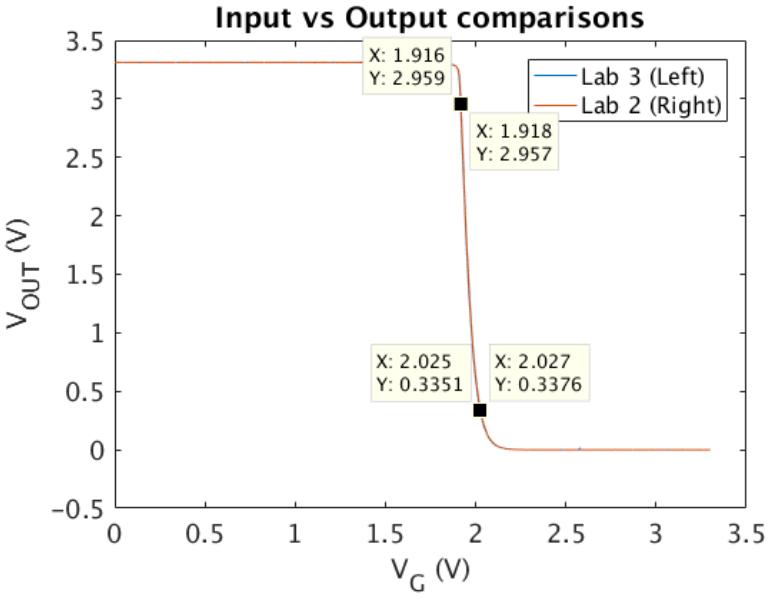

Figure 3: Comparison of DC sweeps with (left) and without (right) added capacitance (both measured). V_{BIAS}=1.0 V

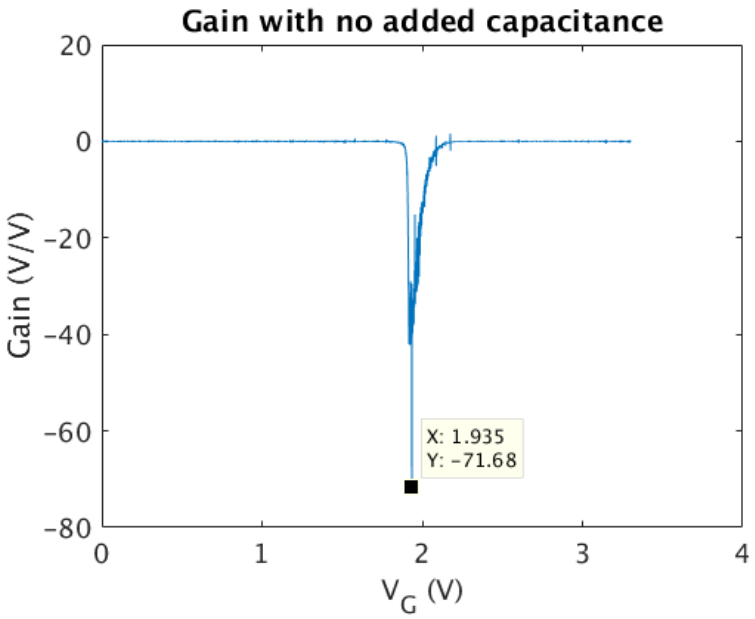

Figure 4: Gain given no added capacitance (calculated from DC sweep measurements)

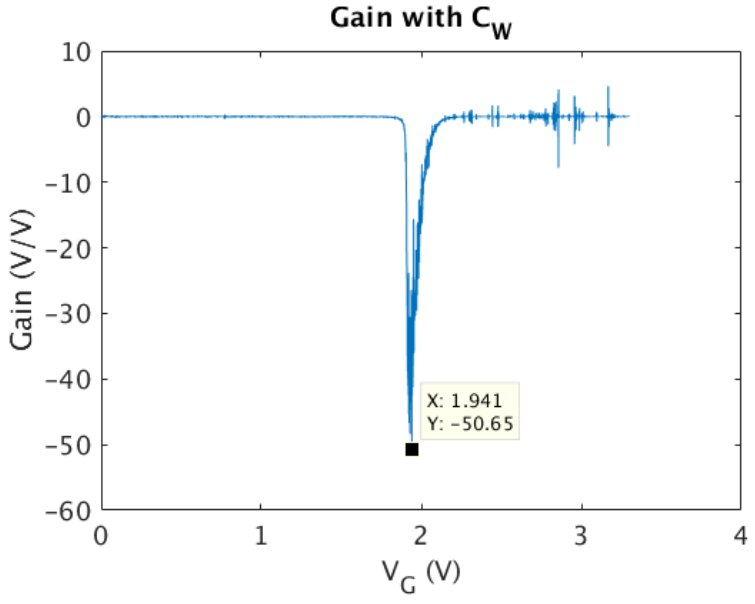

Figure 5: gain given added capacitance between V_{OUT} and ground (calculated from DC sweep measurements

2 Amplifier with capacitance to ground

Here we expected a decrease in bandwidth. In Lab 2, we noticed that the BW was over 2KHz, but after adding the extra resistance and capacitance, the BW dropped to 500Hz. We assumed this drop was a bit large, and proceeded to measure the BW of the circuit without the capacitance to ground. The rough measurement of BW can be seen in figure 8. We have unfortunately achieved a change in BW on our transistor. Since the BW has fallen to 900Hz instead of 2.6KHz as in our previous lab, the fall to 500Hz when adding the capacitance doesn't seen too large. If we had more time, we could replace the transistor, and retrieve new measurements, as it seems the transistor has become faulty. If the transistor is not at fault, we could have achieved a break in one of the wires in our circuit. Other possible faults can be seen in Section 5.
Because of the restive dividers, the relationship between v_I' and v_I is 10:1. Therefore, while calculating gain, we divide our input values by 10. Which will give us the actual gain. We see that the Gain in figure 7 is approximately A_v = 21.

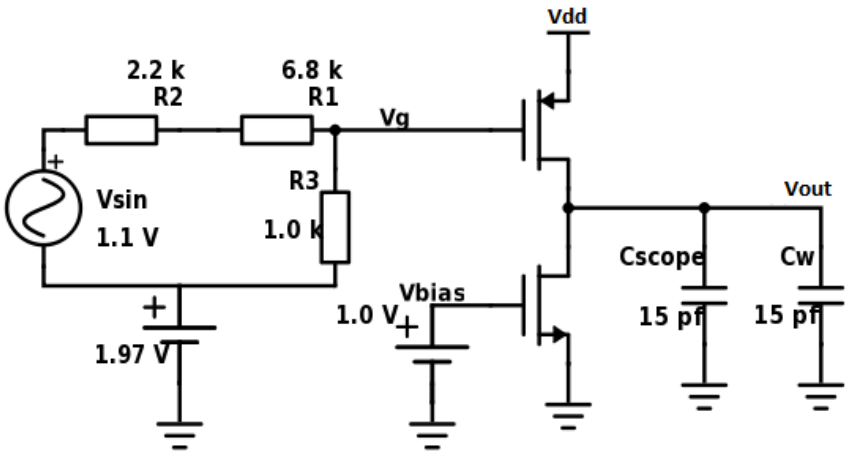

Figure 6: Circuit setup for task 1 and task 2

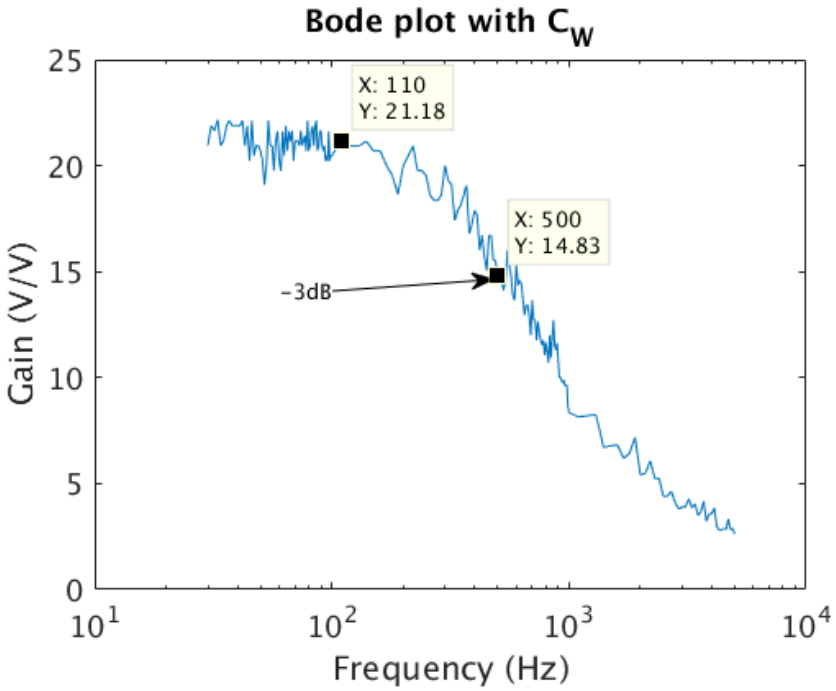

Figure 7: gain vs frequency (bode plot).

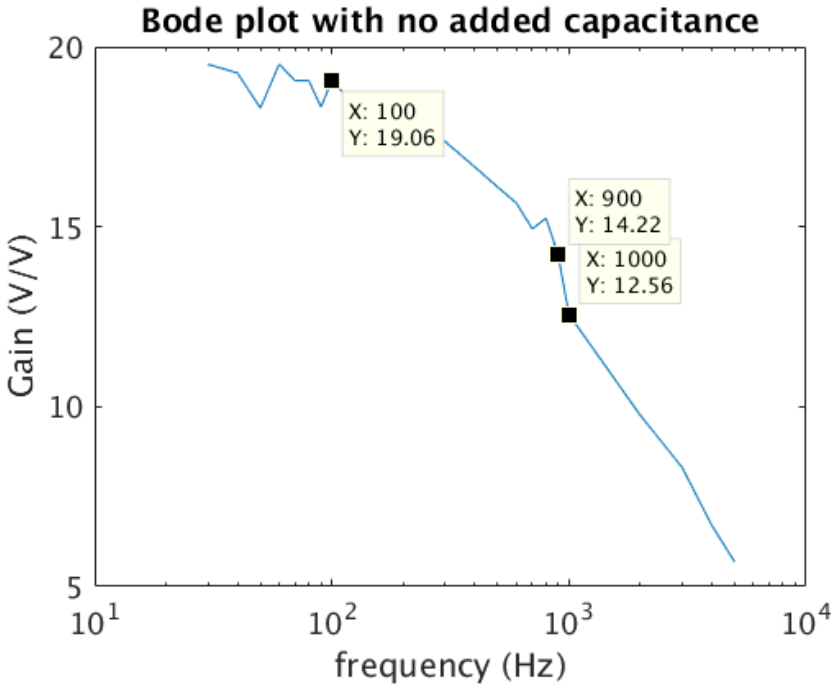

Figure 8: Rough bode plot given no added capacitance. Same circuit and script used as in Lab 2, still large decrease in bandwidth

3 Amplifier characteristics with added miller capacitance

We don't actually expect that much of a difference in dB as described in the task 3 exercise. The reason being that the cut-off given C_{Miller} can be found using $frequency = \frac{1}{R \cdot C} = \frac{1}{10^4 \cdot 15 \cdot 10^{-12}} = \frac{1}{15 \cdot 10^{-8}} \approx 6.7MHz$. We had an idea to use the phase shift to see if we could observe the break point, but as our bandwidth ends at 10 KHz this would not be observable.
What we could have done, was to increase R_S to 10 MΩ. This would in turn cause the break point to be at $\approx 6.7KHz$. If we would have used to 1 MΩ, the break point would have been at approximately 67 KHz. This would not be observable since we end our observations at 5 KHz, the phase would not be observable either since phase shift would have begun at 6.7 KHz.

We don't really observe a difference in BW compared to task 2 in figure 11. This is as we expected, as previously mentioned. In this we also have the possible faults as described in Section 5

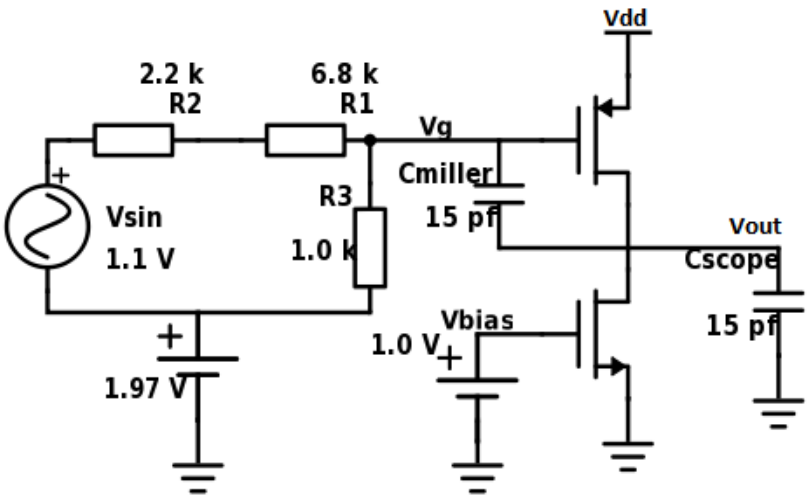

Figure 9: The circuit we used

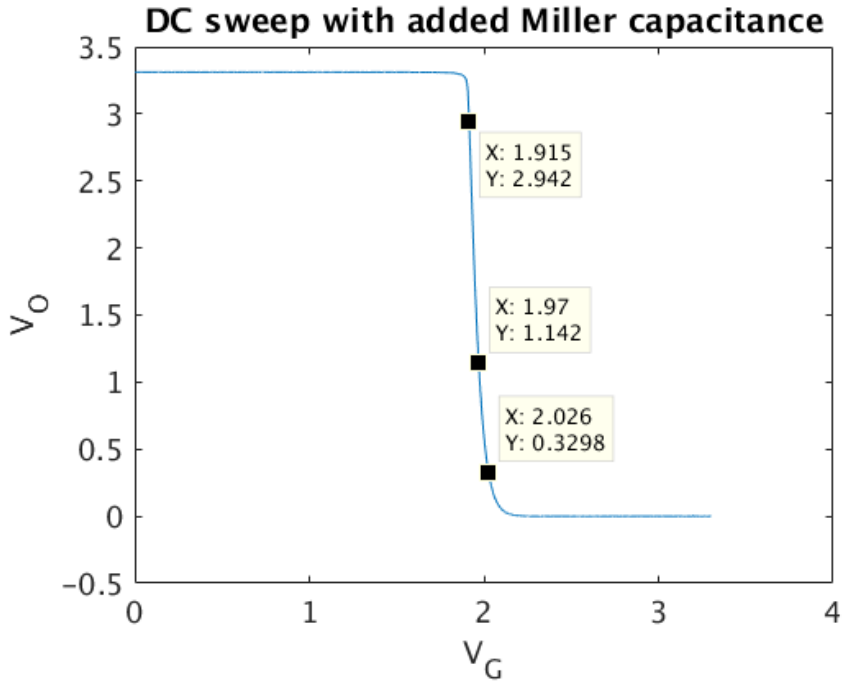

Figure 10: DC sweep for finding active region when miller capacitance present

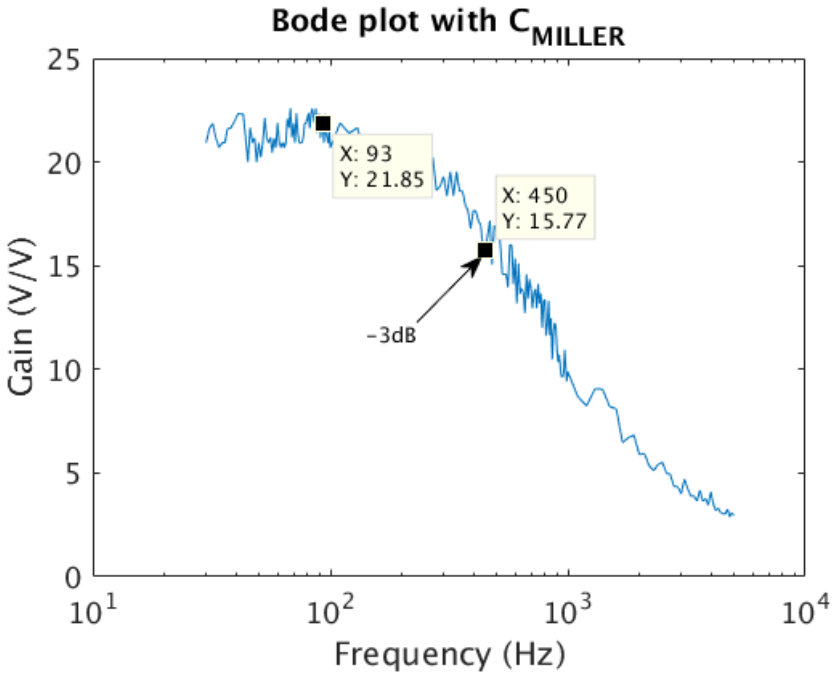

Figure 11: Bode plot with the added miller capacitance between PMOS gate and output

4 Formulas

Formula for finding derivative:

$$A_v = \frac{\Delta y}{\Delta x} = \frac{y(i) - y(i+1)}{x(i) - x(i+1)} \tag{1}$$

Formula for decibel conversion

$$A_v dB = 20 \cdot log(A_v) \tag{2}$$

5 Possible sources of error

As with all measurements in real life, theory and practise does not always co-operate. General sources of error can include parasitic capacitance/impedance from wires, probes, and components, imprecise instruments. As we changed our workstation between lab 2 and lab 3, we could also achieve an error due to difference in instruments. We can also receive faulty measurements due to an incorrect setup, although we have tried to follow the circuit designs we have included in the report. Since we are utilizing Matlab to automate the process, we could achieve errors in our code, that result in wrong measurements and/or computations.

Figure 12: Have this cute giraffe as a reward for correcting so many papers