

```
#define XPAR_CACHE_CONTROLLER_0_BASEADDR 0x8102000  
#define XPAR_CACHE_CONTROLLER_0_HIGHADDR 0xb102fff
```

```
/* Definitions for peripheral PS7_OCMC_0 */
```

```
#define XPAR_PS7_OCMC_0_BASEADDR 0xb800c000
```

```
#define XPAR_PS7_OCMC_0_HIGHADDR 0xb800cff
```

```
/* Definitions for peripheral PS7_PMU_0 */
```

```
#define XPAR_PS7_PMU_0_BASEADDR 0xb8891000
```

```
#define XPAR_PS7_PMU_0_HIGHADDR 0xb8891fff
```

```
/* Definitions for peripheral PS7_QSPI_LINEAR_0 */
```

```
#define XPAR_PS7_QSPI_LINEAR_0_BASEADDR 0xfc000000
```

```
#define XPAR_PS7_QSPI_LINEAR_0_HIGHADDR 0xfcffffff
```

```
/* Definitions for peripheral PS7_SCUC_0 */
```

```
#define XPAR_PS7_SCUC_0_BASEADDR 0xf8f00000
```

```
#define XPAR_PS7_SCUC_0_HIGHADDR 0xf8f000fc
```

```
/* Definitions for peripheral SLCR */
```

```
#define XPAR_SLCR_BASEADDR 0xb8000000
```

```
#define XPAR_SLCR_HIGHADDR 0xb8000fff
```

```
/* BOARD definition */
```

```
#define XPS_BOARD_ZYBO
```

```
#define XPAR_PS7_DDR_0_BASEADDRESS 0x100000
```

```
#define XPAR_PS7_DDR_0_HIGHADDRESS 0x20000000
```

```
#define XPAR_PS7_RAM_0_BASEADDRESS 0x0
```

```
#define XPAR_PS7_RAM_0_HIGHADDRESS 0x30000
```

```
#define XPAR_PS7_PAM_1_BASEADDRESS 0xffff0000
```

```
#define XPAR_PS7_M_1_HIGHADDRESS 0xfffffe00
```

```
#define XPAR_CPU_CORE_CLOCK_FREQ_HZ 650000000
```

```
#define STDOUT_BASEADDRESS 0xe0001000
```

```
#define STDIN_BASEADDRESS 0xe0001000
```

```
/* Number of SLRs */
```

```
#define NUMBER_OF_SLRS 0x1
```

```
/* Device ID */
```

```
#define XPAR_DEVICE_ID "7z010"
```

```
#endif /* end of protection macro */
```

The **clock speed** of your CPU is defined here in your `xparameters.h` file:

```
#define XPAR_CPU_CORE_CLOCK_FREQ_HZ 650000000
```

This means the clock speed of your CPU is **650 MHz** (or 650,000,000 Hz). You can use this value to convert clock cycles into time. For instance, if you want to convert the number of clock cycles measured by your timer into seconds, you would do:

```
time_in_seconds = (elapsed_clock_cycles) / 650000000.0;
```

So when you measure the elapsed time in clock cycles with your SCU Timer, you can use this value to calculate the actual time in seconds. Let me know if you need further assistance with this!

so the formula is

Yes, to convert the elapsed clock cycles into time (in seconds), you can use the following formula:

$$\text{Time (in seconds)} = \frac{\text{Elapsed Clock Cycles}}{\text{CPU Clock Frequency (in Hz)}}$$

In your case, with a CPU clock frequency of **650 MHz** (650,000,000 Hz), the formula becomes:

$$\text{Time (in seconds)} = \frac{\text{Elapsed Clock Cycles}}{650,000,000}$$

**Example:**

If your SCU Timer measures **32,500,000 clock cycles**, the time in seconds would be:

$$\text{Time (in seconds)} = \frac{32,500,000}{650,000,000} = 0.05 \text{ seconds}$$

This formula will help you convert the raw clock cycle measurements into actual time units (seconds).

```
#ifndef XPARAMETERS_H /* prevent circular inclusions */  
#define XPARAMETERS_H /* by using protection macros */
```

```
#define XPAR_XCORESIGHTPS_DCC_NUM_INSTANCES 1
```

```
/* Definitions for peripheral CORESIGHT */
```

```
#define XPAR_CORESIGHT_COMPATIBLE xlnx:ps7-coresight-comp-1.00.a
```

```
#define XPAR_CORESIGHT_BASEADDR 0xf8800000
```

```
#define XPAR_CORESIGHT_HIGHADDR 0xf8ffffff
```

```
/* Canonical definitions for peripheral CORESIGHT */
```

```
#define XPAR_XCORESIGHTPS_DCC_0_BASEADDR 0xf8800000
```

```
#define XPAR_XCORESIGHTPS_DCC_0_HIGHADDR 0xf88fffff
```

```
#define XPAR_XCORESIGHTPS_DCC_0_COMPATIBLE xlnx:ps7-coresight-comp-1.00.a
```

```

#define XPAR_XDEVCFG_NUM_INSTANCES 1

/* Definitions for peripheral DEVCFG */
#define XPAR_DEVCFG_COMPATIBLE xlnx,zynq-devcfg-1.0
#define XPAR_DEVCFG_BASEADDR 0xf8007000
#define XPAR_DEVCFG_HIGHADDR 0xf80070ff
#define XPAR_DEVCFG_INTERRUPTS 0x4008
#define XPAR_DEVCFG_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral DEVCFG */
#define XPAR_XDEVCFG_0_BASEADDR 0xf8007000
#define XPAR_XDEVCFG_0_HIGHADDR 0xf80070ff
#define XPAR_XDEVCFG_0_COMPATIBLE xlnx,zynq-devcfg-1.0
#define XPAR_XDEVCFG_0_INTERRUPTS 0x4008
#define XPAR_XDEVCFG_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XDMAPS_NUM_INSTANCES 1

/* Definitions for peripheral DMAC_S */
#define XPAR_DMAC_S_COMPATIBLE arm,pl330
#define XPAR_DMAC_S_BASEADDR 0xf8003000
#define XPAR_DMAC_S_HIGHADDR 0xf8003fff
#define XPAR_DMAC_DM_ ↓ _INTERRUPTS 0x400d
#define XPAR_DMAC_S_INTERRUPTS_1 0x400e
#define XPAR_DMAC_S_INTERRUPTS_2 0x400f
#define XPAR_DMAC_S_INTERRUPTS_3 0x4010
#define XPAR_DMAC_S_INTERRUPTS_4 0x4011
#define XPAR_DMAC_S_INTERRUPTS_5 0x4028
#define XPAR_DMAC_S_INTERRUPTS_6 0x4029
#define XPAR_DMAC_S_INTERRUPTS_7 0x402a
#define XPAR_DMAC_S_INTERRUPTS_8 0x402b
#define XPAR_DMAC_S_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral DMAC_S */
#define XPAR_XDMAPS_0_BASEADDR 0xf8003000
#define XPAR_XDMAPS_0_HIGHADDR 0xf8003fff
#define XPAR_XDMAPS_0_COMPATIBLE arm,pl330
#define XPAR_XDMAPS_0_INTERRUPTS 0x400d
#define XPAR_XDMAPS_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XEMACPS_NUM_INSTANCES 1

/* Definitions for peripheral GEM0 */
#define XPAR_GEM0_COMPATIBLE xlnx,zynq-gem
#define XPAR_GEM0_BASEADDR 0xe000b000
#define XPAR_GEM0_HIGHADDR 0xe000bffff
#define XPAR_GEM0_DMA_COHERENT 0x0
#define XPAR_GEM0_INTERRUPTS 0x4016
#define XPAR_GEM0_INTERRUPT_PARENT 0xf8f01000
#define XPAR_GEM0_REF_CLK 0x0

/* Canonical definitions for peripheral GEM0 */
#define XPAR_XEMACPS_0_BASEADDR 0xe000b000
#define XPAR_XEMACPS_0_HIGHADDR 0xe000bffff
#define XPAR_XEMACPS_XEN ↓ _S_0_COMPATIBLE xlnx,zynq-gem
#define XPAR_XEMACPS_0_DMA_COHERENT 0x0
#define XPAR_XEMACPS_0_INTERRUPTS 0x4016
#define XPAR_XEMACPS_0_INTERRUPT_PARENT 0xf8f01000
#define XPAR_XEMACPS_0_REF_CLK 0x0

#define XPAR_XGPIO_NUM_INSTANCES 1

/* Definitions for peripheral AXI_GPIO_0 */
#define XPAR_AXI_GPIO_0_COMPATIBLE xlnx,axi-gpio-2.0
#define XPAR_AXI_GPIO_0_BASEADDR 0x41200000
#define XPAR_AXI_GPIO_0_HIGHADDR 0x4120ffff
#define XPAR_AXI_GPIO_0_INTERRUPT_PRESENT 0x0
#define XPAR_AXI_GPIO_0_IS_DUAL 0x0
#define XPAR_AXI_GPIO_0_GPIO_WIDTH 0x4

/* Canonical definitions for peripheral AXI_GPIO_0 */
#define XPAR_XGPIO_0_BASEADDR 0x41200000
#define XPAR_XGPIO_0_HIGHADDR 0x4120ffff
#define XPAR_XGPIO_0_COMPATIBLE xlnx,axi-gpio-2.0
#define XPAR_XGPIO_0_GPIO_WIDTH 0x4
#define XPAR_XGPIO_0_INTERRUPT_PRESENT 0x0
#define XPAR_XGPIO_0_IS_DUAL 0x0

#define XPAR_XGPIOPS_NUM_INSTANCES 1

/* Definitions for peripheral GPIO0 */
#define XPAR_GPIO0_COMPATIBLE xlnx,zynq-gpio-1.0
#define XPAR_GPIO0_BASEADDR 0x0000a000
#define XPAR_GPIO0_HIGHADDR 0x0000a0ff
#define XPAR_GPIO0_INTERRUPTS 0x4014
#define XPAR_GPIO0_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral GPIO0 */
#define XPAR_XGPIOPS_0_BASEADDR 0x0000a000
#define XPAR_XGPIOPS_0_HIGHADDR 0x0000a0ff
#define XPAR_XGPIOPS_0_COMPATIBLE xlnx,zynq-gpio-1.0
#define XPAR_XGPIOPS_0_INTERRUPTS 0x4014
#define XPAR_XGPIOPS_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XQSPIPS_NUM_INSTANCES 1

/* Definitions for peripheral QSPI */
#define XPAR_QSPI_COMPATIBLE xlnx,zynq-qspi-1.0
#define XPAR_QSPI_BASEADDR 0xe000d000
#define XPAR_QSPI_HIGHADDR 0xe000ddff
#define XPAR_QSPI_CLOCK_FREQ 0xebc200
#define XPAR_QSPI_CONNECTION_MODE 0x0
#define XPAR_QSPI_INTERRUPTS 0x4013
#define XPAR_QSPI_INTERRUPT_PARENT 0xf8f01000
#define XPAR_QSPI_MODE 0x0

```

```

/* Canonical definitions for peripheral QSPI */
#define XPAR_XQSPISPS_0_BASEADDR 0xe000d000
#define XPAR_XQSPISPS_0_HIGHADDR 0xe000dff
#define XPAR_XQSPISPS_0_COMPATIBLE lnxzynq-qspi-1.0
#define XPAR_XQSPISPS_0_CLOCK_FREQ 0xebec200
#define XPAR_XQSPISPS_0_CONNECTION_MODE 0x0
#define XPAR_XQSPISPS_0_INTERRUPTS 0x4013
#define XPAR_XQSPISPS_0_INTERRUPT_PARENT 0xf8f01000
#define XPAR_XQSPISPS_0_QSPI_MODE 0x0
#define XPAR_XQSPISPS_0_QSPI_BUS_WIDTH 0x2

#define XPAR_XSIC_NUM_INSTANCES 1
↓

/* Definitions for peripheral INTC */
#define XPAR_INTC_COMPATIBLE arm,cortex-a9-gic
#define XPAR_INTC_BASEADDR 0xf8f01000
#define XPAR_INTC_HIGHADDR 0xdfbf01ff
#define XPAR_INTC_BASEADDR_1 0xf8f01000
#define XPAR_INTC_HANDLER_TABLE 0x0

/* Canonical definitions for peripheral INTC */
#define XPAR_XSCUGIC_0_BASEADDR 0xf8f01000
#define XPAR_XSCUGIC_0_HIGHADDR 0xf8f01fff
#define XPAR_XSCUGIC_0_HANDLER_TABLE 0x0
#define XPAR_XSCUGIC_0_COMPATIBLE arm,cortex-a9-gic

#define XPAR_XSCUTIMER_NUM_INSTANCES 1

/* Definitions for peripheral SCUTIMER */
#define XPAR_SCUTIMER_COMPATIBLE arm,cortex-a9-twd-timer
#define XPAR_XSCUTIMER_BASEADDR 0xf8f00600
#define XPAR_XSCUTIMER_HIGHADDR 0xf8f0061f
#define XPAR_XSCUTIMER_INTERRUPTS 0x13100d
#define XPAR_XSCUTIMER_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral SCUTIMER */
#define XPAR_XSCUTIMER_0_BASEADDR 0xf8f00600
#define XPAR_XSCUTIMER_0_HIGHADDR 0xf8f0061f
#define XPAR_XSCUTIMER_0_COMPATIBLE arm,cortex-a9-twd-timer
#define XPAR_XSCUTIMER_0_INTERRUPTS 0x13100d
#define XPAR_XSCUTIMER_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XSCUWDT_NUM_INSTANCES 1
↓

/* Definitions for peripheral SCUWDT */
#define XPAR_SCUWDT_COMPATIBLE lnxz,ps7-scuwdt-1.0-a
#define XPAR_XSCUWDT_BASEADDR 0xf8f00620
#define XPAR_XSCUWDT_HIGHADDR 0xf8f006ff
#define XPAR_XSCUWDT_INTERRUPTS 0x10400e
#define XPAR_XSCUWDT_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral SCUWDT */
#define XPAR_XSCUWDT_0_BASEADDR 0xf8f00620
#define XPAR_XSCUWDT_0_HIGHADDR 0xf8f006ff
#define XPAR_XSCUWDT_0_COMPATIBLE lnxz,ps7-scuwdt-1.0-a
#define XPAR_XSCUWDT_0_INTERRUPTS 0x10400e
#define XPAR_XSCUWDT_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XSDPS_NUM_INSTANCES 1

/* Definitions for peripheral SDHC10 */
#define XPAR_SDHC10_COMPATIBLE arasan,sdhci-8.9a
#define XPAR_SDHC10_BASEADDR 0xe0100000
#define XPAR_SDHC10_HIGHADDR 0xe0100fff
#define XPAR_SDHC10_SDIO_CLK_FREQ_HZ 0x2faf080
#define XPAR_SDHC10_SDIO_HAS_CD 0x1
#define XPAR_SDHC10_SDIO_HAS_WP 0x1
#define XPAR_SDHC10_BUS_WIDTH 0x0
#define XPAR_SDHC10_MIO_BANK 0x0
#define XPAR_SDHC10_SDIO_HAS_EMIO 0x0
#define XPAR_SDHC10_SLOT_TYPE 0x0
#define XPAR_SDHC10_SDIO_IS_CACHE_COHERENT 0x0
#define XPAR_SDHC10_CLOCKS 0x15
#define XPAR_SDHC10_CLK_50_SDR_ITAP_DLY 0x0
#define XPAR_SDHC10_CLK_50_SDOR_OTAP_DLY 0x0
#define XPAR_SDHC10_CLK_50_PDDR_ITAP_DLY 0x0
#define XPAR_SDHC10_CLK_50_PDDR_OTAP_DLY 0x0
#define XPAR_SDHC10_CLK_100_SDR_ITAP_DLY 0x0
#define XPAR_SDHC10_CLK_100_SDR_OTAP_DLY 0x0
#define XPAR_SDHC10_CLK_200_SDR_ITAP_DLY 0x0
#define XPAR_SDHC10_CLK_200_SDR_OTAP_DLY 0x0

/* Canonical definitions for peripheral SDHC10 */
#define XPAR_XSDPS_0_BASEADDR 0xe0100000
#define XPAR_XSDPS_0_HIGHADDR 0xe0100fff
#define XPAR_XSDPS_0_BUS_WIDTH 0x0
#define XPAR_XSDPS_0_COMPATIBLE arasan,sdhci-8.9a
#define XPAR_XSDPS_0_CLOCKS 0x15
#define XPAR_XSDPS_0_CLK_50_SDR_ITAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_50_SDOR_OTAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_50_PDDR_ITAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_50_PDDR_OTAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_100_SDR_ITAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_100_SDR_OTAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_200_SDR_ITAP_DLY 0x0
#define XPAR_XSDPS_0_CLK_200_SDR_OTAP_DLY 0x0
#define XPAR_XSDPS_0_SDIO_HAS_CD 0x1
#define XPAR_XSDPS_0_SDIO_HAS_WP 0x1
#define XPAR_XSDPS_0_SDIO_IS_CACHE_COHERENT 0x0
#define XPAR_XSDPS_0_MIO_BANK 0x0
#define XPAR_XSDPS_0_SDIO_CLK_FREQ_HZ 0x2faf080
#define XPAR_XSDPS_0_SLOT_TYPE 0x0

#define XPAR_XTTCPS_NUM_INSTANCES 1

/* Definitions for peripheral TTCO */
#define XPAR_TTTC0_COMPATIBLE arasan,ttco-1.0

```

```

#define XPAR_TTC0_COMPATIBLE cdns,ttc
#define XPAR_TTC0_BASEADDR 0xf8001000
#define XPAR_TTC0_HIGHADDR 0xf8001fff
#define XPAR_TTC0_CLOCK_FREQ 0x6750918
#define XPAR_TTC0_INTERRUPTS 0x400a
#define XPAR_TTC0_INTERRUPTS_1 0x400b
#define XPAR_TTC0_INTERRUPTS_2 0x400c
#define XPAR_TTC0_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral TTC0 */
#define XPAR_XTTCPS_0_BASEADDR 0xf8001000
#define XPAR_XTTCPS_0_HIGHADDR 0xf8001fff
#define XPAR_XTTCPS_0_COMPATIBLE cdns,ttc
#define XPAR_XTTCPS_0_CLOCK_FREQ 0x6750918
#define XPAR_XTTCPS_0_INTERRUPTS 0x400a
#define XPAR_XTTCPS_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XUARTPS_NUM_INSTANCES 1

/* Definitions for peripheral UART1 */
#define XPAR_UART1_COMPATIBLE xlnx,xuartps
#define XPAR_UART1_BASEADDR 0xe0001000
#define XPAR_UART1_HIGHADDR 0xe0001fff
#define XPAR_UART1_CLOCK_FREQ 0x5f5e100
#define XPAR_UART1_CTS_OVERRIDE 0x1
#define XPAR_UART1_CLOCKS 0x18
#define XPAR_UART1_INTERRUPTS 0x4032
#define XPAR_UART1_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral UART1 */
#define XPAR_XUARTPS_0_BASEADDR 0xe0001000
#define XPAR_XUARTPS_0_HIGHADDR 0xe0001fff
#define XPAR_XUARTPS_0_COMPATIBLE xlnx,xuartps
#define XPAR_XUARTPS_0_CLOCK_FREQ 0x5f5e100
#define XPAR_XUARTPS_0_CTS_OVERRIDE 0x1
#define XPAR_XUARTPS_0_CLOCKS 0x18
#define XPAR_XUARTPS_0_INTERRUPTS 0x4032
#define XPAR_XUARTPS_0_INTERRUPT_PARENT 0xf8f01000
↓
#define XPAR_XUSBPS_NUM_INSTANCES 1

/* Definitions for peripheral USB0 */
#define XPAR_USB0_COMPATIBLE xlnx,zynq-usb-2.20a
#define XPAR_USB0_BASEADDR 0xe0002000
#define XPAR_USB0_HIGHADDR 0xe0002fff
#define XPAR_USB0_INTERRUPTS 0x4015
#define XPAR_USB0_INTERRUPT_PARENT 0xf8f01000

/* Canonical definitions for peripheral USB0 */
#define XPAR_XUSBPS_0_BASEADDR 0xe0002000
#define XPAR_XUSBPS_0_HIGHADDR 0xe0002fff
#define XPAR_XUSBPS_0_COMPATIBLE xlnx,zynq-usb-2.20a
#define XPAR_XUSBPS_0_INTERRUPTS 0x4015
#define XPAR_XUSBPS_0_INTERRUPT_PARENT 0xf8f01000

#define XPAR_XXADCPs_NUM_INSTANCES 1

/* Definitions for peripheral ADC */
#define XPAR_ADC_COMPATIBLE xlnx,zynq-xadc-1.00.a
#define XPAR_ADC_BASEADDR 0xf8007100
#define XPAR_ADC_HIGHADDR 0xf800711f

/* Canonical definitions for peripheral ADC */
#define XPAR_XXADCPs_0_BASEADDR 0xf8007100
#define XPAR_XXADCPs_0_HIGHADDR 0xf800711f
#define XPAR_XXADCPs_0_COMPATIBLE xlnx,zynq-xadc-1.00.a

/* Definitions for peripheral PS7_AFL0 */
#define XPAR_PS7_AFL0_BASEADDR 0xf8008000
#define XPAR_PS7_AFL0_HIGHADDR 0xf8008fff
↓
/* Definitions for peripheral PS7_AFL1 */
#define XPAR_PS7_AFL1_BASEADDR 0xf8009000
#define XPAR_PS7_AFL1_HIGHADDR 0xf8009fff

/* Definitions for peripheral PS7_AFL2 */
#define XPAR_PS7_AFL2_BASEADDR 0xf800a000
#define XPAR_PS7_AFL2_HIGHADDR 0xf800afff

/* Definitions for peripheral PS7_AFL3 */
#define XPAR_PS7_AFL3_BASEADDR 0xf800b000
#define XPAR_PS7_AFL3_HIGHADDR 0xf800bfff

/* Definitions for peripheral MC */
#define XPAR_MC_BASEADDR 0xf8006000
#define XPAR_MC_HIGHADDR 0xf8006fff

/* Canonical definitions for peripheral MC */
#define XPAR_MEMORY_CONTROLLER_0_BASEADDR 0xf8006000
#define XPAR_MEMORY_CONTROLLER_0_HIGHADDR 0xf8006fff

/* Definitions for peripheral PS7_DMA_NS */
#define XPAR_PS7_DMA_NS_BASEADDR 0xf8004000
#define XPAR_PS7_DMA_NS_HIGHADDR 0xf8004fff

/* Definitions for peripheral GLOBAL_TIMER */
#define XPAR_GLOBAL_TIMER_BASEADDR 0xf8f00200
#define XPAR_GLOBAL_TIMER_HIGHADDR 0xf8f0021f
↓
/* Definitions for peripheral PS7_GPV_0 */
#define XPAR_PS7_GPV_0_BASEADDR 0xf8900000
#define XPAR_PS7_GPV_0_HIGHADDR 0xf89fffff

```

```

#define XPAR_PS7_IOP_BUS_CONFIG_0
#define XPAR_PS7_IOP_BUS_CONFIG_0_BASEADDR 0xe0200000
#define XPAR_PS7_IOP_BUS_CONFIG_0_HIGHADDR 0xe0200fff

/* Definitions for peripheral L2 */
#define XPAR_L2_BASEADDR 0xf8f02000
#define XPAR_L2_HIGHADDR 0xf8f02fff

/* Canonical definitions for peripheral L2 */
#define XPAR_CACHE_CONTROLLER_0_BASEADDR 0xf8f02000
#define XPAR_CACHE_CONTROLLER_0_HIGHADDR 0xf8f02fff

/* Definitions for peripheral PS7_OCMC_0 */
#define XPAR_PS7_OCMC_0_BASEADDR 0xf8000c00
#define XPAR_PS7_OCMC_0_HIGHADDR 0xf800cff

/* Definitions for peripheral PS7_PMU_0 */
#define XPAR_PS7_PMU_0_BASEADDR 0xf8891000
#define XPAR_PS7_PMU_0_HIGHADDR 0xf8891fff

/* Definitions for peripheral PS7_QSPI_LINEAR_0 */
#define XPAR_PS7_QSPI_LINEAR_0_BASEADDR 0xfc000000
#define XPAR_PS7_QSPI_LINEAR_0_HIGHADDR 0xfcffff

/* Definitions for peripheral PS7_SCUC_0 */
#define XPAR_PS7_SCUC_0_BASEADDR 0xf8f00000
#define XPAR_PS7_SCUC_0_HIGHADDR 0xf8f000fc

```

↓  
/\* Definitions for peripheral SLCR \*/  
#define XPAR\_SLCR\_BASEADDR 0xf8000000  
#define XPAR\_SLCR\_HIGHADDR 0xf8000fff

/\* BOARD definition \*/  
#define XPS\_BOARD\_ZYBO

```

#define XPAR_PS7_DDR_0_BASEADDRESS 0x100000
#define XPAR_PS7_DDR_0_HIGHADDRESS 0x20000000
#define XPAR_PS7_RAM_0_BASEADDRESS 0x0
#define XPAR_PS7_RAM_0_HIGHADDRESS 0x30000
#define XPAR_PS7_RAM_1_BASEADDRESS 0xffff0000
#define XPAR_PS7_RAM_1_HIGHADDRESS 0xfffffe00

```

```
#define XPAR_CPU_CORE_CLOCK_FREQ_HZ 650000000
```

```
#define STDOUT_BASEADDRESS 0xe0001000
#define STDIN_BASEADDRESS 0xe0001000
```

/\* Number of SLRs \*/  
#define NUMBER\_OF\_SLRS 0x1

/\* Device ID \*/  
#define XPAR\_DEVICE\_ID "7z010"

```
#endif /* end of protection macro */
```



The file you shared confirms the CPU clock frequency definition:

```
c Kopier code
#define XPAR_CPU_CORE_CLOCK_FREQ_HZ 650000000
```

This defines the CPU clock frequency as **650 MHz** (650,000,000 Hz).

To convert clock cycles measured by the SCU timer into time (seconds), you can use the following formula:

$$\text{Time (in seconds)} = \frac{\text{Elapsed Clock Cycles}}{650,000,000}$$

If your code measures, for example, **32,500,000 clock cycles**, the time in seconds would be:

$$\text{Time (in seconds)} = \frac{32,500,000}{650,000,000} = 0.05 \text{ seconds}$$

You can use this formula to interpret the output from your SCU timer when measuring the performance of your program.

< 1/2 >

i have the cycles taken to sort :

```
194
659
862
```

< 2/2 >



You can convert these cycle counts into actual time (in seconds) using the formula:

$$\text{Time (in seconds)} \downarrow \frac{\text{Elapsed Clock Cycles}}{650,000,000}$$

Let's calculate the time for each cycle count:

1. For 194 clock cycles:

$$\text{Time} = \frac{194}{650,000,000} = 2.98 \times 10^{-7} \text{ seconds} \approx 0.298 \mu\text{s}$$

2. For 659 clock cycles:

$$\text{Time} = \frac{659}{650,000,000} = 1.01 \times 10^{-6} \text{ seconds} \approx 1.01 \mu\text{s}$$

3. For 862 clock cycles:

$$\text{Time} = \frac{862}{650,000,000} = 1.33 \times 10^{-6} \text{ seconds} \approx 1.33 \mu\text{s}$$

Summary of Results:

- 194 cycles: ~0.298 microseconds ( $\mu\text{s}$ )
- 659 cycles: ~1.01 microseconds ( $\mu\text{s}$ )
- 862 cycles: ~1.33 microseconds ( $\mu\text{s}$ )

These values represent the time taken to sort, based on the number of clock cycles your timer has recorded.

i have another with 34



Let's calculate the time for 34 clock cycles using the same formula:

$$\text{Time (in seconds)} = \frac{\text{Elapsed Clock Cycles}}{650,000,000}$$

For 34 clock cycles:

$$\text{Time} = \frac{34}{650,000,000} = 5.23 \times 10^{-8} \text{ seconds} \approx 0.052 \mu\text{s}$$

Result:

- 34 cycles: ~0.052 microseconds ( $\mu\text{s}$ )

This is the time it took for the sort operation in 34 clock cycles.

i have another with 65 and 26



Let's calculate the time for both 65 and 26 clock cycles using the same formula:

$$\text{Time (in seconds)} = \frac{\text{Elapsed Clock Cycles}}{650,000,000}$$

For 65 clock cycles:

$$\text{Time} = \frac{65}{650,000,000} = 1 \times 10^{-7} \text{ seconds} \approx 0.10 \mu\text{s}$$

For 26 clock cycles:

$$\text{Time} = \frac{26}{650,000,000} = 4 \times 10^{-8} \text{ seconds} \approx 0.04 \mu\text{s}$$

Results:

- 65 cycles: ~0.10 microseconds ( $\mu\text{s}$ )
- 26 cycles: ~0.04 microseconds ( $\mu\text{s}$ )

These are the times it took for the sort operation in these respective cycle counts.

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