TFE4152 Design of Integrated Circuits

Project Presentation

September 2019

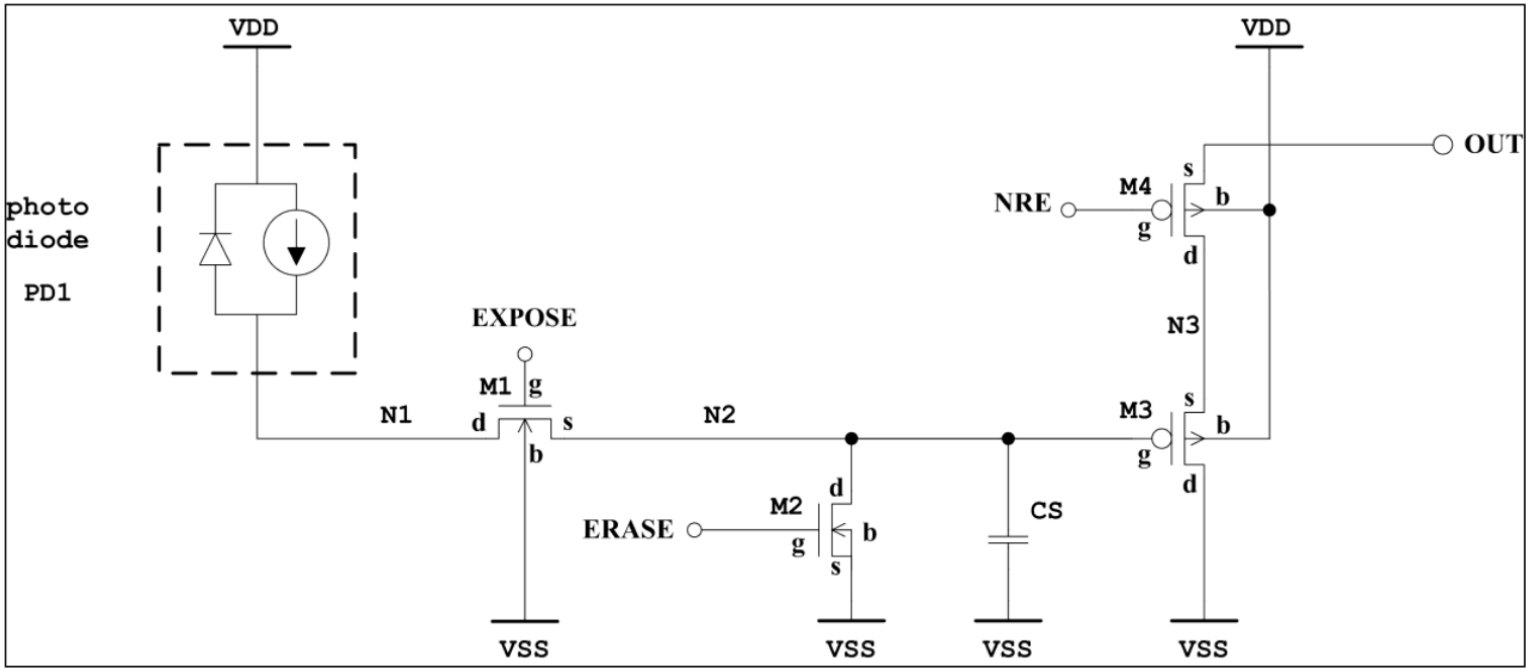
Project Description

- Design of circuits for a four pixel digital camera.
  - Pixel circuit, readout and control circuit
- The pixel circuit and pixel array are analog circuits
  - Light to voltage conversion before analog-to-digital conversion
  - Transistor level design
  - Simulate and verify using AIM-Spice
- The readout control circuit is a digital circuit
  - Controls the operation of the camera.
  - Describe the design using Verilog.
  - Simulate and verify using Active-HDL

The Pixel Circuit

- The circuit topology is given in the specification.
- Your task is to size the components within the constraints given in the specification.
- You will use a 180nm technology
- AIM-Spice is used for circuit simulation.

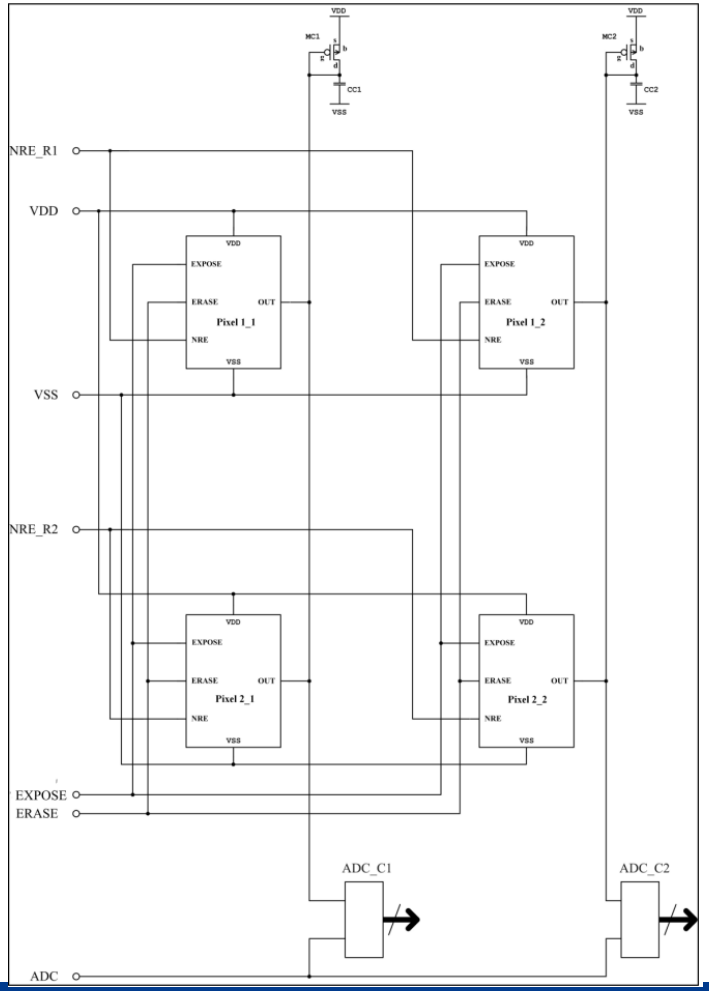
The Pixel Circuit



The Pixel Array

- The pixel circuit will be put into an array
  - Containing 4 pixels
- Two and two pixels share an ADC and an active load.
- The read out of the pixel values are sequenced by a digital circuit that you design.
- In this project we do not design the ADC, and we do not have to think about what happens after the ADC.

The Pixel Array



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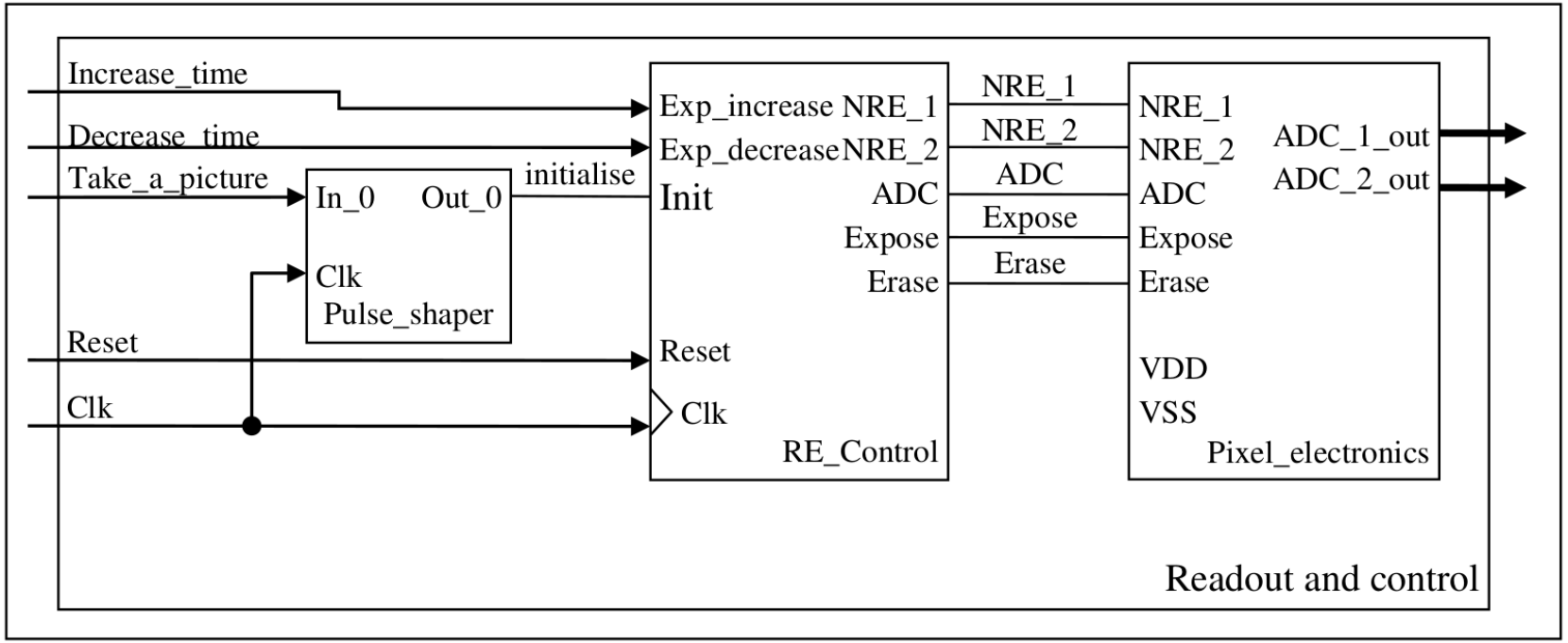
Analog Design

- Before you start, read the specification carefully.
- Make sure you understand what all the components in the circuit do
  - Switches, amplifier, active load, how light is converted to a voltage
- Partition your circuit into smaller parts and test individually
- Combine the part when they work as expected to simulate the whole circuit.

Readout Control Circuit



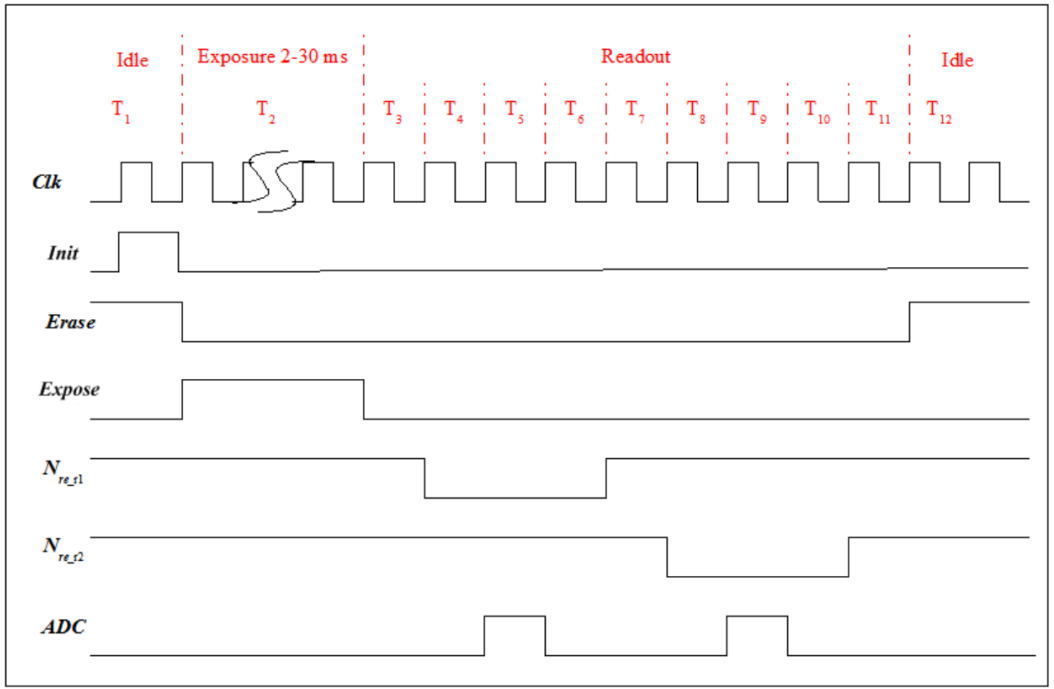
Readout Control Circuit

- Design and describe using HDL (Hardware Description Language)
  - Verilog
- You will use the the program Active-HDL to simulate you designs.

Readout Control Circuit

- Controls the camera
  - Setting and control of the exposure time
  - Control readout of the ADCs
- The readout and control circuit interface is given by the specification.
  - you design the circuit using this interface
- Timing is important
  - Controls the camera
- Timing is given in the specification

Readout Control Circuit



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Digital Design

- Read the specification carefully.
- Partition you design into smaller functional parts and test them individually.
- When all parts have been tested, combine them to simulate and verify the whole circuit.
- You are going to hand in your Verilog code, so be sure to follow the interface naming.
  - Only the design is to be handed in, not the testbenches.
  - All code should still be included in the report as described in the project description.

What are you going to hand in

- You are going to write a technical report
  - There is a description of what is expected in the project description
- You are going to hand in your Verilog design
  - This is the design only, and not the testbench
  - This is your Verilog source files
  - Do not worry about the paths in include statements in the code you hand in, just make sure you hand in every thing that makes up the design.

Important Information

- Two members per group
  - Form a group and send me your names
    - aslak.holen@ntnu.no, subject: TFE4152
  - If you can not find a group, contact me.
- The report counts 30% of the total grade
- Deadline: November 18 before 15:00
- A detailed description of the project and other resources will be uploaded to Blackboard.

Additional tips

- Read the project description carefully!
- Start early!
- Use the exercise hours
  - Thursdays 08:15 – 10:00