Process Technology:
TSMC (CL013G)

High-Speed Single-Port Synchronous Diffusion ROM

rom_4096x8_t13
4096X8, Mux 16, Drive 6

Features

- Precise Optimization for TSMC's Eight-Layer Metal 0.13µm (CL013G) CMOS Process
- High Density (area is 0.05mm^2)
- Fast Access Time (1.55ns at fast@0C process, 1.32V, 0˚C)
- Fast Cycle Time (1.38ns at fast@0C process, 1.32V, 0˚C)
- One Read Port
- Completely Static Operation
- Near-Zero Hold Time (Data, Address, and Control Inputs)

Memory Description

The 4096X8 ROM is a high-performance, synchronous single-port, 4096-word by 8-bit memory designed to take full advantage of TSMC's eight-layer metal, 0.13µm (CL013G) CMOS process.

The diffusion ROM's storage array is composed of diffusion-programmable single-transistor cells with fully static memory circuitry. The diffusion ROM operates at a voltage of 1.2V ± 10% and a junction temperature range of -40.0˚C to +125˚C.

Pin Description

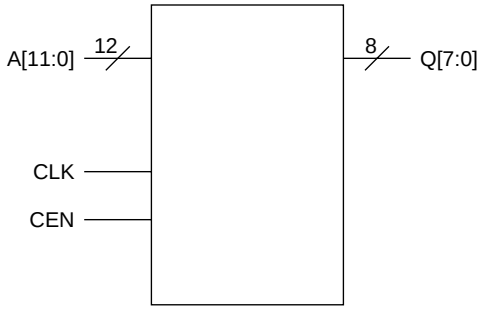
Pin	Description
A[11:0]	Addresses (A[0] = LSB)
CLK	Clock Input
CEN	Chip Enable
Q[7:0]	Data Outputs (Q[0] = LSB)

Area

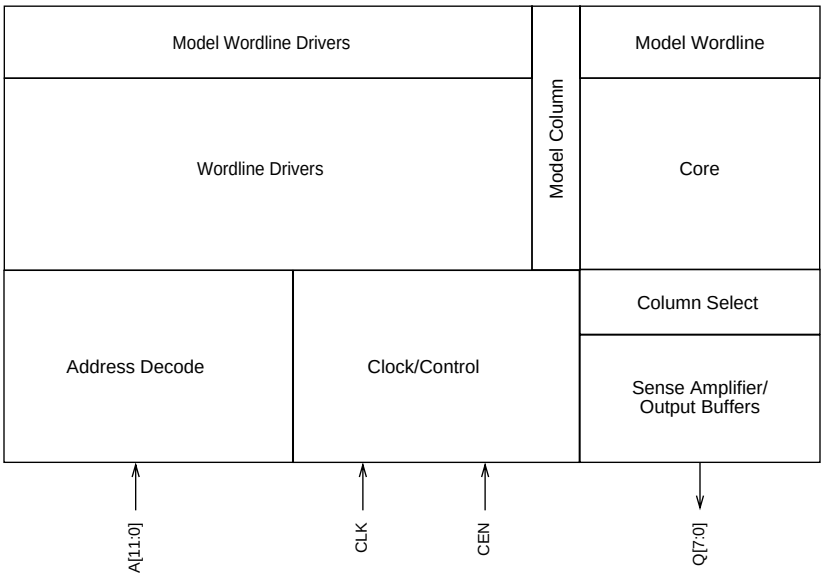
Area Type	Width (mm)	Height (mm)	Area (mm^2)
Core	0.18	0.27	0.05
Footprint	0.23	0.31	0.07

The footprint area includes the core area and user-defined power ring and pin spacing areas.

Symbol

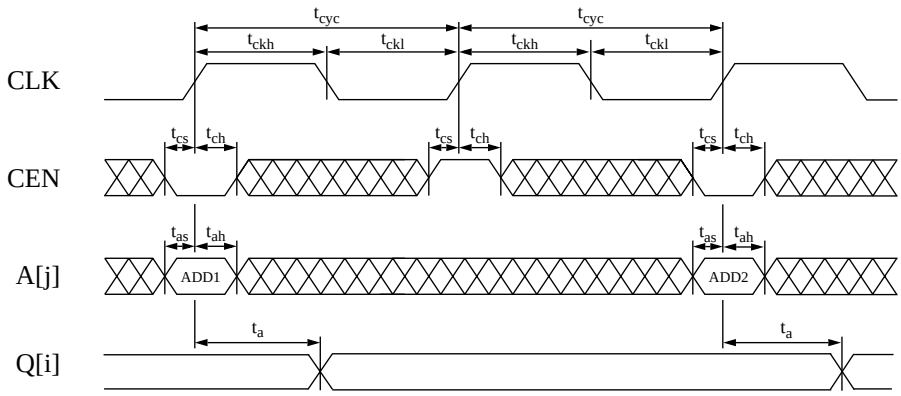


Diffusion ROM Block Diagram



Diffusion ROM Timing Diagram

Figure 1. Synchronous Single Read-Cycle Timing



Rising delays are measured at 50% of VDD and falling delays are measured at 50% of VDD.
Rising and falling slews are measured from 10% VDD to 90% VDD.

Diffusion ROM Logic Table

CEN	Data Out	Mode	Function
H	Last Data	Standby	Address inputs are disabled, and the port cannot be accessed for new reads. Data outputs remain stable.
L	ROM Data	Read	Data on the output bus Q[n-1:0] is read from the memory location specified on the address bus A[m-1:0].

Diffusion ROM Timing

Parameter	Symbol	Fast@-40C Process 1.32V, -40˚C		Fast@0C Process 1.32V, 0˚C		Typical Process 1.20V, 25˚C		Slow Process 1.08V, 125˚C	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Cycle time	t_{cyc}	0.93		0.99		1.38		2.28	
Access time[1,2]	t_a	0.94			1.00		1.55		2.48
Address setup	t_{as}	0.18		0.19		0.27		0.50	
Address hold	t_{ah}	0.00		0.00		0.00		0.00	
Chip enable setup	t_{cs}	0.23		0.25		0.34		0.60	
Chip enable hold	t_{ch}	0.00		0.00		0.00		0.00	
Clock high	t_{ckh}	0.04		0.04		0.06		0.09	
Clock low	t_{ckl}	0.07		0.08		0.13		0.22	
Clock rise slew	t_{ckr}		4.00		4.00		4.00		4.00
Output load factor (ns/pF)	K_{load}		0.47		0.49		0.65		0.91

[1] Parameters have a load dependence (K_{load}), which is used to calculate: $TotalDelay = FixedDelay + (Kload \times Cload)$.

[2] Access time is defined as the slowest possible output transition for the typical and slow corners, and the fastest possible output transition for the fast corner.

Pin Capacitance

Pin	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Value (pF)	Value (pF)	Value (pF)	Value (pF)
A[j]	0.029	0.030	0.028	0.026
CLK	0.472	0.490	0.427	0.446
CEN	0.007	0.007	0.007	0.007

Power

500.00MHz Operation

Condition	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Value (mA)	Value (mA)	Value (mA)	Value (mA)
AC Current	26.045	25.539	22.620	21.471
Peak Current	146.852	142.171	96.132	53.645
Deselected Current[1]	2.198	2.312	1.941	1.891
Standby Current[2]	0.003	0.011	0.006	0.041

[1] Value assumes diffusion ROM is deselected, all addresses switch, and 50% of input pins switch. The logic-switching component of deselected power becomes negligibly small if the input pins are held stable by externally controlling these signals with chip select.

[2] Value is independent of frequency and assumes all inputs and outputs are stable.

Clock Noise Limit

Signal	Fast@-40C Process 1.32V, -40˚C		Fast@0C Process 1.32V, 0˚C		Typical Process 1.20V, 25˚C		Slow Process 1.08V, 125˚C	
	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)	Pulse Width (ns)	Voltage (V)
CLK	10.00	0.60	10.00	0.59	10.00	0.58	10.00	0.54

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure.

Power and Ground Noise Limit

Signal	Fast@-40C Process 1.32V, -40˚C	Fast@0C Process 1.32V, 0˚C	Typical Process 1.20V, 25˚C	Slow Process 1.08V, 125˚C
	Voltage (V)	Voltage (V)	Voltage (V)	Voltage (V)
Power	0.13	0.11	0.12	0.11
Ground	0.13	0.11	0.12	0.11

The power/ground noise limit is the maximum supply voltage transition allowable without causing a memory failure.