SIP Release Notes
8 January 2021

IOSF Sideband Endpoint PIC
Revision 2021WW02_RTL1P0_PICr35

RTL Updates:

HSDs:

1. 22011612815: "Issue with Bulk RATA is different from Legacy RATA on treg_cerr logic is fixed in this release"
2. 14013117381: "SBE Completion Fencing Legacy 8b SBE deasserts CFENCE signal due to incorrectly decoding Posted transaction"
3. 14013279301: "SBE TSA and mat version update"
4. 22011522174: "SGCDC CDC enhancements for SBE - tracking ticket"
5. 14012676022: "TFM - FWD MDF - IOSF EP has syn2sim error"
6. 22011376452: "Define legal combo values of usyncselect and SIDE_USYNC_DELAY, AGENT_USYNC_DELAY parameter settings"
7. 22011368758: "Logic used for assertion code which needs to be put in retention list in UPF is guarded under INTEL_SIMONLY"
8. 14012006477: "Add RTL assertion around relationship between agent_clkreq and mmsg signals"
9. 14011334385: "Doc Update - Sideband Endpoint handling of SAIRS EH when configured with GLOBAL_EP=1 and RX_EXT_HEADER_SUPPORT=0"
10. 1409390433: "SBEP's difference tmsg_*valid signal behavior between sync/async modes"

Backend Updates:

General Updates.

Validation Updates:

General Updates.

Known Issues:

None.

Special Considerations and Instructions:

- This SBE release uses the "IOSF_SVC_2020WW49" version of SVC in IRR with constraints on hierarchical headers insertion.
- For support file an **HSD** at SIP HSD
- The Zircon scores are uploaded to the PEARL now at SBE Zircon Scores
- This is SBE release PICr35 with TSA version 20.36.06, all commands are in cfg/README_EP_PICr35 file
- Please note that Sideband Endpoint instantiations need to be uniquified in all IP's per the SEG POR instantiation and uniquification methodology to avoid module collisions with other instances of the endpoint with other IPs.
- Please read integration guide carefully for handling current clock request logic

- Please read integration guide carefully for conditions of locally clock gating the agent_clk in asynchronous endpoints.
- Please read integration guide carefully for any necessary power gating logic that may be needed.
- **NOTE:** CTECH_LIB_NAME must point to a valid synthesisable CTECH library when synthesising the IP.
- **NOTE:** CTECH_LIB_NAME must point to a valid synthesisable/behavior CTECH library when simulating the IP.