CDA Module

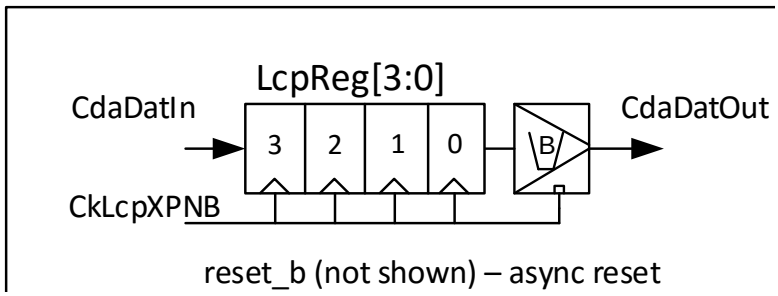
Source RTL in globalclk repo - src/rtl/clk_cda/gclk_make_clk_cda.sv

Interfaces

Port name	Width	Direction	Description
clk_in	1	In	Functional Clock input
clk_out	1	Out	Functional Clock output
CkLcpXPNB	1	In	Shift clock
reset_b	1	In	Async reset (active low)
CdaDatIn	1	In	Serial shift data input
CdaDatOut	1	Out	Serial shift data output

Shift

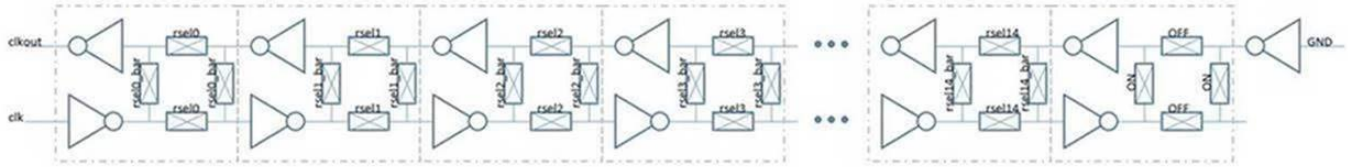
Shift interface designed to look like normal LCP cell (4 bit):



Decode

The CTECH CDA cell (ctech_lib_sdg_programmable_delay_clk_buf) has 15 control bits (rsel0..rsel14).

The clock comes in from the left and exits back to the left after taking one of several different loops.



Here is the decode of 4 bit LcpReg to the 15 rsel bits:

LcpReg[3:0]	rsel0	rsel1	rsel2	rsel3	rsel4	rsel5	rsel6	rsel7	rsel8	rsel9	rsel10	rsel11	rsel12	rsel13	rsel14	Comment
0000	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	shortest
0001	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	
0010	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	
0011	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	
0100	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	
0101	1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	
0110	1	1	1	1	1	1	0	X	X	X	X	X	X	X	X	
0111	1	1	1	1	1	1	1	0	X	X	X	X	X	X	X	
1000	1	1	1	1	1	1	1	1	0	X	X	X	X	X	X	
1001	1	1	1	1	1	1	1	1	1	0	X	X	X	X	X	
1010	1	1	1	1	1	1	1	1	1	1	0	X	X	X	X	
1011	1	1	1	1	1	1	1	1	1	1	1	0	X	X	X	
1100	1	1	1	1	1	1	1	1	1	1	1	1	0	X	X	
1101	1	1	1	1	1	1	1	1	1	1	1	1	1	0	X	
1110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
1111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	longest