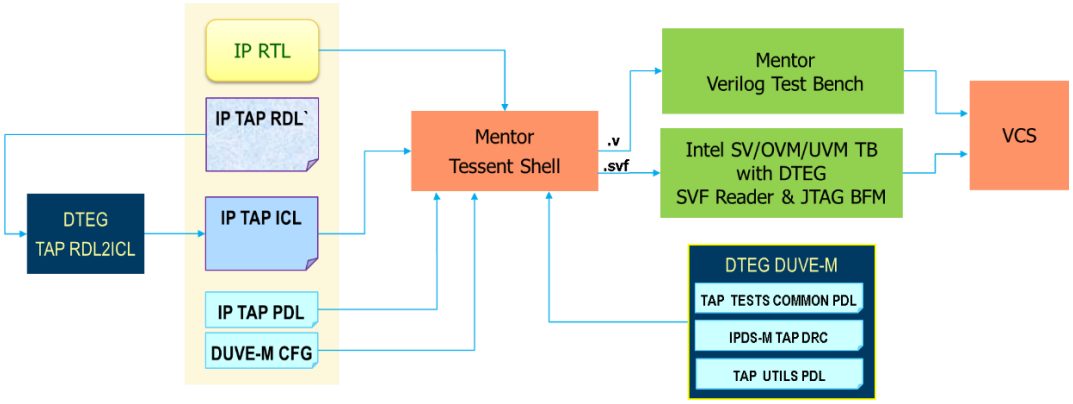
Overview	DUVE-M (DTEG Unified Validation Environment (Mentor)) is a generic infrastructure and tests for DFx/TAP validation and test content development based on the IEEE 1687 ICL/PDL standard and collateral. It is compatible with Intel-specific TAP architectures and features and can be easily tuned to support different design configurations and test requirements. The tool includes the TAP RDL2ICL utility for generating IP-level ICL from the existing TAP RDL.
Tool Block Diagram	Typical Use of DUVE-M for IP Level Validation 
Required Tool Inputs	▪ RTL: Verilog description of the top-level module in the project ▪ TAP spec: Specification of TAP registers in SystemRDL format (Intel-specific) ▪ DFx/TAP ports: Specification of DFx/TAP ports in ICL format ▪ PDL tests: Project-specific tests in PDL format
Tool Outputs	▪ TAP ICL: TAP register specification in ICL format ▪ Verilog Test Bench: Test or validation patterns in Verilog format (requires Tessent Shell)
Tool Coverage	DUVE-M provides tests to cover all aspects of TAP ICL versus RTL validation: ▪ TDI-TDO continuity ▪ TAP IR/TDR resets ▪ TDR Read-Write access ▪ TDR Security ▪ Reserved Opcodes In addition, included procedures and utilities allow writing generic PDL tests and accessing RTL/ICL/PDL metadata in the Tessent Data Models.

Tool Scripts	▪ TAP RDL2ICL (tap_icl_gen.pl): Utility to convert existing IP TAP RDL to ICL ▪ Tessent dofile (gen_val_tests.do): Pattern generation flow
Related Tools	Siemens (Mentor Graphics) Tessent Shell is required for use of DUVE-M infrastructure.
Power, Area, and Gate Count	Not applicable