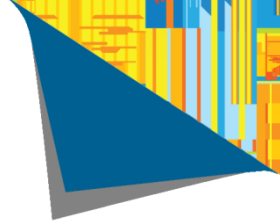

P1276 HDUSPSR SRAM Compiler

Specification

Intel Confidential
Revision 1.0, May 2022
Disclosed Pursuant to CNDA

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Document Revision History

Revision Number	Date	Comments
1.0	May. 2022	Initial version for final view (FV) Added L2P diagrams for CM2 and CM4 non-butterfly

Contents

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1 P1276 HDUSPSR SRAM

1.1 Overview

This document describes the design specifications for the Intel Corporate Memory Organization (CMO) P1276 **H**igh **D**ensity **U**niform **S**ingle **P**ort **S**hort **R**ange (HDUSPSR) SRAM Compiler. The topics covered in this guide are the SRAM features, functions, pin settings and physical integration guidelines. Table 1 shows a summary of the HDUSPSR SRAM compiler and the supported memory range per SRAM instance.

Table 1. P1276 HDUSPSR SRAM Summary

Compiler Name	Ports	Power	Technology	Bitcell Type	Architecture	Range (Kb)
Small Range HDU (HDUSPSR) Compiler	1RW	Single-Rail	P1276.4	WPHCCU	Non-Butterfly/Butterfly (1 or 2 banks)	0.5 – 160

1.2 Features

The P1276 HDUSPSR SRAMs support a variety of features to address specific System-On-Chip (SOC) design needs. The SRAMs implement fully synchronous design with the capability of single-cycle throughput and fast clock-to-out through self-timed read (better SRAM latency/access time). The SRAM sub-array contains input latches. All functional inputs are latched on the rising edge of the input clock. Output data is also latched. A memory read occurs from the selected address when read enable is asserted during high phase of the clock. A memory write happens to the selected address when write enable is asserted during high phase of the clock. Table 2 summarizes the memory features. Additional features include:

- High-Performance Single Port (1RW) 6T bit-cell Design (WPHCCU)
- Read and write-assist for improved yield
- Separate Data-In / Data-Out Busses
- Optional integrated power-switch
- Supports bit enable for write. Byte enable is supported in the DFX wrapper.
- Supports extensive clock gating to lower standby power
- BIST and ATPG logic are supported in the DFX wrapper

Table 2. P1276 HDUSPSR SRAM Specification

Compiler Features			
Bitcell Type	6T WPHCCU (P1276.4)		
Periphery Device Types	Nominal/SVT/HVT		
Functionality			
Ports	1RW		
Clocks	1		
Bit/Byte Write	Supported		
Throughput	1 cycle		
Latency	Self-timed < 1-cycle		
Read Assist (VMIN/Yield)	Yes		
Write Assist (VMIN/Yield)	Yes		
Standard Array Range			
Banks	**2**		
Column Mux	**4**	**8**	
Number of Entries (NW)	128 – 2048*	256 – 4096*	
NW Increment	32	64	
Number of Data Bits (NB)	8 - 80	8-40	
NB Increment	1	1	
Banks	**1**		
Column Mux	**2**	**4**	**8**
Number of Entries (NW)	64 - 1024	64 - 1024	128 - 2048
NW Increment	32	32	64
Number of Data Bits (NB)	16 - 160	8 - 80	8 - 40
NB Increment	1	1	1
Integration			
Metal Usage	Exclusive M01-M05 with M05 power and IO ports		
Single Rail Mode	Single rail configurations with no Level Shifters.		
Power Modes			
Array Sleep	Supported in PG configurations. Internal Clock Gating and Array Sleep. Periphery is powered up. Not available for lower voltages. (see power mode section)		
Periphery Sleep	Supported in PG configurations. Internal Clock Gating and Periphery is power-gated off.		
Periphery + Array Sleep (Deep Sleep)	Supported in PG configurations. Internal Clock Gating and Array Sleep enabled. Periphery is power-gated off.		
Shut Down (Power-gated)	Supported in PG configurations. Entire SRAM is power-gated off.		
DFT Features			
BIST	Supported as an external synthesizable Soft IP - DFX Wrapper		

DFM Features	
Row Redundancy	Double Row; Logic in DFX Wrapper
Column Redundancy	Extra IO supported; Mux outside Hard IP. Refer to DFX section of integration guide.
Assist Control	Read and Write Assist Supported
Operating Voltage Range	
	0.55V/0.65V/0.75V/0.85V/1.1V -40C/100C

1.3 SRAM Instance Naming

The CMO P1276 SRAM naming convention is shown in Figure 1. Specific naming designators are left blank if not used for features such as bit/byte enable, redundant rows, redundant columns, and halos. Refer to section 1.1 for information on the retention build option.

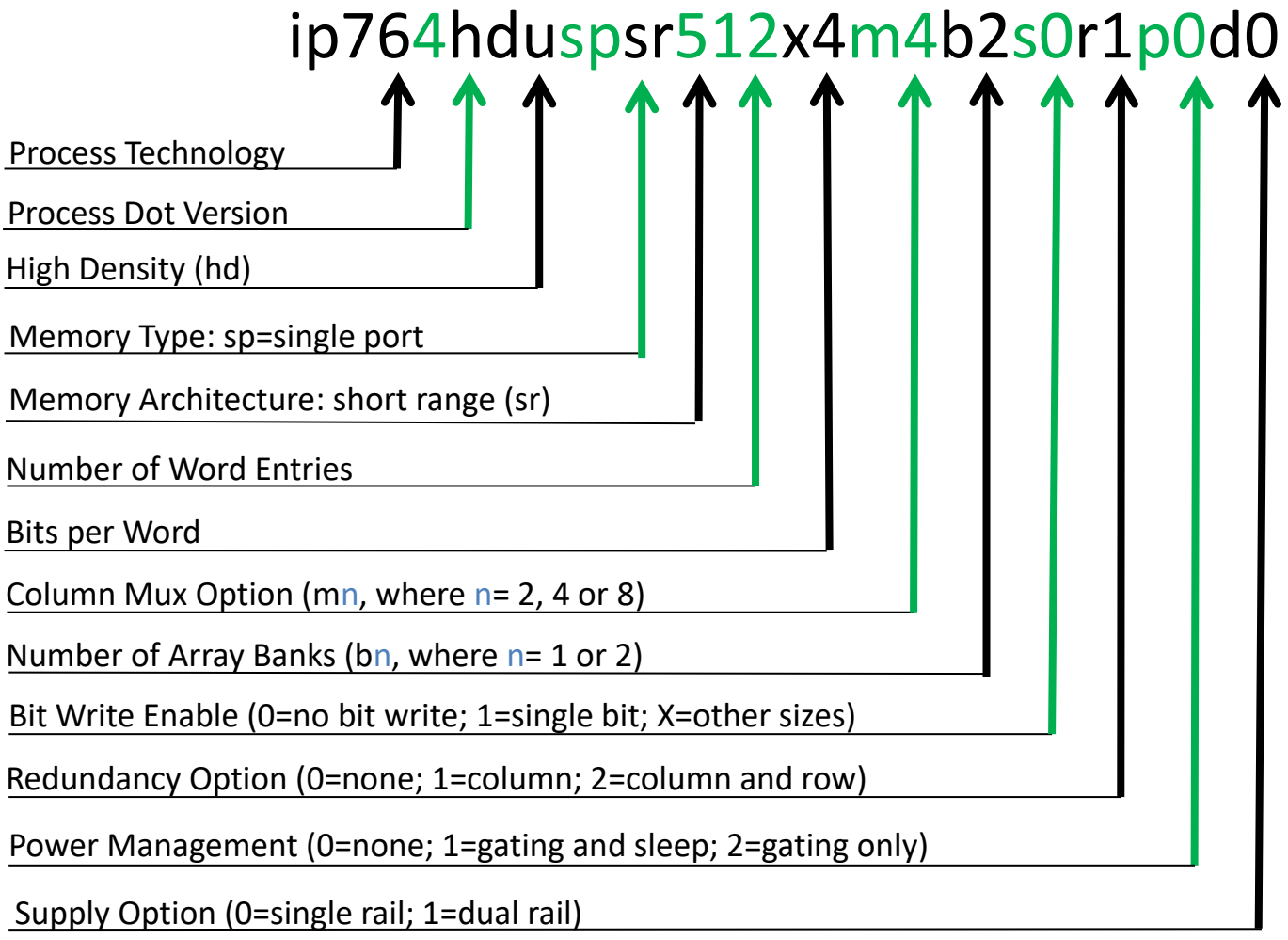

Figure 1. P1276 SRAM Naming Convention

Example 1: A single rail WPHCCU SRAM on P1276.4 process with 2048 word entries, column mux of 4, 72 bits of data, 2 array banks, write bit enabled, 1 bit column of redundancy, power gated, and single supply rail would be named ***ip764hduspsr2048x72m4b2s1r1p1d0***.

1.4 Pin/Port Interface List

Table 3 gives a comprehensive Pin/Port interface list with descriptions for P1276 memories. The "1" notation implies a logical high equal to supply voltage *vddp*.

The subsequent Table 4 will describe in greater detail the functions and settings of specific configurable pins.

Important notes:

- Functional inputs (Table 3) should be isolated either in the DFX wrapper or at the partition level to prevent metastable/crowbar current conditions.
- Power management enable (PME) pins are not available at the hard block for non-power gated (non-PME) SRAM builds. These PME pins are *arysleep*, *sbc[1:0]*, *pshutoff*, *shutoff*, and *shutoffout*.
- Row redundancy (*redrowen[1:0]*) pins are only available for "r2" compiler instance builds.

Table 3. Pin/Port Interface List for P1276 Memory Blocks

Pin Name	Direction	Signal Type	Active/ Polarity	Description
clk	Input	Functional	H/L	Clock input
adr[log$_2$***NW***-1:0]	Input	Functional	H/L	Read/Write Address, ***NW*** = Number of word entries.
ren	Input	Functional	H	Read Enable; if "1", a Read is performed at adr[log$_2$NW-1:0]. Should not be high if ***wen***=”1” within setup time window.
wen	Input	Functional	H	Write Enable; if "1", a Write is performed at adr[log$_2$NW-1:0]. Should not be high if ***ren***=”1” within setup time window.
din[***NB***-1:0]	Input	Functional	H/L	Data to be written at memory address adr[log$_2$***NW***-1:0] when wen ="1". ***NB*** = Number of bits.
wbe_b[***NBYTE***-1:0]	Input	Functional	L	Bit or Byte Write Enable, no mixed bit/byte enables. A bit/byte is written only if the corresponding enable is "0". Note Byte Enable is done in DFx wrapper. For byte enable, ***NBYTE*** = Number of byte enables (e.g. 32 bits, 8 bits per byte enable -> ***NBYTE*** = 4). For bit enable, ***NBYTE*** = Number of bits (e.g. 32 bits, bit enable -> ***NBYTE*** = 32).
q[***NB***-1:0]	Output	Functional	H/L	Data read from memory address adr[log$_2$NW-1:0] when ren="1". ***NB*** = Number of bits.
arysleep	Input	PMU	H	Value of "1" enables array sleep feature. "0" disables it. **This pin has built-in reset function for internal self-timed clock.**
shutoff	Input	PMU	H	Power gate signal. If "1", SRAM is power gated and outputs are firewalled.
pshutoff	Input	PMU	H	Value of "1" enables deep sleep feature if arysleep=1 or periphery sleep if arysleep=0.
shutoffout	Output	PMU	H	Output power gate signal. A toggle will occur on the pin after the shutoff pin is switched so that memories can be daisy chained together to mitigate high inrush current during shutdown recovery. Shutoffout falling edge reflects the delay of the power gate daisy chain but does not ensure the memory is fully powered up.
async_reset	Input	PMU	H	Async_reset enable signal. "0" during normal active operation; Value of "1" resets the data outputs. **This pin has built-in reset function for internal self-timed clock.**
sbc[1:0]	Input	FUSE		Sleep bias level control bus for when arysleep=1.
mce	Input	FUSE		Enables pin programmable control of timing margin settings, references default value supporting all operating voltages when set to 0.
rmce[3]	Input	FUSE		Internal min-delay timing margin fuse.
rmce[2:0]	Input	FUSE		Read margin control bus.
wmce[1:0]	Input	FUSE		Write margin control bus.
ra[1:0]	Input	FUSE		Read assist level control bus.
wa[2:0]	Input	FUSE		Write assist level control bus
wpulse[2:0]	Input	FUSE		Write pulse duration control bus.
stbyp	Input	FUSE		Overrides self-timed clocking to support debug. Forces the read to occur at falling edge of clock *clk*.
vddp	Input	Supply	H	Memory periphery power supply – always included. Connected to array for single rail supply configurations.
vss	Input	Supply	L	Common ground.

1.5 Configuration Options

The following options in Table 4 are configurable using Fuses or Control and Status Registers. The "[**Safe power-up**]" setting in blue color font is used for first-time silicon power-up. After first-time silicon power-up debug is successful, the "**Recommended Standard Setting**" in green color font should be used.

Configuration pins should **NEVER** be tied off to ground with the intention of reducing the number of Fuses/CSRs. They are configurable for a reason; as more silicon data becomes available, the recommended standard settings and safe power-up setting may change. Please re-check Table 4 every time a new revision to the integration guide is released as pin updates may occur.

Table 4. Configuration Pin Description

Pin Name	Functionality	State Description	Safe Silicon Power-up
sbc[1:0]	Used to program sleep strength to control array retention supply voltage.	[00] – safe power-up setting [01] – conservative setting [10] – setting for Vddp >=0.75V [11] – setting for vddp >=0.85V *PME enabled instances only.	[*00*]
wpulse[2:0]	Enables/disables write-assist circuit and controls SRAMVCC droop pulsewidth for write-assist.	[001] - Gives shortest pulsewidth [000] - Gives 2nd shortest pulsewidth [010] - Gives 2nd longest pulsewidth [011] - Gives longest pulsewidth [1xx] - Disables write-assist circuit	[*000*]
mce	Margin Control Enable	[0] – Hardwired to optimal read/write margin setting [1] – Disables overrides, allows *mce pins to be toggled	[*0*]
wmce[1:0]	Controls WLKILL/RCVR timing	[11] - Enables shortest delay [10] - Next shortest delay [01] - Long delay [00] - Enables longest delay	[*00*]
rmce[3]	Internal Min-delay Timing Margin	[0] – Default optimized timing [1] – Added delay for improved internal min-delay margins	[*0*]
rmce[2:0]	Controls sense-amp enable timing in debug mode	[000] – Slowest tracker setting with largest SA differential [010] - Slower tracker setting [100] - Slow tracker setting [001] - Slow tracker setting [110] - Fast tracker setting [011] - Fast tracker setting [101] - Faster tracker setting [111] – Fastest tracker setting with smallest SA differential	[*000*]
wa[2:0]	Controls SRAMVCC droop level during Write Assist.	[001] – Strongest write assist [000] – 2nd strongest write assist [011] – 2nd weakest write assist [010] – Weakest write assist	[*000*]
ra[1:0]	Controls WL voltage droop during Read Assist.	[11] – Weakest read assist [01] - 2nd Weakest RA, TMG [10] – 2nd Strongest RA, TMG [00] - Strongest read assist	[*00*]
stbyp	Debug mode	[0] – Self time [1] – Burn-in synchronous mode	[*0*]

1.5.1 Timing Modes

The HDUSPSR compiler includes various timing modes to offer benefits in integration flexibility and timing optimization. In most cases, the HDUSPSR compiler is used at or above 0.65V for a wide temperature range and the TM1 (default) setting would be applicable. However, other timing settings such as TM2 offers lower Vmin and TM3 offer unique setting for high performance requirement. Timing mode descriptions:

- **MCE=0** (TM1): Disables margin control enable (MCE). When MCE=0, the (rmce, wpulse, wmce) pins will be overridden to the ***TM1*** setting which as shown in the table below.
- **TM0**: Self-Timed Debug (safe slower setting). Not characterized.
- **TM1**: Supports full functional spec across full temperature range and voltages equal or greater than 0.65V. Converged for TTTT and all R-scale corners (90%-ile per AD guideline).
- **TM2**: Low Vmin setting that supports projects with ITD capability and binning. Converged at 0.55V to 1.1V and 100C to 125C with TTTT/RFSF/RFFS/RFFF (50%-ile per AD guideline). Without ITD, the design is converged at 0.7V to 1.1V and full temperature range for TTTT and all R-scale corners (90%-ile per AD guideline).
- **TM3**: High performance setting that supports projects with ITD capability and binning. Converged at 0.65V to 1.1V and 100C to 125C with TTTT/RFSF/RFFS/RFFF (50%-ile per AD guideline). Without ITD, the design is converged at 0.8V to 1.1V and full temperature range for TTTT and R-scale corners (90%-ile per AD guideline).

Table 5. HDUSPSR Timing Mode Settings

Description		Timing Mode Setting				
		MCE=0	TM0	TM1 (Default)	TM2	TM3*
Configuration Pin	mce	0	1	1	1	1
	rmce[3:0]	- - - -	0000	0011	0001	0101
	wpulse[2:0]	- - -	001	001	001	001
	wmce[1:0]	- - -	10	11	11	11
	wa[2:0]	- - -	011	011	000	000
	ra[1:0]	- - -	01	01	01	01
	stbyp	0	0	0	0	0
Voltage Range (V)		0.65 to 1.1	Vmin to 1.1	0.65 to 1.1	0.7 to 1.1	0.8 to 1.1
Temperature Range (C)		-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Read/write/pulsewidth analysis		TTTT, R*[1]	TTTT, R*[1]	TTTT, R*[1]	TTTT, R*[1]	TTTT, R*[1]
ITD Compensation		No	No	No	Yes	Yes
TTTT Hot Only	Voltage Range (V)				0.55 to 1.1	0.65 to 1.1
	Temp. Range (C)				100 to 125	100 to 125
	Converged PVTs				TTTT/RF*	TTTT/RF*

ITD = Inverse Temperature Dependence
*1: systematic sigma=1.96 and random sigma=5.68 per AD guideline

Due to the fact that several timing mode configurations are available for memories operating at or above 0.65V, the timing .lib syntax contains the use of conditionals as outlined in Table 6. Each .lib file will contain SDF conditional statements associated with valid timing mode (TM1, TM2 and TM3) for a given voltage/temperature band but will default to TM100 if an invalid condition is selected. The TM100 timing returns "out of bounds" values (e.g. >100 ns) that are intended to highlight an erroneous TM selection issue at the integration level. For TMIN timing .libs, there are no conditional statements.

Table 6. Liberty File Timing Mode Contents

Liberty File Name	Conditional .lib	Timing Content	Power Content	TM1	TM2	TM3	TM100
tttt_0.55v_0.55v_100c_tttt.lib	No	Yes	Yes	TM100 Timing	TM2 Timing	TM100 Timing	TM100 Timing
tttt_0.65v_0.65v_100c_tttt.lib	Yes	Yes	Yes	TM1 Timing	TM2 Timing	TM3 Timing	TM100 Timing
tttt_0.65v_0.65v_-40c_tttt.lib	Yes	Yes		TM1 Timing	TM2 Timing	TM100 Timing	TM100 Timing
tttt_0.85v_0.85v_100c_tttt.lib	Yes	Yes	Yes	TM1 Timing	TM2 Timing	TM3 Timing	TM100 Timing

tttt_0.85v_0.85v_-40c_tttt.lib	Yes	Yes		TM1 Timing	TM2 Timing	TM3 Timing	TM100 Timing
tttt_1.1v_1.1v_100c_tttt.lib	Yes	Yes	Yes	TM1 Timing	TM2 Timing	TM3 Timing	TM100 Timing
tttt_1.1v_1.1v_-40c_tttt.lib	Yes	Yes		TM1 Timing	TM2 Timing	TM3 Timing	TM100 Timing
tmin_0.55v_0.55v_100c_tttt.lib	No	Yes			*see note		
tmin_0.65v_0.65v_100c_tttt.lib	No	Yes				*see note	
tmin_0.65v_0.65v_-40c_tttt.lib	No	Yes		*see note			
tmin_0.85v_0.85v_100c_tttt.lib	No	Yes				*see note	
tmin_0.85v_0.85v_-40c_tttt.lib	No	Yes				*see note	
tmin_1.1v_1.1v_100c_tttt.lib	No	Yes				*see note	
tmin_1.1v_1.1v_-40c_tttt.lib	No	Yes				*see note	

* TMIN .libs (hold convergence) represent the fasted available timing mode for a given voltage band

1.6 Address Space

The address bus breakdown for column **mux 4** instances is:
adr [*X*:6][*4:2*] → selects word lines, where *X*=($\log_2$***NW***)-1 rounded up
adr [5] → value of `0' selects right side, `1' selects left side
adr [1:0] → selects bitlines[3:0]

The address bus breakdown for column **mux 8** instances is:
adr [*X*:7],[5:3] → selects word lines, where *X*=($\log_2$***NW***)-1 rounded up
adr [6] → value of `0' selects right side, `1' selects left side
adr [2:0] → selects bitlines[7:0]

If an instance does not contain a power of two address space, then some addresses combinations will point to locations without bitcells. Reading of these locations will return random data. Reading and writing to the phantom locations will consume about the same current as accessing a valid location. For example, take the address space of instance ip7631hduspsr1536x32m4b2s1r0p1d0:

[($\log_2$***NW***)-1:0] = [($\log_2$***1536***)-1:0] → adr [10:0]

This column mux4 SRAM has 192 rows per bank (butterfly architecture = 2 banks per block), but the address pins will cover up to 256 rows per bank. Therefore, the rows 193-256 will be "phantom" and unused.

1.7 Timing Waveforms for Read and Write

The following diagrams show the Read and Write Timing Waveforms. All timing events are referenced off the rising edge of the clock *clk*. Memory read occurs from the selected address when read enable *ren* is asserted during high phase of the clock (Figure 2). Memory write happens to the selected address when write enable *wen* is asserted during high phase of the clock (Figure 3).

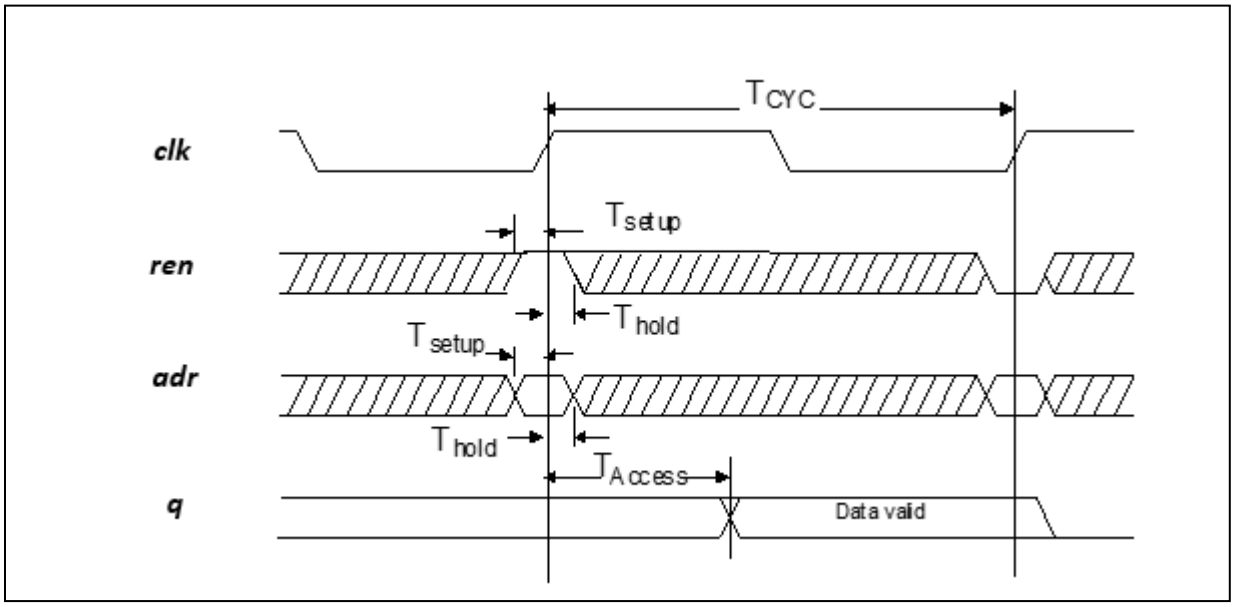

Figure 2. Read Timing Waveform

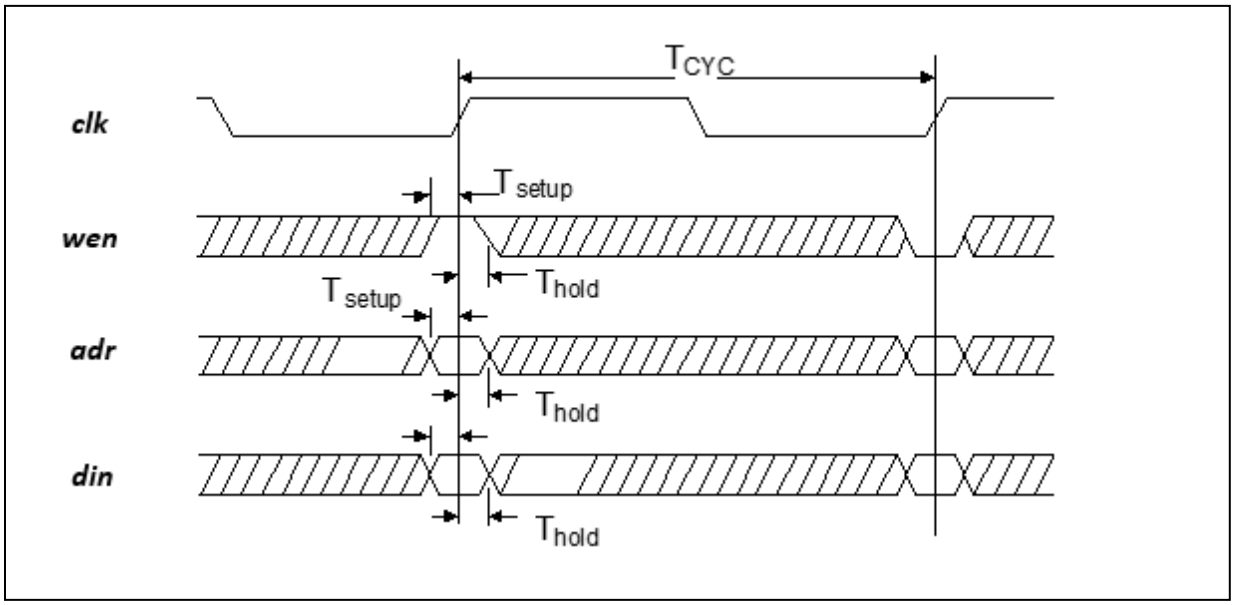

Figure 3. Write Timing Waveform

1.8 Collateral Views Provided

Listed in Table 7 are a few example collateral views that will be available for P1276 SRAMs according to release maturity. More detailed information on collateral views and directory structure can be found in the separate ip76*_RELEASE_NOTES.txt file.

Table 7. SRAM Design Collateral Views

#	EDA View	EV	UV	FV
1	Verilog / RTL, including UPF support	Yes	Yes	Yes
2	LEF (.lef)	Yes	Yes	Yes
3	Liberty NLDM (.lib), including UPF and POCV Support	Yes	Yes	Yes
4	CCSN: HDK compliant (ccsn.lib)	-	-	Yes
5	LVS netlist (.sp)	-	Yes	Yes
6	Layout (oasis)	-	Yes	Yes
7	Tessent (LVLib), Logical to physical map	Yes	Yes	Yes
8	Fastscan (Mentor ATPG)	Yes	Yes	Yes
9	Datasheet (<pvt>_datasheet.txt)	Yes	Yes	Yes
10	Databook (.pdf)	Yes	Yes	Yes
11	Model Guide for RTL including DFX wrapper (.pdf)	Yes	Yes	Yes
12	MOSFET Info File (.mosfet_info)	-	-	Yes
13	FAFI bit map support (_mbist.map, _spbist.map)	-	-	Yes

1.9 PVT Corners and LIB syntax

Timing LIB files are named with the process/voltage/temperature (PVT) scheme shown in Table 8, where the PVT corners are specific to each project.

Table 8. Timing LIB naming syntax as a function of PVT
(EXAMPLE ONLY)

vddp *Interface** (V)	Process	Temp (C)	LIB Name
VDDP	TTTT	temp	{blockname}_skew_vddp_vddp_temp.lib
0.75	TTTT	70	{blockname}_tttt_0.75v_0.75v_70c.lib

* vddp supplies power to the partition logic

1.10 SRAM Power Management

1.10.1 Power Supplies

The input supply rail is named vddp.

SOC needs to provide robust power delivery to SRAM to ensure IR drop is within limits. While connecting SRAM M5 power ports to partition M6 power rails, VIA5 need to be dropped at every M5/M6 intersection. Special attention needs to be paid to extra M5 power rails over the power switches (a.k.a power-gate) where most of the current draw occurs.

1.10.2 Power Saving Mode

NOTE: This following section only applies to power management enabled (PME) SRAMs. The "p1" instance naming notation means the SRAM supports PME.

Power management enabled SRAMs offer periphery sleep (*pshutoff*), array sleep (*arysleep*), deep sleep (*arysleep + pshutoff*) and a full shutoff (*shutoff*) states to save power. Stored array data are retained in the "sleep" states but are lost in the "shutoff" state. Definitions are as follows.

All configurations:

- **Active Mode** - SRAMs perform read, write and idle operations. All logic and bitcell arrays are fully powered on.

PG Configurations Only:

- **Periphery Sleep** (*pshutoff*) – Periphery is power gated off to save leakage. The bitcell array is still powered up at full supply voltage
- **Array Sleep** (*arysleep*) - SRAM bitcell array goes into a sleep state. An internal sleep circuit lowers the bitcell array internal power rail (SRAMVCC) to a voltage above a predefined retention Vmin level (TD/TMG spec). ***Note: arysleep can only be asserted when vddp >= 0.75v.***
- **Deep Sleep** (*arysleep + pshutoff*) – The periphery is power gated off to save leakage. The bitcell array is still powered and in sleep mode. ***Note: arysleep can only be asserted when vddp >= 0.75v.***
- **Shutdown** (*shutoff*) – SRAM is power gated off: all internal power rails collapse and array data is lost.

Table 9 shows that PME specific pins are not available for no-power-gate builds of the compiler.

Table 9. HDUSPSR Compiler Power Management Features

MODE	Pin(s)	Power-Gate Option Support	
		NPG (p0)	PG (p1)
Periphery shutoff	pshutoff	NO	YES
Array Sleep	arysleep, sbc[1:0]	NO	YES
Deep Sleep	pshutoff, arysleep	NO	YES
Shutoff	shutoff	NO	YES
Shutoff Output	*shutoffout*	NO	YES

HDUSPSR SRAMs (with PME enabled) have built-in distributed power switches which gate power to internal power rails. The un-gated *vddp* power supply ports are on M5 and will be connected up to M6 at the partition level through Via5. The gated power supply is completely internal to the SRAM and distributed in M2/M3/M4. Power switches are daisy-chained inside the SRAM to reduce di/dt current during power-up. The *pshutoff* signal controls only the periphery logic power gates and the *shutoff* signal control both the periphery and array power gates. The *shutoff* power gate signal goes through an internal delay chain which is then output as *shutoffout* signal.

To reduce rush current at the SOC level, daisy-chaining of the shutoff pin of the SRAMs (by tying *shutoffout* from one SRAM to the *shutoff* of the next SRAM) inside each partition or unit is recommended. Asserting *shutoff* high shuts down power to the entire SRAM including array and periphery. This will ensure that the current profiles associated with *shutoffout*→*shutoffout* sequencing work as intended. In other words, this will power up or wake up each SRAM in the series chain to reduce power up di/dt. In case of multiple SRAMs waking up from array sleep or deep sleep states, we recommend staggering individual SRAMs waking up using external delay chains or latches for *arysleep and pshutoff* signals. Refer to the timing lib for the exact wake up latency, setup and hold times.

Table 10 below shows the availability of pins for various configurations.

Table 10. P1276 Compiler Pin Options

	SINGLE RAIL	
PIN	**NPG**	**PG**
async_reset	YES	YES
shutoff	NO	YES
shutoffout	NO	YES
pshutoff	NO	YES
arysleep	(tied off in softwrapper)	YES
sbc[1:0]	(tied off in softwrapper)	YES
vddp	YES	YES

1.10.3 Array Sleep Settings

As stated multiple times, the power modes that support array sleep should only be used at 0.75V or above. The *sbc[1:0]* pins determine the strength the bitcell voltage reduction and are tuned for specific voltage ranges as shown in Table 11.

Table 11. Supported Array Sleep Settings

sbc[1]	sbc[0]	Voltage Range Support	Setting Description
0	0	0.75V to 1.1V	Conservative
0	1	0.75V to 1.1V	Conservative
1	0	0.75V to 1.1V	Optimized for >=0.75V
1	1	0.85V to 1.1V	Optimized for >=0.85V

1.10.4 Allowable Power Scenarios

Table 12 shows the range of power scenarios that are either supported or not supported by the P1276 HDUSPSR SRAMs. Descriptions of the allowable power scenarios are given in subsequent sections.

Table 12 also shows the static state of the various power modes but not the transition in and out of these modes. Please refer to the subsequent waveforms for more details.

Table 12. Supported Power States for P1276 SRAMs

Power Scenario		1	2	3	4	5
Power Mode		**Active**	**Periphery Sleep**	**Array Sleep**	**Deep Sleep**	**Shutoff**
Requires PG 'p1' build?		**No**	**Yes**	**Yes**	**Yes**	**Yes**
Supported Voltage Range (V)		0.55 to 1.1	0.55 to 1.1	0.75 to 1.1	0.75 to 1.1	0.55 to 1.1
Date Output (1)		1/0	0 (forced)	1/0	0 (forced)	0 (forced)
Internal Power Rail States	Vcc (Bitcell)	On	On	Array sleep	Array sleep	Off
	Vcc (Periphery logic)	On	Off (Gated)	On	Off (Gated)	Off (Gated)
	Vcc (Array logic)	On	On	On	On	Off (Gated)
SRAM PME inputs[2]	*Arysleep*[2]	0	0	1	1	0 /1
	pshutoff	0	1	0	1	0/1
	shutoff	0	0	0	0	1
	sbc[1:0]	00-11	00-11	00-11	00-11	00-11

[1] *arysleep* usage requires that the primary voltage rail is >= 0.75V

[2] PME (power mode enable) pins should always be on the "always on domain" and can't go 'X' in these scenarios. These include: shutoff, pshutoff, arysleep, sbc[1:0].

1.10.4.1 Power Scenario 1 (Active, PG/NPG configurations)

The SRAMs perform read, write and idle operations. All periphery devices and bitcell arrays are fully powered.

1.10.4.2 Power Scenario 2 (Periphery sleep, PG configurations only)

The waveforms in Figure 4 show the typical active and periphery sleep operation forP1276 SRAMs. In this mode, the internal Vccsram is powered up (*shutoff*=0). SRAMs in active mode are reading, writing, or idling. During the transition from active to sleep ($\mathbf{T_{AS}}$), the *pshutoff* pin needs to be enabled high '1' following the last read/write cycle. This powergates the periphery in the SRAM sub-blocks to save leakage. In addition, the output data latches reset to '0'.

For the transition from periphery sleep to active, the wake time ($\mathbf{T_{WK}}$) is given in the lib file to insure that all the internal array power rails and bit lines are fully pre-charged up. (Refer to the timing lib for the exact wake up latency.)

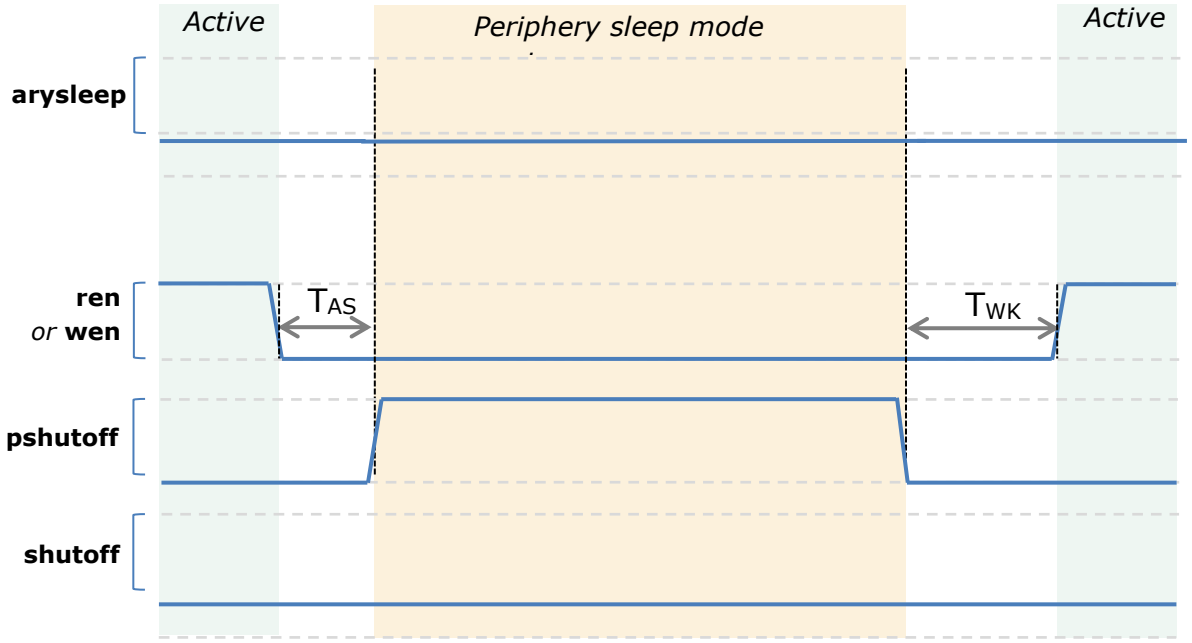

Figure 4. Scenario 2 – Transitions between active/periphery sleep modes

1.10.4.3 Power Scenario 3 (Array Sleep, PG configurations only)

The waveforms in Figure 5 show the typical active and array sleep operation for P1276 SRAMs. In the active mode, the internal Vccsram is powered up (*shutoff*=0, *pshutoff*=0). SRAMs in active mode are reading, writing, or idling. During the transition from active to sleep ($\mathbf{T_{AS}}$), the *arysleep* pin needs to be enabled high '1' following the last read/write cycle.

For the transition from sleep to active, the wake time ($\mathbf{T_{WK}}$) should follow timing lib to insure that all the internal array power rails and bitlines are fully recharged up. ***Sleep operation is not allowed for supply voltages less than 0.75v as this leads to array supply going below the minimum retention levels and memory losing stored data.***

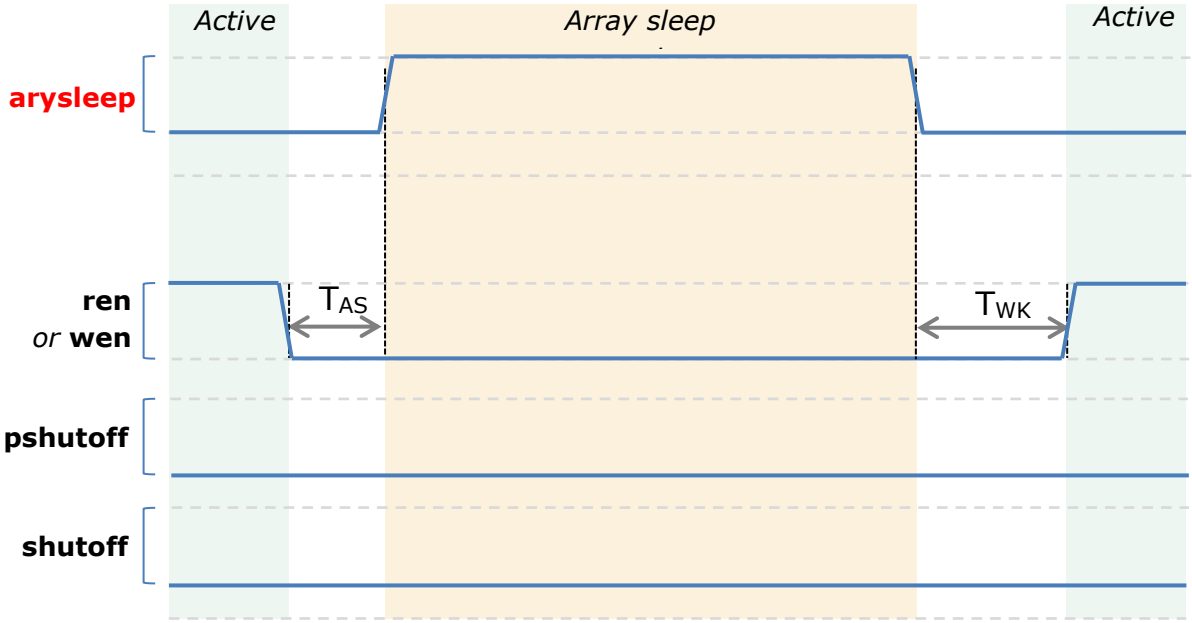

Figure 5. Scenario 3 – Transitions between active/array sleep modes

1.10.4.4 Power Scenario 4 (Deep sleep, PG configurations only)

As stated in Figure 6, in deep sleep scenario, both the peripheral (pshutoff is asserted) and the array (arysleep is asserted) are put to sleep. The waveforms in show the typical active and deep sleep operation forP1276 SRAMs. In this mode, the internal Vccsram is powered up (*shutoff*=0). SRAMs in active mode are reading, writing, or idling. During the transition from active to sleep (**T_{AS}**), the *pshutoff* pin needs to be enabled high '1' following the last read/write cycle. This powergates the periphery in the SRAM sub-blocks to save leakage. In addition, the output data latches reset to '0'. The powergating of the periphery and the sleep mode of the array result in "deep sleep."

For the transition from deep sleep to active, the wake time (**T_{WK}**) is given in the lib file to insure that all the internal array power rails and bit lines are fully pre-charged up. (Refer to the timing lib for the exact wake up latency.)

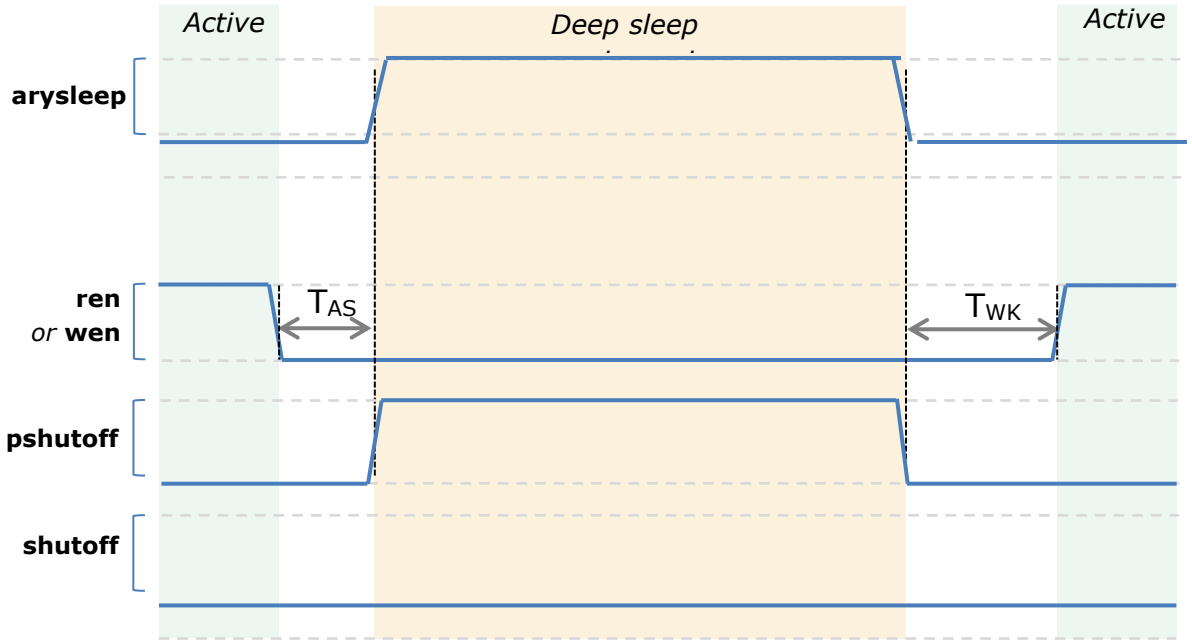

Figure 6. Scenario 4 – Transitions between active/deep sleep modes

1.10.4.5 Power Scenario 5 – Shutdown (PG configurations only)

During shutdown mode, see in Figure 7, the Vccsoc rail *vddp* is powergated and the bitcells and periphery are shut off. In addition, the output data latches reset to '0'. vddp is gated inside the SRAM using distributed power switches that are controlled by *shutoff*. The power switches are daisy-chained inside the SRAM to reduce *di/dt* during power-up. The delayed version of *shutoff* is output as the *shutoffout* signal; this enables multiple SRAMs at the unit level to have a staggered power-up to further reduce peak current.

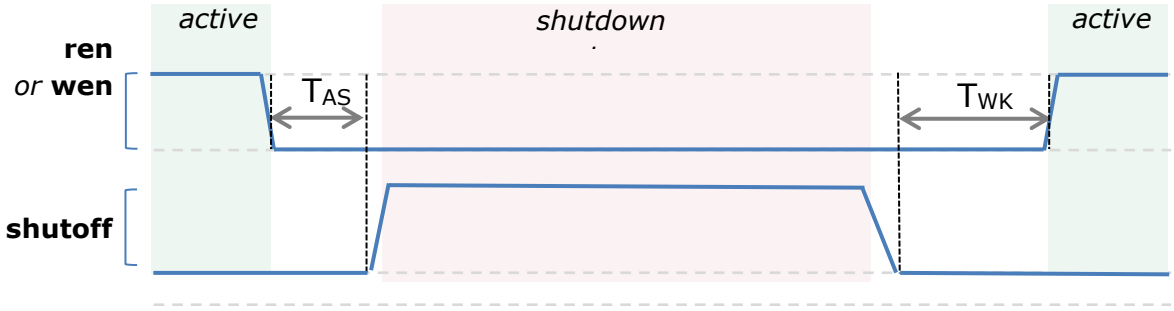

Figure 7. Scenario 5 – Transitions between active/shutdown modes

1.10.5 Power Domain Diagrams

1.10.7.1 Single Rail, Power Gated Build

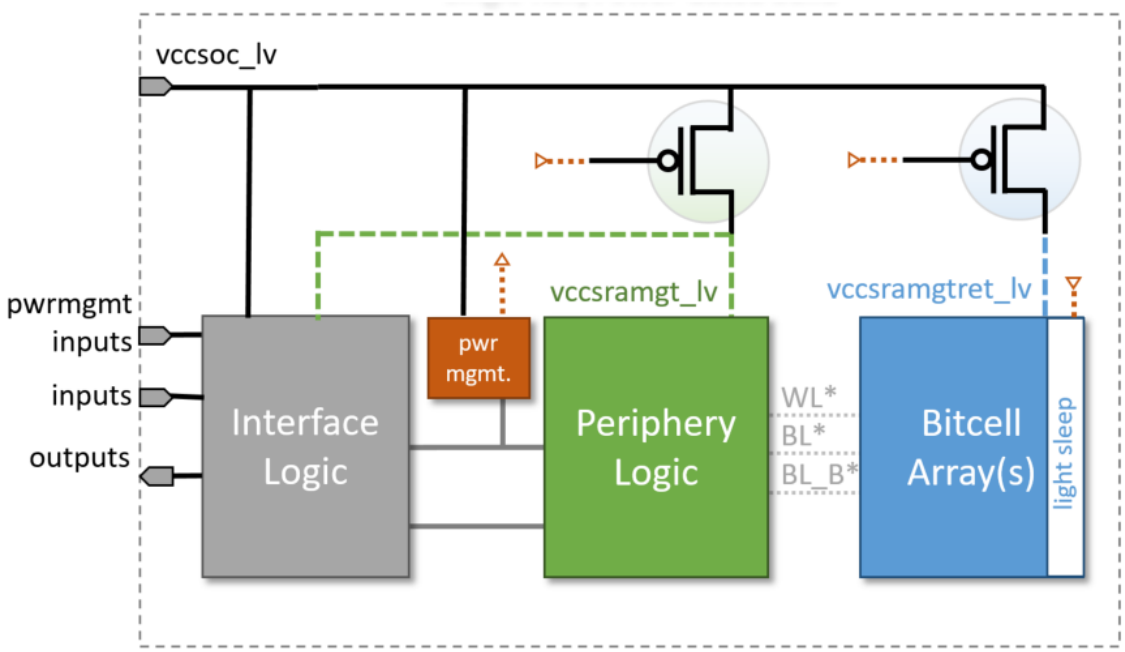

Figure 8. Single Rail, Power Gated Build

1.10.7.2 Single Rail, No Power Gates Build

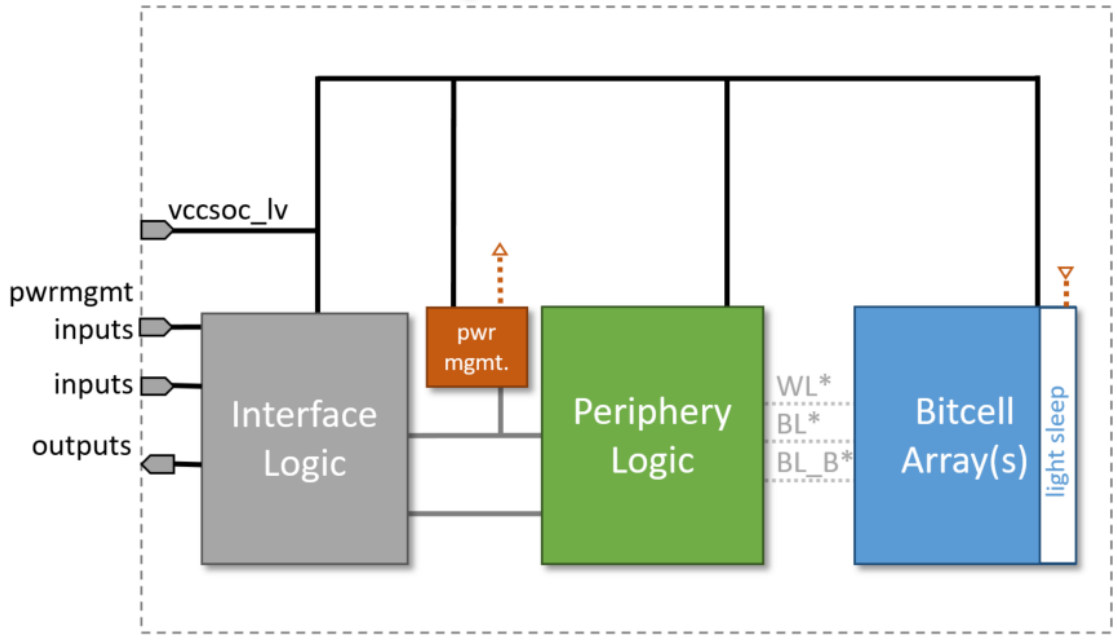

Figure 9. Single Rail, No Power Gates Build

1.11 Self-Timed Bypass Mode

P1276 HDUSPSR SRAMs feature a Self-Timed Design where the internal operation is independent of the falling edge of input clock ***clk***. To stress the design at extreme conditions, there is a Self-Timed Bypass mode where the falling edge of input clock decides the internal timing and sequence of operations. This allows relaxed internal pulse widths and margins which increase directly with the pulse width of input clock. This mode enables the SRAM to be functional at HVQK burn in conditions (TTTT 1.4V 110C) and is selected by setting ***stbyp*** pin to 1 as shown in Table 4.

1.12 SRAM Repair

The ***ip76*_Model_Guide.pdf*** describes the specifications, implementation and functionality of the repair options. SRAM repair guidelines vary between projects and are based on a variety of factors such as unit memory size, process, operating voltage, temperature (PVT) and more. Each project should consult their product quality, reliability and engineering (QRE) team and TD/TMG for specific repair guidelines to meet yield and VccMin distribution goals.

1.13 DFX Wrapper

Details on wrapper interfaces can be found in the ***ip76*_Model_Guide.pdf*** documentation.

2 Physical Integration Guidelines

2.1 SRAM Floor plan & Layout

SRAMs are constructed using a compiler/tiling tool. The following top level supercells are used to build the SRAMs with placement floorplan shown in Figure 10:

ARRAY/IO: bit-cells, sense amp and other column circuits producing one I/O information

WLDRV: contains decode and final WLDRV logic

TIMER: generates necessary clocks for the SRAM operation; The Timer is built with 8DG standard cell library.

Halo: The yellow outline are the halos. SRAMs are built with a halo ring on the periphery, which provides the transition between SRAM and standard cell logic. The design is compliant to AURA Halo methodology defined in ***P1276.4 PDK0.5 Layout Design Rules (IRCS#60758)*** and is backward compatible with 720/960 Halo HIP boundary rules defined in ***P1276.4 Hard IP Physical Integration Requirements (IRCS#60564)*** Redbook ratified in ***P1276 Physical Integration WG*** (Chair: Allen Bodin and Luis Cuellar).

HDUSPSR SRAMs are also built with the following top-level specifications:

- These SRAMs follow P1276 diffusion grid (DG) of 30 nm, and poly pitch (PP) of 50nm.
- The HIP width and height must be integer multiples of modular grid (MDG) width (OGD) and height (PGD).
  - The MDG is 300nm (OGD) X 240nm (PDG).
- SRAMs have M5 ports for signals and power.
- All M5 will be backed off by 90nm from the IP boundary.
- The HIP signal and power ports are not required to be centered along any ASIC wire tracks.
- M5 signal port widths can be any legal M5 widths defined in ***P1276.4 Hard IP Physical Integration Requirements (IRCS#60564)*** Redbook.
- All signal ports meet port length and placement requirements defined in ***P1276.4 Hard IP Physical Integration Requirements (IRCS#60564)*** Redbook.
- SRAM is completely filled up to M5, and Via5 and above are usable by full-chip integration.

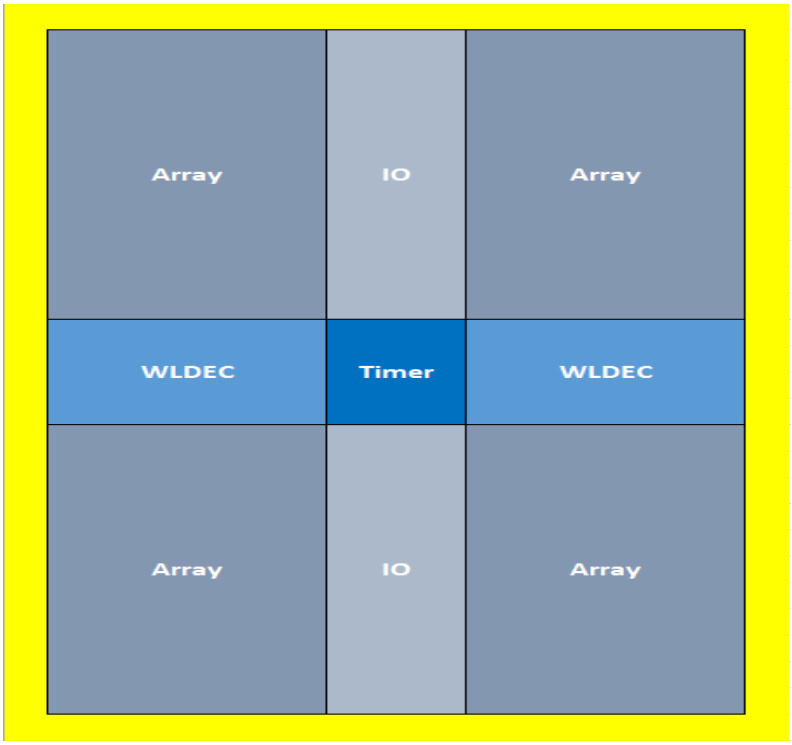

Figure 10 SRAM Floor plan for entries: <=2048 mux4, <= 4096 mux8 (BF example)

2.2 Halo Descriptions

The halo solution compliant to AURA Halo methodology with depopulated boundary wires, designed to be backward compatible with 720/960 LEGO boundary spec requirements. All requirements are fully compliant to ***P1276.4 PDK0.5 Layout Design Rules (IRCS#60758)*** Redbook and checked by TD runsets.

2.3 SRAM Hard Intellectual Property (HIP) Top Level Guidelines

- Each HIP aligns to the following width and height guidelines:
  - Width is divisible by 0.3 microns
  - Height is divisible by 0.24 microns
- All input/output ports are on metal 5
- All power and ground ports are on metal 5
  - VDDP
  - VSS
- In single-rail configuration – VDDP and VSS:
  - M5 power rails will be placed in compliance to ***P1276.4 Hard IP Physical Integration Requirements (IRCS#60564)*** Redbook.
  - Additional M5 VDDP/VSS are added strategically over regions with poor M5 power/ground coverage.

- Each HIP is enclosed by HIP-level internal "halo" cells to ensure border conditions are clean to ***P1276.4 PDK0.5 Layout Design Rules (IRCS#60758)*** Redbook.

2.3.1 Abutment and Flipping

- Abutment in the X and Y directions are allowed for the SRAM HIP.
- The HIP is flip-able in both X and Y directions.

2.4 MOSFET Device Types Used

HVT, SVT and NOMINAL devices are used in the periphery (timer, IO, wldec).
NHPSRHCCU / PHPSRHCCU devices are used in the WPHCCU bitcell array.

2.5 Logical to Physical Mapping (L2P)

Each HDUSPSR instance may have 1 or 2 banks. The right most bank is always bank 0 as shown in Figure 11and Figure 12.

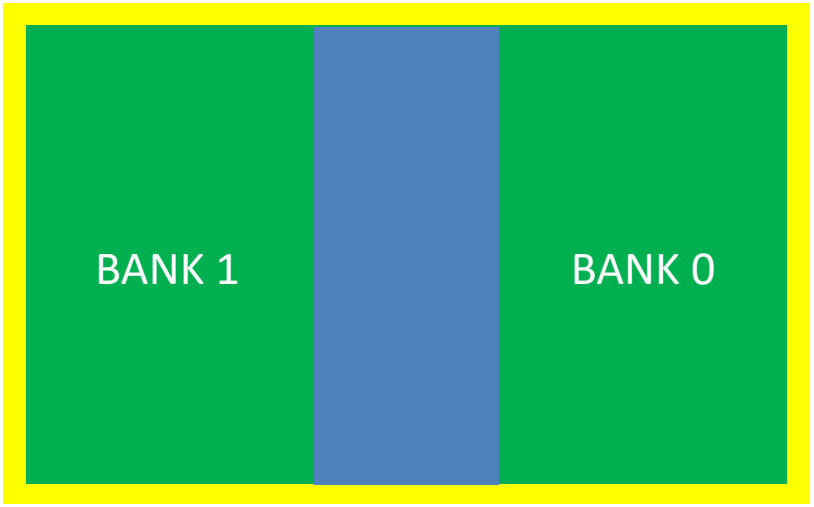

Figure 11. HDUSPSR 2 bank design

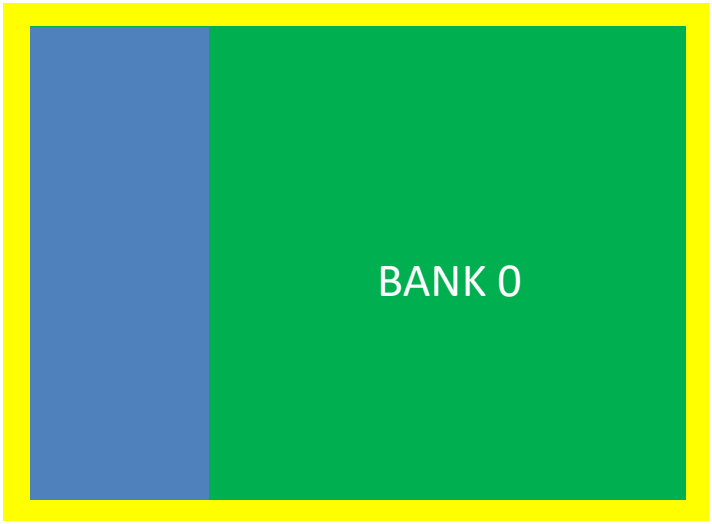

Figure 12. HDUSPSR 1 bank design

Each bank has a minimum of 32 rows and a maximum of 256 rows.

The supported column mux is 2, 4 and 8. In each row, the top most is column 0, and increments downwards. (See Figure 13)

Logical Bits Order:

The bottom most bit is bit 0 and the top most is MSB. (See Figure 13)

Address Bus Break down from MSB to LSB:

- **Row address MSB**: [1 to 5 bits], depending on memory size
- **Bank address**: [1 bit], selecting left or right bank.
- **Row address LSB**: [3 bits]. Ensure 8 row increment in each bank.
- **Column address**: [2 to 3 bits], depending on column mux selection.

Figure 13 shows the example of L2P mapping of a 4096x39m8b2r2 instance.

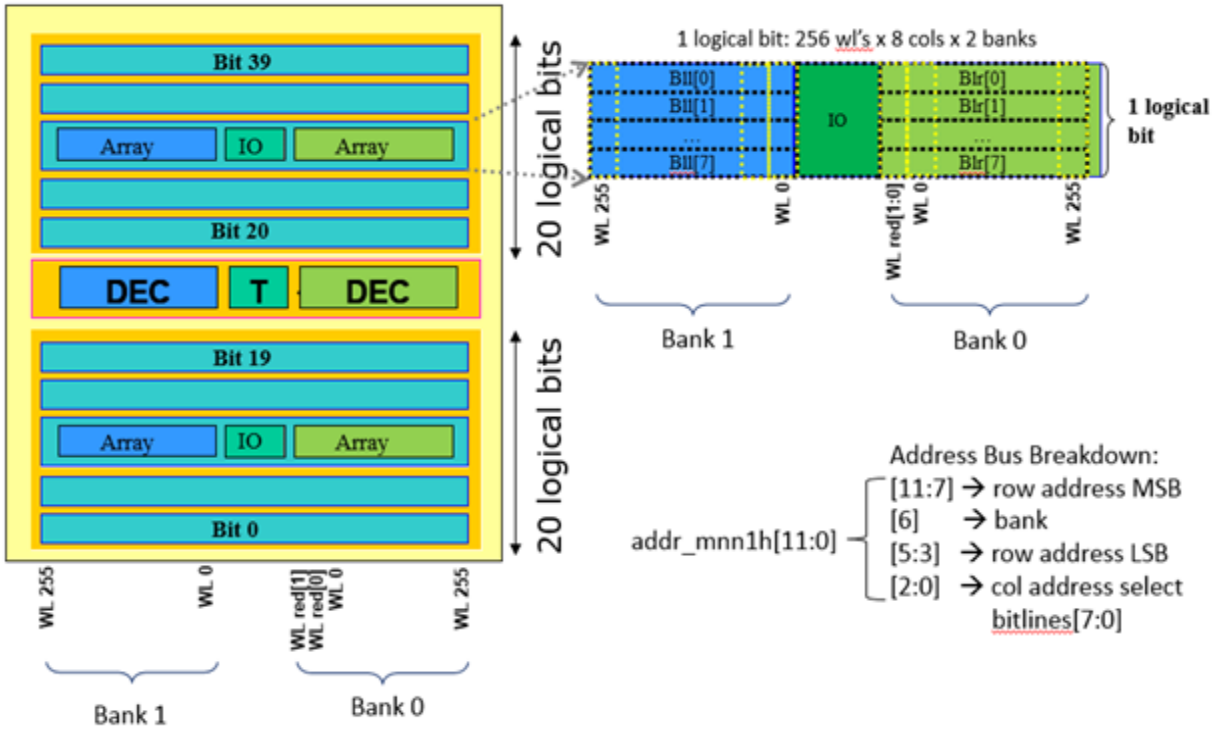

Figure 13. HDUSPSR 40 logical bits 4096x39m8b2r2

Figure 14 shows the example of L2P mapping of a 1024x79m4b1r2 instance.

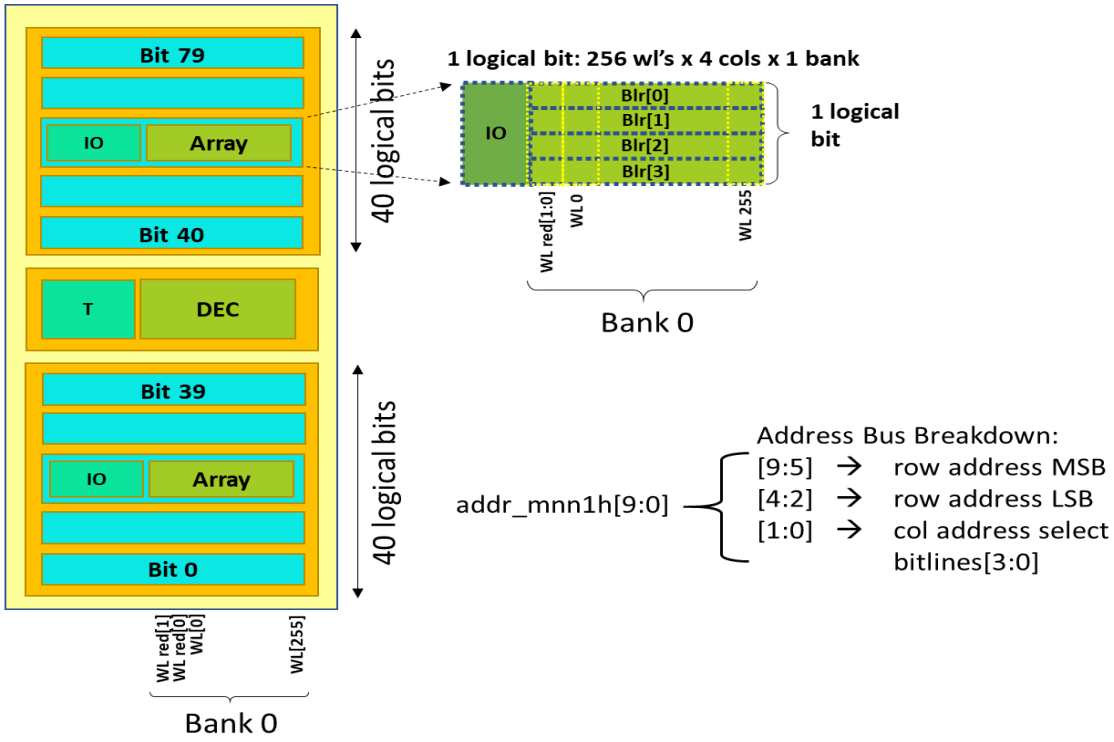

Figure 14. HDUSPSR 80 logical bits 1024x79m4b1r2

Figure 15 shows the example of L2P mapping of a 1024x159m2b1r2 instance.

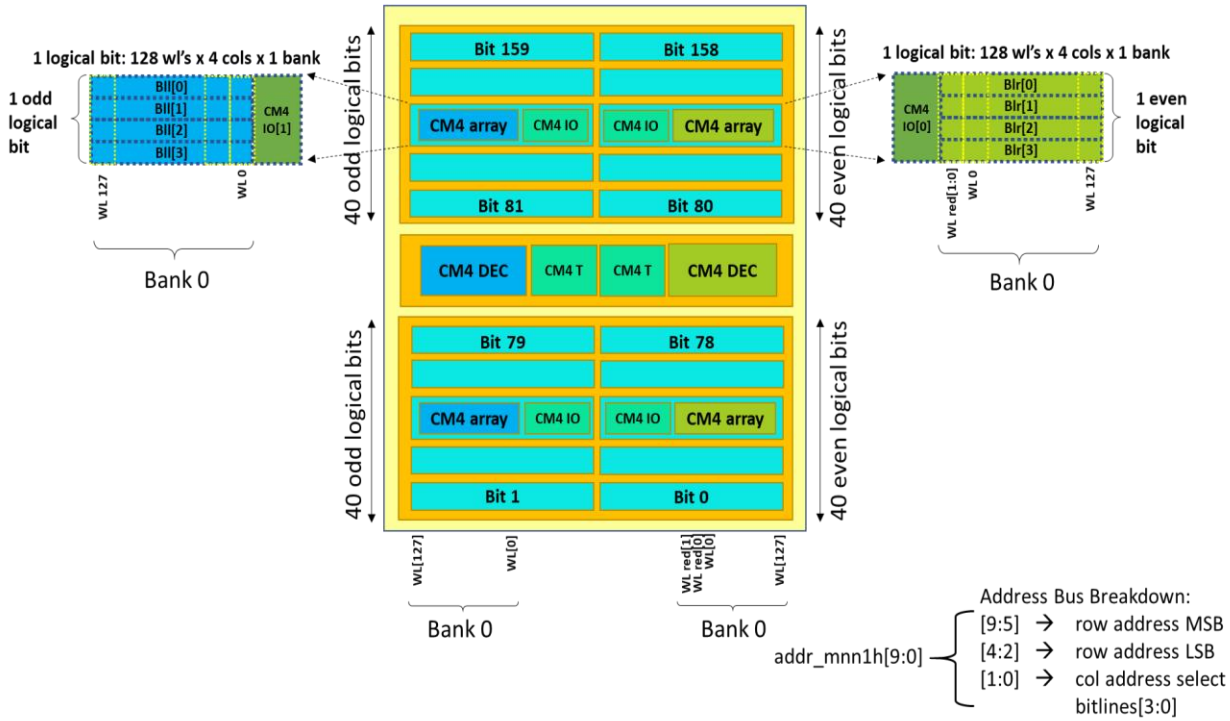

Figure 15. HDUSPSR 160 logical bits 1024x159m2b1r2