# PGCB + CDC Revision 1.23.4 Release Notes

## PGCB Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- [1805838597] - TFM update to MAT 1.5 and HDK 1.5 - TSA ver. 1813.18ww13d
  - Spyglass Lint tool enablement
  - Spyglass CDC tool enablement
- IPDS Score 99% with TFM HDK with MAT 1.5 / 1813.18ww13d

## CDC Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- [1406527877] - Fixed assertion for clkreq/clkack in ClockDomainController to reference the correct clock
- [1805838597] - TFM update to MAT 1.5 and HDK 1.5
  - Spyglass Lint tool enablement
  - Spyglass CDC tool enablement
- IPDS Score 99% with TFM HDK with MAT 1.5 / 1813.18ww13d

# PGCB + CDC Revision 1.23.3 Release Notes

## PGCB Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- [220410622] - TSA migrated to EIG1713.
- [1504401548] - Invalid file names causing turnin issue (issue found on some projects)- Fixed
- IPDS Score 99% with TFM HDK with MAT 1.05.02 / EIG1713.

## CDC Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- [220650395] – Asynchronous deassertion of SB reset during wam reset causes system failure (Global reset) –this is a future fix. There is a PMC/punit FW workaround for this issue, attached in the HSD, IRR and also copied in the drop in the following folder:

  PGCB_with_CDC_PIC0_2017WW41_R1.23.3_V0/doc/PGCB_CDC_Potential_Issue_and_FW_Workaround_for_Async_Reset_De-assertion_on_Warm_Reset_Exit.pptx
- [220410622] - TSA migrated to EIG1713.

- [1504401548] - Invalid file names causing turnin issue (issue found on some projects) - Fixed
- IPDS Score 99% with TFM HDK with MAT 1.05.02 / EIG1713.

**Refer to ZirconQA IP Dashboard for IPDS Scoring on this release:**
https://zircon.fm.intel.com/zircon/zirconIPDashboardTable.php?top_filter_checkbox=0&Proj_id=5663&IP_id=21764&milestone_filter=4&Ver_id=25&App_id=all&showlatest=0

# PGCB + CDC Revision 1.23.2 Release Notes

## PGCB Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- CDC Lint Enabled.
- IPDS Score 99% with TFM HDK with MAT 1.4.1 / EIG1639.

## CDC Changes:

**RTL Changes:**

- No Change.

**Doc/Assertion/Environment Changes:**

- CDC Lint Enabled.  CDC constraints updated.
- IPDS Score 99% with TFM HDK with MAT 1.4.1 / EIG1639.

Refer to ZirconQA IP Dashboard for IPDS Scoring on this release:
https://zircon.fm.intel.com/zircon/zirconIPDashboardTable.php?top_filter_checkbox=0&Proj_id=5663&IP_id=21764&milestone_filter=4&Ver_id=25&App_id=all&showlatest=0

*TSA 1.05.02/EIG1713 pending DTS tool issue resolution.

# PGCB + CDC Revision 1.23.1 Release Notes

## PGCB Changes:

**RTL Changes:**

- Updated Intel Copyright header per Lintra required regex.

**Doc/Assertion/Environment Changes:**

- TFM updated to HDK with MAT 1.4.1 / EIG1639. Refer to <IP_ROOT>/README.txt for more details.

## CDC Changes:

**RTL Changes:**

- Updated Intel Copyright header per Lintra required regex.

**Doc/Assertion/Environment Changes:**

- TFM updated to HDK with MAT 1.4.1 / EIG1639. Refer to <IP_ROOT>/README.txt for more details.

Refer to ZirconQA IP Dashboard for IPDS Scoring on this release:
https://zircon.fm.intel.com/zircon/zircon/zirconReleaseDashboardTable.php?top_filter_checkbox=0&Proj_id=13013&IP_id=21764&milestone_filter=4&Ver_id=25&App_id=1&showlatest=0

# PGCB + CDC Revision 1.23 Release Notes

## PGCB Changes:

**RTL Changes:**

- [1405184871] Enhancement - Add new SCAN DFT control signal to PGCB component.

**Doc/Assertion/Environment Changes:**

- [1404088966] Doc update - DFX override diagram update.

## CDC Changes:

**RTL Changes:**
There are no RTL changes to CDC.

**Doc/Assertion/Environment Changes:**

- [1604198999] – Assertion clock and sampled-value function $past clock did not match. Replaced clock with pgcb_clk.

# PGCB + CDC Revision 1.22 Release Notes

## PGCB Changes:

**There are no changes to PGCB.**

## CDC Changes:

**RTL Changes: Hotfixes to 1.21 release**

- [1504110638] Defect – For IPs with PGCB clock frequency faster than main clock only: CDC state machine could get stuck at CDC_OFF_PENDING state in case the CDC logic misses clkack negation before asserting next clkreq.
- [1604083741] Defect – Combo logic between clock domain crossing. In the meta-stability enhancement logic added in rev 1.21, a flop is missing for one signal crossing from PGCB to Main clock domain. There is a possibility that the signal can cause glitch and cause undesirable behavior.

**Doc/Assertion/Environment Changes:**.

- [1207792508] Assertion Enhancement – Relax assertion to avoid false fails during 3to1 meta-stability model simulation.
- [1404875888] Assertion Enhancement– Turn off X-prop checks on SVA behavioral codes. The assertions checks are still performed.

# PGCB + CDC Revision 1.21 Release Notes

## Common Changes:

**RTL Changes:**

- ❑ PGCB CTECH map file update – Meta-Stability Required Parameter and define changes.

**Doc/Assertion/Environment Changes:**

- ❑ [1404074824] Assertion improvements for reset awareness:
- ❑ Tool version upgrades
- ❑ Updated Lintra Waivers
- ❑ Updated CDC Waivers

## CDC Changes:

**RTL Changes:**

- ❑ [1404136840] Defect - CG_LOCK_ISM=1 and ISM_AGT_IS_NS=0: CDC component should assert ism_lock 1 clock earlier to lock agent ISM.
- ❑ [1206405592] Enhancement – Xprop tool compliant coding update. No functional change.
- ❑ [1503996414] Enhancement – Logic enhancement to avoid potential timing issue with PowerGateReady signal caused by meta-stability during IP-Accessible entry.
- ❑ [1504001217] Enhancement – Logic enhancement to prevent spurious unlock_all assertion during IP-Inaccessible entry due to meta-stability issue
- ❑ [1207621082] Enhancement - Potential race/deadlock condition due to unlock_ism signal (cdc_restore_pg) assertion could cause issue in CDC S/M

**Doc/Assertion/Environment Changes:**.

- ❑ [1504089630] aClkreq hold assertions in CdcMainClock fail if pgcb_reset_b

## PGCB Changes:

**RTL Changes:**

- ❑ [1404446776] Defect – 1.16 Hot Fix for BXT-E0 Warm Reset Bug: Changes related to support for synchronous reset support for Warm Reset flow.

**Doc/Assertion/Environment Changes:**

- ❑ [1404351430] PGCB asserts enhancement for config register value change.

# PGCB + CDC + PCGU Revision 1.20 Release Notes

## Approximate Normalized Gate Counts:

| Module | Approx. Gate Count |
|---|---|
| **Pgcbunit** | 900 |
| **ClockDomainController** | 1600 |
| **Pcgu** | 280 |
| **pcgu_aww** | 100 |

## Common Changes:

**Significant Changes:**

[2281759] Requirement - Provide .sig files for VISA insertion

- With this release of the PGCB blocks, we are providing .sig files to be used by the IP to insert VISA within the blocks using the VISA insertion tool. **The *_visa vector outputs are still available but it is recommended that IPs let them dangle and instead use the provided .sig files to enable easier silicon debug**.

[2267263] Requirement - Updated to SIP CTECH methodology – requires integrating IPs to include global CTECH libraries in their ACE environment

**Doc/Assertion/Environment Changes:**
[2392384] Replaced `ifdef ASSERT_ON with `ifndef SVA_OFF so assertions are enabled by default
[2266993] Removed ASSERT_ON in HDL files
[2246425] Updated CDC Waivers

## CDC Changes: (interface changes and new parameters are highlighted)

**RTL Changes:**
[2244996] Requirement - fism_dfx_clkgate_ovrd now ungates gclock instead of gate (Chassis ECN: 1570764)
[2247919] Enhancement - Added SCAN Reset Bypass muxes on reset_b and pok_reset_b inputs to CDC
[2392454] Enhancement - fismdfx_force_clkreq now keeps PGD fully awake and unlocked (instead of just asserting clkreq)
[2280804] Enhancement – clkreq output is now driven only from pgcb_clk domain (rather than mix between pgcb/func clk)
[1275945] Enhancement – Added prescc_clock input for CDCs that are used pre-SCC
[2266757] Enhancement – CDC FSM now always waits for clkack to assert before moving out of a parked state
[2245023] Enhancement – CDC only looks at clkgate_disabled in ON state to prevent potential hang scenario
[2267264] Defect - Moved u_gclockEnAckSync to long clock tree branch
[2280824] Defect – CDC always moves from RESTORE to ON to prevent potential hang scenario returning to PGATE
[2244989] Defect – ISM will now unlock in SYNCON_ISM when CG_LOCK_ISM is set
[2244791] Defect – gclock_active now deassert 8 clocks before gclock is gated

**Doc/Assertion/Environment Changes:**
[2243993] Documented that it is acceptable for the CDC be in the process of gating clocks while sleep toggles on IP-Inaccessible PG entry
[2249492] Called out need to waive Caliber violations regarding logic on reset due to DFx and force_rst_b
[2246461] Updated a_pgcb_pwrgate_active_2 assertion
[2245424] Assertion updates
[2244732] Clarified ITBITS min values is 3
[2245761] Updated to state greset_b is synchronized to clock instead of gclock
[2245509] Clarified gclock_active behavior in spec

## PGCB Changes: (interface changes and new parameters are highlighted)

**RTL Changes:**
[2247555] Requirement – PGCB to support SCAN Dump
- DFx Sequencer updated:
  - Decoupled pgcb_bypass and pgcb_ovr, so the Sequencer can be moved to a specific state before invoking overrides
  - Changed reset state of DFX Sequencer to be Powered On [2244571]

[2280823] Requirement - Provided option for PGCB to force on clocks while power is ramping for contention clearing
- Renamed *ip_pgcb_frc_clk_srst_en* to *ip_pgcb_frc_clk_srst_**cc**_en*, when set PGCB asserts *pgcb_ip_force_clks_on* and waits for *ip_pgcb_force_clks_on_ack* before requesting power-up from PMC, deassertion of force_clks_on remains the same.

[2280825] Requirement – DFx Sequencer now deasserts sleep before deasserting reset to initialize SR cells
[2244992] Requirement – New pgcb_sleep2 output added to provide means for multiple state-retention domains (XHCI request)
- IP's not using pgcb_sleep2 can let it dangle

[2267262] Enhancement – Replaced RTL muxes with mx22 muxes in DFx logic for better glitch prevention
[2279699] Defect – Updated boundary_locked to assert when clocks are gated when ISM_AGT_IS_NS is set

**Doc/Assertion/Environment Changes:**

[2266897] Cleaned up assertions with potential Large Memory Footprints
[2244151] Updated IP-Inaccessible waveforms to show pg_rdy_ack_b deasserting at the same time as pwrgate_active
[2249492] Called out need to waive Caliber violations regarding logic on reset due to DFx and force_rst_b
[2245081] Misc. doc updates
[2267412] Moved Reset States Table for DEF_PWRON to IO Table section and clarified that values are only for DEF_PWRON==1
[2247058] Updated doc to show UNGATE_TIMER encodings

### PCGU Changes: (interface changes and new parameters are highlighted)

**RTL Changes:**
[2280815] Fix to avoid potential glitch on pgcb_clkreq when pgcb_rst_b asserts gracefully

- PCGU:
  - Removed async_pgcb_rst_b input, added async_pmc_ip_wake and pgcb_pok input
  - Added DEF_PWRON parameter
- PCGU_AWW:
  - sync_wakes_source_b now stays asserted until sync_clkvld is high
- PGCBCG Reference Design:
  - Integrated new PCGU
  - Removed async_pgcb_rst_b and cfg_pgcb_clkgate_disabled inputs

[2266758] Updated PGCBCG reference design to contain clock gate cell

- Removed sync_clkvld output, added pgcb_gclk output

**Doc/Assertion/Environment Changes:**
[2267629] Fixed typos in PCGU HDL file

# PGCB + CDC Revision 1.15 Release Notes

### CDC Changes:

Release of Version 1.15 with fix for the issue below:

[HSD: 2243998] IOSF primary compliance issue seen with CDC v1.1 version (ISMPM 033)

### PGCB Changes:

- NO changes to PGCB for this version.

# PGCB + CDC Revision 1.1 Release Notes

### CDC Changes: interface changes and new parameters are highlighted).

Release of Version 1.1 with following changes:

1. 2 new input DFx signals (fscan_clkgenctrl*) and other bypass logic added to support usage of the CDC in pre-SCC mode. 1 new output signal (gclock_enable_final) added to support SCC related considerations (refer to Appendix for more information). Added new parameter, PRESCC, for this change.
2. Support for separating out functional clock (on short clock tree) controlled by clock_gate within CDC from functional clock used by other logic within CDC (SD requirement) – for details, refer to section on CDC Behavior Details. Addition of new parameters related to this change - DSYNC_CG_EN, FLOP_CG_EN and CG_LOCK_ISM.
3. Support for Restore of IP blocks that are powered-ON by default (Chassis PG ECN 1570775).
4. Several documentation updates (see change bars)

5. New module CdcMainCg.sv has been added for CDC

Implemented the following HSDs:

**Key changes:**
[HSD: 1277154] CDC PV violation with clock-gate combi logic
[HSD: 1277155] CDC needs parameter to allow it to be used preSCC
[HSD: 1277156] [BXT] PGCB/CDC need ability to default to restore state

Corner-case bugs (some are related to above changes):
[HSD: 2243684] CDC should treat ism_agent as gclock_req_sync
[HSD: 2243686] CDC boundary_locked does not default to locked
[HSD: 2243688] CDC could hang in FORCE_READY
[HSD: 2243801] CDC to add parameter to support assertion of ISM_LOCK with de-assertion of gclock_active

**Assertion fixes:**
[HSD: 2243601] [ASSERTION] CDC a_ism_agent_1 is looking at sync version of gclock_req_async
[HSD: 1276710] [ASSERTION] CDC Clkgate holdoff assertion fires falsely for IP-Inaccessible Entry
[HSD: 1276742] [ASSERTION] CDC a_reset_b_1 assertion needs to be disabled for DEF_PWRON

### PGCB Changes:

- NO interface/parameter changes.
- Version 1.1 release with following minor updates:
  - Change to reset state for case of DEF_PWRON == '1' (Chassis ECN 1570775) – HSD: 1277156 PGCB/CDC need ability to default to Restore state .
  - Documentation updates (see change bars)

# PGCB + CDC Revision 1.0 Release Notes

**NOTE:** For the CDC, certain existing requirements and behavior have been more clearly documented. For the PGCB, there are clarifications with reference to the requirement on the pg_rdy_req_b handshake (applicable to IPs that do not use the CDC). Please refer to the changebars in the corresponding integration documents for details.

### CDC Interface Changes:

- New Ports:

| Signal Name | Dir | Description | Instructions |
|---|---|---|---|
| fismdfx_clkgate_ovrd | input | DFx override to force GATE the gclock output | Connect to fism[p\|s]dfx_clkgate_ovrd at IP top-level<br>if this CDC controls an IOSF clock, otherwise can tie 0 |

- New Parameters:

| Parameter Name | Description | Instructions |
|---|---|---|

| | | |
|---|---|---|
| ISM_AGT_IS_NS | If this is set to '1', the *_locked signals are driven as the output of a flop. However, if this is '0' (default value), then the locked signals assert combinatorial manner (in the same cycle that the CDC logic determines that conditions to lock the ISM are satisfied). The de-assertion of the *_locked signals always happens through the output of a flop. | Please refer to section 3.4.1 of the integration guide.<br><br>Note: a value of '1' will produce 0.8 locking behavior |
| RSTR_B4_FORCE | If set to '0' (default), the CDC will ignore RESTORE if pwrgate_force asserts (legacy behavior)<br><br>If set to '1', ensures the CDC will complete any pending RESTORE flow before honoring pwrgate_force. | For SPT, IP's should set this to '0' as restore is not POR.<br><br>For other projects, if a restore is required to completed after a PG exit before starting to do an IP-Inaccessible entry, then this should be set to '1' |

## PGCB Interface Changes:

- Port Changes:

| Old Signal Name | New Signal Name | Change Description | Instructions |
|---|---|---|---|
| ftap_tck | pgcb_tck | Updating name to avoid confusion with ftap_tck from cluster tap | pgcb_tck should be mapped to an IP top level port of the same name. This tck should not be gated by the cluster tap. |

## CDC HSDs:

1275944 Enhancement [1.0] [RTL] CDC Pre-Flop ISM Locked Update (Parameterized)

- Change to cause ism_locked signal and boundary_locked signals to assert in combinatorial manner in response to ISM idle or clkreq de-assertion followed by hysteresis expiration (a parameter, ISM_AGT_IS_NS, is provided to revert to v0.8 behavior – flopped version) – motivation is to support ISM pre-locking even for those cases where next_state is not available

1275023 Enhancement [1.0] [RTL] CDC should implement DFx ISM clockgate override

- Support for fism[p|s]dfx_clkgate_ovrd (applicable for CDCs that control prim/side_clk domains)

1276028 Enhancement [1.0] [RTL] CDC to keep clocks ungated during IP-Inaccessible Entry

- Change to ungate (and keep ungated) the clocks during IP-Inaccessible PG entry flow (to support cases where some part of an IP may require a clock from different domain in order to let the

primary/side ISM reach Idle state) until the actual beginning of PG flow by PGCB (as indicated through assertion of pgcb_pwrgate_active)

1274883 Defect [1.0] [RTL] CDC Need To Solidify Config Register Clock-Crossing Recommendation

- Changes to using the configuration values for timers such that CDC does not allow any async changes to the timer values to impact CDC logic while the corresponding enables are de-asserted. SW is required to set the corresponding *disable, before modifying the *holdoff values if the *holdoff values are asynchronous to the CDC clock domain.

1276305 Defect [1.0] [RTL] [FPV] CDC will skip RESTORE if in IP-Accessible PG when ForcePwrgatePOK is received

- Added RSTR_B4_FORCE parameter to make CDC handle a restore before honoring a pwrgate_force

1276562 Defect [1.0] [RTL] CDC Deadlock Possible Going from IP-Accessible to IP-Inaccessible

- IP is required to ensure pwrgate_active is deasserted before asserting and IP-Inaccessible PG request to the PGCB. This updates the CDC to ensure this requirement is handled for IPs using the CDC.

1275943 Defect [1.0] [RTL] CDC Force reset mux should use ctech cell for SCAN bypass

- Use ctech cells in force reset mux structure for SCAN compliance

1275328 Defect [1.0] [RTL] CDC is dropping one clock cycle after reset

- Fix for the issue where if an IP is powered on by default, the clock is running while in reset but gated for a few clock cycles just after pgcb_rst_b reset de-assertion

1275250 Defect [1.0] [RTL] 0.8 CDC assertion error

- Change to wait for pgcb_pok signal to be synced over to functional clock domain before unlocking ISMs/boundaries

1276564 Enhancement [1.0] [RTL] CDC reset value of POK will be 0 regardless of DEF_PWRON

- CDC's that default to ON (DEF_PWRON==1) will now drive their POK low until side_rst_b deasserts. Early Boot IPs will need to tie their POK's to '1'.

1276565 Defect [1.0] [ASSERTIONS] CDC - Enable Doublesync Checks

- Doublesync metastability modeling and pulse-width checks have been enabled on the CDC's doublesyncs. For failures seen, IPs should review and explicitly disable if falsely flagging. Refer to the integration guide for suggestions on disabling these features.

1276308 Defect [1.0] [RTL] [FPV] CDC will not assert clkreq during restore

1276306 Defect [1.0] [RTL] [FPV] CDC can report pwrgate_ready after RESTORE before the main clock is ready

1276307 Defect [1.0] [RTL] [FPV] CDC unlock_ism deassertion will always cross to Main clock domain before unlock_all assertion

1276309 Defect [1.0] [RTL] [FPV] CDC can enter ON state with clkreq and clkack low

1276310 Defect [1.0] [RTL] [FPV] CDC clock should ungate in CGATE if force_pgate_req

1276311 Defect [1.0] [RTL] [FPV] CDC breaks gclock_req/ack in RESTORE

1276548 Defect [1.0] [RTL] [FPV] CDC Race between unlock_all and force_pgate_req synchronizers

1275787 Enhancement [1.0] [ASSERTIONS] Power Gating Assertions needed in CDC/PGCB

1275024 Enhancement [1.0] [WAIVER] CDC/PGCB lintra waivers for Rev0.8

1274997 Enhancement [1.0] [ASSERTION] PGCB/CDC assertions missing on I/Os

1275343 Enhancement [1.0] [DOC] CDC documentation to call out requirement that clocks be available on IP-Inaccessible exit

1275588 Enhancement [1.0] [DOC] CDC Documentation Update for clock gate disable

### PGCB HSDs:

1274704 Defect [1.0] [RTL] PGCB needs to assert pgcb_sleep in IP-Inaccessible flows

- PGCB will now assert pgcb_sleep during IP-Inaccessible flows (removed workaround). The VCS modeling issue with sleep deasserting while resets are asserted has been fixed.

1276108 Enhancement [1.0] [RTL] Change PGCB ftap_tck port name to pgcb_tck

- Port name change from ftap_tck to pgcb_tck

1276045 Enhancement [1.0] [RTL] PGCB DFx overrides for pgcb_pok AND pgcb_pwrgate_active

- If the DFx Sequencer is enabled, it will also control pgcb_pok and pgcb_pwrgate_active

1275787 Enhancement [1.0] [ASSERTIONS] Power Gating Assertions needed in CDC/PGCB

1275024 Enhancement [1.0] [WAIVER] CDC/PGCB lintra waivers for Rev0.8

1275942 Enhancement [1.0] [DOC] PGCB Spec Needs to Better Document sleep_en behavior

1276566 Defect [1.0] [RTL] PGCB Restore Updates

# PGCB + CDC Revision 0.80 Release Notes

### CDC Interface Changes:

- New Ports:

| Signal Name | Dir | Description | Instructions |
|---|---|---|---|
| fismdfx_force_clkreq | input | DFx force assert clkreq | Connect to fism[p\|s]dfx_force_clkreq if this CDC controls an IOSF clock, otherwise can tie 0 |

| | | | |
|---|---|---|---|
| cdc_visa[23:0] | output | CDC observability signals | Connect to IP's VISA muxes (lane in on Visa mux)<br>Recommendation is that the IP has at least a small ULM in the AON domain which the CDC and PGCB VISA signals would connect to |

- Port Changes:

| Old Signal Name | New Signal Name | Change Description | Instructions |
|---|---|---|---|
| pgcb_reset_b | pgcb_rst_b | Updating name to match Integration Guide + PGCB | Map existing connection to new port name |
| dt_clkungate | fscan_clkungate | Updating to Chassis naming convention | Update the connection to new name |
| dt_scanrst_b | fscan_byprst_b[RST+DRIVE_POK:0] | Updating to Chassis naming convention and updating to have per-reset-synchronizer controls, the total number will be:<br># resets in CDC + 1 (if DRIVE_POK is set) | Concatenate this vector with other fscan_byprst_b vectors in IP and bring to the top level. |
| dt_scanrstbypen | fscan_rstbypen[RST+DRIVE_POK:0] | Updating to Chassis naming convention and updating to have per-reset-synchronizer controls, the total number will be:<br># resets in CDC + 1 (if DRIVE_POK is set) | Concatenate this vector with other fscan_rstbypen vectors in IP and bring to the top level. |

## PGCB Interface Changes:

- New Parameters:

| Parameter Name | Description | Instructions |
|---|---|---|
| UNGATE_TIMER | PGCB DFx Sequencer Power On Timer Duration | Bring to IP Top Level (default to 2'b01) |
| USE_DFX_SEQ | PGCB DFx switch to disable DFx sequencer | Bring to IP Top Level (default to 1)<br>Project Specific Parameter:<br>SPT: 1 – will be using the Sequencer |

| | | |
|---|---|---|
| | | BXT: 0 – will not be using the sequencer |

- New Ports

| Signal Name | Dir | Description | Instructions |
|---|---|---|---|
| ftap_tck | input | JTAG clock used by PGCB DFx Sequencer | Bring to IP Top Level |
| fdfx_powergood_rst_b | input | DFx reset used by PGCB DFx Sequencer | Bring to IP Top Level |
| pmc_pgcb_fet_en_b | input | PFET Enable from PMC | Connect to IP Top level PFET Enable Port |
| pgcb_ip_fet_en_b | output | PFET Enable with DFx Override | Final PFET control to be hooked up in UPF |
| fdfx_pgcb_bypass | input | PGCB DFx Bypass Enable | Bring to IP Top Level |
| fdfx_pgcb_ovr | input | PGCB DFx Sequencer Control (1=Power Up, 2=Power Down) | Bring to IP Top Level |
| fscan_ret_ctrl | input | DFx Override Value for sleep (if fscan_mode==1) | Bring to IP Top Level |
| fscan_mode | input | DFX Override Enable for sleep | Bring to IP Top Level |

- Removed Ports

| Signal Name | Dir | Description |
|---|---|---|
| pgcb_force_prim_rst_b | output | Defeatured in 0.71, now removed |
| ip_pgcb_fuse_valid | input | Defeatured in 0.71, now removed |

- Port Changes:

| Old Signal Name | New Signal Name | Change Description | Instructions |
|---|---|---|---|
| pgcb_visa[15:0] | pgcb_visa[23:0] | Increasing size of VISA vector | Connect to always-on VISA ULM |

- The following **existing** ports are now used during Warm Reset when frc_clk_srst_en==1
  - cfg_trsvd0[1:0]
  - cfg_trsvd1[1:0]

**CDC HSDs:**

- HSD 1274581 - (Enhancement) - [0.8] CDC needs observability signals (VISA)
- HSD 1274316 - (Enhancement) - [0.8] CDC needs clkreq DFx overrides
- HSD 1274469 - (Enhancement) - [0.8] CDC needs to use CTECHs for reset forcing structure

- HSD 1274580 - (Enhancement) - [0.8] CDC to implement 0 cycle clock ungate

- HSD 1274682 - (Defect) - [0.8] CDC should reset to ON_PENDING if DEF_PWRON == 1

- HSD 1274584 - (Defect) - [0.8] CDC Large input cone for idle timer causing PV violations

- HSD 1274685 - (Defect) - [0.8] CDC will not always wake up if power gated and powergated_enabled conditions change

- HSD 1274684 - (Defect) - [0.8] CDC powergateready should enforce priority of pmc_ip_wake

- HSD 1274683 - (Defect) - CDC FSM should reset on pgcb_rst_b

- HSD 1274578 - (Defect) - [0.8] CDC needs per-reset SCAN bypass controls
  - Per-reset mux bypass signals added
  - Updated signal names on CDC:
    - dt_scanrst_b -> fscan_byprst_b
    - dt_scanrstbypen -> fscan_rstbypen

- HSD 1274582 - (Defect) - [0.8] CDC should lock ISMs/Boundary in CGATE states for IP-Inaccessible PG
  - ISMs will be locked in CGATE/CGATE_PENDING states for a forced PG entry, live ISM state will then be ignored until PG entry/exit are complete
  - For a forced pg entry, gclock_req will be ignored in the CGATE_PENDING state
  - Fixed issue where timer will not expire in CGATE_PENDING if do_force_pgate=1 and gclock_req=1, so the FSM hangs here.

- HSD 1274583 - (Defect) - [0.8] CDC idle timer rolls over if cfg_clkreq_ctl_disabled is set

- HSD 1274633 - (Defect) - [0.8] Need Lintra waivers for CDC/PGCB violations

**PGCB HSDs:**

- HSD 1274633 - (Defect) - [0.8] Need Lintra waivers for CDC/PGCB violations

- HSD 1274074 - (Enhancement) - [0.8] PGCB Rev0.7rc should provide a mechanism to enable synchronous reset propagation during the Warm Reset Flow
  - PGCB will now force clocks on in WARM Reset if frc_clk_srst_en==1 to allow resets to propagate to sync-reset logic

- HSD 1274295 - (Enhancement) - [0.8] PGCB should wait for all_pg_rst_up before deasserting force_clks_on during context propagation window
  - Moved waiting for all_pg_rst_up on arc from CLKSOFFACK_CP -> ACCSRETLOW, to arc from CLKSONACK_CP -> CLKSOFF_CP

- HDS 1274669 - (Enhancement) - [0.8] PGCB needs to add Non-Functional DFx Hooks
  - Implemented DFx Sequencer and override latches/muxes
  - New Interface Signals:
    - jtag_tck
    - fdfx_powergood_rst_b
    - pmc_pgcb_fet_en_b

        - pgcb_ip_fet_en_b
        - fdfx_pgcb_bypass
        - fdfx_pgcb_ovr
        - fscan_ret_ctrl
        - fscan_mode

- HSD 1274297 - (Defect) - [0.8] PGCB should not stagger force resets- need to remvoe force_prim_rst_b pin and fuse_valid pin from PGCB
    - Removed force_late_rst_b and ip_pgcb_fuse_valid and renamed force_early_rst_b to force_rst_b
        - This is to fix the bug regarding async reset deassertion while the clocks are running