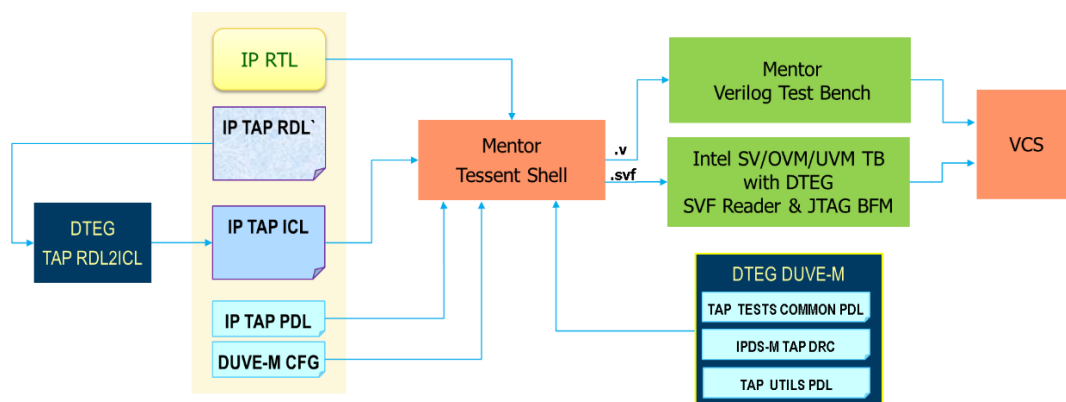


**Overview** DUVE-M (DTEG Unified Validation Environment (Mentor)) is a generic infrastructure and tests for DfX/TAP validation and test content development based on the IEEE 1687 ICL/PDL standard and collateral. It is compatible with Intel-specific TAP architectures and features and can be easily tuned to support different design configurations and test requirements. The tool includes the TAP RDL2ICL utility for generating IP-level ICL from the existing TAP RDL.

**Tool Block Diagram**

Typical Use of DUVE-M for IP Level Validation



<b>Required Tool Inputs</b>	<ul style="list-style-type: none"> <li>▪ RTL: Verilog description of the top-level module in the project</li> <li>▪ TAP spec: Specification of TAP registers in SystemRDL format (Intel-specific)</li> <li>▪ DfX/TAP ports: Specification of DfX/TAP ports in ICL format</li> <li>▪ PDL tests: Project-specific tests in PDL format</li> </ul>
<b>Tool Outputs</b>	<ul style="list-style-type: none"> <li>▪ TAP ICL: TAP register specification in ICL format</li> <li>▪ Verilog Test Bench: Test or validation patterns in Verilog format (requires Tessent Shell)</li> </ul>
<b>Tool Coverage</b>	<p>DUVE-M provides tests to cover all aspects of TAP ICL versus RTL validation:</p> <ul style="list-style-type: none"> <li>▪ TDI-TDO continuity</li> <li>▪ TAP IR/TDR resets</li> <li>▪ TDR Read-Write access</li> <li>▪ TDR Security</li> <li>▪ Reserved Opcodes</li> </ul> <p>In addition, included procedures and utilities allow writing generic PDL tests and accessing RTL/ICL/PDL metadata in the Tessent Data Models.</p>

<b>Tool Scripts</b>	<ul style="list-style-type: none"> <li>▪ TAP RDL2ICL (tap_icl_gen.pl): Utility to convert existing IP TAP RDL to ICL</li> <li>▪ Tessent dofile (gen_val_tests.do): Pattern generation flow</li> </ul>
<b>Related Tools</b>	Siemens (Mentor Graphics) Tessent Shell is required for use of DUVe-M infrastructure.
<b>Power, Area, and Gate Count</b>	Not applicable



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