IOSF Sideband Endpoint
Intel Corporation Soft IP

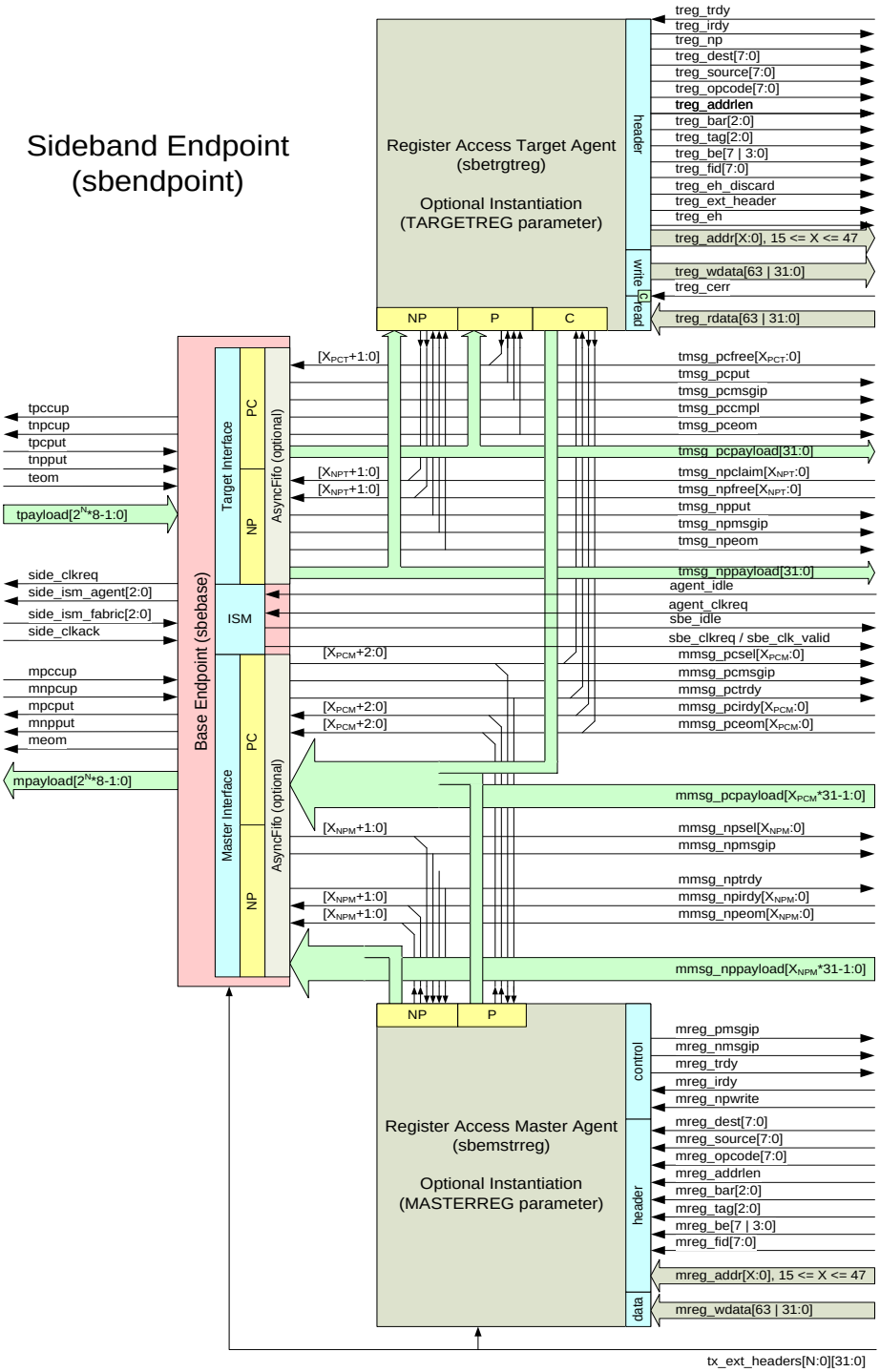
Overview

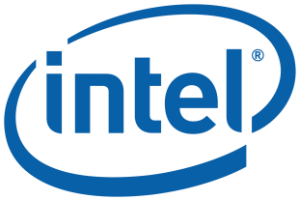
The IOSF Sideband Endpoint provides a connection to the IOSF Sideband Message Interface. It exposes a flexible set of interfaces to enable agent-specific logic with access to the IOSF sideband network. In addition, the Endpoint provides optional register access target and master services in order to ease handling of the register access messages defined in the IOSF specification.

Features

- Parameterized sideband payload width, with support for payload widths of 1, 2, or 4 bytes
- Parameterized ingress queue depth
- Optional asynchronous FIFOs for clock synchronization
- Flexible interfaces (tmsg/mmsg) for connecting agent-specific logic that needs access to the IOSF sidebnad network. The tmsg/mmsg interfaces support a parameterized number of posted/non-posted master/targets
- Ability to automatically return an unsuccessful completion for inbound non-posted messages that are not claimed by any "widget" on the tmsg interface
- Optional register access master and target "widgets" that attach to the tmsg/mmsfg interface to provide a register access interface (treg/mreg) to the associated agent

IP Block Diagram





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Major Interfaces

- IOSF Sideband Message Interface
- tmsg/mmsg/treg/mreg IP-specific interfaces

Applications

The Sideband Interface can serve as a multi-purpose chip-wide (out-of-band) communication fabric for specifically defined services and for any implementation-specific services.

The types of services provided are:

- Access to Peripheral Component Interconnect Express (PCIe) config, memory, or I/O mapped address space
- Access to privately mapped configuration registers (implementation-specific)
- INTx assert/deassert messages sent out-of-band
- General virtual wire messages (implementation-specific)
- Distribution of fuse values (implementation-specific)
- Power management broadcast messages (implementation-specific)

Performance Parameters

The gate count listed below is an estimate. Actual values are heavily influenced by the clock frequency, physical constraints, and technology employed.

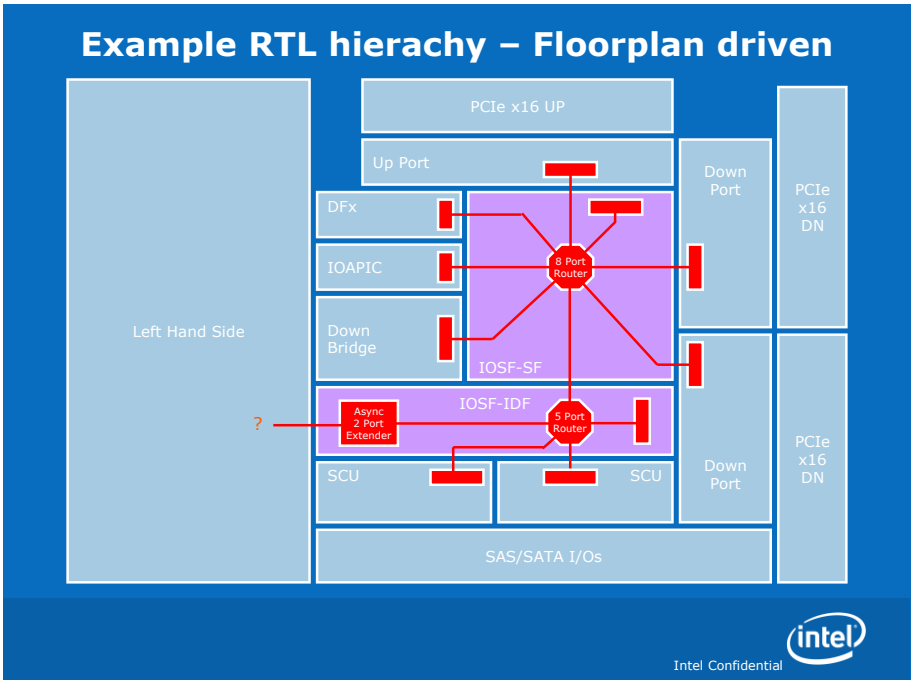
Gate Count Estimate

Component	Gate Count Estimate
sbendpoint	Approximately 3000 to 7000 equivalent NAND gates, depending on the chosen configuration

Deliverables

- RTL in SystemVerilog
- Customer documentation
- Release Notes
- Testbench environment in OVM
- Test cases, cover points, and assertions
- Lintra, Clock Domain Crossing (CDC), Spyglass, Logical Equivalency Testing (LEC), Synthesis coverage scripts

SoC Integration & Related Products



Security Audits

This IP passed the following SDL audits:

- S0

Safety Audits

This IP passed the Functional Safety HW Process Safety Audit (PSA) for Mule Creek Canyon PCH and Jasper Lake CPU, for the Elkhart Lake platform.