Slave TAP (sTAP)
Intel Corporation Soft IP

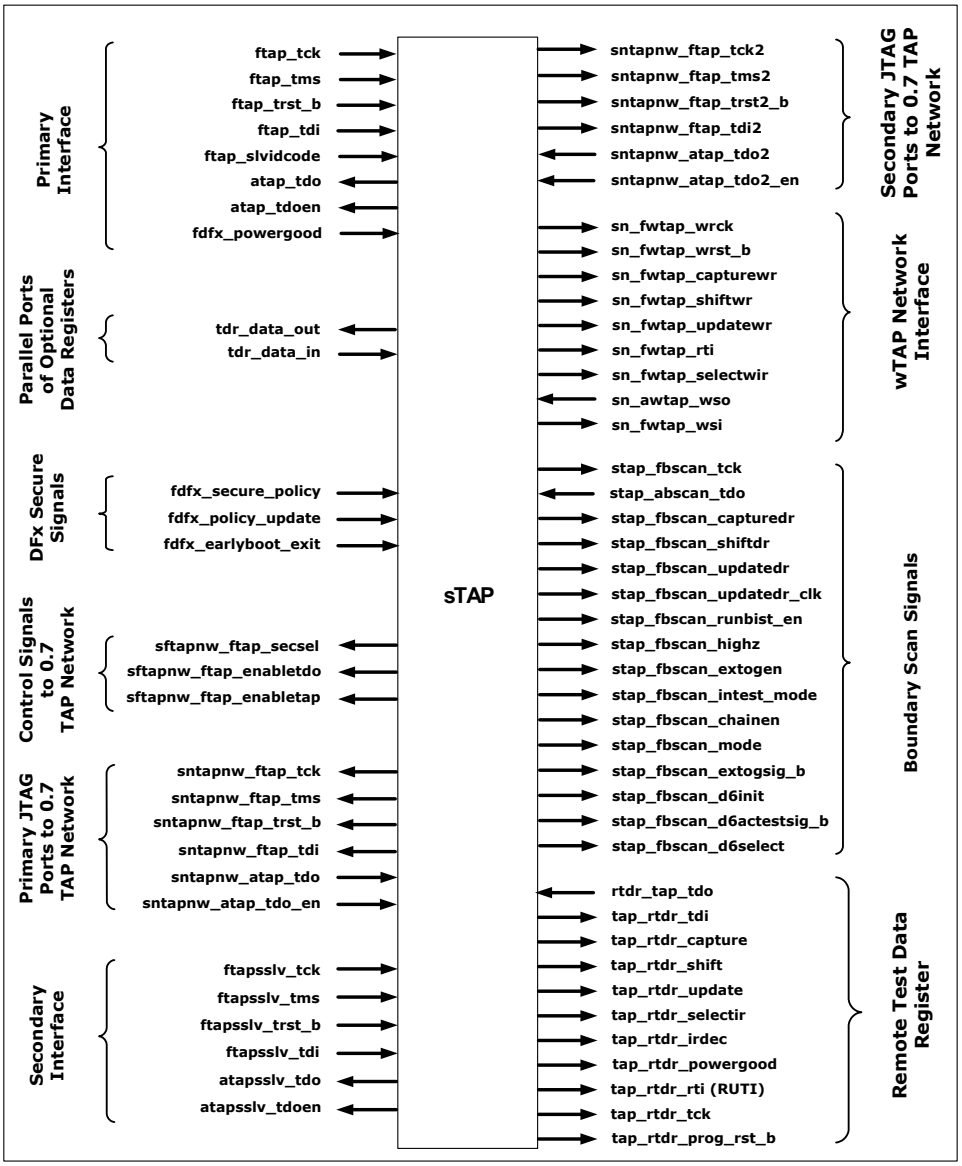
Overview

Slave TAP (sTAP) soft IP is a parameterized RTL component compliant to IEEE 1149.1, which gets connected to the other Slave TAPs or Wrapper TAPs (wTAP) to form a TAP Network (compliant to 1149.7 T0) in an SoC. This provides testability through JTAG to the IP or design block where it is instantiated.

Features

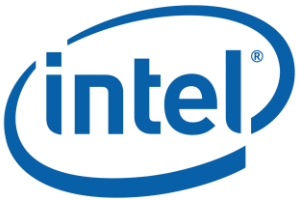
- IEEE1149.1 compliant and can drive sub TAP network that is IEEE1149.7 T0 compliant
- SoC_TAP_HAS_rev088 compliant
- Supports all modes of its TAP network:
  - Normal
  - Exclude
  - Decoupled
  - Shadow
- User-strapable DEVICE SLVIDCODE
- User-configurable Test Data Registers (TDR)
- Supports wTAP Networks in parallel and in series
- Supports TAP Networks
- Supports secondary TAP ports
- Supports boundary scan mode
- Supports remote TDRs
- All internal and remote TDRs are cleared by programmable reset.
- Provides a parameter generation Perl utility to guide Slave TAP configuration

IP Block Diagram



Major Interfaces

- **Primary JTAG Interface:** The JTAG 1149.1 specification is an industry standard test interface. The most important use for the 1149.1 TAP is the serial communication protocol to access private registers for testing and debugging SoC components. This is the most widely used capability at Intel, with an entire tool set, the In-target Probe (ITP), built around it for microprocessor and chipset debugging. This interface contains the standard pins (tck, tms, trst_b, tdi, tdo, tdo_en).
- **Secondary Interface:** A secondary TAP port is an option available to the integration team for two reasons:
  - The first is parallel testing of agents in the SoC. This helps to reduce test time as the number of the agents in a SoC increases with smaller geometries available in future fabrication processes.
  - The second reason is that test content that is validated from a base product can be readily ported to a derivative product.
- **DFx Secure Interface:** The DFx secure interface is an implementation-specific set of values that only has meaning to an agent that decodes a value for enabling DFx in a secure environment. A security engine or fuse block is the source of the information and the DFx Secure interface distributes this information throughout the DFx fabric to enable a particular feature or a group of features.
- **Boundary Scan Interface:** This provides various state machine controls (capture, shift, update) and data to make the boundary-scan cells operate. Boundary-scan control cells drive the output enables of one or more bidirectional output pins. The boundary scan register is distributed around the I/O pads of the chip.
- **TAP Network Interface:** This interface is behind the Slave TAP that connects to a TAP Network IP. This in turn enables connection of various Slave TAPs. The TAP.7 specification defines a methodology to include (normal), exclude, or decouple (remove) TAPs from the network to reduce TCK cycles for reading or writing test data registers in any TAP on the network.
- **wTAP Network Interface:** This interface is behind the sTAP that enables connection of various wTAPs in a serial or a parallel configuration with the sTAP.
- **TDR Interface**: This interface is behind the sTAP that forms a bus for the parallel data out that connects to custom logic blocks outside this IP. This is the output of the shadow register. The data from the custom block can be captured and read out through TAP or written into this custom block by shifting in a value and updating it.
- **Remote TDR Interface:** A remote Test/Debug Register (RTDR) is a register that resides outside of the TAP controller. This provides various state machine controls (capture, shift, update, irdecode, ruti) and data (TDI, TDO) to make the RTDRs operate.



Applications

- Accessing TAP private registers for testing and debugging SoC components
- IO testing for Boundary scan
- Connecting to Remote Test Data Register
- Hosting a sub-network that has multiple TAPs beneath it
- Connecting wTAPs

Benefits

- Easy to integrate with documented examples of usage
- Silicon proven IP in multiple products in Intel since the since 2010
- Fully parameterized IP that helps in optimizing gate count based on usage needs
- Periodic feature updates along with support

Power and Performance Parameters

The following table shows the values for several area and power parameters based on the 1273 process.

Parameter Type	Value
Gate Count	3283
Total Dynamic Power	0.195 mW
Leakage Power	1.7 uW

The following table shows the values for several area and power parameters based on the 1274 process.

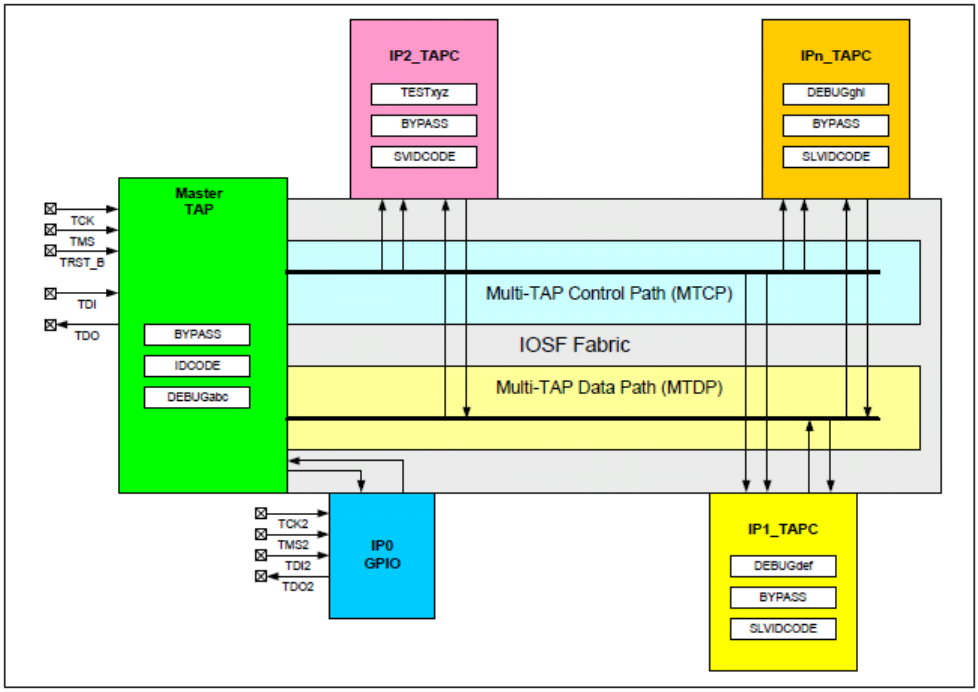
Parameter Type	Value
Gate Count	2737
Total Dynamic Power	0.1296 mW
Leakage Power	17 uW

Deliverables

- Customer documentation
- RTL
- Test cases, cover points, and assertions
- Testbench environment in OVM
- Lintra, CDC, Spyglass, LEC, Synthesis, coverage scripts, and FPV scripts
- A parameter generation Perl utility
- Release notes

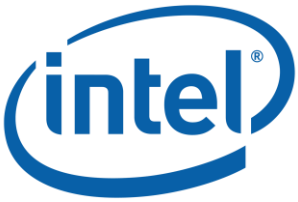
SoC Integration and Related Products

The following block diagram shows the sTAP and how it integrates with other family product offerings (Chip-level TAP, TAP Network) for an SoC.



Security Audits

This IP has DFx Secure Plugin to adhere to security.



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