Chassis Power Gating Central Controller Verification IP

FAQ

# FAQ

What are all the configs that need to be set in the agent using set\_config configuration methods?

The is\_active config needs to be set at the IP level to OVM\_ACTIVE and OVM\_PASSIVE at the FC/SOC level. Is is set to OVM\_PASSIVE by default.

The hasPrinter config needs to be set to 1.

What is the IS\_ACTIVE parameter in the testisland for?

The IS\_ACTIVE parameter in the test-island is for setting the correct direction for all the signals in the test-island at the IP and FC/SOC level.

It needs to be set to 1 in IP level and 0 in the FC/SOC level.

Note that IS\_ACTIVE parameter will override is\_active enum if they are not equal

What should the parameters NUM\_SIP\_PGCB, NUM\_FAB\_PGCB, NUM\_SW\_REQ, NUM\_PMC\_WAKE and NUM\_FET be set to?

That depends on the power architecture of the IP you are validating. Please talk to your architect or designer to find out how many SIP PGCBs, fabric PGCBs and FET blocks are there in your IP.

I am using the IOSF Fabric VC in my test environment. So if there is no fabric PGCB in my test environment, how should I configure the agent and test-island?

In the test\_island, set the NO\_FAB parameter to 1.

I am validating the fabric and there are no SIP PGCBs in my environmenr. How should I configure the agents and test\_island?

If there is no SIP PGCB in your test environment, set NO\_SIP parameter to 1.

Should I use the AddFETBlock method?

Yes. You need to first add FET block and only then add PGCBs. You will add as many FET blocks as specified by the test-island parameter NUM\_FET.

Should I use the AddSIPPGCB and AddFabricPGCB method?

Yes. If you have a SIP PGCB in your environment, you need to use the AddSIPPGCB method. You will add as many SIP PGCBs as specified by the test-island parameter NUM\_SIP\_PGCB.

Similarly, if you have a Fabric PGCB in your environment, you need to the AddFabricPGCB method. You will add as many Fabric PGCBs as specified by the test\_island parameter, NUM\_FAB\_PGCB

What should the fet\_index, sw\_ent\_index and pmc\_wake\_index be set to?

This depends on the power architecture of the IP you are validating. Several PGCBs can be put under the same FET block and those will have the same fet\_index. Similarly, several PGCBs can be controlled by the same SW request and PMC wake request. The sw\_req\_index and pmc\_wake\_index should be used to specify the mapping of SW req and PMC wake signal to PGCB.

How should the fet\_en\_ack be connected in the testbench

<https://sharepoint.amr.ith.intel.com/sites/ChipsetHWSoC_PowerIP/Power%20WIKI%20Documents/Steps%20to%20drive%20IP%20ack_port.docx>

But when power gating, it is possible that PMC will not actually turn off the power( i.e the fet\_en\_b to the PGD) if the fet is shared with another PGD. How do I emulate that?

There are several levels of control

To have the BFM never send any response, you can set the noResponse parameter in the ResponseSeqItem. This means that the BFM will not assert or deassert the ack. It will also result in end-of-test errors because the req/ack is a full handshake.

To delay the pg\_ack\_b you can constrain the delays in the CCAgentResponseSeqItem.

There is also a mode in which the fet is never turned off.

The BFM is not deasserting the pmc\_ip\_pg\_ack\_b to the IP? How can be debug this issue?

First check to make sure that the clk to the BFM is running. The clk should be connected to pgcb\_clk.

Also make sure the reset\_b is deasserted. The reset should be connected to pgcb\_rst\_b.

How do I connect a scoreboard to the monitor.

Please refer to the tracker userguide section 1.6 for details on how a scoreboard can be connected.

How does pmc\_ip\_pg\_wake get deasserted

It has to be deasserted by the test using DEASSERT\_PMC\_WAKE command. It does not deassert automatically.