rcf\_widgets

Integration Guide

IP Rev. 1.5

Intel Restricted Secret

Copyright © 2014, Intel Corporation. All rights reserved.

Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

\* Other names and brands may be claimed as the property of others.

This document contains information on products in the design phase of development.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED OR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked “reserved” or “undefined.” Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your Intel account manager or distributor to obtain the latest specifications and before placing your product order.

Copies of documents that have an order number and are referenced in this document or in other Intel literature can be obtained from your Intel account manager or distributor.

Contents

[1 Introduction 7](#_Toc536791681)

[1.1 Audience 7](#_Toc536791682)

[1.2 Supported Projects 7](#_Toc536791683)

[1.3 Terminology 7](#_Toc536791684)

[1.4 Related Documents 7](#_Toc536791685)

[1.5 Opens, Risks, and Assumptions 8](#_Toc536791686)

[1.6 Contact Information 8](#_Toc536791687)

[1.7 Document Revision History 8](#_Toc536791688)

[2 Quick Start 10](#_Toc536791689)

[2.1 Downloading Sub IP 10](#_Toc536791690)

[2.2 Integrity Checks for Standalone IP 10](#_Toc536791691)

[3 Overview 11](#_Toc536791692)

[3.1 cdc\_wrapper 11](#_Toc536791693)

[3.1.1 IP Block Diagram 11](#_Toc536791694)

[3.1.2 CDC\_wrapper Functional Interface 11](#_Toc536791695)

[3.1.3 VISA, DFx 14](#_Toc536791696)

[3.1.4 ClockDomainController changes 15](#_Toc536791697)

[3.1.5 Integration examples 16](#_Toc536791698)

[3.1.6 Agent Endpoint responsibilities 16](#_Toc536791699)

[3.1.7 Timing Diagrams 16](#_Toc536791700)

[3.1.8 Security Questionaire 16](#_Toc536791701)

[3.2 dft\_reset\_sync 17](#_Toc536791702)

[3.2.1 Interface signals 17](#_Toc536791703)

[3.2.2 Parameters 17](#_Toc536791704)

[3.2.3 IP Block Diagram 17](#_Toc536791705)

[3.2.4 Functional description 17](#_Toc536791706)

[3.2.1 Security Questionaire 19](#_Toc536791707)

[3.3 ip\_disable 19](#_Toc536791708)

[3.4 fuse\_hip\_glue 19](#_Toc536791709)

[A required by the fuse group that needed a repo in $IP\_MODELS. Not for general consumption. 19](#_Toc536791710)

[4 Design Information for Integration 20](#_Toc536791718)

[4.1 RTL Directory Structure 20](#_Toc536791719)

[4.2 Clock, Power and Reset Domains 20](#_Toc536791720)

[4.2.1 Clock Domain Diagram 20](#_Toc536791721)

[4.3 Embedded Building Blocks/Custom Logic 20](#_Toc536791722)

[4.4 RTL Configuration Parameters 20](#_Toc536791723)

[4.4.1 Mandatory Parameters 20](#_Toc536791724)

[4.4.2 Boundary Scan Parameters 21](#_Toc536791725)

[4.4.3 Test Data Register Parameters 21](#_Toc536791726)

[4.5 Testbench Parameters 21](#_Toc536791727)

[4.6 IP Straps 21](#_Toc536791728)

[4.7 Fuses 21](#_Toc536791729)

[4.8 Power Information 22](#_Toc536791730)

[4.8.1 Power Supply 22](#_Toc536791731)

[4.8.2 Static Clock Gating 22](#_Toc536791732)

[4.8.3 Power Gating 22](#_Toc536791733)

[4.8.4 Bumps and Their Power Domains 22](#_Toc536791734)

[4.9 Power-up Requirements 22](#_Toc536791735)

[4.10 Macros used by IP 22](#_Toc536791736)

[4.11 Other Design Considerations 22](#_Toc536791737)

[4.12 DFx Considerations 22](#_Toc536791738)

[4.12.1 DFx Top-Level Signals 22](#_Toc536791739)

[4.12.2 DFx Clock Definition 22](#_Toc536791740)

[4.12.3 Clock Crossings 22](#_Toc536791741)

[4.12.4 N/ADebug Registers 22](#_Toc536791742)

[4.12.5 Scan – Clock Gating in RTL 22](#_Toc536791743)

[4.12.6 Scan – Reset Override 22](#_Toc536791744)

[4.12.7 TAP and Associated Registers 23](#_Toc536791745)

[4.13 System Startup 23](#_Toc536791746)

[4.13.1 Power-up Sequence 23](#_Toc536791747)

[4.13.2 Initialization Sequence 23](#_Toc536791748)

[4.13.3 Device Configuration 23](#_Toc536791749)

[4.13.4 Header for Windows Boot 23](#_Toc536791750)

[4.14 Security Considerations 23](#_Toc536791751)

[4.14.1 Security Threats 23](#_Toc536791752)

[4.14.2 Security Tests 23](#_Toc536791753)

[4.14.3 Interface Signals Implemented for Security 23](#_Toc536791754)

[4.15 RTL Design Libraries 23](#_Toc536791755)

[4.16 RTL Uniquification 23](#_Toc536791756)

[4.17 Emulation Support 23](#_Toc536791757)

[5 Verification Information for Integration 24](#_Toc536791758)

[5.1 IP Testbench Overview 24](#_Toc536791759)

[5.2 Reusable IP Testbench Components 24](#_Toc536791760)

[5.2.1 Collage or Sandbox Files 24](#_Toc536791761)

[5.2.2 IP Environment 24](#_Toc536791762)

[5.2.3 N/A. IP does not has any fuse requirements.Sequences 25](#_Toc536791763)

[5.2.4 Ip does not used any sequences or extended sequences.Miscellaneous 26](#_Toc536791764)

[5.3 Environment Settings and Files 26](#_Toc536791765)

[5.3.1 Base Test 26](#_Toc536791766)

[5.3.2 N/AConfiguration Object 26](#_Toc536791767)

[5.3.3 API 26](#_Toc536791768)

[5.4 N/ADescription of Reusable Tests 26](#_Toc536791769)

[5.5 Description of Reusable Automation Scripts 26](#_Toc536791770)

[5.6 N/ASupported Compiler Options for Simulation 26](#_Toc536791771)

[5.7 Reusable Simulation RUNMODEs 27](#_Toc536791772)

[5.8 RTL Verification Libraries 27](#_Toc536791773)

[6 Tools and Methodology for Integration 28](#_Toc536791774)

[6.1 Supported Tools 28](#_Toc536791775)

[6.2 Environment Variables 28](#_Toc536791776)

[6.3 HIP Libraries Included in Release 28](#_Toc536791777)

[6.3.1 Register Files or SRAM 28](#_Toc536791778)

[6.3.2 M-PHY and Related Libraries 28](#_Toc536791779)

[6.4 Directory Structure 29](#_Toc536791780)

[6.5 Ace 29](#_Toc536791781)

[6.6 Lintra 29](#_Toc536791782)

[6.7 Synthesis 29](#_Toc536791783)

[6.7.1 Clocks 29](#_Toc536791784)

[6.7.2 Clock Diagram 30](#_Toc536791785)

[6.7.3 Constraint Files 30](#_Toc536791786)

[6.7.4 Scan Insertion 30](#_Toc536791787)

[6.8 Formal Verification 30](#_Toc536791788)

[6.9 CDC 30](#_Toc536791789)

[7 Physical Integration 31](#_Toc536791790)

[8 Integration Test Plan 32](#_Toc536791791)

[9 Appendix 33](#_Toc536791792)

[9.1 Subsystem connectivity details 33](#_Toc536791793)

About This Template

How to Use This Template

Do not remove any headings from this document. If you do not need the headings to describe your IP, enter “Not applicable” under the heading. This lets the reader know that you did not overlook this topic.

In the main document that follows, add new headings that you need to fully describe the integration of this IP. Add them in the appropriate chapters.

Most red text in this document contains instructions for filling out the section where it appears. The tag for most of this red text is called “Gaps.” You should replace this text with the content appropriate for that section, ensuring that the text is tagged appropriately (for example, with the BodyText or List Bullet style). If a section is not relevant, do not remove it; instead just replace the “Gap” text with “Not applicable” and apply the BodyText style.

Goal of This Document

This document should contain all information an integration team would need to accomplish the task without needing to seek help from another source. Try not to refer to other documents for required information; do so only if you include specific instructions for obtaining those documents, and only if you are sure your audience has access to them. Verify all links. This should be a self-contained guide for integration.

# Introduction

## Audience

The information in this document is intended for an integration or design team that is using this IP.

## Supported Projects

This document supports the following projects at the listed RTL maturity level. Type “NA” if this IP is not included in a specific project, or remove those project names from the table.

|  |  |
| --- | --- |
| Project Name | IP Maturity Level |
| CNX | 1P0 |
| KNH | 1P0 |
| ICX | 1P0 |
| ERL |  |
| SPR | 0P5 |
| BER-D | 0P5 |
|  |  |

## Terminology

The table below defines uncommon terms used in this document.

|  |  |
| --- | --- |
| Term | Definition |
| CDC | Clock Domain Controller, IRR logic |
| ForcePwrGatePOK | IOSF SB message telling the IP to prepare for reset |
| side\_pok, prim\_pok | Indication of whether or not the endpoint can accept traffic |
|  |  |
|  |  |

## Related Documents

If you need more information on this IP, you may find these documents helpful.

|  |  |
| --- | --- |
| Document Title | Location |
| [Chassis Reset Architecture HAS v1\_0RC1\_review](https://sharepoint.amr.ith.intel.com/sites/MDGArchMain/Converged/chassisWG/HAS%2010%20RC%20%20Q4%202013/Chassis%20Reset%20Architecture%20HAS%20v1_0RC1_review.pdf) | <https://sharepoint.amr.ith.intel.com/sites/MDGArchMain/Converged/chassisWG/HAS%2010%20RC%20%20Q4%202013/Forms/AllItems.aspx> |
| [Chassis Power Management HAS Rev1 0RC1\_review](https://sharepoint.amr.ith.intel.com/sites/MDGArchMain/Converged/chassisWG/HAS%2010%20RC%20%20Q4%202013/Chassis%20Power%20Management%20HAS%20Rev1%200RC1_review.pdf) |
| pkgS LTF slides | HSD 1011440773 |
| Warm reset LTF slides | HSD1404020485 |
| Introductory meeting slides | $IP\_RELEASES/reference\_library/<version>/doc/ForcePwrGatePOK.pptx |
| Release Notes |  |
| Signal List |  |
| GPSB endpoints and cdc\_wrappers | <https://sharepoint.amr.ith.intel.com/sites/10nmServer/chassis/RCF/Shared%20Documents/GPSB%20endpoints%20and%20cdc_wrappers.xlsx> |
| VISA connectivity | <https://sharepoint.amr.ith.intel.com/sites/10nmCon/CHASSIS/MsgChn/DFD/Shared%20Documents/0.8%20Parameter%20Spreadsheets/0p8_redrop1_ww30j_1_dtf_visa_packetizer_parameters.xlsx> |

## Opens, Risks, and Assumptions

|  |  |  |  |
| --- | --- | --- | --- |
| Item # | Description | Comment | Status (Open or Closed)/Date |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

## Contact Information

If you need additional help, use the contact information below.

|  |  |  |
| --- | --- | --- |
| Function | Name | Email |
| IP Architecture | John Ayers, Hartej Singh | [john.r.ayers@intel.com](mailto:john.r.ayers@intel.com), [artej.singh@intel.com](mailto:) |
| IP Verification | N/A |  |
| IP Integration | Ken Correll | [ken.correll@intel.com](mailto:ken.correll@intel.com) |
| Doc Template Owner | Susann Flowers | [susann.flowers@intel.com](mailto:susann.flowers@intel.com) |
|  |  |  |
|  |  |  |

## Document Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision Number | Description of Change | Date | Revised By |
| 0.4 | Integrated previous separate integration guides into one document | 15ww28.5 | Ken Correll |
| 0.5 | Updated for the 0p5 drop | 15ww50 | Ken Correll |
| 0.6 | Added section detailing Agent Endpoints responsibilities (3.1.4), fixed some typo’s | 15ww51.4 | Ken Correll |
| 0.7 | Added I/O signal list for dft\_reset\_sync and fpg\_pok | 16ww02.5 | Ken Correll |
| 0.8 | Added notes on integrating the cdc\_wrapper into the subsystem | 16ww06 | Ken Correll |
| 0.9 | Added example of VISA connectivity and location of spreadsheet, added additional IOSF SB Endpoint parameter to set to 1 | 16ww37 | Ken Correll |
| 0.10 | Added another parameter option for the dft\_reset\_sync | 16ww45 | Ken Correll |
| 0.11 | Clarified section 3.1.3 – Visa connectivity | 16ww51.5 | Ken Correll |
| **1.0** | 1p0 update, parameters for cdc\_wrapper | 17ww08.3 | Ken Correll |
| 1.1 | Added path to find the security questionaires, fixed I/O for visa outputs | 17ww28f | Ken Correll |
| 1.2 | Clarify connection requirements for pgcb\_rst\_b, pok\_reset\_b and ip\_pm \_wake – HSD’s sent to modify connection to pgcb\_rst\_b | 17ww45.1 | Ken Correll |
| 1.3 | Updated cdc\_wrapper diagram to show extra pipe stages | Ww47.1 | Ken Correll |
| 1.4 | Update for wave3, pok\_mgr has been removed | 18ww16 | Ken Correll |
| 1.5 | Include new IP’s ip\_disable & fuse\_hip\_glue – release version: | 19ww5c | Ken Correll |

# Quick Start

## Downloading Sub IP

The cdc\_wrapper, dft\_reset\_sync and pok\_mgr models are in rcf\_widget\_library repo

$IP\_RELEASES/rcf\_widget\_library/<version>/

Note that all have been uniquified with rcfwl\_ prefix.

## Integrity Checks for Standalone IP

Following are steps for running standalone integrity checks of this IP. It is assumed that the environment variable IP\_ROOT is set to the path of the IP collateral.

1. Build the model:

bman -dut rcfwl -mc=cdc\_wrapper

bman -dut rcfwl -mc=dft\_reset\_sync

bman –dut rcfwl –mc= ip\_disable

bman –dut rcfwl –mc=fuse\_hip\_glue

~~bman -dut rcfwl -mc=pok\_mgr~~

or to build all ~~three~~

bman –dut rcfwl

1. Run a simple regression:

There are no standalone regressions for the cdc\_wrapper or dft\_reset\_sync. Regression is done at chassis level. ~~Pok\_mgr does have verification collateral~~

1. Run synthesis:  
   febe –dut rcfwl  
   febe –dut rcfwl –s all +s .dc +s .fv +s .caliber -flow ip\_release -gkturnin

# Overview

## cdc\_wrapper

### IP Block Diagram

The CDC\_wrapper takes the CDC from IRR and adds circuitry to make it function correctly without the inclusion of a PGCB. In addition, support has been added to include synchronizer cells where necessary and to attach to multiple endpoints.



This drawing is available in the repo doc/widget block diagrams.vsdx, tab cdc\_wrapper.

This document describes the cdc\_wrapper. The ClockDomainController integration guide, with notes on using the CDC without the normally accompanying PGCB is in the CDC Integration Guide\_notes.docx.

### CDC\_wrapper Functional Interface

The CDC Integration Guide\_notes.docx remains the guide to understanding the CDC. More information on the interface signals is in that document while here the connections to the surrounding circuitry is described.

#### Parameters

Only CDC parameters that are exposed in CDC\_wrapper are listed. Other CDC parameters are explained in the CDC Integration guide.

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Default | Valid Values | Description |
| DEF\_PWRON | 0 | **0,1** | **Default Power On**: Determines whether the initial state after reset\_b de-assertion is powered on or powered off.  If this is set to one clkreq and pok will be asserted. When set to zero, clkreq, pok and gclock\_active will be de-asserted.  Prefered state is 0. |
| IT\_BITS | 4 | ≥1 | **IDLE TIMER BITS:** must match the values set in inputs like cfg\_clkreq\_syncoff\_holdoff |
| AREQ | 1 | ≥1 | **Asynchronous Clock Requests:** Determines the number of asynchronous clock request inputs. Providing dedicated inputs for different asynchronous sources ensures glitch free aggregation of different requests but will require per-request synchronization, increasing design area/cost.  This parameter is SIP-specific (does not depend on SOC where SIP is being used). |
| NUM\_EP\_ATTACHED | 1 | ≥1 | Number of endpoints attached – used to size the bitwise OR of the ISM bits |
| ISM\_AGT\_IS\_NS | 0 | 0,1 | Not to be used without consultation |
| DFX\_NUM\_OF\_FEATURES\_TO\_SECURE | 1 | 1 | SecurePlugin parameter |
| DFX\_SECURE\_WIDTH | 4 | 4 | SecurePlugin parameter |
| DFX\_USE\_SB\_OVR | 0 | 0 | SecurePlugin parameter |
| DFX\_VISA\_BLACK | 2’b11 | 2’b11 | SecurePlugin parameter |
| DFX\_VISA\_GREEN | 2'b01 | 2'b01 | SecurePlugin parameter |
| DFX\_VISA\_ORANGE | 2'b10 | 2'b10 | SecurePlugin parameter |
| DFX\_VISA\_RED | 2'b00 | 2'b00 | SecurePlugin parameter |
| DFX\_EARLYBOOT\_FEATURE\_ENABLE | {1’b0, DFX\_VISA\_GREEN} | {1’b0, DFX\_VISA\_GREEN} | SecurePlugin parameter |
| DFX\_SECURE\_POLICY\_MATRIX | 0x692492854519 | 0x692492854519 | SecurePlugin parameter |

#### Functional Interface Signals

NOTE: For pgcb\_rst\_b, pok\_reset\_b, ip\_pm\_wake, pmrc domain is the same as the pm\_ip\_side\_rst\_b[pmrc domain] that is used for the endpoint the cdc\_wrapper is connected to.

|  |  |  |  |
| --- | --- | --- | --- |
| Name | I/O | Clock | Connection |
| pgcb\_clk | Input | - | Local PMA’s pmsb\_clk (x4 clock) |
| pgcb\_rst\_b | Input | pgcb\_clk | Pm\_ip\_side\_rst\_b[pmrc domain] |
| Clock | Input | - | Clock for the domain being controlled  side\_clk or prim\_clk |
| clkack | Input | Async | PMA or clkreqaggr response to clkreq generated by cdc\_wrapper |
| clkreq | Output | Pgcb\_clk | Connect to PMA input or to clkreqaggr |
| pok\_reset\_b | Input | async | Pm\_ip\_side\_rst\_b[pmrc domain] |
| gclock\_req\_async[AREQ-1:0] | In | clock | Asynch clock requests from end point |
| ism\_fabric  [NUM\_EP\_ATTACHED-1:0] | In | Clock | ISM bits for all the EP’s associated with this cdc\_wrapper |
| ism\_agent  [NUM\_EP\_ATTACHED-1:0] | In | Clock | ISM bits for all the EP’s associated with this cdc\_wrapper |
| cfg\_clkgate\_disable | In | Async | tie ‘0 |
| cfg\_clkreq\_ctl\_disable | In | Async | tie ‘0 |
| cfg\_clkgate\_holdoff | In | Async | tie ‘0 |
| cfg\_pwrgate\_holdoff | In | Async | tie ‘0 |
| cfg\_clkreq\_off\_holdoff | In | Async | tie ‘4 |
| cfg\_clkreq\_syncoff\_holdoff | In | Async | tie ‘4 |
| forcepgpok\_pok | In | Async | Type field [0] from decoded ForcePwrGatePOK message. |
| forcepgpok\_pgreq | In | Async | Type field [1] from decoded ForcePwrGatePOK message. |
| ip\_pg\_wake | In | Pgcb\_clk | pm\_ip\_wake[pmrc domain] |
| pok | out | Clock | Connect to all the associated endpoint pok inputs, and to PMA input ip\_pm\_pok[n] |
| gclk\_async\_ack\_synced  [AREQ-1:0] | out | Clock | Ack for gclock\_req\_async inputs |
| ism\_locked | Out | Clock | Connect to agent side\_ism\_lock\_b |

### VISA, DFx

Visa lane assignments are made by the DFD group and are maintained here: <https://sharepoint.amr.ith.intel.com/sites/10nmCon/CHASSIS/MsgChn/DFD/SitePages/Home.aspx>.

|  |  |  |  |
| --- | --- | --- | --- |
| Name | I/O | Clock | Connection |
| fismdfx\_force\_clkreq | input | clock |  |
| fscan\_byprst\_b[1:0] | input | clock |  |
| fscan\_rstbypen[1:0] | input | clock |  |
| fscan\_shiften | input | clock |  |
| fscan\_latchopen | input | clock |  |
| fscan\_latchclosed\_b | input | clock |  |
| fscan\_clkungate | input | clock |  |
| fscan\_clkungate\_syn | input | clock |  |
| fscan\_mode | input | clock |  |
| fscan\_sdi | Input | clock |  |
| ascan\_sdo | output | clock |  |
| fglobal\_visa\_start\_id\_pgcb\_clk[8:0] | Input | pgcb\_clk |  |
| fglobal\_visa\_start\_id\_clk[8:0] | Input | clock |  |
| fvisa\_serstrb | Input |  |  |
| fvisa\_frame | Input | clock |  |
| fvisa\_serdata | Input | clock |  |
| avisa\_debug\_data\_pgcb\_clk[7:0] | output | pgcb\_clk |  |
| avisa\_strb\_clk\_pgcb\_clk | output | pgcb\_clk |  |
| avisa\_debug\_data\_clk[15:0] | output | clock |  |
| avisa\_strb\_clk\_clock[1:0] | output | clock |  |
| fdfx\_powergood | Input | clock |  |
| fdfx\_secure\_policy[DFX\_SECURE\_WIDTH-1:0] | Input | policy\_update |  |
| fdfx\_earlyboot\_exit | Input | clock |  |
| fdfx\_policy\_update | Input |  |  |
| oem\_secure\_policy[DFX\_SECURE\_WIDTH-1:0] | Input | policy\_update |  |

For wave1 IP’s only: Note that the clock associated with avisa\_debug\_data\_clk should be the same clock that is connected to the cdc\_wrapper.clock pin, but directly from the CCDU to the adl.

For all other versions, the standard connection for avisa\_debug\_data\_clk includes the clock pin associated with those two lanes

### ClockDomainController changes

There have been a few modifications to the imported ClockDomainController:

1. Add SDG compliant INTEL\_SVA\_OFF and INTEL\_SIMONLY defines to
   1. rcfwl\_CdcMainClock.sv
   2. rcfwl\_CdcPgClock.sv
   3. rcfwl\_ClockDomainController.sv
2. modify parameters for a ctech\_doublesync so that randomization is between 1 and 2 clocks (HSD 1405876123) in rcfwl\_CdcPgClock.sv to eliminate an assertion that is harmless in this application

### Integration examples

The following example show how a cdc\_wrapper could be connected to a sbbridge.



In this drawing, red denotes the global GPSB fabric but does not show the router whose port connects to the bridge global endpoint. Similarily green denotes the local GPSB fabric and does not show the routers envolved to generate it.

### Agent Endpoint responsibilities

The cdc\_wrapper generates a POK signal for an endpoint based off of the agent’s ISM bits after the indication that a ForcePwrGatePOK message has been received by the PMA through the PMA’s outputs ForcePGPOK\_type outputs.

It is the agent’s responsibility to make sure that the endpoints ISM bits do not transition to the IDLE state if there is an outstanding NP request. This is done by setting the IOSF\_Sideband\_Endpoint parameter ISM\_COMPLETION\_FENCING to 1 and EXPECTED\_COMPLETIONS\_COUNTER to 1.

It is also the agent’s responsibility to expose the IOSF\_Sideband\_Endpoint input pin side\_ism\_lock\_b. This pin will be driven by the cdc\_wrapper and will keep the endpoint from transitioning out of the idle state once pok has been deasserted.

### Timing Diagrams

<to be supplied>

### Security Questionaire

This document can be found in this directory, QuestionnaireExport\_cdc\_wrapper.xlsx.

## dft\_reset\_sync

### Interface signals

|  |  |  |
| --- | --- | --- |
| Signal name | I/O | Description |
| clk\_in | Input | Clock that the incoming reset is to be synchronized to |
| rst\_b | Input | Incoming asynchronous reset |
| fscan\_rstbyp\_sel | Input | DFX reset bypass select |
| fscan\_byprsb\_b | Input | DFX reset signal |
| synced\_rst\_b | Output | reset output where deasserting edge is synchronized to clk\_in |

### Parameters

|  |  |
| --- | --- |
| Name | description |
| STRAP | 0: circuit acts as a reset synchronizer for the deasserting edge only  1: circuit simplifies to a dfx controlled mux (see diagram below)  2: synchronizes both assertion and deassertion of the incoming reset |

### IP Block Diagram

The dft\_reset\_sync is a small circuit that can be used to synchronize the deasserting edge of an asynchronous reset with dft related features included.

### Functional description

When the strap parameter is set to ‘0’ (the default case):



When the strap parameter is set to ‘1’, the circuit simplifies to:



The clk input will still be present and dangling.

With the strap parameter set to 2 the circuit synchronizes both edges of the incoming reset.



### Security Questionaire

This document can be found in this directory, QuestionnaireExport\_dft\_reset\_sync.xlsx.

## ip\_disable

A simple ciruit to allow a single named IP to intercept control signal coming from the PMA and disable their assertion or deassertion if an IP is to be disabled.

Parameter: INPUT\_SIGNAL\_POLARITY = 0 // 0 to disable active high signal, 1 to disable active low signal

Logic:

if (INPUT\_SIGNAL\_POLARITY == 1) // to disable an active low input – keep it low

begin : AND

logic ip\_disable\_b;

rcfwl\_ctech\_lib\_inv ipd\_inv(.a(ip\_disable), .o1(ip\_disable\_b));

rcfwl\_ctech\_lib\_and ipd\_and(.a(ip\_disable\_b), .b(signal\_in), .o(signal\_out));

end

else // to disable an active high input – keep it high

begin : OR

rcfwl\_ctech\_lib\_or ipd\_or(.a(ip\_disable), .b(signal\_in), .o(signal\_out));

end

## fuse\_hip\_glue

## A required by the fuse group that needed a repo in $IP\_MODELS. Not for general consumption.

# Design Information for Integration

This chapter is targeted to the IP verification team responsible for integrating this IP into a local test bench.

## RTL Directory Structure

$MODEL\_ROOT/src/rtl/widgets/\*

## Clock, Power and Reset Domains

Power Domain for the cdc\_wrapper should be always be Vinf.

### Clock Domain Diagram

## Embedded Building Blocks/Custom Logic

N/A

|  |  |  |
| --- | --- | --- |
| Name | Library | Synthesis exchange? |
|  |  |  |
|  |  |  |
|  |  |  |

## RTL Configuration Parameters

The following tables list all RTL configuration parameters for this IP. If the parameter is derived, it must not be changed by the user.

### Mandatory Parameters

cdc\_wrapper:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter Name | Derived? | Range | Default | Descriptions (including interdependencies) |
| DEF\_PWRON | NO | 0/1 | 0 | Determines state of pok and clkreq outputs coming out of reset |
| RST | No | 1 to N | 1 | Optional synch path for resets used by the subsystem |
| AREQ | No | 1 to N | 1 | Number of asynchronous clkreq’s being attached |
| NUM\_EP\_ATTACHED | No | 1 to N | 1 | Number of EndPoints attached – number of ISM ports |

dft\_reset\_sync:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter Name | Derived? | Range | Default | Descriptions (including interdependencies) |
| Strap | NO | 0/1/2 | 0 | Determines the functionality per section 3.2.2 |

### Boundary Scan Parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter Name | Derived? | Range | Default | Descriptions (including interdependencies) |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

### Test Data Register Parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter Name | Derived? | Range | Default | Descriptions (including interdependencies) |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

## Testbench Parameters

The following table lists all testbench configuration parameters for this IP.

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter Name | Range | Default | Descriptions (including interdependencies) |
|  |  |  |  |
|  |  |  |  |

## IP Straps

|  |  |
| --- | --- |
| Strap | Purpose |
|  |  |
|  |  |
|  |  |

## Fuses

Not applicable.

## Power Information

### Power Supply

Vinf

### Static Clock Gating

Not applicable

### Power Gating

Not applicable.

### Bumps and Their Power Domains

Not applicable

## Power-up Requirements

Not applicable.

## Macros used by IP

Not applicable.

## Other Design Considerations

Not applicable

## DFx Considerations

### DFx Top-Level Signals

### DFx Clock Definition

### Clock Crossings

### N/ADebug Registers

### Scan – Clock Gating in RTL

Document the override signal that makes clocks free-running in scan mode.

### Scan – Reset Override

Describe the mechanism to override reset during scan mode.

### TAP and Associated Registers

## System Startup

### Power-up Sequence

Not applicable

### Initialization Sequence

Not applicable

### Device Configuration

Not applicable

### Header for Windows Boot

Not applicable

## Security Considerations

Not applicable

### Security Threats

Not applicable.

### Security Tests

Not applicable.

### Interface Signals Implemented for Security

Not applicable.

## RTL Design Libraries

## RTL Uniquification

The cdc\_wrapper, dft\_reset\_sync, ~~and pok\_mgr~~ models in rcf\_widget\_library has been uniquified with the prefix rcfwl.

To uniquify, run the script: scripts/uniquifyme <prefix>

## Emulation Support

Not applicable

# Verification Information for Integration

## IP Testbench Overview

## Reusable IP Testbench Components

Following are details of interfaces that are to be connected at the SoC level.

|  |  |  |
| --- | --- | --- |
| Signal | Connect to | Description |
|  |  |  |
|  |  |  |

### Collage or Sandbox Files

### IP Environment

Not applicable

#### Configuring the IP Environment

Not applicable

#### Saola Environment Walkthrough

Following are the components of RAL:

|  |  |
| --- | --- |
| File | Description |
| N/A | N/A |
|  |  |
|  |  |

#### Saola/RAL Components

|  |  |  |  |
| --- | --- | --- | --- |
| SAOLA components | Description | SoC recommendations | Required? |
| N/A |  |  |  |
|  |  |  |  |
|  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| RAL components | Description | SoC recommendations | Required? |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

#### System Manager

Not applicable

### N/A. IP does not has any fuse requirements.Sequences

Sequences are located here: N/A

#### Sequence for Bringing up the IP

#### N/ABFM Sequences

|  |  |  |  |
| --- | --- | --- | --- |
| Sequence Name | Description | Parameters | Saola Phase |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

#### IOSF Primary/Sideband BFM Sequences

|  |  |  |  |
| --- | --- | --- | --- |
| Sequence Name | Description | Parameters | Saola Phase |
| N/A |  |  |  |
|  |  |  |  |
|  |  |  |  |

#### Other Reusable Sequences

|  |  |  |  |
| --- | --- | --- | --- |
| Sequence Name | Description | Parameters | Saola Phase |
| N/A |  |  |  |
|  |  |  |  |
|  |  |  |  |

#### IP Test Sequences

|  |  |  |
| --- | --- | --- |
| Test Sequence Name | Parameters | Function |
| N/A |  |  |
|  |  |  |
|  |  |  |

#### SoC Requirements for Sequence Reuse

#### Sequence File Dependencies

### Ip does not used any sequences or extended sequences.Miscellaneous

#### Using the Runtime or Post-Processing Checkers

Not applicable

#### Environment Files

Not applicable

#### Coverage

Not applicable.

## Environment Settings and Files

### Base Test

### N/AConfiguration Object

Not applicable

### API

## N/ADescription of Reusable Tests

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test Name | Runcmd | Range | Transaction | Source |
| N/A |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

## Description of Reusable Automation Scripts

## N/ASupported Compiler Options for Simulation

The table below summarizes the supported options.

|  |  |  |
| --- | --- | --- |
| Argument | Input | Example |
| N/A |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

## Reusable Simulation RUNMODEs

|  |  |
| --- | --- |
| RUNMODE | Description |
| N/A |  |
|  |  |
|  |  |

## RTL Verification Libraries

|  |  |  |
| --- | --- | --- |
| Library | Version | Special usage |
| N/A |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# Tools and Methodology for Integration

## Supported Tools

The following tools are used in the integration of this IP. For versions supported by each release, see Release Notes in the "doc" directory of the release package.

* VCSMX
* OVM
* Ace
* SaolaLintra
* Design Compiler
* Conformal
* 0-In

## Environment Variables

Set the following environment variables as listed.

|  |  |
| --- | --- |
| Variable | Description |
| N/A |  |
|  |  |
|  |  |

## HIP Libraries Included in Release

|  |  |  |
| --- | --- | --- |
| Library | Version | Location |
| N/A |  |  |
|  |  |  |
|  |  |  |

### Register Files or SRAM

Not applicable

### M-PHY and Related Libraries

|  |  |  |
| --- | --- | --- |
| Library | Version | Date |
| N/A |  |  |
|  |  |  |
|  |  |  |

## Directory Structure

Doc

Cfg

Bin

Src

Tools

Target

## Ace

Paths to acerc: $MODEL\_ROOT/cfg/rcf\_widget\_library.acerc

Location of udf file:$MODEL\_ROOT/cfg/rcfwl\_hdl.udf

Model to use when importing libraries:

rcfwl\_cdc\_wrapper\_rtl\_lib

rcfwl\_dft\_reset\_sync\_rtl\_lib

~~rcfwl\_pok\_mgr\_rtl\_lib~~

Elaboration options not exported:N/A

Required content in sip\_shared\_libs:N/A

## Lintra

Lintra Version: per tool contour

Lintra location : tools/lintra/

Location of waiver files: tools/lintra/waivers

Location of Lintra patches & configuration: N/A

Location of Lintra report file for warnings and errors:

$MODEL\_ROOT/target/lint/<model\_name> /<model\_name>.log

## Synthesis

All synthesis constraints and io definitions are in tools/syn/<model>/inputs

### Clocks

1. Primary Clocks

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| No. | Clock name | Clock period | Clock waveform | Clock source |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

1. Generated Clocks

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. | Clock Name | Master Clock Name | Master Clock Source | Edges | Source |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

### Clock Diagram

### Constraint Files

Not applicable

### Scan Insertion

Not applicable

## Formal Verification

Not applicable

## CDC

Not applicable

# Physical Integration

This chapter is intended to capture the aspect ratio requirements and any fixed size impact, etc., of memories that will be used in the IP.  It is not intended to be “accurate” so much as an indication of what the impact and limitations might be.  As this information will be based on the current memories, it would be only as accurate as the current design.

|  |  |
| --- | --- |
| Array type and number of instances | N/A |
| Functional usage (how many bits are used) |  |
| Highest functional clock frequency |  |
| Floorplan details |  |
| Security requirements |  |
| IP power draw limitations for array testing |  |

# Integration Test Plan

Not applicable

# Appendix

## Subsystem connectivity details

For more information on the connectivity planned with the cdc\_wrapper in your subsystem, please refer to the ‘GPSB endpoints and cdc\_wrappers’ spreadsheet reference in section 1.4

and to the integration examples in section 3.1.3.