Chassis Power Gating Monitor and Tracker

User Guide

2013WW26

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|  |  |  |
| --- | --- | --- |
| Revision | Date | Description |
| 0.71 | WW46.1 | * Enhancements/Bug fixes * [4796471](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=4796471) – tracker now prints Accessible flow properly * [4796548](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=4796548) – user can now specify any tradker name. * Updated block diagram. * Added clarifications and fixed typos. See change bars |
| 0.73 |  | * + Support for new restore flow.   + Support for warm reset flow (INACCESSIBLE\_PON state)   + Please see the monitor state machine. |
| 2013WW25 | WW25 | * Support for d3 and d0i3 signals and DFX signals fdfx\_pgcb\_bypass and fdfx\_pgcb\_ovr |
| 2013WW26 | WW26 | * Added coverage model (see tracker/monitor userguide section 1.7 ). * Made following bug fixes.  |  |  |  | | --- | --- | --- | | [5077365](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=5077365) | [Assertions are not using fab\_pmc\_pg\_rdy\_ack\_b, fab\_pmc\_pg\_rdy\_nak\_b synced to PMC clockdomain](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=5077365) | [Bug](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=5077365) | | [5077849](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=5077849) | [pok values in the monitor not reset correctly during global reset event](https://vthsd.intel.com/hsd/seg_softip/bug/default.aspx?bug_id=5077849) | Bug | |

# Chassis Power Gating Monitor and Tracker

The Chassis Power Gating Monitor/Tracker will be used in any Chassis compliant IP to validate the workings of power gating flows using a runtime scoreboard or a post processing MOAT. In the PMC env the model interfaces with the signals between the Central Controller(RTL) and a number of PGBCs (BFMs). In any other IP the setup is the same except the Central Controller will be a BFM and the PGCB will be RTL.

The block diagram shows an example of the CC BFM in a SIP and in a fabric test environment.

NOTE: Please see the userguide for details on the env and the configuration object.

NOTE: There could be an environment where both and fabric and SIP exists too.



**Chassis power gating tracker in a SIP env**



**Chassis power gating tracker in Fabric env**

This tracker tracks the Chassis power gating interface (SIP and fabric) and the side and prim pok signals. It also prints the state of each PGCB and prints out a message when an IP goes to inaccessible, accessible or powered on state.

## 

## PowerGatingMonitorSeqItem - Monitor transaction Item

The table below shows all the variables in the monitor transaction item

|  |  |  |
| --- | --- | --- |
| Variable Name | Type | Description |
| startTime | time | The start time of the event |
| typ | PowerGating::EventType | **MSG** : this means the cycle is an message that prints the state of a SIP  **FAB**: a fabric event  **SIP**: a SIP event  **FET**: a FET event  **SIG** : resets  **POK**: pok signal |
| evnt | PowerGating::Event\_e | Specifies the event type.  Possible values are specified in in the below table. |
| source | int | This is the index number of the SIP or Fabric PGCB, FET block, POK or PMC wake.  The value would be < NUM\_SIP\_PGCB or NUM\_FAB\_PGCB or NUM\_SB\_EP or NUM\_PRIM\_EP or NUM\_PMC\_WAKE |
| sourceName | string | This the name of the SIP or SIP PGCB or Fabric PGCB or the FET block name as specified in the config object. |
| state | PowerGating::MonitorState | The current power state of the SIP, SIP PGCB or Fabric PGCB.  Please see the state machine diagram for more details on the states of the SIP PGCB and Fabric PGCBs.  In addition , the possible SIP states are:  **INACCESSIBLE\_PON** : this corresponds to warm reset. The SIP is in this state if all PGCBs are in INACC\_PON.  **INACCESSIBLE\_POFF** : this corresponds to cold reset. The SIP is in this state id all PGCBs are in INACC\_POFF and all poks are deasserted.  **ACCESSIBLE\_POFF** : The SIP is in this state if all the PGCBs are in ACC\_POFF state.  **ACCESSIBLE\_PON**: The SIP is in this state if all the PGCBs in the UG state.  OPEN: function disable case |

The table below shows the typ and possible events, what the sourceName means and where is the state valid.

|  |  |  |  |
| --- | --- | --- | --- |
| typ | evnt | soureName | state |
| SIG | RST\_ASD,  RST\_DSD,  Reset asserted and deasserted | Not applicable | Not applicable |
| POK | PRIM\_POK\_ASD,  SIDE\_POK\_ASD,  PRIM\_POK\_DSD,  SIDE\_POK\_DSD,  Side and prim POK asserted or deasserted. | The name is either the SIP name or the SIP PGCB name depending on whether the POK is from an EP in a PGD or an AON domain. | Not applicable |
| FET | FET\_ON  FET\_OFF  FET\_ON\_ACK  FET\_OFF\_ACK  FET off/on and fet\_en\_ack\_b assertion/deassertion | The name of the fet block as specified in the config object | Not applicable |
| SIP | SIP\_PG\_REQ,  SIP\_UG\_REQ,  SIP\_PG\_ACK,  SIP\_UG\_ACK,    SIP\_RESTORE,  SIP\_RESTORE\_DSD,  FDFX\_BYPASS\_ASD,  FDFX\_BYPASS\_DSD,  FDFX\_OVR\_ASD,  FDFX\_OVR\_DSD,  D3\_ASD,  D3\_DSD,  D0I3\_ASD,  D0I3\_DSD  The SIP pg handshakes | The SIP PGCB name as specified by the config object. | The current state of the SIP PGCB |
| PMC\_SIP\_WAKE,  PMC\_SIP\_WAKE\_DSD,  PMC wake assertion/deassertion | The name is either the SIP name or the SIP PGCB name depending on whether the PMC\_WAKE is for an EP in a PGD or an AON domain. | Not applicable |
| SW\_PG\_REQ,  SW\_PG\_REQ\_DSD, | The SIP PGCB name as specified by the config object. | Not applicable |
| FAB | FAB\_IDLE,  FAB\_IDLE\_EXIT  FAB\_PG\_ACK,  FAB\_PG\_ACK\_DSD,  FAB\_PG\_NACK  FAB\_PG\_NACK\_DSD  FAB\_PG\_REQ,  FAB\_UG\_REQ,  Fabric signal assertion and deassertion | The Fabric PGCB name as specified by the config object. | The current state of the fabric PGCB |
| MSG | Not applicable | The name of SIP whose state is being reported | The current state of the SIP. The possible values are specified in the above table. |

## Agent Functions to get configuration information

Scoreboards can know the configuration information using the getConfig function.

|  |  |  |
| --- | --- | --- |
| Function | Return type | Description |
| getConfig | PowerGatingConfig array | This returns PowerGatingConfig ovm objects. Use the methods specified below to get the configuration information all SIPs and Fabric connected to the agent. |

#### PowerGatingConfig functions

|  |  |  |
| --- | --- | --- |
| Function | Return type | Description |
| getSIPPGCBConfig | PowerGatingSIPFabConfig array | This returns an array of ovm objects indexed by the signal index 0 to NUM\_SIP\_PGCB |
| getFabricPGCBConfig | PowerGatingSIPFabConfig array | This returns an array of ovm objects indexed by the signal index 0 to NUM\_FAB\_PGCB |
| getSIPConfig | PowerGatingSIPFabConfig array | This returns an array of ovm objects containing configuration information about the SIPs. |

##### PowerGatingSIPPGCBConfig

|  |  |  |
| --- | --- | --- |
| Function | Return Type | Description |
| getName | String | Name of the SIP/Fabric PGCB or the SIP |
| getSIPName | String | Name of the SIP that PGCB is connected to. This is only valid for SIP PGCB configuration. |
| getFETName | String | Returns in the name of the fet\_en\_b signal that is connected to this SIP/Fabric PGCB |
| getSideEPIndex | int array | Returns the array of signal index of the side\_pok signals that is connected to this SIP PGCB. This is only valid for SIP PGCB configuration. |
| getPrimEPIndex | int array | Returns the array of signal index of the prim\_pok signals that is connected to this SIP PGCB. This is only valid for SIP PGCB configuration. |
| getAONSideEPIndex | int array | Returns the signal index of all Side EPs in the AON domain in the SIP. This is only valid for SIP configuration. |
| getAONPrimEPIndex | int array | Returns the signal index of all Prim EPs in the AON domain in the SIP This is only valid for SIP configuration. |

## Monitor state machines

The state machine diagram shows all the possible states of the monitor transaction item’s state and the tracker will print.

### SIP PGCB state machine



**SIP PGCB state machine**

The state machine shows all the possible states of a SIP PGCB that gets printed in the tracker. These are also the possible values of the state in the monitor sequence item.

### Fabric PGCB state machine



**Fabric PGCB state machine**

The state machine shows all the possible states of a Fabric PGCB that gets printed in the tracker. These are also the possible values of the state in the monitor sequence item.

## Tracker Overview

This tracker will print the change in state of all the Chassis power gating interface signals along with the current state of the PGCBs.

The example below has 3 SIP PGCBs name PGD1, PGD2 and PGD3 and 3 Fabric PGCBs. The SIP PGCBs belong to the GPIO SIP.

The trakcer first prints configuration information that shows how the SIPs an fabrics are mapped to the fet blocks, side and primary endpoints.

## Sample Output

=============================================================================================================

Tracker(PowerGatingPrinter) : Instance(ccAgent01printer)

=============================================================================================================

SIP PGCBs tracked in this tracker are :{PGD1} {PGD2} {PGD3} {PGD4}

SIPs tracked in this tracker are :{TEST} {GPIO}

Fabric PGCBs tracked in this tracker are :{FAB0} {FAB1} {FAB2}

CONFIGURATION MAPPING

SIP PGCB MAPPING

==========================================

| |SRC | MAPPING |

| PGCB | IN | SIP | FET | SIDE | PRIM |

==========================================

| PGD1 | 0 | GPIO | DOM0 | 0, | -- |

| PGD2 | 1 | GPIO | DOM1 | 1, | -- |

| PGD3 | 2 | GPIO | DOM2 | 2, | -- |

| PGD4 | 3 | | DOM3 | -- | -- |

FABRIC PGCB MAPPING

====================

| |SRC | |

| PGCB | IN | FET |

====================

| FAB0 | 0 | DOM0 |

| FAB1 | 1 | DOM0 |

| FAB2 | 2 | DOM0 |

SIP AON MAPPING

=======================

| | AON MAPPING |

| SIP | SIDE | PRIM |

=======================

| TEST | -- | 1, |

| GPIO | -- | 0, |

END CONFIGURATION MAPPING

=============================================================================================================

| | | NAME | | | STATE |

| | | PGCB | | | |

| | | /IP |SRC | | |

| TIME | TYP | /FET | IN | EVENT | PGD1 | PGD2 | PGD3 | PGD4 | FAB0 | FAB1 | FAB2 |

=============================================================================================================

| 1000.0 ns| SIG | -- | 0 | RST\_DSD | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD1 | 0 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD2 | 1 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD4 | 2 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | GPIO | 3 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100125.0 ns| SIP | PGD2 | 1 | SIP\_UG\_REQ | INAPF | UG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100165.0 ns| SIP | PGD1 | 0 | SIP\_UG\_REQ | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100165.0 ns| SIP | PGD3 | 2 | SIP\_UG\_REQ | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100175.0 ns| POK | GPIO | 0 | PRIM\_POK\_ASD | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100185.0 ns| FET | DOM1 | 1 | FET\_ON | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100185.0 ns| FET | DOM1 | 1 | FET\_ON\_ACK | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100245.0 ns| SIP | PGD2 | 1 | SIP\_UG\_ACK | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100335.0 ns| FET | DOM0 | 0 | FET\_ON | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100335.0 ns| FET | DOM0 | 0 | FET\_ON\_ACK | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100365.0 ns| POK | PGD2 | 1 | SIDE\_POK\_ASD | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100425.0 ns| SIP | PGD1 | 0 | SIP\_UG\_ACK | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| FET | DOM2 | 2 | FET\_ON | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| FET | DOM2 | 2 | FET\_ON\_ACK | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| POK | PGD1 | 0 | SIDE\_POK\_ASD | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

=============================================================================================================

| | | NAME | | | STATE |

| | | PGCB | | | |

| | | /IP |SRC | | |

| TIME | TYP | /FET | IN | EVENT | PGD1 | PGD2 | PGD3 | PGD4 | FAB0 | FAB1 | FAB2 |

=============================================================================================================

| 100525.0 ns| SIP | PGD3 | 2 | SIP\_UG\_ACK | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100535.0 ns| MSG | GPIO | -- | GPIO is in ACCESSIBLE\_PON state

| 100665.0 ns| SIP | PGD1 | 0 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | PGD2 | 1 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | PGD4 | 2 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | GPIO | 3 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100745.0 ns| POK | PGD3 | 2 | SIDE\_POK\_ASD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100765.0 ns| POK | PGD3 | 2 | SIDE\_POK\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100775.0 ns| SIP | PGD3 | 2 | SIP\_PG\_REQ | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100775.0 ns| POK | GPIO | 0 | PRIM\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100805.0 ns| POK | PGD1 | 0 | SIDE\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100805.0 ns| POK | PGD2 | 1 | SIDE\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100835.0 ns| SIP | PGD3 | 2 | SIP\_PG\_ACK | PWRON | PWRON | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100855.0 ns| SIP | PGD2 | 1 | SIP\_PG\_REQ | PWRON | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100895.0 ns| SIP | PGD1 | 0 | SIP\_PG\_REQ | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109385.0 ns| FET | DOM2 | 2 | FET\_OFF | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109385.0 ns| FET | DOM2 | 2 | FET\_OFF\_ACK | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109435.0 ns| SIP | PGD1 | 0 | SIP\_PG\_ACK | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109495.0 ns| FET | DOM0 | 0 | FET\_OFF | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109495.0 ns| FET | DOM0 | 0 | FET\_OFF\_ACK | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109505.0 ns| SIP | PGD2 | 1 | SIP\_PG\_ACK | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109515.0 ns| MSG | GPIO | -- | GPIO is in INACCESSIBLE\_POFF state

| 109605.0 ns| FET | DOM1 | 1 | FET\_OFF | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

#### Configuration information

CONFIGURATION MAPPING

SIP PGCB MAPPING

==========================================

| |SRC | MAPPING |

| PGCB | IN | SIP | FET | SIDE | PRIM |

==========================================

| KVM | 0 | CSME | DOM0 | 0, | -- |

| PMT | 1 | CSME | DOM1 | 1, | -- |

| SUSR | 2 | CSME | DOM2 | 2, | -- |

FABRIC PGCB MAPPING

====================

| |SRC | |

| PGCB | IN | FET |

====================

| FAB0 | 0 | DOM0 |

| FAB1 | 1 | DOM0 |

| FAB2 | 2 | DOM0 |

SIP AON MAPPING

=======================

| | AON MAPPING |

| SIP | SIDE | PRIM |

=======================

| CSME | -- | 0, |

The tracker prints configuration information for the user and MOAT to know the mapping between a PGCB and pmc\_wake, sw\_req etc.

User can disable printing the configuration information using DisableCOnfigPrinting methos provided in the config object.

Note that in an environment where there are no fabric PGCB, the FABRIC PGCB MAPPING table is not printed.

Similarly, in an environment where there are no SIP PGCBs, the SIP PGCB MAPPING table is not printed.

If there are no AON endpoints in the env, the SIP AON MAPPING table is not printed.

|  |  |
| --- | --- |
| Field | Description |
| PGCB | The name (as specified though the config object) of the SIP or Fabric PGCB.  For fabrics, the only configuration information is the fet\_en mapping. |
| SRC IN | The signal index of the SIP or Fabric PGCB |
| MAPPING | SIP - The name of the SIP (as specified in the config object) of the SIP that PGCB belongs to  FET - This is the mapping information of fet\_en\_b. This is the name of the fet\_en the PGCB is connected to.  SIDE and PRIM – These are index of the side and prim poks of the EPs the PGD this PGCB is controlling. Multiple indices are separated by a comma. |
| AON MAPPING | SIDE and PRIM EP – These are the index of the AON side and prim poks in the SIP. Multiple indices are separated by a comma. |

#### Fields of the tracker

NOTE: The number of columns within the STATE column will depend on the number of PGCBs.

|  |  |
| --- | --- |
| Field | Description |
| TIME | The time the event occured |
| TYP | The type of cycle  **MSG** : this means the cycle is an message that prints the state of a SIP  **FAB**: a fabric event  **SIP**: a SIP event  **FET**: FET event  **SIG** : resets  **POK**: POK signals |
| NAME PGCB/IP/FET | Whenever the cycle type is SIG, this field is printed as --.  **PGCB NAME**  The name (as specified though the config object) of the SIP or Fabric PGCB or FET block.  Whenever the cycle type is FAB or SIP, this field represents the name of the SIP or Fabric PGCB.  Whenver the event is POK, this field represents the name of the SIP PGCB where the event is happening.  **SIP NAME**  The name (as specified through the config object) of the SIP.  Whenever the cycle type is POK, this field represents the name of the SIP where the event is happening. This is only valid for AON side and prim EPs.  **FET NAME**  Whenever the cycle is FET, this represents the name of the FET domain where the event is happening. |
| SRC IN | The source singal index of the PGCB/FET, wake, sw req or POK signal  Since there could be multiple EPs within a PGCB and multiple AON EP within an SIP, this fields specifies the index of the POK that changes. |
| EVENT | The type of event. The possible events are specified in the the monitor transaction item cmd above. |
| STATE | The currect state of all the PGCBs. See state machine for possible values.  NOTE: The field names are variable since they are the names specified during configuration.  NOTE: Also The number of columns within the STATE column will depend on the number of PGCBs.  Note that the initial state of the PGCBs needs to be specified though the config object. |

The table below shows the typ and possible events, what the sourceName means and where is the state valid.

|  |  |  |
| --- | --- | --- |
| TYPE | EVENT | NAME PGCB/IP/FET |
| SIG | RST\_ASD,  RST\_DSD,  Reset asserted and deasserted | Not applicable |
| POK | PRIM\_POK\_ASD,  SIDE\_POK\_ASD,  PRIM\_POK\_DSD,  SIDE\_POK\_DSD,  Side and prim POK asserted or deasserted. | The name is either the SIP name or the SIP PGCB name depending on whether the POK is from an EP in a PGD or an AON domain. |
| FET | FET\_ON  FET\_OFF  FET\_ON\_ACK  FET\_OFF\_ACK  FET off/on and fet\_en\_ack\_b assertion/deassertion | The name of the fet block as specified in the config object |
| SIP | SIP\_PG\_REQ,  SIP\_UG\_REQ,  SIP\_PG\_ACK,  SIP\_UG\_ACK,    SIP\_RESTORE,  SIP\_RESTORE\_DSD,  FDFX\_BYPASS\_ASD,  FDFX\_BYPASS\_DSD,  FDFX\_OVR\_ASD,  FDFX\_OVR\_DSD,  D3\_ASD,  D3\_DSD,  D0I3\_ASD,  D0I3\_DSD  The SIP pg handshakes | The SIP PGCB name as specified by the config object. |
| PMC\_SIP\_WAKE,  PMC\_SIP\_WAKE\_DSD,  PMC wake assertion/deassertion | The name is either the SIP name or the SIP PGCB name depending on whether the PMC\_WAKE is for an EP in a PGD or an AON domain. |
| SW\_PG\_REQ,  SW\_PG\_REQ\_DSD, | The SIP PGCB name as specified by the config object. |
| FAB | FAB\_IDLE,  FAB\_IDLE\_EXIT  FAB\_PG\_ACK,  FAB\_PG\_ACK\_DSD,  FAB\_PG\_NACK  FAB\_PG\_NACK\_DSD  FAB\_PG\_REQ,  FAB\_UG\_REQ,  Fabric signal assertion and deassertion | The Fabric PGCB name as specified by the config object. |
| MSG | Not applicable | The name of SIP whose state is being reported |

#### How to read MSG printed?

|  |
| --- |
| The only MSG the tracker prints in the state of a SIP.  The possible SIP states are:  INACCESSIBLE\_PON : this corresponds to warm reset. The SIP is in this state if all PGCBs are in INAPN and all the AON POKs are deasserted.  INACCESSIBLE\_POFF : this corresponds to cold reset. The SIP is in this state id all PGCBs are in INAPF and all AON POKs are deasserted.  ACCESSIBLE\_POFF : The SIP is in this state if all the PGCBs are in ACPOF state.  ACCESSIBLE\_PON: The SIP is in this state if all the PGCBs in the PWRON state.  OPEN: function disable case |

#### How to read the configuration information and the tracker?

=============================================================================================================

| | | NAME | | | STATE |

| | | PGCB | | | |

| | | /IP |SRC | | |

| TIME | TYP | /FET | IN | EVENT | PGD1 | PGD2 | PGD3 | PGD4 | FAB0 | FAB1 | FAB2 |

=============================================================================================================

| 1000.0 ns| SIG | -- | 0 | RST\_DSD | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD1 | 0 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD2 | 1 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | PGD4 | 2 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100045.0 ns| SIP | GPIO | 3 | PMC\_SIP\_WAKE | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100125.0 ns| SIP | PGD2 | 1 | SIP\_UG\_REQ | INAPF | UG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100165.0 ns| SIP | PGD1 | 0 | SIP\_UG\_REQ | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100165.0 ns| SIP | PGD3 | 2 | SIP\_UG\_REQ | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100175.0 ns| POK | GPIO | 0 | PRIM\_POK\_ASD | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100185.0 ns| FET | DOM1 | 1 | FET\_ON | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100185.0 ns| FET | DOM1 | 1 | FET\_ON\_ACK | UG\_HS | UG\_HS | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100245.0 ns| SIP | PGD2 | 1 | SIP\_UG\_ACK | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100335.0 ns| FET | DOM0 | 0 | FET\_ON | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100335.0 ns| FET | DOM0 | 0 | FET\_ON\_ACK | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100365.0 ns| POK | PGD2 | 1 | SIDE\_POK\_ASD | UG\_HS | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100425.0 ns| SIP | PGD1 | 0 | SIP\_UG\_ACK | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| FET | DOM2 | 2 | FET\_ON | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| FET | DOM2 | 2 | FET\_ON\_ACK | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100475.0 ns| POK | PGD1 | 0 | SIDE\_POK\_ASD | PWRON | PWRON | UG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

=============================================================================================================

| | | NAME | | | STATE |

| | | PGCB | | | |

| | | /IP |SRC | | |

| TIME | TYP | /FET | IN | EVENT | PGD1 | PGD2 | PGD3 | PGD4 | FAB0 | FAB1 | FAB2 |

=============================================================================================================

| 100525.0 ns| SIP | PGD3 | 2 | SIP\_UG\_ACK | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100535.0 ns| MSG | GPIO | -- | GPIO is in ACCESSIBLE\_PON state

| 100665.0 ns| SIP | PGD1 | 0 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | PGD2 | 1 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | PGD4 | 2 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100665.0 ns| SIP | GPIO | 3 | PMC\_SIP\_WAKE\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100745.0 ns| POK | PGD3 | 2 | SIDE\_POK\_ASD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100765.0 ns| POK | PGD3 | 2 | SIDE\_POK\_DSD | PWRON | PWRON | PWRON | PWRON | PWRGT | PWRGT | PWRGT |

| 100775.0 ns| SIP | PGD3 | 2 | SIP\_PG\_REQ | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100775.0 ns| POK | GPIO | 0 | PRIM\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100805.0 ns| POK | PGD1 | 0 | SIDE\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100805.0 ns| POK | PGD2 | 1 | SIDE\_POK\_DSD | PWRON | PWRON | PG\_HS | PWRON | PWRGT | PWRGT | PWRGT |

| 100835.0 ns| SIP | PGD3 | 2 | SIP\_PG\_ACK | PWRON | PWRON | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100855.0 ns| SIP | PGD2 | 1 | SIP\_PG\_REQ | PWRON | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 100895.0 ns| SIP | PGD1 | 0 | SIP\_PG\_REQ | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109385.0 ns| FET | DOM2 | 2 | FET\_OFF | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109385.0 ns| FET | DOM2 | 2 | FET\_OFF\_ACK | PG\_HS | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109435.0 ns| SIP | PGD1 | 0 | SIP\_PG\_ACK | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109495.0 ns| FET | DOM0 | 0 | FET\_OFF | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109495.0 ns| FET | DOM0 | 0 | FET\_OFF\_ACK | INAPF | PG\_HS | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109505.0 ns| SIP | PGD2 | 1 | SIP\_PG\_ACK | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109515.0 ns| MSG | GPIO | -- | GPIO is in INACCESSIBLE\_POFF state

| 109605.0 ns| FET | DOM1 | 1 | FET\_OFF | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

| 109605.0 ns| FET | DOM1 | 1 | FET\_OFF\_ACK | INAPF | INAPF | INAPF | PWRON | PWRGT | PWRGT | PWRGT |

The above high-lighted event indicates that the pmc\_ip\_pg\_wake signal asserted for PGD1..

So in the subsequent events, you see that PGD1 is waking up.

The second highlighted event shows the POK is asserting. The NAME column is “GPIO” which shows it is a AON pok.

The third high-lighed event is a message that shows that all the PGCBs in GPIO are PWRON state and all the AON POKs are asserted.

The fourth high-lighted event indicates DOM2 fet block is turning off.

## Using the Monitor and Tracker

This section provides an example of necessary steps to implement the connection between monitor and tracker.

Refer to section 10 in the userguide for more detail information on the configuration methods

### Naming the tracker file

The user can specify the tracker name using setTrackerName method in the configuration object of the agent. Please see the usergudie for more information on the method.

### Connecting A Scoreboard to the Testbench

This section provides an example of necessary steps to implement the connection between monitor and Scoreboard.

Here is an example scoreboard.

class TestScoreboard extends ovm\_scoreboard;

`ovm\_component\_utils(TestScoreboard)// register component to the factory

//analysis fifo for receiving the transactions

analysis\_fifo#(PowerGatingMonitorSeqItem) monitor;

local PowerGatingMonitorSeqItem Packet\_in; // Transactions from input monitor

// define constructor

function new( string name , ovm\_component parent = null );

super.new( name , parent );

endfunction //new

function void build();

ovm\_object temp;

monitor= new("power FIFO");

Packet\_in= new;

endfunction// build

task run();

forever begin

string str1, str2;

monitor.get(Packet\_in);

$sformat(str1,"TYP = %3s, EVENT = %10s, SOURCE\_NAME = %4s, STATE = %5s", Packet\_in.typ, Packet\_in.evnt, Packet\_in.sourceName, Packet\_in.state);

//print it out

ovm\_report\_info(get\_full\_name(), {" SCOREBOARD TRANSACTION: ", str1});

end

endtask:run

endclass: TestScoreboard

This scoreboard can be connected to the monitor as shown below in the

testSB = TestScoreboard::type\_id::create("SB", this);

During the connect phase, the agent’s analysis port should be connected to the scoreboard’s analysis fifo. The agent’s analysis port of called monitorAnalysisPort.

ccAgent.**monitorAnalysisPort**.connect(testSB.monitor.analysis\_export);

### Getting configuration information

The agent has a getConfig() method that can be used ot get configuration information for scoreboards. Please see section 1.2 in this document for details on the methods.

### Controlling Messages

There is a method DisableCOnfigPrinting provided in the config object to disable printing the configuration information onto the tracker.

The configuration is not printed by default.

## Coverage Model

The coverage model can be disabled using the argument +define+DISABLE\_CHASSIS\_POWER\_GATING\_COVERAGE

|  |  |  |
| --- | --- | --- |
| **Description** | **Cover Property/Covergroup name** | **Associated check (eventually need to link to the rules ss)** |
| If there are multiple PGCBs, cover all permutations of Accessible PG and PWRON state.   covergroup cov\_permute\_acc\_state @(pmc\_ip\_pg\_ack\_b);  option.comment = "Cover each PGCB in Acc state while other PGCBs are in Pwron state";  permute\_acc\_states: coverpoint pmc\_ip\_pg\_ack\_b iff ($countones(side\_pok) == NUM\_SB\_EP && $countones(prim\_pok) == NUM\_PRIM\_EP);  endgroup | cov\_permute\_acc\_state | IP-specific |
| ip\_pmc\_pg\_req\_b -> 0 followed by pmc\_ip\_pg\_ack\_b -> 0 while reset\_b == 1 | cov\_pg\_req\_ack\_fell | Power Gating Assertions |
| ip\_pmc\_pg\_req\_b -> 1 followed by pmc\_ip\_pg\_ack\_b -> 1 while reset\_b == 1 | cov\_pg\_req\_ack\_rose | Power Gating Assertions |
| negedge of sw\_pg\_req\_b (pg\_req\_b == 1) followed by pg\_req\_b -> 0 while reset\_b == 1 | cov\_sw\_pg\_fell | Power Gating Assertions |
| posedge of sw\_pg\_req\_b while pg\_req\_b == 0 while reset\_b == 1 | cov\_sw\_pg\_rose | IP-specific. IP must not wake up. |
| negedge of sw\_pg\_req\_b (pg\_req\_b == 1) when pmc\_wake = 1 while reset\_b == 1 | cov\_sw\_pg\_asd\_pmc\_wake1 | IP-specific. IP must not power gate. |
| negedge and posedge of fet\_en\_b while reset\_b = 1 | cov\_fet\_fell, cov\_fet\_rose | Power Gating Assertions |
| posedge and negedge of pmc\_wake while reset\_b = 1 | cov\_pmc\_wake\_rose | Power Gating Assertions |
| negedge and posedge of prim\_pok while reset\_b = 1 | cov\_prim\_pok\_\* | Power Gating Assertions |
| negedge and posedge of side\_pok while reset\_b = 1 | cov\_side\_pok\_\* | Power Gating Assertions |
| posedge and negedge of pmc\_ip\_restore\_b while reset\_b = 1 | cov\_restore\_fell | Power Gating Assertions |
| negedge and posedge of fab\_pmc\_idle while reset\_b = 1 | cov\_fab\_idle\_rose, cov\_fab\_idle\_fell | Power Gating Assertions |
| pmc\_fab\_pg\_rdy\_req\_b -> 0 followed by ack -> 0 | cov\_fab\_pg\_req\_fell\_ack | Power Gating Assertions |
| pmc\_fab\_pg\_rdy\_req\_b -> 1 followed by ack -> 1 | cov\_fab\_pg\_req\_rose | Power Gating Assertions |
| pmc\_fab\_pg\_rdy\_req\_b -> 0 followed by nack -> 0 | cov\_fab\_pg\_req\_fell\_nack |  |
| Each PGCB in PWRON and Accessible PG state | cov\_pwron\_acc\_state | Power Gating Assertions |
| Each PGCB in Inaccessible POFF state (cold reset/sleep state) | cov\_inacc\_state | Power Gating Assertions |
| Each PGCB in Inaccessible PON state (warm reset state) | N/A | IP-specific or Chassis boot and reset coverage model |
| pmc\_wake -> 1 which PGCB in Inaccessible state | cov\_pmc\_wake\_in\_inacc\_state | Power Gating Assertions |
| pmc\_wake -> 1 which PGCB in Accessible state | cov\_pmc\_wake\_in\_acc\_state | Power Gating Assertions |