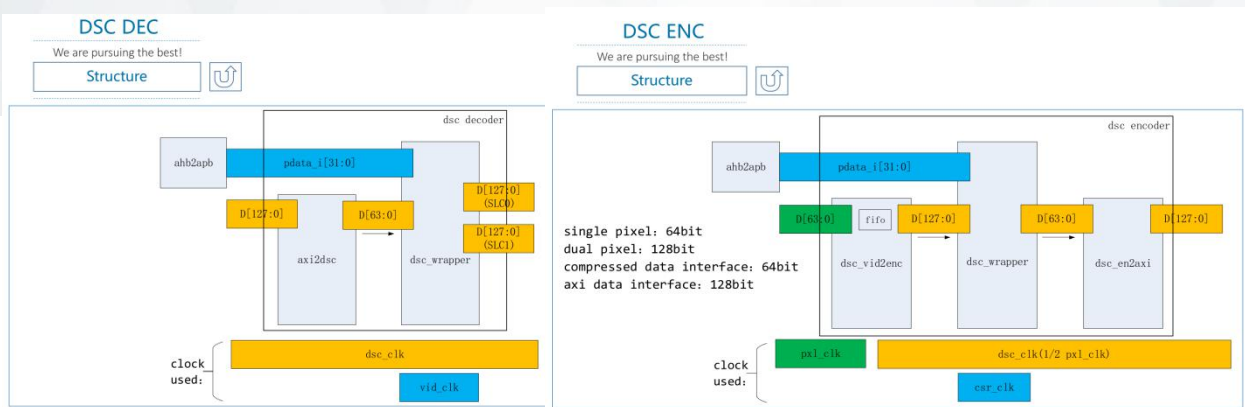


部分项目内容展示

DSC IP Simulation & Integration:



enc dec structure

Structure

ESC:

low power memory with bist -> normal .11 memory

```
tsln40lphsb1024x144m4f_250a_ttlplv25c.v 1024x16x4
tsln40lphsb1024x24m8f_250a_ttlplv25c.v
tsln40lphsb2048x24m4f_250a_ttlplv25c.v
tsln40lphsb256x128m4f_250a_ttlplv25c.v 256x4x2
tsln40lphsb256x64m4f_250a_ttlplv25c.v
tsln40lphsb256x8m4f_250a_ttlplv25c.v
tsdn40lpa1024x64m4f_130b_ttlplv25c.v 612x4x2
tsdn40lpa64x40m4f_130b_ttlplv25c.v

S011HD2P_512X64M2.v
S011HD2P_64X40M2.v
S011HDSP_1024x24M8.v
S011HDSP_1024x36M8.v
S011HDSP_2048x24M8.v
S011HDSP_256x64M8.v
S011HDSP_256x8M8.v
```

DSC:

low power memory with bist -> normal .11 memory

```
tsln40lphsb128x128m4f_250a_ss0p99vm40c.v
tsln40lphsb256x72m4f_250a_ttlplv25c.v 128x16x2
tsln40lphsb512x72m4f_250a_ttlplv25c.v 512x16x2
tsdn40lpa256x48m4f_130b_ttlplv25c.v
tsdn40lpa256x64m4f_130b_ttlplv25c.v

S011HD2P_256X48M2.v
S011HD2P_256X64M2.v
S011HDSP_256X36M8.v
S011HDSP_512X36M8.v

S011HDSP_256x64M8.v
```

使用 smic .11 mc 工具产生 memory 替换 ip 环境 memory

可节省的dsc_enc/dec memory, 基于SMIC011 SP Ram										
Module	Whole Module Syn Area	Original Mem Size in Design	跑不满	无法产生	Num	Actually Used Size	Actual Total Area	Ideal Size	Ideal Area	Ideal预计节省比例
enc	8050000	1024x16			16	1024x16	965712	512x16	621984	35.59%
		512x128	✓		4	512x128	1067040	256x128	767520	28.07%
		128x48		✓	16	256x48	1172928	128x48	-	-
		128x6		✓	16	256x6	220416	128x6	-	-
dec	6900000	128x48		✓	8	256x48	586464	128x48	-	-
		64x512	✓	✓	4	256x512	3070080	32x512	-	-

优化 memory 选择与使用以节省面积

dsc 中有 128x128 的端口 ram。
我们的 memory compiler:
单口 ram:深度最低 256, 位宽最高 64bit。
双口 ram:深度最低 128, 位宽最高 64bit。
可以两个 ram 一组来实现 128bit 位宽。
如果使用单口 ram:
一个 256x64 端口 ram 面积为 1170x82=95940, 8 个 95940x8=767520。
如果使用双口 ram:
一个 128x64 双端口 ram 面积为 630x185=116550, 8 个 116550x8=932400。

SMIC HD Single-Port SRAM Compiler 0.11um G Logic Process

Instance Name: S011HDSP

Words: 256

Multiplexer Width: 8

Bits: 64

Configuration: Words 256 Mux 8 Bits 64

Relative Footprint: 1170 x 82

SMIC HD 2-Port SRAM Compiler 0.11um G Logic Process

Instance Name: S011HD2P

Words: 128

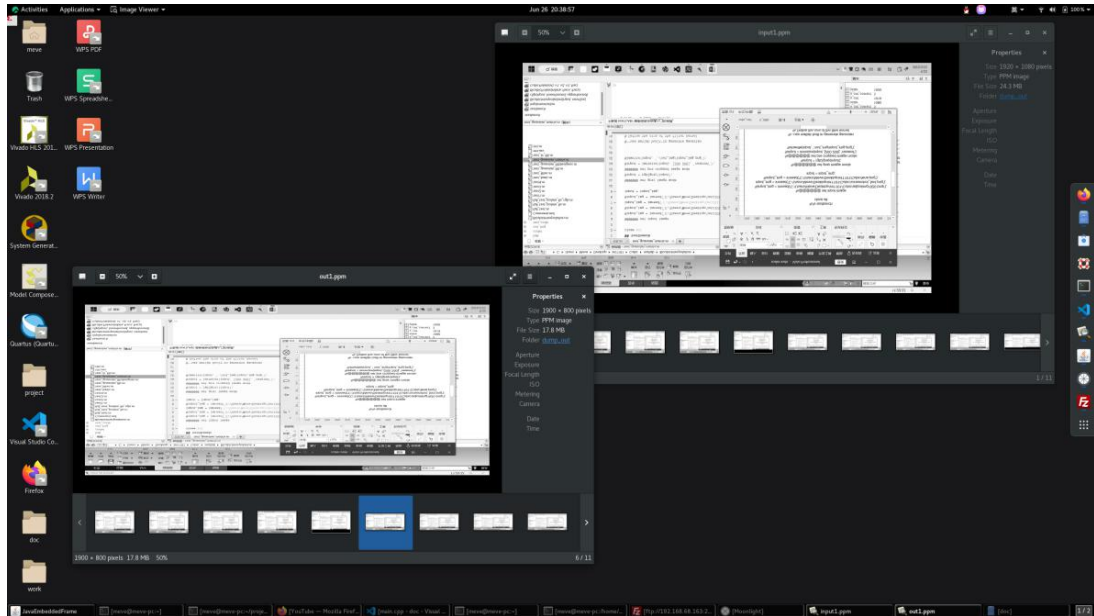
Multiplexer Width: 2

Bits: 64

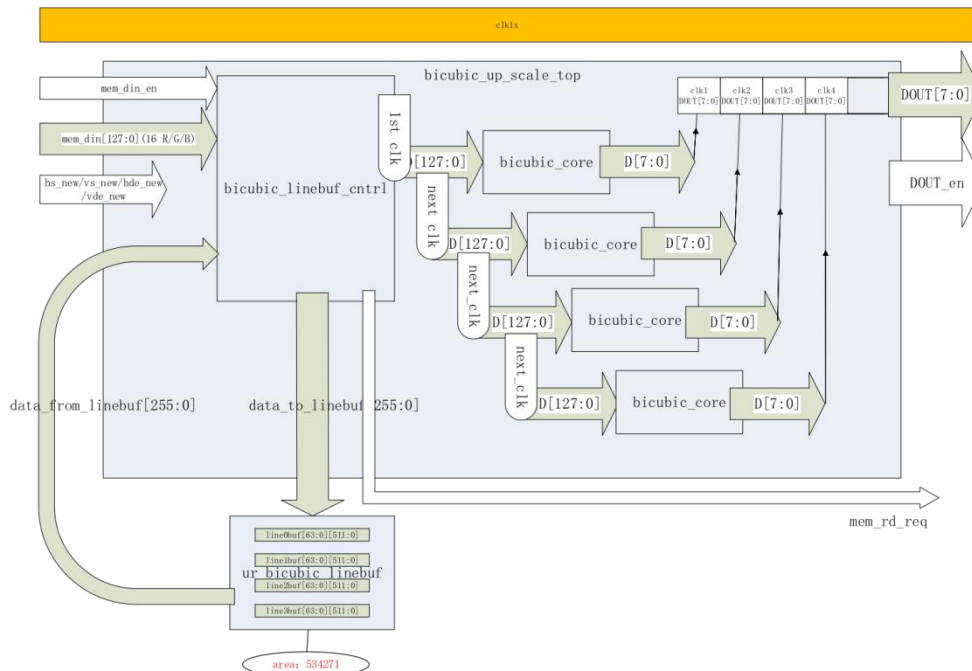
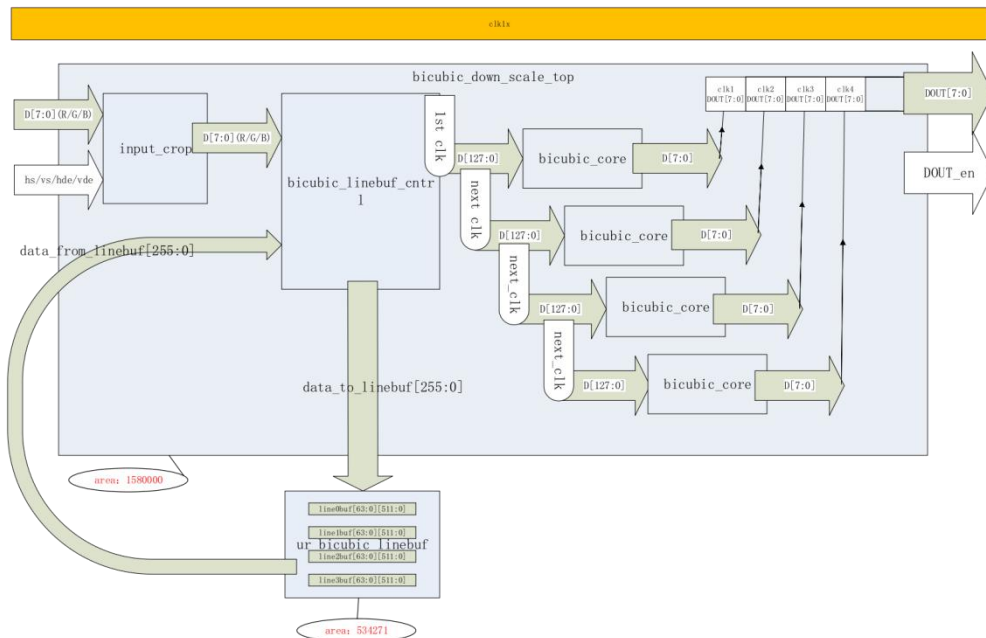
Configuration: Words 128 Mux 2 Bits 64

Relative Footprint: 630 x 185

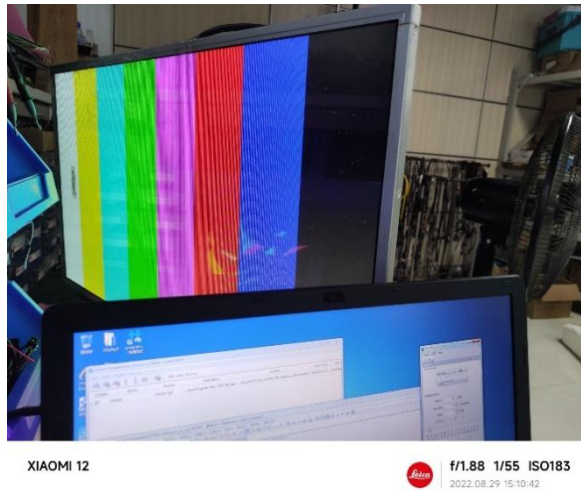
● 2D Scaler:



Example of 2D Scaler for 1920x1080 scale down to 1900x800



● TCON Project:



1856 TCON 项目 FPGA 上屏测试图

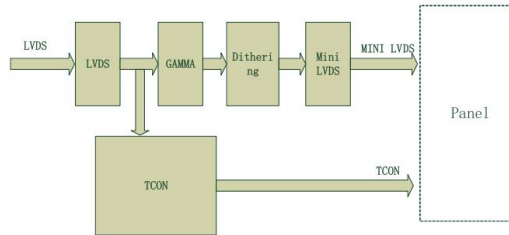
LVDS SPEC

We are pursuing the best!

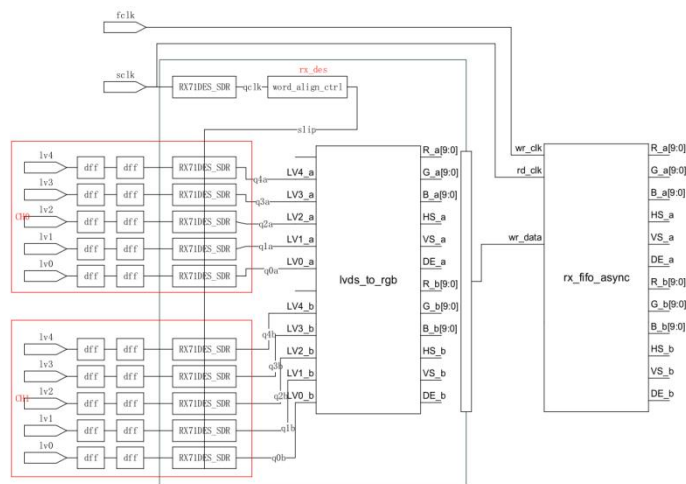
General

lvds_rx to mini-lvds_tx:

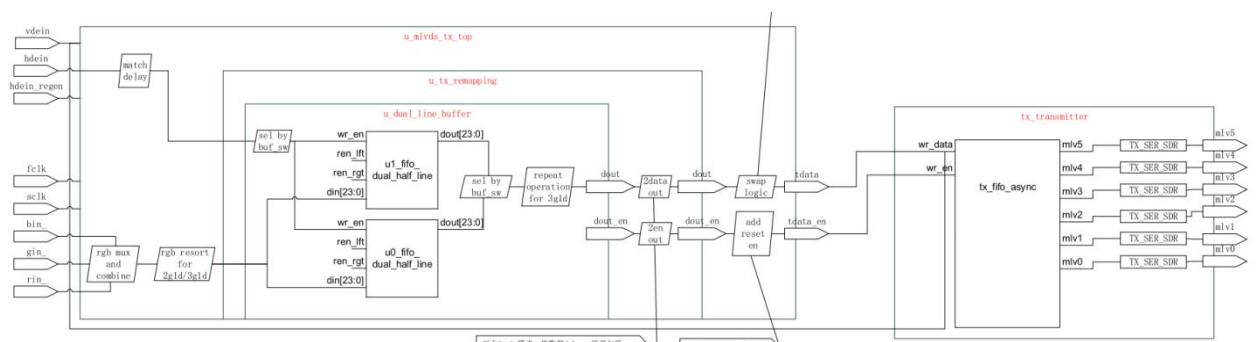
lvds_rx接收lvds信号（vesa/jeida 1ch/2ch RGB666/RGB888/RGB101010），通过将每个通道的lvds串行数据缓存，得到对应的7bit 序列，通过RGB信号在lvds通道上的不同映射标准，解出对应的R、G、B、HS、VS、DE信号，RGB信号可以进行一些处理再发送给mini-lvds tx。
mini-lvds_tx在收到数据后，只将rgb信号对应映射标准，通过mini_lvds通道发送。hs、vs、de单独发送。



System Structure

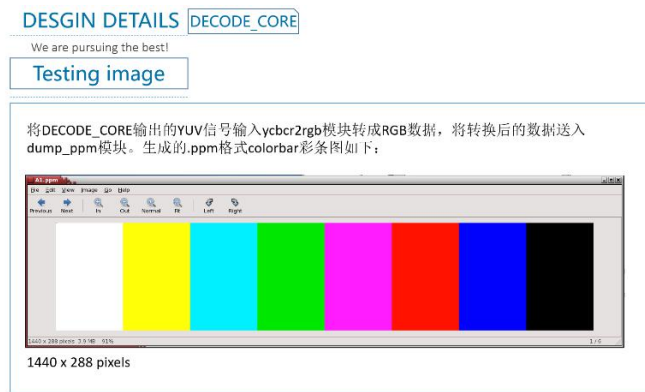


lvds rx structure

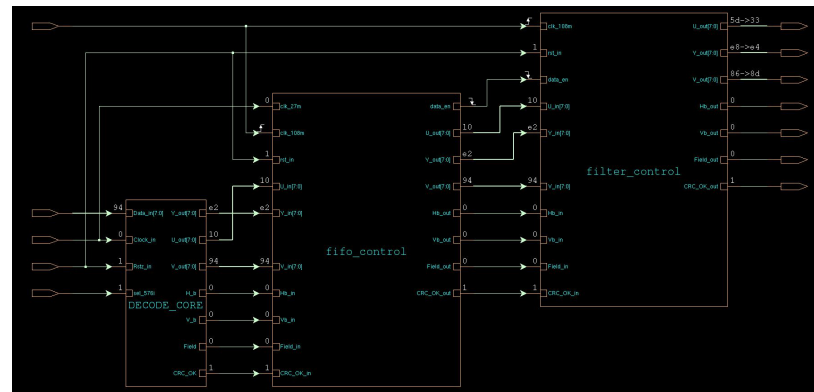


mini-lvds tx structure

- BT656 Decoder:



解码测试图



Project Structure

- Others