

22 April 2017

Microprocessor  $\Rightarrow$  Sujan Sir

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26 April 2017

### Reference Books

1. Microprocessor and Interfacing

— Douglas V. Hall

Final

(3 or 2 set)  $\rightarrow$  8085

(3 or 4 set)  $\rightarrow$  8086

(1 or 2 set)  $\rightarrow$  Advance Processor

Total # set Questions.

## Lec - 1

■ What is Microprocessor?

process  $\Leftrightarrow$  manipulate

■ What about micro?

Microchip was invented in the early 1970.

■ Was there ever a "mini" - processor?

— No

■ Definition of Microprocessor

xm न त्रये रा!

■ Programmable Device

The sequence of instructions

■ Instructions

The group of operations is called an instruction set.

## It takes in

Through input device

## It numbers

- A binary digit is called a bit.
- The group of bits is called a word.

## It words, bytes etc

## It Arithmetic and Logic Operations

## It stored in memory

8086 mainly 1 byte के रूप में।

## It produces

Human readable form.

## It Microcomputer, Microprocessor and Microcontroller

Microcomputer - It computer or processing unit होता है।  
microprocessor उसी रूप।

Microcontroller - silicon chip which includes micro processor  
I/O in a single chip.

## It takes in

Through input device

## It Numbers

- A binary digit is called a bit.
- The group of bits is called a word.

## It words, bytes etc

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8086 mainly 1 byte कर्म करता।

## It Produces

Human readable form.

## It Microcomputer, Microprocessor and Microcontroller

Microcomputer - for Computer OR processing unit लिए  
microprocessor use करता।

Microcontroller - silicon chip which includes microprocessor,  
I/O in a single chip.

## Microprocessor Vs Microcontroller

Micro controller  $\rightarrow$  direct I/O port connect করা হয়ে—

বাস।

Q. What are the differences between Microprocessor and Micro controller? (এই দুটি গুরুত্বপূর্ণ)

## Block Diagram of Microcontroller

### Memory

### Memory Hierarchy (Important)

- Capacity
- Cost
- Access time

\* Q. Memory Hierarchy কি নিচে দিক শোনো—  
বোতাম অন্তরে Access time. why?

Ans. Because Bus এর Access এবং আরেক উপর এবং  
Bus is slower.

### Memory Map Address

## ■ Instruction Execution cycle

1. Fetch
2. Decode
3. Execute

\* Modern processor କେବଳ — କାର୍ଯ୍ୟକ୍ଷତି — parallelly କରି —  
which is called "Pipelining".

## ■ How does Microprocessor Connects to External World?

Address Decoder : Decode କେବୁ — particular address  
send କରି — ଖାଲି ।

## ■ Kind of Languages :

### ■ Machine Language :

8-bit

$$2^8 = 256 \quad \left( 256 \text{ ଏହି } (ଚର୍ବି — ଟଙ୍କୁଡ଼ି — ଓ ଅଛି) \right)$$

\* Binary ଏହି ପରିବର୍ତ୍ତି Hexadecimal  $\rightarrow$  Convert କରି — ଏହି ।

### ■ Assembly Language :

Symbolic Code use କରି — ଏହି for easy understanding.

## Assembling the Program

— Hand Assembly

— Assembler

29 April 2017

Lec - 2

## Electrical Numerical Integrator and Calculator

- The first Transistor was created in 1947.
- The first Integrated Circuit was created in 1959.
- 1<sup>st</sup> intel processor was 4004.

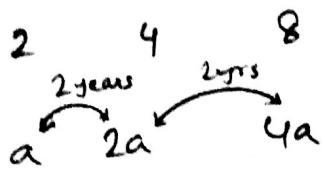
## Moore's Law

আম্বু-লি-টি-২ সহৃদয়- "Integrated Circuit" double ২৮৯ মাস  
(24 months)

## \* Math

2017-তে Transistor প্রতি MMFT 4000, 2021 কত?

কত-নেবুর কত হবে? (Using Moore's Law)



$$ax^0 \ ax^1 \ ax^2$$

$$\boxed{ax^{\frac{n}{2}}}$$

Generalised form

$$\therefore T_n = ax^{\frac{n}{2}}$$

$$= 4000 \times 2^{\frac{5}{2}}$$

## Processor Terminology (એમ વિદેશ પરિવ.)

### Cache

Level 1 (L1)

Level 2 (L2)

Level 3 (L3)

\* Q. Cache use કરીને એવી પ્રોફેર્માન બેઠા? (Q. Why performance better with cache?)

→ Because, it keeps in hand the next set of instructions and the data that is currently needed.

### Clock Speed

### Instruction Set

" Instruction Set એવી એવી Processor અનુકૂળ માનતું જો એવી "

## ■ Bus Speed

## ■ Timeline of Microprocessor

## ■ The Core Series (Cont.)

Die  $\Leftrightarrow$  chip

## ■ Microarchitecture

"Architecture" change ৰাখিবলৈ কোন "Generation" change  
কি? - Processor কি?

## ■ Multithreading

Casual ক্ষেত্র  $\Rightarrow$  Resource sharing

"Thread" কৈভীভুল program লোড কৰিব আবশ্য, এই ক্ষেত্রে  
light-weight ক্ষেত্রে parallelly কৰিব কথাটো সম্ভব।  
বিলুপ্তি, মূলধৰণ গুরুত্ব কৰা নাইপুঁ।"

## ■ Multicore

Logical Core means "thread"

Physical Core means "Physically present cores"

## ■ Hyper-Threading

one core handles two threads at once. As a result,  
throughput increases.

Throughput → Maximum rate at which something can be processed.

### ■ Turbo-Boost

Dynamically increases the performance of the processor

03 May 2017

### ■ 8085 Microprocessor Architecture

#### ■ Functional blocks of 8085 Architecture

■ Memory point  $\rightarrow$  H, L, SP (stack pointer)  $\rightarrow$  PC (Program Counter)

■ Stack is a data structure which is in RAM.

■ New address  $\rightarrow$  old Address  $\rightarrow$  Jump  $\rightarrow$  Program Counter 'stack' use

\* SID  $\rightarrow$  Serial Input Data

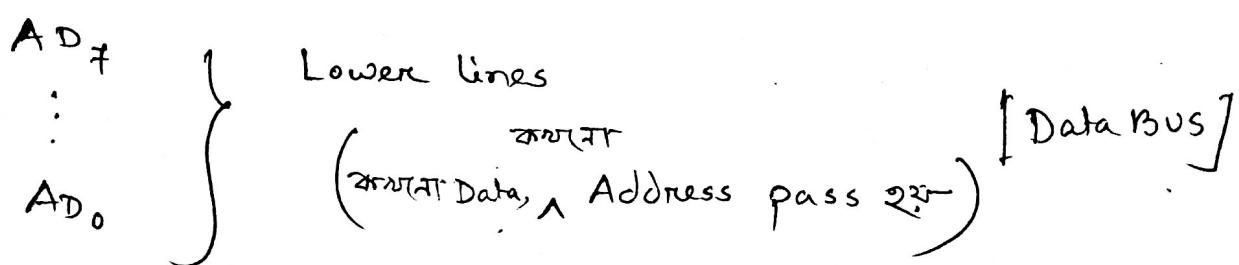
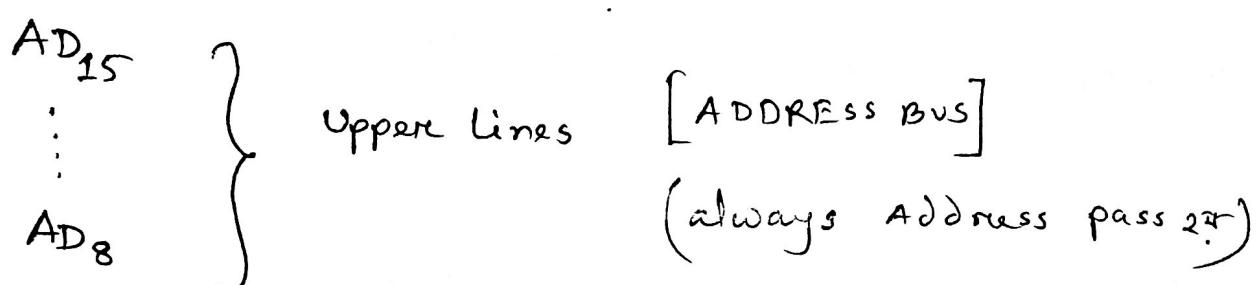
SOD  $\rightarrow$  Serial Output Data

SIM used 2<sup>8</sup>- Data  
 RIM used 2<sup>8</sup>- Data      output হয় - একটা,  
                                   input হয় - দুটা।

SIM  $\Leftrightarrow$  SOD

RIM  $\Leftrightarrow$  SID

\* মাইক্রো (মাইক্রো priority  $\Rightarrow$  INT 7.5



Bus  $\rightarrow$  4 অক্ষরের operation করে পারে।

0000 - FFFF সম্পূর্ণ মেমোরি Address Bus  $\rightarrow$  64KB হাতে।

16 pin ;  $2^{16} = 64\text{ KB}$

Address Bus  $\rightarrow$  ফলে তেজ লিনেসে address input হাতে।

Suppose, '2' হয় - ১০ - 10 (binary of 2). first Address line  $\rightarrow$  1, second line  $\rightarrow$  0 হাতে।

## Pin Diagram of 8085

- \* 10 ♂ Memory 'Read' ↗
- 01 ♂ Memory 'Write' ↗

## Logic Pinout of 8085

\*  $x_1, x_2$  ♂- clockpulse generate ↗ 1

\* 6 logical groups.

\* ALE  $\Rightarrow$  Address Latch Enable

ALE = 1 ♂ lower line  $\hookrightarrow (A_{D_0} \dots A_{D_7})$  address नम्बर 1

ALE = 0 ♂ lower line  $\hookrightarrow (A_{D_0} \dots A_{D_7})$   $\hookrightarrow$  Data नम्बर 1

\* Processor "RESET" ♂ प्रोसेसर value "0000H" रहा। इसके साथ मल्टीप्लिकेशन Register "CLEAR" भी।

20 May 2017

## 8085 Pin Diagram Description (3/7)

- \* TRI-STATED  $\Rightarrow$  Isolated
- \* RESET-IN  $\Rightarrow$  Input Pin
- \* 1-bit  $\leftrightarrow$  transfer  $\Rightarrow$  one SOD 3 SOD used  
মধ্যে।
- \* slide (5/7) Important!!
  - $\hookrightarrow$  READY & HOLD SIGNALS
- \* Processor এবং পরিবেশ অন্তর্ভুক্ত Peripheral Device এবং  
Speed এবং কার্যক্রম processor ফর কিছুটা অণুভা করতে হয়।  
 $\overline{RD}$ ,  $\overline{WR}$   $\curvearrowright$  Bar (Bar) means Active [ 0 একান্তে Read করা ]  
Low [ 1 একান্তে Read করা ]
- \* HOLD & HOLD-A একান্তে used মধ্যে।
- \* 8085 Pin Diagram Description (6/7) উল্লেখ করতে

মধ্যে।

## MACHINE CYCLE

I/O/M (output) memory এবং I/O operation ফর পূর্ণ

କେବେ ?

→ ସୁମଧୁର ଅନ୍ତର୍ଗତ ଲିପି (I/O ପ୍ରାଙ୍ଗଣ) ହେଉଥିବା ଚାଲାଏ ।

By Timing Diagram (Cont.) [1B-Question ପରିମାଣ] [7/8 Marks]

\* OP CODE Fetch ହେଉଥିବା 4th clock-cycle ମାଟରେ ।

[ $T_1, T_2, T_3, T_4$ ]

\* 8085 ଲାଗେ SEGMENT section (ତର୍ଫେ । ଲୋକେ Address

Bus 16-bit ଲୋକେ ।

\* 8085 ଲାଗେ RAM ଲୋକେ size =  $2^{16}$  = 64 KB

\* 8086 ଲାଗେ RAM ଲୋକେ size = 1 MB

\* MULTIPLEX  $\Rightarrow$  ଯେତେବେଳେ Address, ଯେତେବେଳେ Data

\* ALE = 1  $\Rightarrow$  Address ମାଟର

ALE = 0  $\Rightarrow$  Data ମାଟର

[ALE  $\Rightarrow$  Address Latch Enable]

\* ଅନ୍ତରକାଳୀନ ସିଗ୍ନାଲ ହେଉଥିବା (ପ୍ରାଙ୍ଗଣ କିମ୍ବା Thickene Band)

use କାହିଁ 2ଟି ।

\* 2<sup>nd</sup>, 3<sup>rd</sup> & 4<sup>th</sup> clock cycle use କାହିଁ OP CODE ଲାଗେ Operation

ଲୋକେ ।

\*  $T_1$  (1<sup>st</sup>) cycle  $\Rightarrow$  Address fetch କାହିଁ 2ଟି ।

\* Memory (କାହିଁ Data Read (ଅନ୍ତରକାଳୀନ) କାହିଁ ପାଇଁ ISOLATED

১০৮৮ দেশব্রহ্ম হাস্ত, খণ্ড-৩  
২৪০৮০ Processor কেন্দ্র প্রক্রিয়া-গুণ-পরীক্ষা  
এখন অস্ট্ৰীয় Address ও Data Bus use কোৱ গোৱা।

Quiz-01 [ আগামী-৪৫৩৩ ] (২৪.০৫.১৭)

24 May 2017

Lecture = 5

## Instruction Set of 8085

→ 8085 is an 8-bit device. It can have up to ( $2^8 = 256$ ) bit instructions.

### Classification of Instruction Set

There are 5 types

### Instruction and Data Format

Each instruction has 3 parts.

### Data Transfer Operations

Mov, Mvi, Lda and Sta ⇒ copy operations of the data from the source to the destination.

- \* I/O via AX - Accumulator Register (AX) used for I/O
- \* AUXILIARY CARRY bit (AC) 3rd bit - check after I/O
- \* "H-L" register pair value (HL) memory address register

\* 8085 मध्ये memory Segmented नाही

\* MOV A, B

MOV A, M

(H-L)

अंदरूनीचे address define करा।

OA OF

\* H-L दोने घटक Register, ज्ञात करताना 16-bit हिस्ते  
used होते आहेत।

\* MVI B, 60H

Immediate

(Direct (दोनों ओऱ्ह) Instruction  
वा संकेत Data)

31 May 2017

## Data Transfer Operations

LDAX D

Accumulator දැඩ්පාර් යටුත් වෙත X තොමිල මක්සු - අංක

Register

6<sup>th</sup> "pair" use කිරීම | D වෙත pair "D-E". ගෙවී "D" වෙත  
value පෙන්වනු ලබයි "E" වෙත value ගිහෙවයුරුකා final result  
පාඨම් නැත් |

\* LXI (Load extended Immediate) → "x" යාක්ෂින් "pair" use කිරීම  
\* "M" මක්සු "Memory" දැක්වයා "H-L" (location of memory)

check කිරීම |

H → මුදල 16

L → මුදල 00

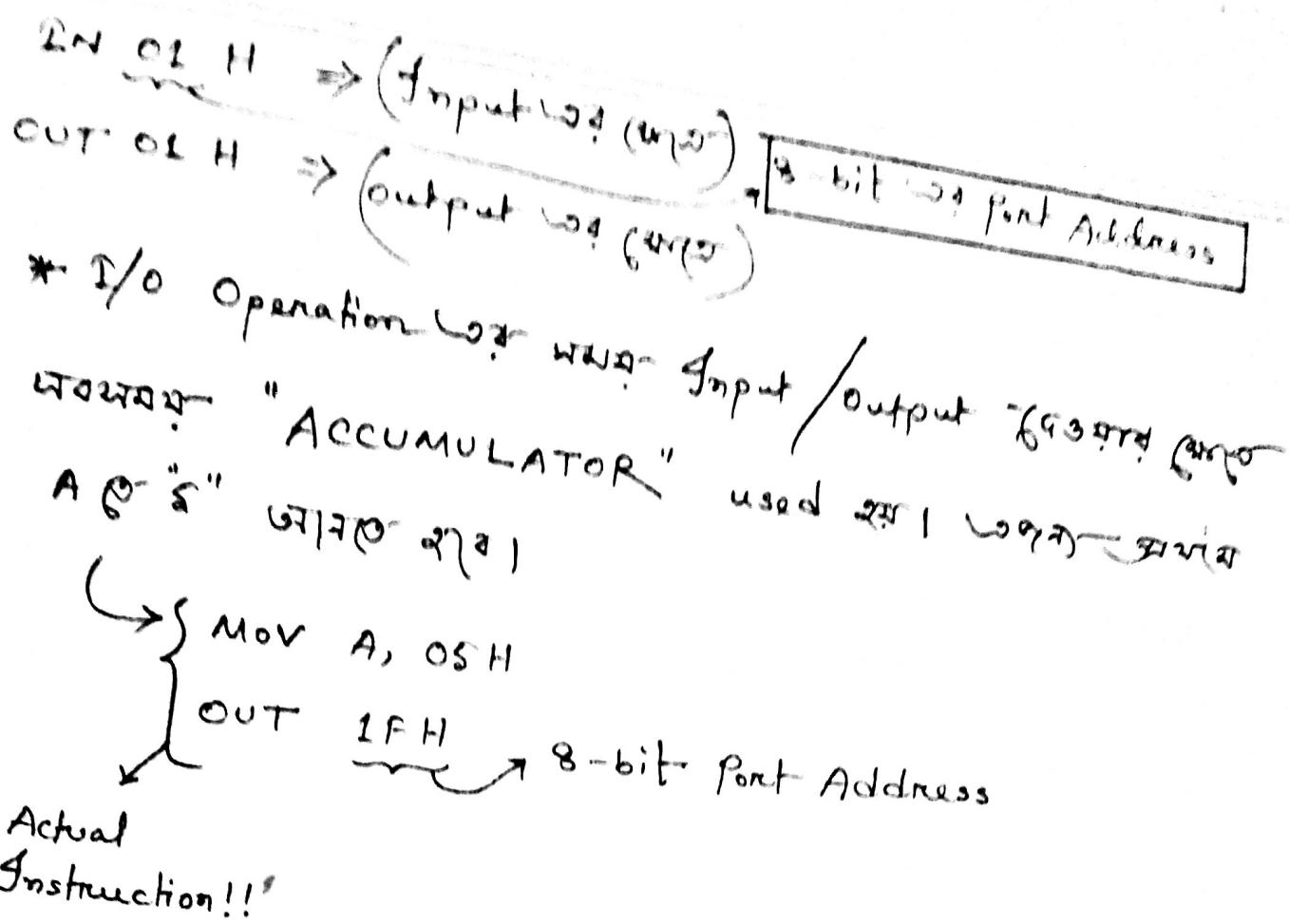
\* LHLD ⇒ Load H-L registers direct

\* 1st Address 1 byte Data ගෝන් කිරීම |

\* XCHG ⇒ "H-L" & "D-E" වෙත value exchange කිරීම |

\* 8085 → ADD මෘදුමයි A වෙත මුදල 2<sup>nd</sup> |

\* slide (Lec-5) වෙත (28 - 30) page අනු 1  
"Compare" 3 එකු (54 - 56 page)  
(79 - 82), 85, 86



\* ADD  $\Rightarrow$  Add Immediate

\* Q. "JUMP" & "CALL" का मतलब क्या?  
 (Jump करके Return)  
 (Jump करके Return करके)

\* Program का "Delay" कैसे करें? - "Nop" use करें।

\* "8085" का Address 16-bit है।

\* I/O 8-bit addressing है।

\* LHLD

(2050)

→ 2-byte addressing

\* "Lec-5" slide (2050) - highest "5/10" Marks (2050)  
smallest xm → 1

## Addressing Modes

MOV A,M      } ⇒ Register Indirect Addressing

ADD A,00      } ⇒ Immediate Addressing

JMP 1600      } ⇒ Direct Addressing

CMA  
RAL      } ⇒

07 Jun 2017

## Lec # 6

### The Instruction Execution

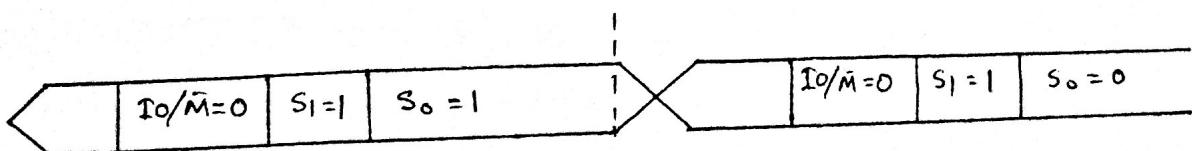
T-state varies from instruction to instruction.

Q. Given instruction  $\text{LDR R1, [R2]}$  — machine cycle  
or Instruction cycle কিরণ কৰ।

- \*  $\rightarrow$  Timing Diagram আকার এখ—  
ক্ষয় কোর operation হ'ল, তে Label করত হবে।
- \* প্রযোগ অনেকগুলো— Signal মানে Band  
ওমায়ের ফুলাম হ'ল।
- \* 'X' signal মানে বিভা' শব্দ হ'ল, ওয়ে প্র' থেক' signal  
Activate হ'ল।
- \* .... (ত) মানে স্বতন্ত্র  $\Rightarrow$  "isolated"
- \* READ করা' এন্ট' Processor হ'ল T2 ও T3 mainly  
used হ'ল।

- \* T4 cycle mainly DECODING এবং কোর্স ব্যবহার করে।
  - \* "Memory Read machine" cycle এ T4 state এর মতো না, because কোর্স "DECODING" এবং অন্যান্য পরিপন্থ না।
  - \* "Memory Write Machine Cycle" ও same.
  - \* Machine cycle (1-6) একটি হতে পারে।
  - \* Hex code এবং byte মধ্যে Normally কোর্স এবং পরিপন্থ Operation এর machine cycle আলাদা।
- Ex. A000ch  $\xrightarrow{78}$  1 byte = 1st operation আলাদা  
(Instruction Fetch)

- \* Example 1  $\rightarrow$   $I_0/\bar{M}=0$  এবং  $S_1=1$  - Band অবস্থা signal - দেখানো।
- \*  $\overline{RD}$  এবং ( $\overline{RD} = 0$ ) - এর মানে কি? (for Read Operation)
- \* Example-2  $\rightarrow$  Instruction Fetch & Read ইত্য৷  
Operation-2 - কি?



#### \* Example-6

STA 526A H  $\rightarrow$  memory এ S26A location Data  
A  $\leftarrow$  store করা।

## Lec - 7

### ■ Counters

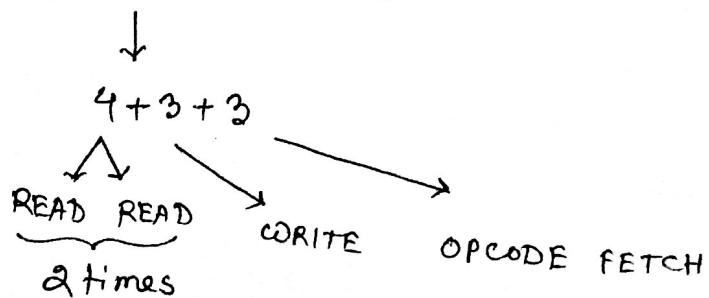
- \* 60400 1F instruction ने 0 का value for '0' का लूप किया, तो तरीका zero flag = 1 का होगा।
- \* 41H Loop का value 'FF' set करने के लिए हाथ, गहरा, सर्वांगी संचयन करने वाले loop होते हैं for cx register.

### ■ Using a Register pair as a Loop Counter

- \* 'OR' operation Accumulator पर करते हैं।

### ■ Delay Loop :

JNZ Loop  $\Rightarrow$  10 T-states



$$T_{\text{delay}} = 7 + (255 \times 14 - 3)$$

$$T_{\text{delay}} = T_0 + T_L$$

↓                    ↓  
outside loop      Inside loop

$$T_0 = 7$$

$$T_L = (255 \times 14 - 3)$$

4

Nested Loops for Delay:

1st inner loop  $\rightarrow$  Delay calculate  $\Rightarrow 1$

$$T_{\text{Loop}_1} = \overbrace{255 \times 14 - 3}^{T_{L_{\text{Loop}_1}}} + 7 \quad T\text{-states}$$
$$T_{\text{Loop}_2} = \{16(14+x) - 3\} + 7 \quad T\text{-states}$$

\* '0', '1' वाले सभी फॉर्म एंड कम लास्ट

bit extract 2<sup>0</sup> 1

\* "ANI"  $\Rightarrow$  AND Immediate

05 July 2017

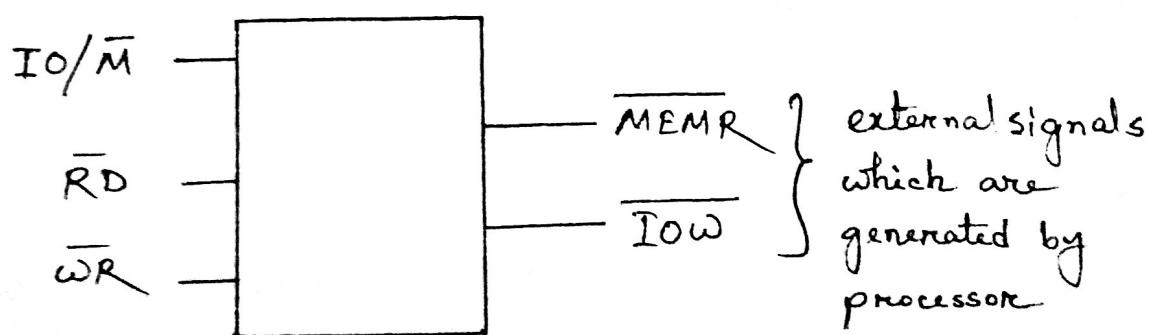
Lec - 9

## Interfacing I/O Device

\* Difference between Memory mapped I/O and Peripheral Mapped I/O . } exam ও অন্তরে!

\*  $\overline{\text{MEMR}}^A \Leftrightarrow \overline{\text{MEMR}}$

\* মেমোরি value সংগৃহ করে এবং অন্তরে Accumulator  
ৰে Load করতে হবে।



\* IN/OUT signal রেখা timing diagram with short description (যেমন কার্য)

## Input Interfacing Circuit

Address Decoders  $\Rightarrow$  যাত্র address হিসেবে, প্রেরণ Activate কৰে।

chip select "low" -কৰে Buffer IC "active" হবে।

\* EXAMPLE এইখন আমি কোন নথি লেখা নামিব।

\* EXAMPLE 1 :

IO Device  $\rightarrow$   $\boxed{IOR} = 0$  হবে always.

\* আমি fig দিব ক্ষমতি এবং।

\* IN দিলে IOR active হবে।

\* OUT দিলে IOW active হবে।

\* EXAMPLE 2 :

IOR, IWR থেকে ক্ষমতি হবে তার signal থেকে Address

ধৰা গৰা।

\* EXAMPLE 3 :

আমি অন্ধে না!!

## Stack & Subroutine

### The Stack

0000

:

FFFFD ②

FFFE ③

FFFF → Stack Pointer (SP) '\$' sign ହାତୀ  
(ଶକ୍ତି ହାତୀ)  
→ Stack initialize ହାତୀ

LXI SP, FFFFH

PUSH Rp → Register Pair

\* Lower Byte / Address ହାତୀ ଆମେ ହାତୀ

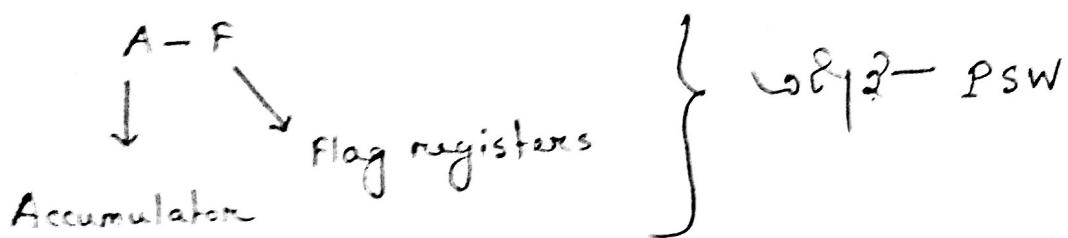
\* word Register Push ହାତୀ ହାତୀ, Pair use ହାତୀ ହାତୀ

\* Counter Decrement, then use! ⇒ Stack (PUSH)

\* PSW ⇒ Program Status Word.

PUSH B  $\Rightarrow$  B will be stored at address 07  
Push A[7:1]

\* after use, then increment  $\Rightarrow$  Stack (Pop)



### The POP instruction

PUSH B

B - C

02

B - C  
0A 02

PUSH D

02 03

0A

D - E

...

D - E

02

02 03

POP D

0A 02

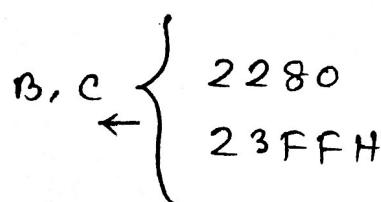
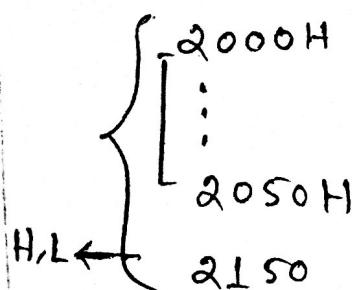
POP B

\* for order  $\Rightarrow$  PUSH args, order - Opposite order  $\Rightarrow$  pop

args 2131

08 July 2017

Example - 9.1, 9.2



SP ← 2400H

### Subroutines :

Q. Why we write subroutines?

CALL ⇒ Subroutine call  $\text{47A1}$

RET ⇒ Return  $\text{47A1}$

\* "CALL" instruction  $\text{47A1}$  value stack  $\rightarrow$  store  $\text{27A1}$   
 $\text{27B1}$ "

\* Upper  $(\text{byte})$  value  $\rightarrow$  first  $\rightarrow$  store  $\text{27A1}$  "stack"  $\rightarrow$  1

\* "CALL" instruction execute  $\text{27A1}$   $\rightarrow$  next instruction  
 $\rightarrow \text{27B1}$

POP  $\Rightarrow$  increment (READ)

PUSH  $\Rightarrow$  decrement (WRITE)

12 July 2017

### Problem Statement

\* Stack use করে কোথা (light related problems)

\* Subroutine প্রক্রিয়া কিম্বা প্রয়োগ করা হবে।

Delay produce 2<sup>56</sup> |

\* xm is light-related problem নির্দেশ করে।

\* 1st Register হিসেবে Delay করারা উচিত নহ'ল because

FF একটি (not more than that) Delay করার খালি।

\* 2nd register হিসেবে FF ওয়ে চেছি। কিন্তু Delay করার খালি।

\* Delay 1 sec করার পাই কিনা গ- count নথি

value দিয়ে পুরো হাল।

Non-Maskable Interrupt : Mask করা শুরু না

\* Processor রেখা না, but for interrupt ক্ষেত্রে  
-রেখা  $\Rightarrow$  Non-vector

\* x-m-l-w Diagram এর Interrupt process করা  
ক্ষেত্রে ফিল্টার মাইল সহজ হব।

RST  $\Rightarrow$  RESTART

\* 8 RSTs

flash  $\Rightarrow$  whether all inputs are 1 or 0.

\* "DISABLE" Processor নিয়ে নির্ভুল ক্ষেত্র, code ও ক্ষমতা  
হবে না।

15 July 2017

## ■ 8085 Interrupts:

\* xm → soft interrupt -  $\text{INT}^{\text{A}}$  (soft address ask for)  
(Service Routine)

sm<sup>3</sup>

## ■ Manipulating the Masks

## ■ How SIM interprets the Accumulator

\* Page-27 sm

\* RIM  $\Rightarrow$  Read Interrupt Mask

\* enable  $\Rightarrow$  0 कर्तुम् अन्तर्भूत 1 कर्तुम् ।  
(Interrupt<sup>↑</sup>)

\* ANI 20H = 0 कर्तुम् Enable कर्तुम्, otherwise Next code will  
be executed.

\* 1 कर्तुम् Pending Masked.

\* RST 6.5 0 कर्तुम् ENABLE कर्तुम् ।

8085

WAP (M) 3<sup>rd</sup> Question

Advanced Processor  $\Rightarrow$  1<sup>st</sup> Question  
8086  $\Rightarrow$  2<sup>nd</sup> Question

Quiz - 3 [Q&A]

Stack subroutine & Interrupt  
changed!

1. Stack and Subroutine
2. Lec - 11
3. Addressing Mode X
4. Interrupt ✓

19 July 2017

## Lecture-11

### Q) Features of 8086

- \* ODD Location (মুক্তি Long read এবং স্মার্ট EVEN Location মুক্তি)
- 2075 → 2 byte data
- 00520 → FF
- 00521 → 20
- \* Microprocessor মনে কর এবং EVEN location থেকে Data read করা। (মুক্তি, লজিক কস্ট এবং প্রতি)
- \* Garbage মনে কর - value ফিল - Lower byte → শাখা।
- \* EVEN location (মুক্তি 1st operation মুক্তি)

### Q) Architecture of 8086

- \* Z80 structure এবং একটি নির্দেশ রেজিস্টার।

- \* General Purpose Registers mainly → 4 R

Segment Register	→ 4 R
Pointer Register	→ 5 R

- \* Internal bus → 16 bit (As Databus)

External bus → 20 bit

- \* 1st Instruction execute করা যাব - পদক্ষেপ করা ক্ষমতা করা।

- \* Q. CPU Unit ലോ ഏറ്റവും മുൻ്നെത്ത് ?
- \* Q. CPU Segment ലോ എന്ത് പ്രാണ OFFSET?
- \* 1st segment highest 64 KB എന്ത് അർഹം?
- \* Code Segment ലോ എന്ന് "IP" used 20-1
- \* DS: SI / DI
- \* SS → SP (offset ഫോർമാറ്റ് used 20- only during PUSH/POP)
  - BP (stack ലോ value കാര്യാല്പാദിഷ്ട്)
  - [Based Addressing Mode ഫോർമാറ്റ് used 20-]
- \* ES: SI / DI (ഡാജിനൽ ഡി ലോ എന്ന് used 20-)
  - [ES ലോ എന്ന് കാർഗ്ഗരാഡ് ദിസ്ട്രിബ്യൂട്ടേം സ്യെസ്റ്റം എന്ന്]
- \* AX → MUL / DIV ലോ എന്ന് - Mainly used 20-1
- BX → ഫോറ്മാർ ലോ Base location Point എന്ന്,
  - (കേൾ BX ലോ memory for Refer എന്ത് അർഹം)
  - [ഒരു പു ഡിX ലോ എന്ന് കാർഗ്ഗരാഡ് എന്ന്]
- CX → Counter, Loop, Shift, Rotate
- DX → Data hold area (Mainly Division ലോ
  - (അർഹം used 20-)

\* 8085 → FLAG → 51F  
 \* 8086 → FLAG → 11F [Control Flag → 31F  
 Status Flag → 81F]

Q. 8086 ലോ instruction-based ques. must answer in  
 ↳

■ Nested Task Flag  $\rightarrow$  am (far, am)

GOPL  $\rightarrow$  STF

IF  $\rightarrow$  Interrupt Enable flag

DF  $\rightarrow$  string word direction flag set 1

TF  $\rightarrow$  Debug word word set 2

## Memory Address Calculation

Logical Address  $\rightarrow$  Segment - OFFSET pair

\* 10H  $\rightarrow$  32 bit offset AX  $\rightarrow$  1 bit shift of 1

\* Example BT  $\rightarrow$  100000 practise add 1

\* STACK word size  $\rightarrow$  64 KB

SS :  $\rightarrow$  0000 (END)  
· FFFE (Bottom)

\* (SS : SP) word combination 'present value' mean

offset 1

decrement by 2  $\rightarrow$  2 byte data string or 1

\* AX = 1234

SS = 0105

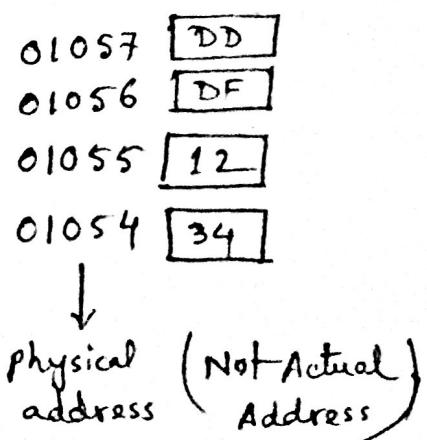
SP = 0006

PUSH AX

POP BX

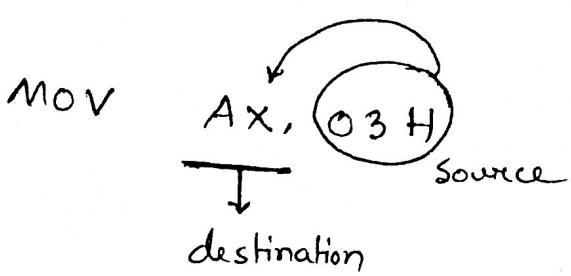
POP AX

SP [0006]  $\leftarrow$   
SS [0105] \* 10<sup>1</sup>



- \* SS तरी value मध्ये same वर्गात |
- Q. PUSH & POP instruction ला Math xm ला must असत्र!
- \* मानवीक program असता, अंगठीचे नवीन - असता
- अंगठी stack असत्र |
- \* In program ला नवीन segment Register change करा -  
तर, OFFSET change करा -

### Addressing Mode



\* Addressing mode generally source ला addressing mode करा करा |

\* Register Addressing mode ला 90° करा तर memory access करा तर, तरी physical Address calculate करा करा |

02 August 2017

## Microprocessor 8086 ADDRESSING MODES

### Immediate Addressing Mode

Memory Access अस्ति लागता (N/A)

(प्र इन्स्ट्रुक्शन अस्ति ऑपरेन्डर - Operand के. Memory Access  
कर्त्तव्य अस्ति गैरके Memory Addressing Mode एली।

$$PA = \text{Seg} * 10H + \text{offset}$$

↑

EA (Effective Address)  
(16 bit)

(physical Address)  
(20 bit)

\* Effective Address & Physical Address mainly memory

Accessing अस्ति उपयोग कर्त्तव्य अस्ति।

[ SI ] → offset अस्ति उपयोग कर्त्तव्य।

\* Problem segment अस्ति mention नर अस्ति खाली  $\Rightarrow DS$

↓  
(Question)  
Value (दिया गया)  
मान (Ans)

\* ADD AX, [SI]  $\Rightarrow$  Register Indirect Addressing Mode

$$EA = SI$$

$$PA = DS * 10H + EA$$

\* Based Addressing Mode  
Indexed Addressing Mode  
 $Mov DX, [BX+04]$   
 $EA = BX + 04$   
 $PA = DS * 10H + EA$

### Based-Indexed Addressing Mode

\* Based-Indexed with Displacement

\* BX for use of indexing w/o reg!

\* 2 reg increment op's

\*  $Mov CX, 04H \quad BX + 300$

$Mov BX, 00H$

Loop<sub>1</sub>:  $ADD AX, [BX + 0300]$

$INC BX, 2$

Loop Loop<sub>1</sub>

\* AX (8086 Microprocessor) দ্বারা নিয়ে Word operation.

গুরুত্ব 34 পর্যন্ত Data এলেমেন্ট 34 → AL ও 32 → AH  
12

finally, 12 34 হবে।

কিন্তু, যদি শুধুমাত্র AL/AH হ্যান্ডেল গুরুত্ব MP প্রক্রিয়া ফ্রি-

Byte operation. গুরুত্ব 34 হ্যান্ডেল Data এলেমেন্ট 34 → AL/AH ও -  
12 → mov হ্যান্ডেল 12

হবে।

\* 4 [BX] → valid!

[BX] 4 → Invalid!

$$EA = \text{reg} + \text{Displacement}$$

\* Displacement হ্যান্ডেল নথিজ - Constant খেল অপেক্ষাকৃত আকার

হবে।

## Flag Registers

\* Overflow = 1 表示 sign overflow 2進位 1

\* unsigned overflow 2進位 carry flag = 1 表示

\* Sign <sup>overflow</sup> <sub>number</sub> unsigned 2進位 表示 進位 和 等於 0 [Independent]

16 bit

$$2^{16}$$
$$0 - (2^{16} - 1)$$

$$0 - 65535$$

\* Types of overflow

\* carry flag = 1 表示 unsigned overflow

\* 2進位 sign bit different 2進位 sign overflow 2進位

\* Trap flag = 1 表示  $\Rightarrow$  Processor single execute mode  
ए क्ल थाय

\* Assume  $A_x$  &  $B_x$  both contains positive numbers.  
 Show that, there is a carry into the MSB but no carry out from MSB if and only if sign overflow occurs.

05 Aug 2017

- \* 8086 Block Diagram
  - \* Code Segment Register
  - \* Minimum Mode Configuration }
  - \* Maximum " "

সে কোন একটি must আসবে,

↳ Diagram ~ বর্তনি মিষ্টি, [৬ মেমোরি আসবে]

{ min = 1 Processor

Q. Pin (ਕੁਸ਼ਟ ਵਰਗ), ਕਿਨ੍ਹੇ ਲਿਖੋ 2/2 : { min = 1 processor  
 max = multi-Processor

\* Data Bus = 16-bit → Demultiplex 2<sup>4</sup>  
 Address Bus = 20-bit ਮਾਤਰਾ Data, ਕਿਸੇ address ਨਹੀਂ।

A<sub>19</sub> | S<sub>6</sub>  
A<sub>18</sub> | S<sub>5</sub>  
A<sub>17</sub> | S<sub>4</sub>  
A<sub>16</sub> | S<sub>3</sub>

} 282273 Address, 282273 status 27721

Bus high enable = high bit କେବଳ enable ହୁଏ ।

- NMI  $\Rightarrow$  Non Maskable Interrupt

\* READY pin / RESET

TEST

INTR

NMI

MN /  $\overline{MX}$

\* Left ଲୋଡ୍ ଅତିକ୍ରମ MAX

Right ଲୋଡ୍ ଅତିକ୍ରମ Min

\* Max / Min mode କେବଳ Pin description ଆବଶ୍ୟକ ନା !

\* କେବଳ min / max .

\*\* Max ଲୋଡ୍ Min mode କେବଳ Configuration  $\Rightarrow$

must କରିବ !!

\* Transceivers  $\Rightarrow$  data କେବଳ ଆଜାନୀ ହେବାକୁ !

Max / Min mode configuration  $\Rightarrow$  4-5 line description

\* 4-bit Timing Diagram ( ସବୁ must ଆବଶ୍ୟକ )

( Description ଲାଗିବା ପାଇଁ ) !

09 August 2017

Advanced Processors [ 1 set notes ]

8086

286

386

486

Pentium



Only Features (2/3 of 8086)

Diagram in

Pentium Registers : 16-bit [ Pin Diagram given ]  
32-bit

Flag Registers : 8-bit

Pentium (2 mode)

→ Real Mode

→ Protected Mode

\* 16 bit ലഭ്യമായ 1 MB മെംറ്റീസ് Memory Access ദിവസം നിലച്ചു.

32 bit ലഭ്യമായ 4 GB മെംറ്റീസ് Memory Access ദിവസം നിലച്ചു.

\* Descriptors for point or selector.

\* Segment mainly selector or hold ആണ്.

\* 16 Descriptors memory or 8 byte space hold ആണ്.

## Descriptors:

Base : 7, 4, 3, 2

Limit : (LH) 6, L, 0

$G=0 \Rightarrow 1 MB$

$G=1 \Rightarrow 4 GB$

End = Base + Limit if  $G=0$

End = Base + Limit  $\times 4 KB$  if  $G=1$

Decimal + 1  
segment size

decimal + 1

(End - Base) + 1

$10FA \times 4 KB = 10FAFFF$

Q. Excess byte का value क्या है ?

→ AV  $\Rightarrow$  Available or Not

→ D  $\Rightarrow$  Default mode

Q. Descriptor की कीमत क्या है ?

\* Maths + Explanation

\* xm  $\rightarrow$  Base Address कीमत नहीं है। List / chart

मात्र काम्पिट रखें।

\* Selector का 1st 2-bit  $\Rightarrow$  Request Privilege Level

Q. Request Privilege Level की कीमत क्या है ? किसका value क्या है ?

⇒ TI ⇒ Table Indicator

⇒ Global Descriptor Table

Steps :-

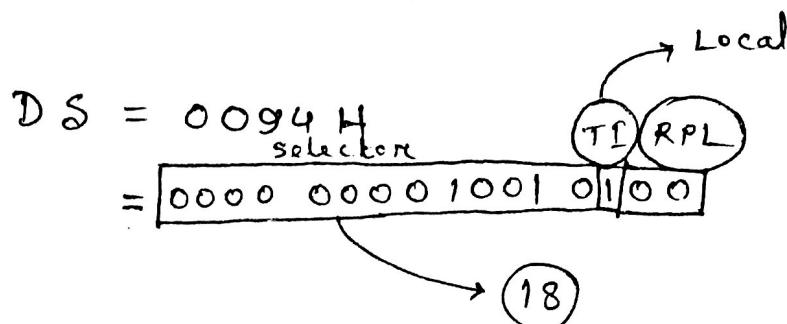
1. Table Indicator (TI)

2. Local/Global selector

3. Select 18

\* CSE 3107 Final Ques Fall-2016 .doc

→ Q. 7 (a)



8-byte descriptor selector!

\* 1st → Base calculate 18

Base = 7, 4, 3, 2

= AA100201 } 32-bit base address

Limit = 3001F ← } Lower Half Register  
= (LH) 6, 1, 0

Gr = 6 no. byte ← MSB

= 1

∴ End = AA100201h + 3001F ← 4K  
= " + 3001FFFFh

## Slide → Interrupts on 8086 Microprocessor

\* Con't interrupt list numbers (नियमीय संख्या),  
Or respective workflow.

Q. इन कोई interrupt call 20, तथा  
चर्की-की-steps show 20।