MD TOUFIQ HASAN ANIK

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Education

- **Ph.D. Candidate in Computer Engineering** **Aug.2018 - Jul.2024 (Exp.)**
  University of Maryland Baltimore County (UMBC)
  CGPA: 3.86/4.00 *[Transcript]*
- **Masters in Computer Engineering** **May 2021**
  University of Maryland Baltimore County (UMBC)
  CGPA: 3.86/4.00 *[Transcript]*
- **B.Sc. in Electrical and Electronic Engineering** **Dec. 2016**
  BRAC University, Dhaka, Bangladesh
  CGPA: 3.70/4.00 (High Distinction) *[Transcript]*

Professional Experiences

- **Research Assistant, Secure Reliable and Testing Lab, UMBC** **2018 - present**
  - *Areas*: Hardware Security & Reliability, Cryptographic Hardware, ASIC Design Flow, FPGA, VLSI Testing, On-Chip Sensors, Side-Channel Attacks, Fault Detection, Comp. Architecture, Device Aging.
  - *Advisor*: Dr. Naghmeh Karimi
- **Computer Architecture Graduate Intern, DPA, Intel Corporation** **Summer 2021 & 2022**
  - Functional Verification of x86 Xeon CPU.
  - Fault analysis on processor micro architecture and system-level.
  - Program Vulnerability Factor modeling, Silent Data Error modeling.
  - ***Impact:*** Designed reliability matrix assisting fault tolerant architecture development.
- **Hardware Security Researcher Intern, IPAS, Intel Corporation** **Summer 2020**
  - Modeling hardware attacks on processors.
  - Developed security assessment framework for vulnerability estimation.
  - ***Impact:*** Enhanced security measures of designs.
- **Mentor for K12 High School Interns, (6 Interns) SECRETS Lab, UMBC** **2019 - present**
- **Teaching Assistant, UMBC** **2018 - 2019**
  - Hardware Security
  - C Prog. & Embedded Sys.
  - VLSI Design
- **Reviewer:**
  - Journal: IEEE Access, JETTA, TCAD
  - Conference: DAC, DATE, VTS

Technical Skills

- **Programming Languages:** Python (LeetCode, Hackerrank solver), C, C++, MATLAB
- **Hardware Description Languages:** Verilog, SystemVerilog, VHDL, Spice
- **Computer Architecture:** SoC Design, CPU, x86, ARM, RISC-V, GPU
- **FPGA / ASIC Chip Development:**
  - ASIC Design Flow, RTL Design, Testing, Verification, Synthesis, Reliability, Aging, DRC, LVS, DFT
  - HW-SW Co-design, Accelerator, Computer Architecture, Pipeline, Parallel, Serial, Unrolled, UART
  - Developed ASIC with 42 Cryptographic cores: RTL-to-GDSII, IO, Memory, Controller, PnR, PPA
  - Designs: IPs, ROs, On-Chip Sensors, Crypto, PUF, DSP, Carry Chain, FIFO, FSM, PLL, PROM
- **EDA Tools:**
  - Synopsys: HSpice, VCS, Tetramax, Primetime, Design Compiler, ICV-Netrun
  - Cadence: Xcelium, Genus (Cad. Certified), Conformal, Innovus (Cad. Certified), Virtuoso, Jaspergold
  - Intel: ModelSim, Presto, Simics
- **Hardware Security**: Side-Channel, Power Analysis, Fault Injection, Threat modeling, Security Verif.
- **Machine Learning:** Pytorch, TensorFlow, ML Hardware / Accelerator Design
- **FPGA:** Xilinx Vivado, ISE, Altera Quartus, SAKURA-G
- **Instrument:** Oscilloscope, Signal Generator, EM/Power Probe
- **Framework/Tool/Software development:** Python, TCL, Perl, Shell

Key Projects

- **ASIC Chip Development:** Tape out 65nm ASIC Chip includes 42 Cryptographic Cores, Arch: Serial, Pipeline, Parallel, Unrolled, Wrapper, Memory, Verification, PPA, PnR, RTL-to-GDSII.
- **Physical Attacks in Light of Device Aging:** Power Analysis on SCA Countermeasures. PPA vs Security, Proposed Aging resilient Countm., Attacks on ASIC Sim., FPGA, SoC, Cloud FPGA.
- **On-Chip Digital Sensors:** Fault/Attack Detection, Characterized, Aging Resilient dim. for optimized HW, Calibration, Framework, Evaluated on ASIC Sim. and FPGA, HW Macro.
- **FPGA Designs:** Multi Tenant Cloud FPGA security, Crypto, AI Accelerator, ARM Processor, Time Transfer, Phase Meas., TDC sensors, UART, Macro, DSP, ASIC Emulation, Power/EM side channel.

Publications **(Google Scholar: bit.ly/gsmthanik)**

Journals:

1. **M. T. H. Anik**, H. I. Reefat, J. Danger, S. Guilley, and N. Karimi, "Multi-modal Pre-silicon Evaluation of Hardware Masking Styles", *Under Review on Journal of Electronic Testing (JETTA)*, Mar. 2024.
2. **M. T. H. Anik**, et al., "On the Resiliency of Protected Masked S-Boxes against Template Attack in the Presence of Temperature and Aging Misalignments," *IEEE Trans. on VLSI (TVLSI)*, Mar. 2024. *[Online]*
3. **M. T. H. Anik** et al., "Testing and Reliability Enhancement of Security Primitives: Methodology and Experimental Validation," *Journal of Microelectronics Reliability*, Jun. 2023. *[Online]*
4. **M. T. H. Anik**, M. Ebrahimabadi, J. Danger, S. Guilley, and N. Karimi, "Reducing Aging Impacts in Digital Sensors via Run-time Calibration", *Journal of Electronic Testing (JETTA)*, 37, Feb. 2022. *[Online]*
5. B. Fadaeinia, **M. T. H. Anik**, N. Karimi and A. Moradi, "Masked SABL: a Long Lasting Side-Channel Protected Design Methodology", *IEEE Access*, vol. 9, Jun. 2021. *[Online]*
6. **M. T. H. Anik**, J. Danger, S. Guilley and N. Karimi, "Detecting Failures and Attacks via Digital Sensors," *IEEE Trans. on Computer-Aided Design (TCAD)*, Jul. 2020. *[Online]*

Conferences:

7. **M. T. H. Anik**, H. I. Reefat, J. Danger, S. Guilley, and N. Karimi, "Spying Multi-Tenant FPGAs without Manual Placement and Routing" *submitting to IEEE Symp. on VLSI (ISVLSI)*, Jun. 2024.
8. **M. T. H. Anik**, H. I. Reefat, J. Danger, S. Guilley, and N. Karimi, "Aging-Induced Failure Prognosis via Digital Sensors" *Great Lakes Symp. on VLSI (GLSVLSI)*, Jun. 2023. *[Online]*
9. **M. T. H. Anik** et al., "Testing and Reliability Enhancement of Security Primitives," *IEEE Int. Symp. on Defect and Fault Tolerance Systems (DFTS)*, Oct. 2021. *[Online]*
10. K. Huang, **M. T. H. Anik**, and N. Karimi, "Real-Time IC Aging Prediction via On-Chip Sensors," *IEEE Symposium on VLSI (ISVLSI)*, Jul. 2021. *[Online]*
11. M. Ebrahimabadi, **M. T. H. Anik** et al., "Using Digital Sensors to Leverage Chips' Security" *Conf. on Physical Assur. and Inspection of Electronics (PAINE)*, Dec. 2020. *[Online]*
12. **M. T. H. Anik**, B. Fadaeinia, A. Moradi and N. Karimi, "On the Impact of Aging on Power Analysis Attacks Targeting Power-Equalized Cryptographic Circuits", *ASP-DAC*, Jan. 2021. *[Online]*
13. **M. T. H. Anik**, et al., "On-Chip Voltage and Temperature Digital Sensor for Security, Reliability, and Portability", *IEEE Int. Conference on Computer Design (ICCD)*, Oct. 2020. *[Online]*
14. **M. T. H. Anik**, R. Saini, J. Danger, S. Guilley, and N. Karimi, "Failure and Attack Detection by Digital Sensors", *IEEE European Test Symposium (ETS)*, May 2020. *[Online]*
15. **M. T. H. Anik**, S. Guilley, J. Danger, and N. Karimi, "On the Effect of Aging on Digital Sensors," *Int. Conference on VLSI Design (VLSID)*, Jan. 2020. *[Online]*

Hardware Demos:

1. COOL PUF: A Temperature Resilient PUF Assuring Reliability, HOST 2023, **1st Place Winner** *[Online]*
2. Implementing Digital Sensor on FPGA Detecting Faults, HOST 2022, **2nd Place Winner** *[Online]*

Honors and Awards

1. Finalist, PhD Competetion, VTS, 2024
2. Finalist, PhD Competetion, HOST, 2024
3. 1st position, Hardware Demo, HOST, 2023
4. 2nd position, Hardware Demo, HOST, 2022
5. Finalist, Emb. Security Chall., CSAW, 2021
6. 2nd position, Emb. Security Chall., CSAW, 2018
7. NSF Travel grant, HOST, 2022 & 2023
8. Travel grant, SecDev, Washington D.C, 2019
9. Travel grant, CSAW, NYU, 2018
10. Best Young Innovator Award, DIF, BD, 2017
11. Convocation Distinction, BRACU, 2017
12. Dean's list (Five Times), BRACU, 2013 - 2016
13. Vice chancellor's list, Edu. Excell., BRACU, 2014
14. BRACU Merit Scholar (Tuition Remiss.), '13-'16
15. Runner Up, ELECTROQUEST, BRACU, 2015
16. Edu. Board Scholarship (Top Result), SSC, 2010