Chittagong University of Engineering & Technology

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

NAME OF THE EXPERIMENT / REPORT

DC Analysis and Symbol Creation of Inverter and AND Gate

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COURSE TITLE	**:**	VLSI Technology Sessional
EXPERIMENT NO.	**:**	04
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R E M A R K S

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TERM	**:**	I
SECTION	**:**	
GROUP	**:**	G-2

Objectives:

- To familiarize with DC sweep and parametric simulation in ADE L.
- To familiarize with symbol creation from schematic view.

Required Software:

1. Cadence

Design:

DC Simulation:

We will simulate the inverter design using both DC and parametric methods simultaneously. By changing the width of the PMOS transistor, we can determine the transfer characteristics curve (TCC) of the inverter and watch how it affects the transferable qualities.

The Edit Object Properties box will popup when you press 'q' or right-click the body and choose 'Properties' when selecting the PMOS transistor in the schematic editing window. Put w under "Total Width" and hit the tab key on your keyboard. The 'Finger Width' field will be automatically modified. By changing this parameter 'w', we will observe how the width of the PMOS effects its characteristic.

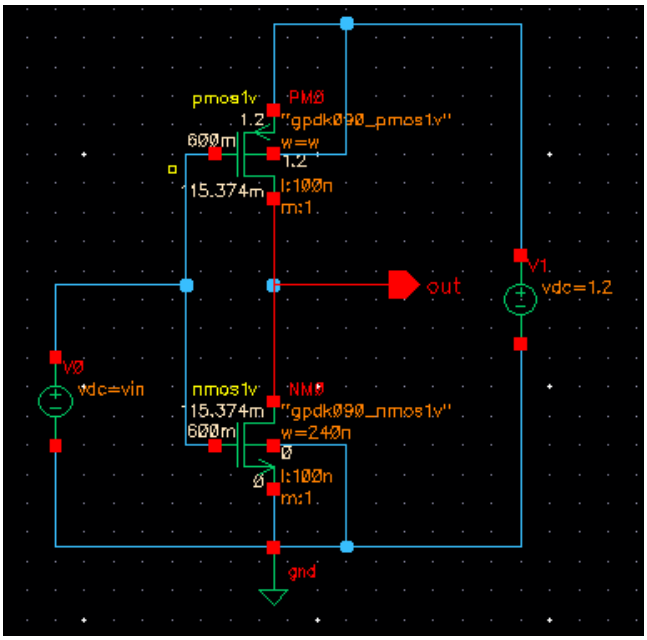

Figure No. 01: Circuit for parametric analysis.

The above Figure No.01 shows the circuit used for the parametric analysis of NMOS varying its width.

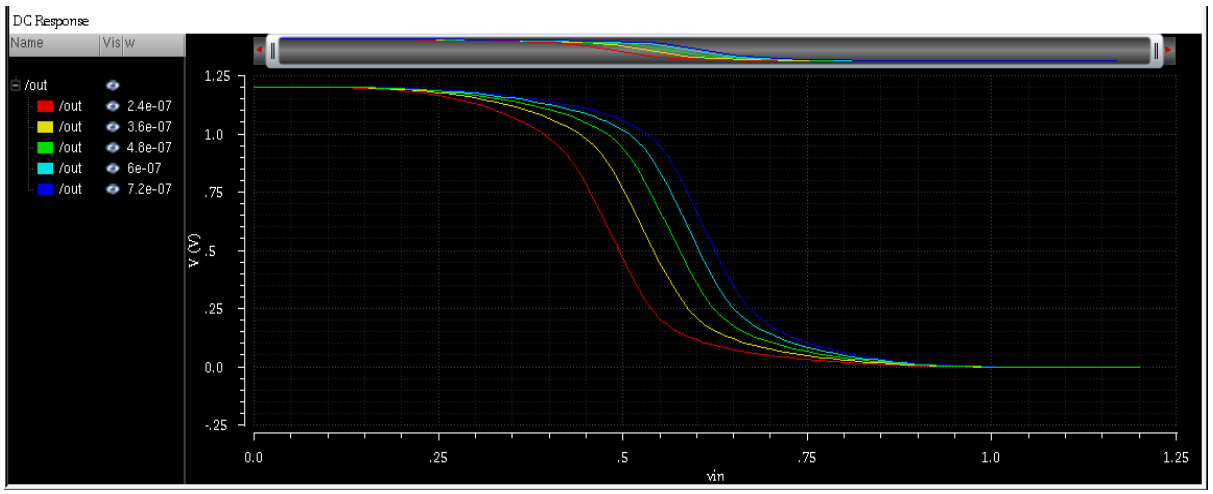

Figure No. 02: PMOS characteristics for varying width.

In Figure No.02 we can see the TCC of the PMOS. To turn off the PMOS negative voltage is required. Here we can see, when the vin is 0V the voltage across the PMOS is around 1.2V which is the supply voltage. With the increase of vin the device turns off. Important part to notice is that when the width of PMOS was small, around 0.5V was required to turn it off but as the width increased the required voltage also increase. The switching speed decreases and current carrying capability also decreases. So, we can infer that with the increase of width of PMOS the required voltage to turn it off also increase.

Symbol Creation:

To use this symbol view for the schematic in a hierarchical design, we will build a symbol for our inverter design. Additionally, the symbol includes properties (cdsParam) associated to it that make it easier to simulate and construct the circuit. To create the symbol at first the inverter schematic was opened from the library. Then to proceed further, Create > Cellview > From CellView was executed and the Cellview From Cellview window appeared. The number of input pins and output pins were then specified. Hence, the symbol was created. To make the symbol more like an inverter symbol it was designed and it finally looked as an inverter.

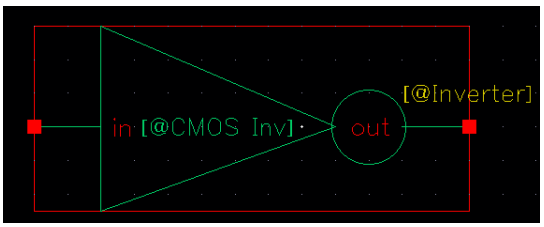

Figure No. 03: Inverter Symbol

AND Gate:

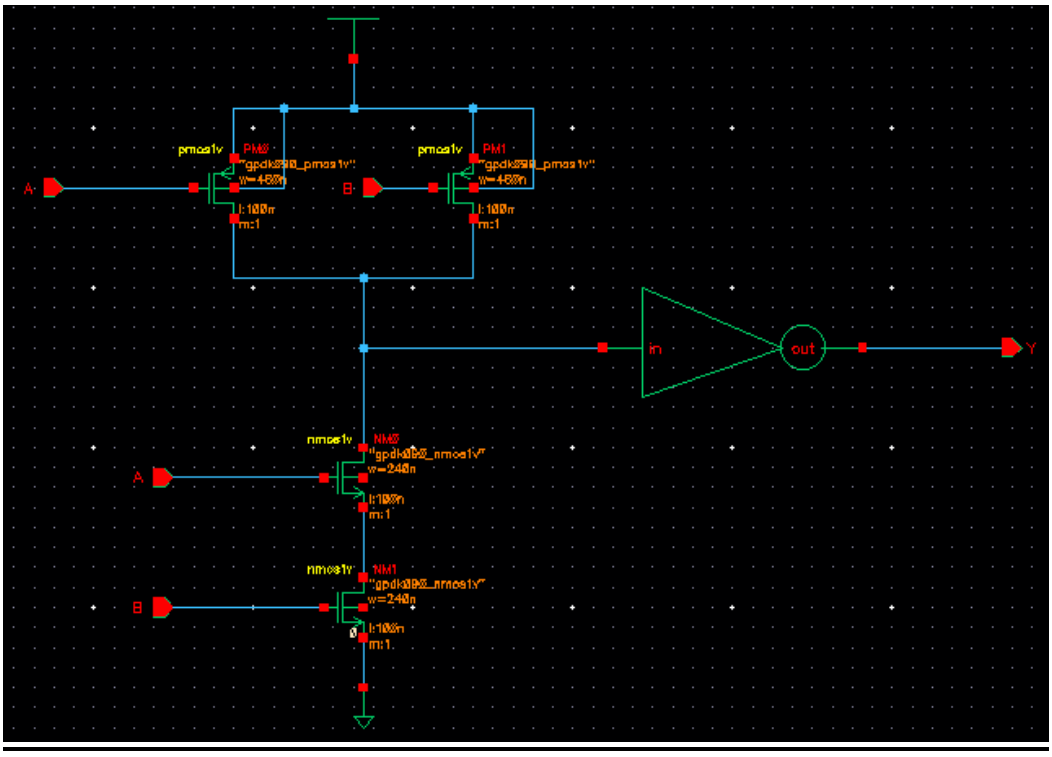

Figure No. 04: AND gate schematic

Similar to an inverter schematic design the schematic of AND gate was also done. In an AND gate, two PMOS and two NMOS was used. The width of the PMOS was taken twice than of NMOS so that their current carrying capability matches. The PMOS were connected in parallel and the NMOS were connected in series. The output was taken from the connection of the parallel PMOS structure and series NMOS structure. The output was then passed through an inverter. This inverter symbol is the one we created earlier. Figure No. 05 shows the input and output curve of the AND gate. Here we can see that it satisfies the AND gate truth table.

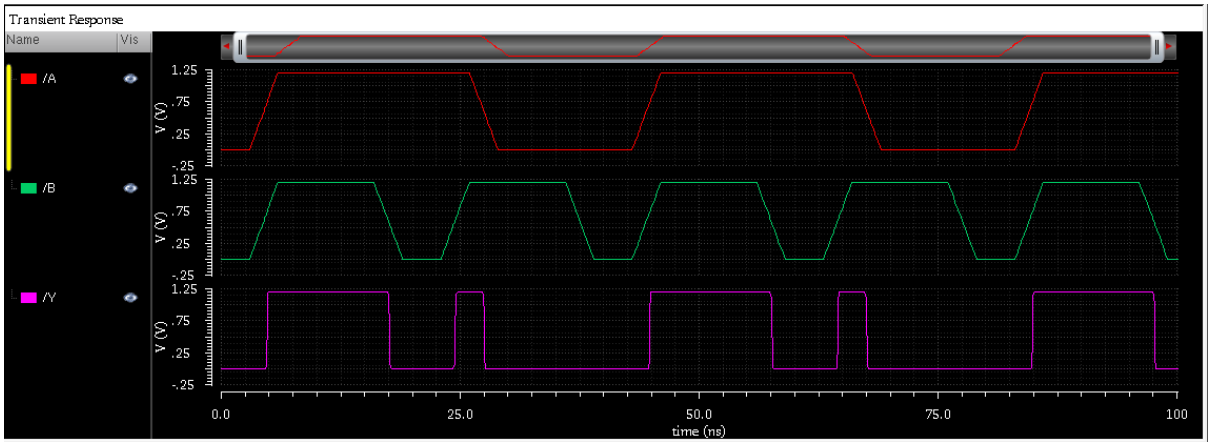

Figure No. 05: AND gate output

Similar to the inverter symbol the AND gate symbol was also created.

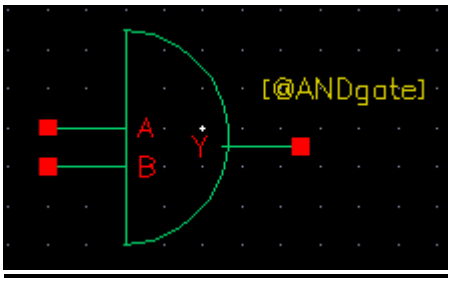

Figure No. 06: AND gate symbol

Home Task:

1. To show the effect of changing NMOS width on the TCC of an inverter:

Similar to the PMOS, the TCC curve of the NMOS can also be obtained. Here, the width of the NMOS was varied and depending on that the TCC was obtained. NMOS requires positive voltage to be turned off. In the curve we can see that when the along with the increase of the width the NMOS requires more positive voltage to be turned off. With the increase of width the current carrying capability increases and change of state is much faster. This results in faster switching speed. The wider the NMOS the less the rise and fall time, hence faster operation.

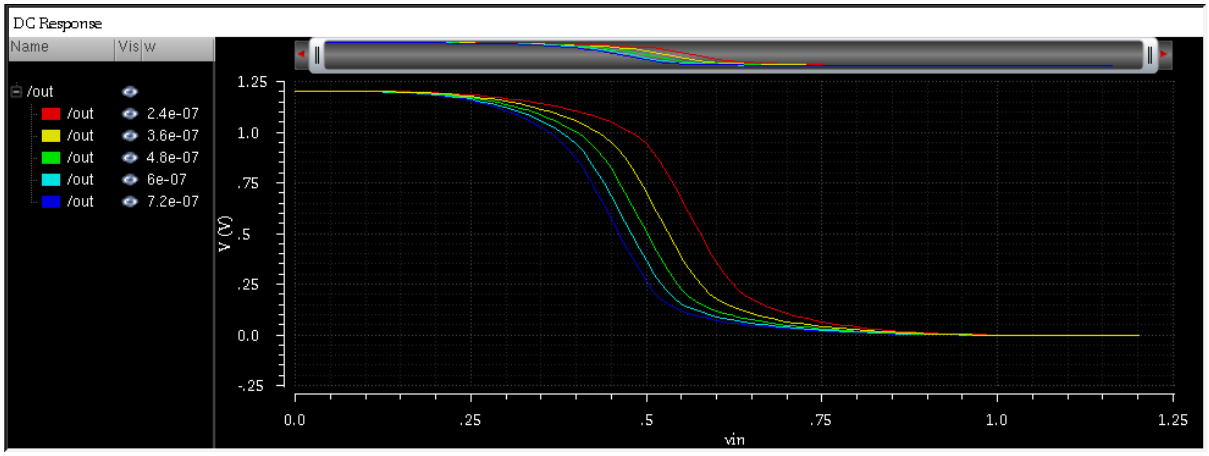

Figure No. 07: TCC of NMOS

2. Design a 2-input OR gate along with its symbol:

The OR gate was also designed similar to the AND gate but in this case the PMOS were connected in series and the NMOS were connected in parallel. The output was passed through the inverter. From the output figure we see that it satisfies the truth table of OR gate.

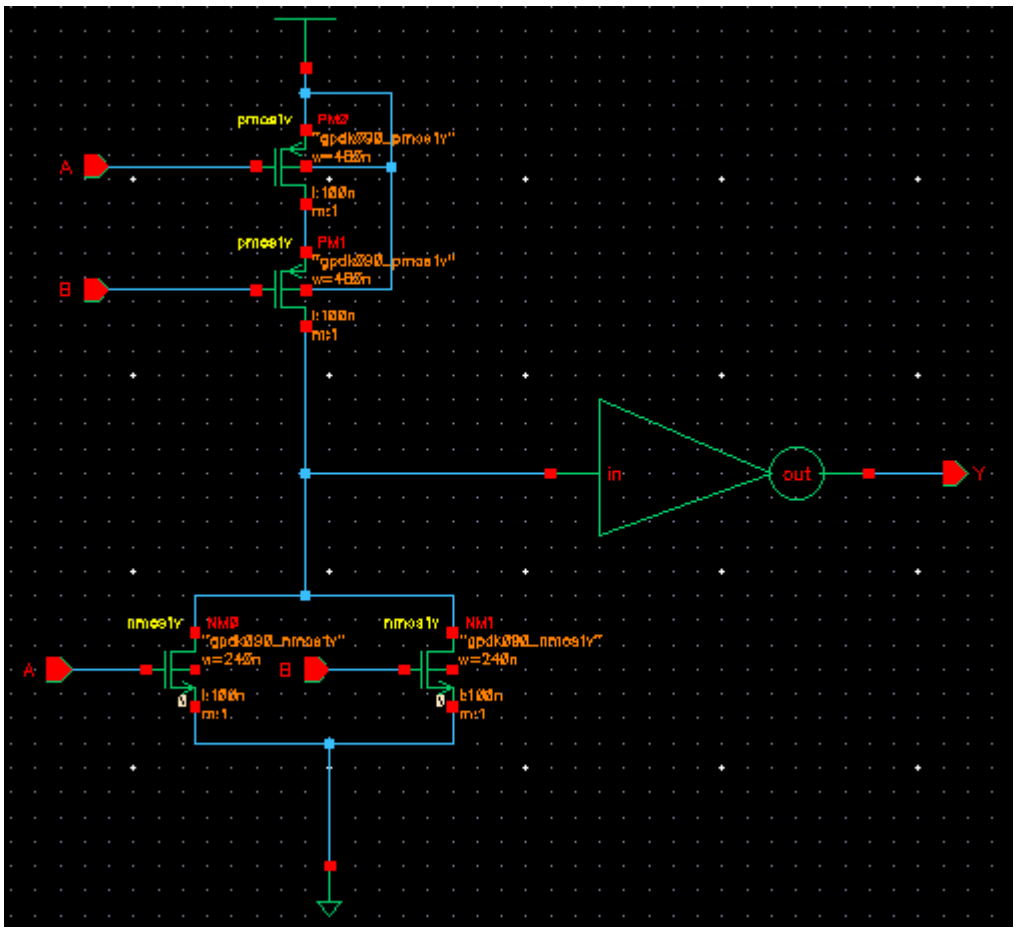

Figure No. 08: Schematic of OR gate.

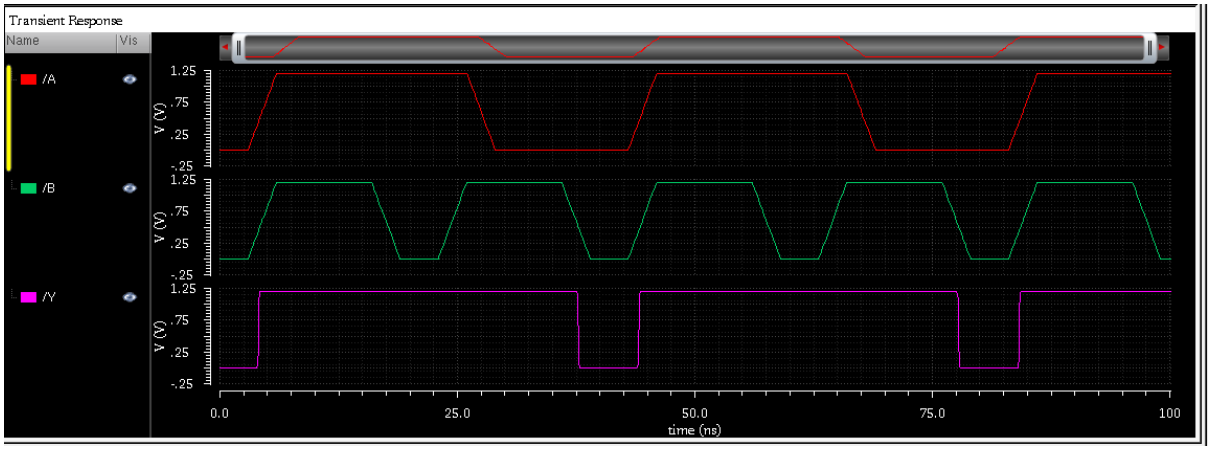

Figure No. 09: OR gate output

The symbol of OR gate was also designed for further use in the hierarchical design.

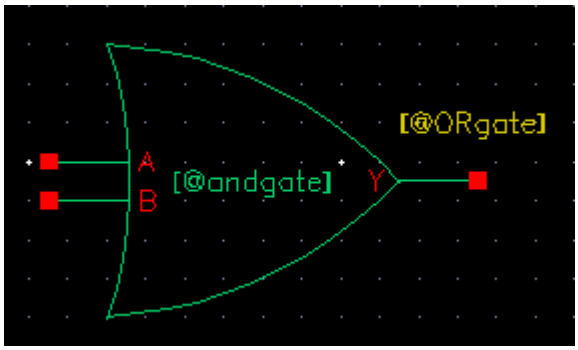

Figure No. 10: OR gate symbol

Discussion:

1. DC simulation and parametric analysis of PMOS and NMOS, symbol design and AND gate design along with its symbol was done in this experiment.
2. The parametric analysis was done by sweeping the width of the MOS and analyzing the TCC.
3. The conventional symbol for inverter was designed using triangle shape and circle for the bubble which denotes active low status.
4. The configuration of the AND gate was designed with the width of NMOS to be half of the PMOS so that the current carrying capability matches.
5. The symbol of two input AND gate was made.
6. The switching capability of MOS greatly depends on the width of the substrate.
7. Connection of the wires were made carefully so that they do not touch each other and form cross connection.