Chittagong University of Engineering & Technology

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

NAME OF THE EXPERIMENT / REPORT

Schematic Driven Layout Design of a NAND Gate Using Virtuoso Layout Suite Editor XL

COURSE NO : ETE 404

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Objectives:

- To familiarize with schematic-driven layout design.
- To perform schematic-level verification, DRC and LVS.
- To perform post-layout simulation of NAND Gate.

Required Software:

1. Cadence

Design:

In this experiment, we performed schematic driven layout design using Virtuoso Layout Editor XL. Virtuoso Layout Editor XL is a schematic-driven layout generation tool. For this we created a 2-input NAND gate.

At first the schematic of the NAND gate was created. For this from CIW File > New > Cellview was executed. 'nmos' and 'pmos' was taken from the gpdk090 library and width was change to 240nm and 480nm respectively. 'vdd' and 'gnd' was taken from analogLib library.

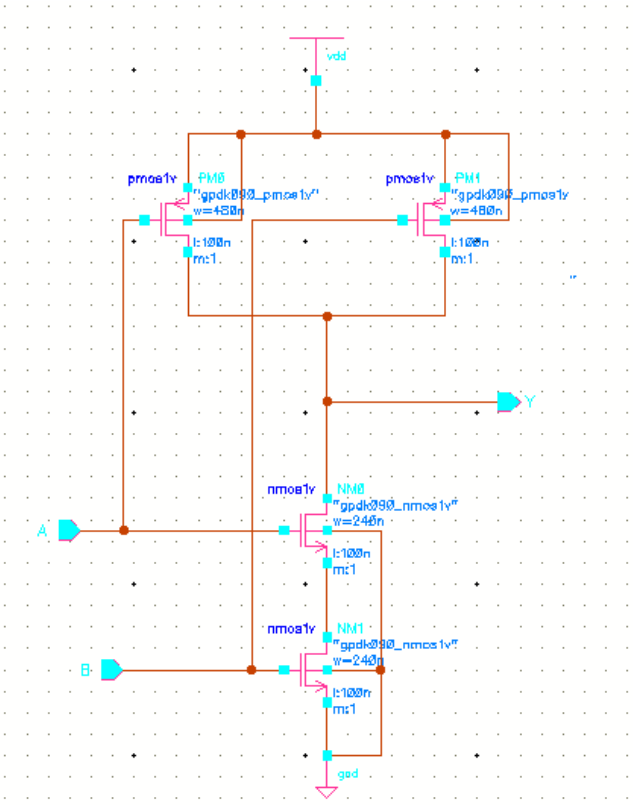

Figure No. 01: NAND gate schematic

After designing the schematic as the above figure, the functionality was tested. For this the ADE L was launched and the schematic was simulated. The input and output curves were found to be as followed.

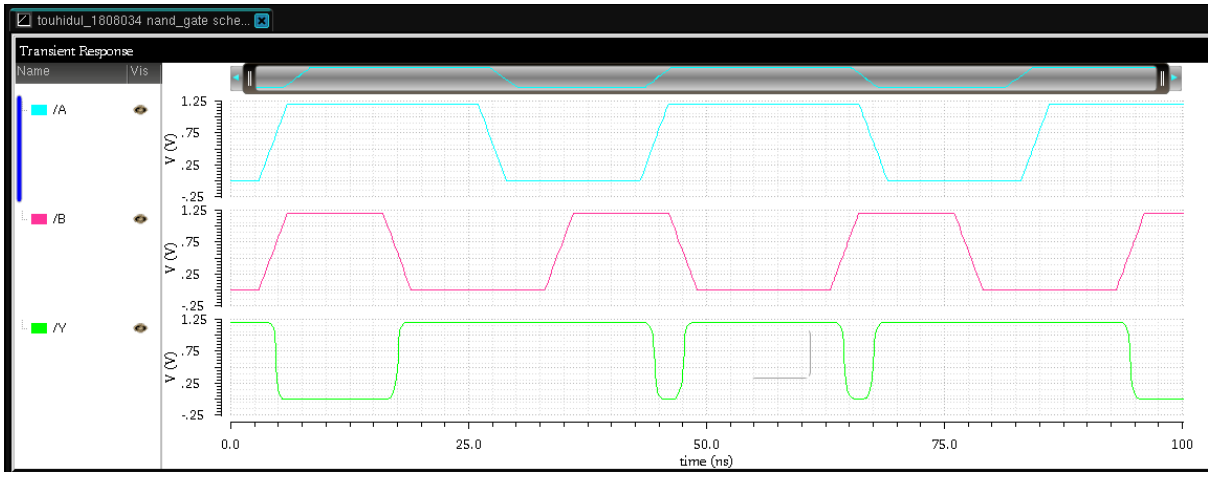

Figure No. 02: NAND gate output

Then the symbol of the NAND gate was created.

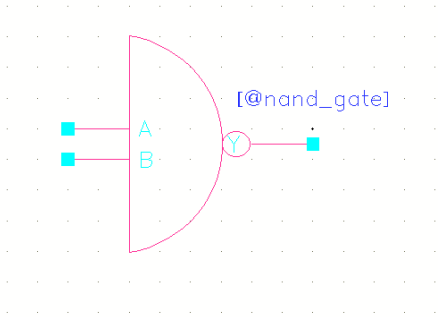

Figure No. 03: NAND gate symbol

Then in the schematic editor window Layout XL was launched. A new file was created. Then Connectivity > Generate > All From Sources was executed. Then from the pop-up 'I/O Pins' tab the layer for all pins was set to Metal1 layer and height was set to 0.1. Then from the display options the major spacing, minor spacing, X and Y snap spacing was defined.

The PR Boundary was deleted. Virtuoso Layout Editor XL (VXL) and gpdk090 allow us to create stacked transistors with shared source/drain areas. When the transistors are selected and moved, fly-lines indicating the connectivity appears. After the stacking the transistors upon one another, different layers were connected to one another by drawing rectangles. To connect one layer to another (e.g., Poly to Metal1 or Metal1 to Metal2), create via by pressing 'o' on keyboard and selecting proper 'Via Definition'. Instantiated M1_PSUB and M1_NWELL cells (that you have created earlier) by pressing 'i' on keyboard and selected the layout view from library browser. Selected the PMOS to connect its source to VDD, there are multiple Metal1wires in the PMOS And the desired path highlighted. Moved vdd! and gnd! pins to the power rails. And make set height 5 μm.

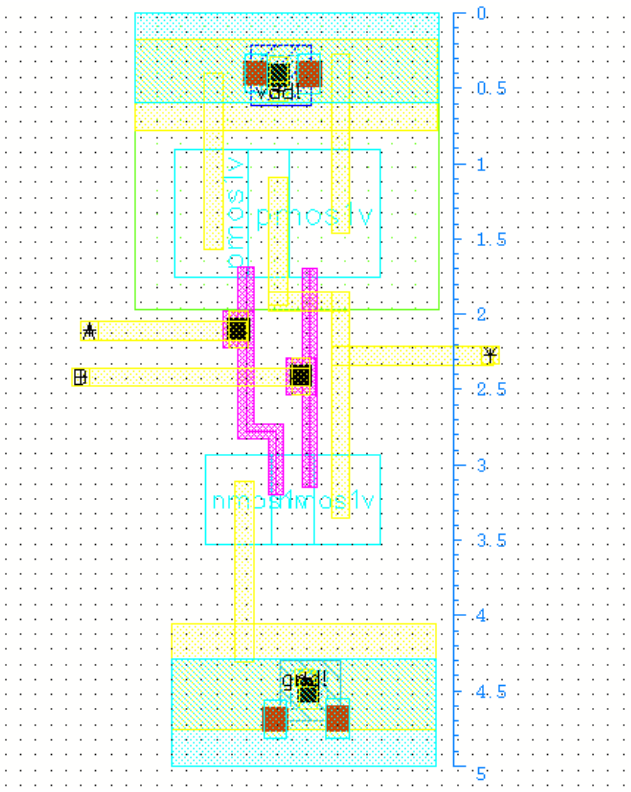

Figure No. 04: NAND gate layout

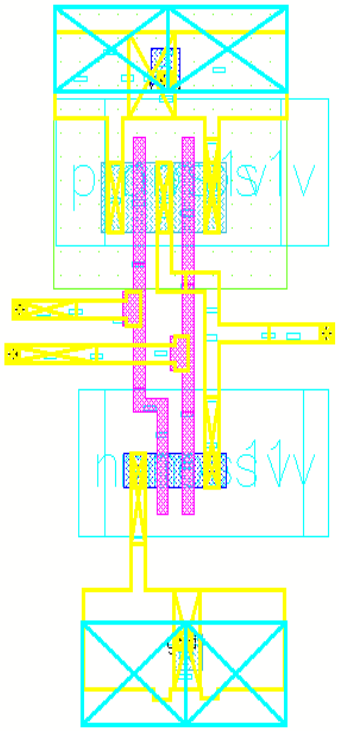

Figure No. 05: NAND gate av_extracted view

After designing the layout. DRC and LVS was performed sequentially. Some errors were found and solved. Hence no DRC or LVS errors remained. After that RCX was performed for the extraction of parasitic capacitance and resistance. After performing RCX the av_extracted layout was simulated and correct functionality was obtained.

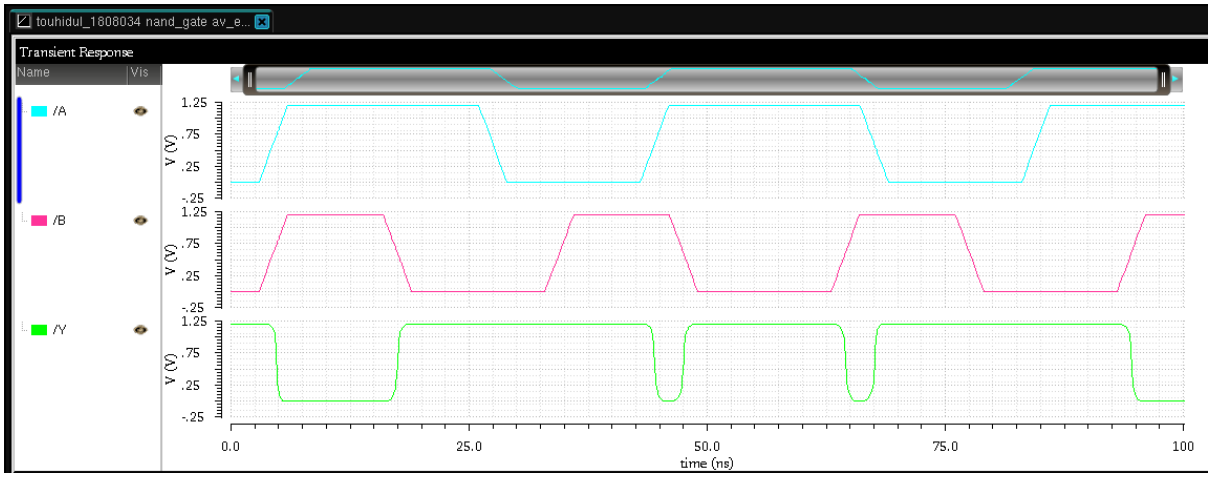

Figure No. 06: NAND gate output from av_extracted view

Home Task:

Stacked Transistors:

In a stacked design, several transistors are vertically connected, which means the source and drain of one transistor are coupled together. Some of the advantages of stacked transistors are:

1. Increased Current Carrying Capability: Transistors can be stacked to widen the effective channel width, boosting the current-carrying capability without considerably expanding the transistor's area or footprint.
2. Improved Speed: The on-resistance (Rds(on)) of the stacked transistors is decreased by increasing the effective channel width, resulting in quicker switching times and better performance.
3. Reduce Parasitic Resistance: Stacked transistors can improve performance and cut power losses by lowering the parasitic resistance that results from the connections between transistors.

Unstacked Transistors:

Each transistor in an unstacked design has its own drain and source terminal, and they are not vertically coupled. Standard CMOS (Complementary Metal-Oxide-Semiconductor) logic designs frequently employ unstacked transistors. Some of the advantages of unstacked transistors are:

1. Better Isolation: Better electrical isolation between devices is made possible by unstacked transistors, which is essential for avoiding undesired coupling and assuring dependable circuit performance.
2. Design Flexibility: Since each transistor can be separately controlled and connected to various circuit nodes as needed by the circuit design, unstacked transistors allow greater design flexibility.
3. Reduce Cross-Talk: Unstacked transistors encounter reduced cross-talk between surrounding devices thanks to the improved isolation, which is crucial for high-performance circuits.

Parasitic resistance of capacitance cause problem while deigning a semiconductor device. In the stacked combination the parasitic resistance is reduced. That is why, transistors are stacked with common drain/source terminals.

Discussion:

1. Schematic driven layout design of NAND gate using Virtuoso Layout Suite Editor XL was done in this experiment.
2. Before running the final simulation and looking at the output waveforms, check all the rules, then fix any errors that surfaced.
3. The DRC errors were fixed in the layout but once DRC is cleared the layout was left untouched.
4. The LVS debug and change of parameters was done to the schematic.
5. The RCX was performed to extract any parasitic resistance or capacitance.
6. Post layout simulation showed the same result as the schematic.