Chittagong University of Engineering & Technology

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

NAME OF THE EXPERIMENT / REPORT

DRC, LVS, RCX and Post-Layout Simulation of an Inverter

COURSE NO : ETE 404

COURSE TITLE : VLSI Technology Sessional

EXPERIMENT NO. : 06

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Objectives:

- To perform Design Rules Check (DRC) and Layout vs. Schematic (LVS).
- To extract parasitic resistance and capacitance from layout.
- To perform transient simulation of extracted view.

Required Software:

1. Cadence

Design:

DRC Using ASSURA:

From the previously created layout, it is now to perform DRC on it. DRC stands for Design Rule Check. For this at first the layout was opened and executed Assura> Technology, then the Assura Technology file was selected. After that a complete DRC was run by executing Assura> Run DRC. If any error or problem occurred then 'Error Layer Window' displayed. After resolving the error and DRC run, no DRC error pop up would appear.

LVS Using ASSURA:

After the DRC check it is now time to match the layout with the previously designed schematic. To do this Assura> Run LVS was executed. If there was any mismatch then the LVS debug window would pop up or else it will show that there is no mismatch of any layers or pins. The LVS debug window shows the list of mismatches between layout and schematic. After resolving the mismatches, a LVS run was executed and no mismatch occurred.

Parasitic Extraction Using RCX:

To perform parasitic extraction using RCX, at first the error free lvs run was opened. Then Assura> Run RCX was executed. The Assura Parasitic Extraction Form appeared and 'Extracted View' was selected in output. In the Extraction tab 'Extraction Type' was chosen to be RC. After the successful run, Assura RCX run of lvs1 completed successfully will appear.

The av_extracted view was then opened and the output waveform, power and delay were calculated. For this, ADE L was launched and everything was set as the previous lab.

The delay was found to be 117.2ps and the maximum delivered power to be 38.621 μW.

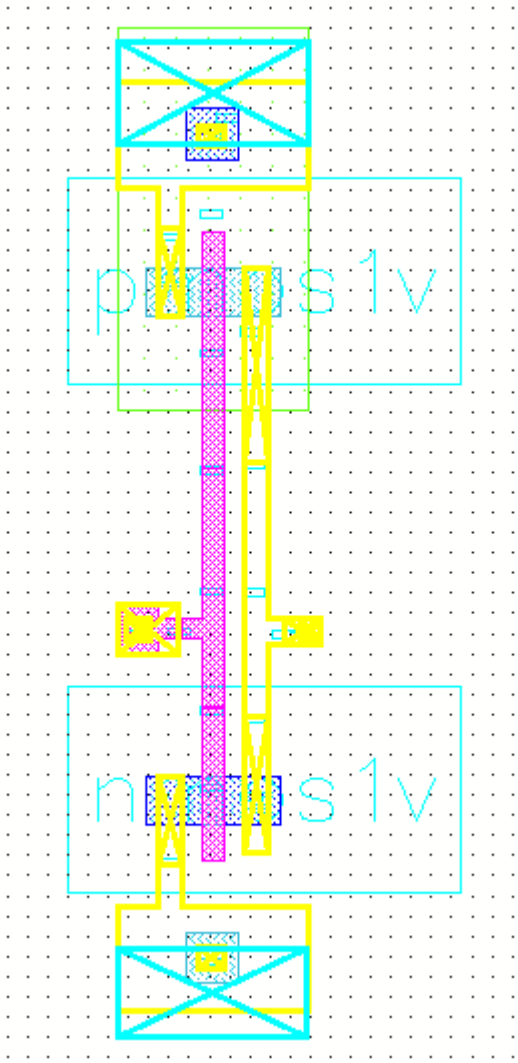

Figure No. 01: av_extracted view of Inverter

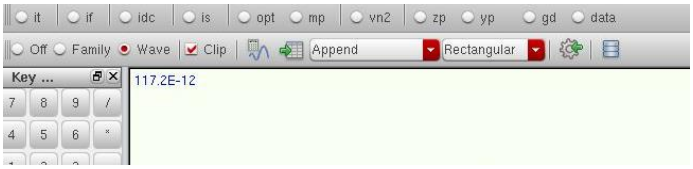

Figure No. 02: Delay of the Inverter

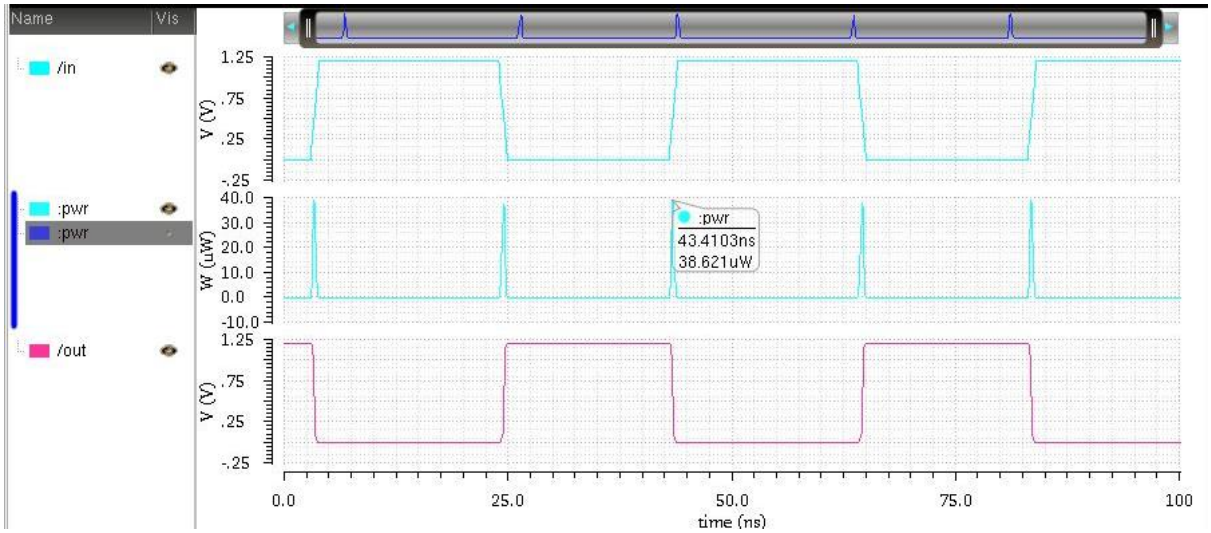

Figure No. 03: Output waveform and power consumption

Discussion:

1. DRC (Design Rule Check), LVS (Layout vs. Schematic), RCX (Resistance-Capacitance Extraction), and post-layout simulation of an inverter were all used in this experiment.
2. Before running the final simulation and looking at the output waveforms, check all the rules, then fix any errors that surfaced.
3. The DRC errors were fixed in the layout but once DRC is cleared the layout was left untouched.
4. The LVS debug and change of parameters was done to the schematic.
5. The power and latency were also measured using a waveform calculator.
6. Minimum width and distance were maintained to avoid error.