Chittagong University of Engineering & Technology

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

NAME OF THE EXPERIMENT / REPORT

Layout Generation of an Inverter using Virtuoso L

COURSE NO : ETE 404

COURSE TITLE : VLSI Technology Sessional

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Objectives:

- To create a layout view of the basic inverter in Virtuoso Layout Editor.
- To design the layout keeping basic design rules in mind.
- To design cell layout of a constant height for use in hierarchical design.

Required Software:

1. Cadence

Design:

The patterns of the metal, polysilicon, oxide, or diffusion layers that make up an integrated circuit are displayed using planar geometric shapes to describe a circuit using Layout. The Design Rule Checking (DRC) procedure examines if the circuit's intended layout upholds the rules outlined by the process. The Layout Versus Schematic (LVS) step determines if a specific integrated circuit layout preserves the design's pre-defined schematic or circuit diagram.

The new cellview is opened as the Layout view when Virtuoso has been launched from the terminal.The documentation should be followed while changing the display choice. The NMOS and PMOS transistors of an inverter are made up of layers called oxide, Nimp, Cont, and Poly in the NMOS inverter. The layers of a PMOS inverter are oxide, pimp, cont, and poly.

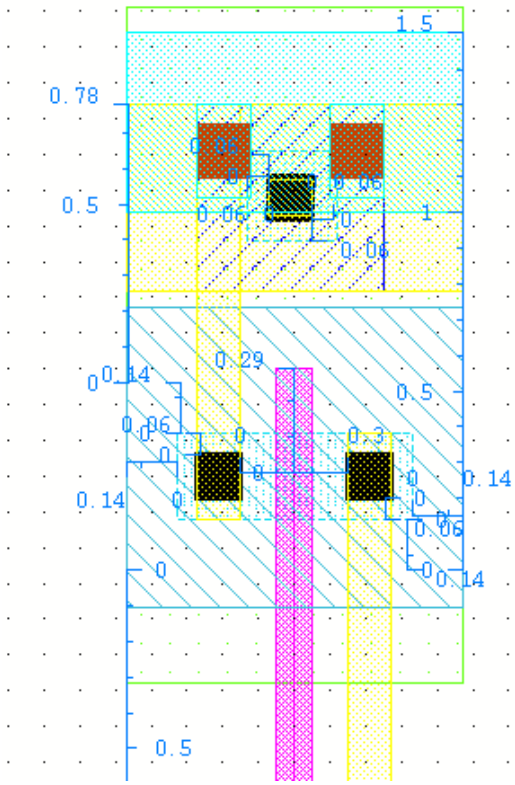

Figure No.01: Layout of PMOS

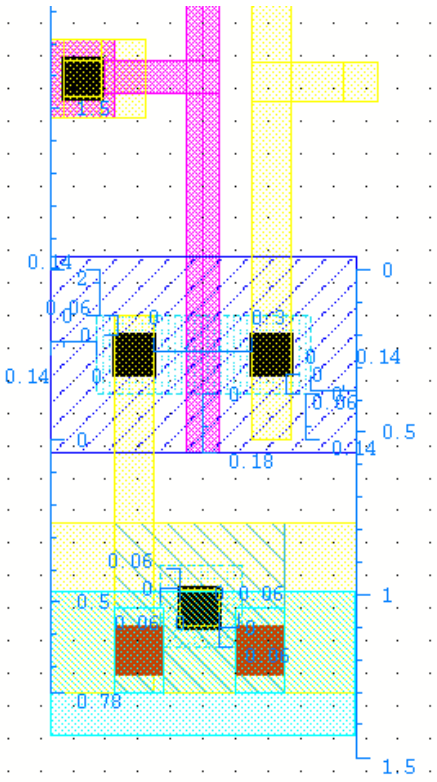

Figure No.02: Layout of NMOS

In order to connect NMOS and PMOS, a poly layer was positioned between them after their creation and maintained them 2 m away.The contact for the NMOS and PMOS body terminals was then established. These components are Cont, Oxide, and Nimp (for the PMOS body) or Pimp (for the NMOS body).'Metal1 (drw)' layer is used to connect the source and drain regions of the NMOS and PMOS to their appropriate body terminals. Both the PMOS and the body contact for the PMOS are enclosed by the rectangle of Nwell (drw).

The vdd pin was added to the PMOs contact, the gnd pin was added to the NMOS contact, the vin pin was added to the 'M1_POv', and the vout pin was connected to the metal connection lines while inserting pins at the poly silicon layer.rectangle was drawn for the pin. Finally, 0.5 m wide Metal2 paths were introduced for connecting power rails to Metal1's power nets using a Metal1 to Metal2 via by using the 'make via' command.

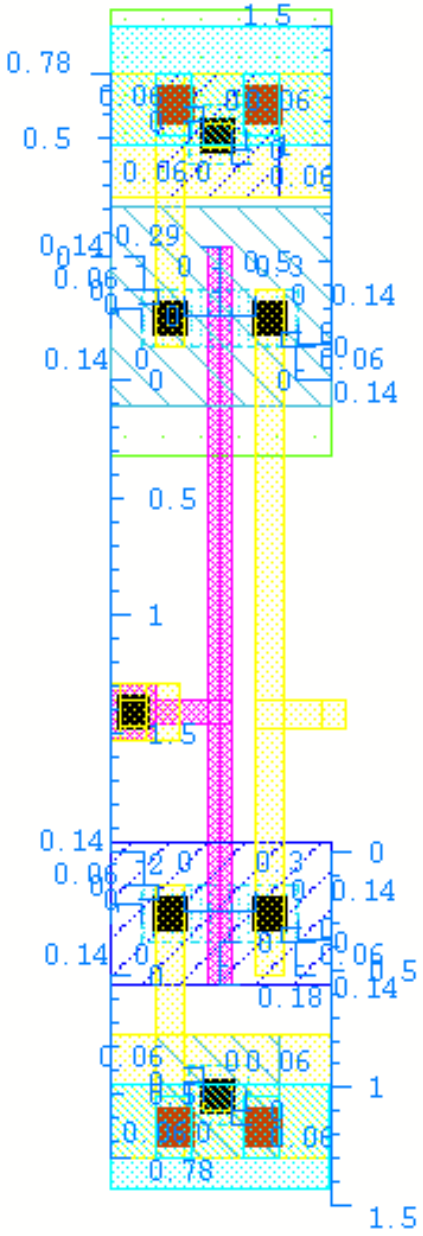

Figure No.03: Layout of an Inverter.

Home Task:

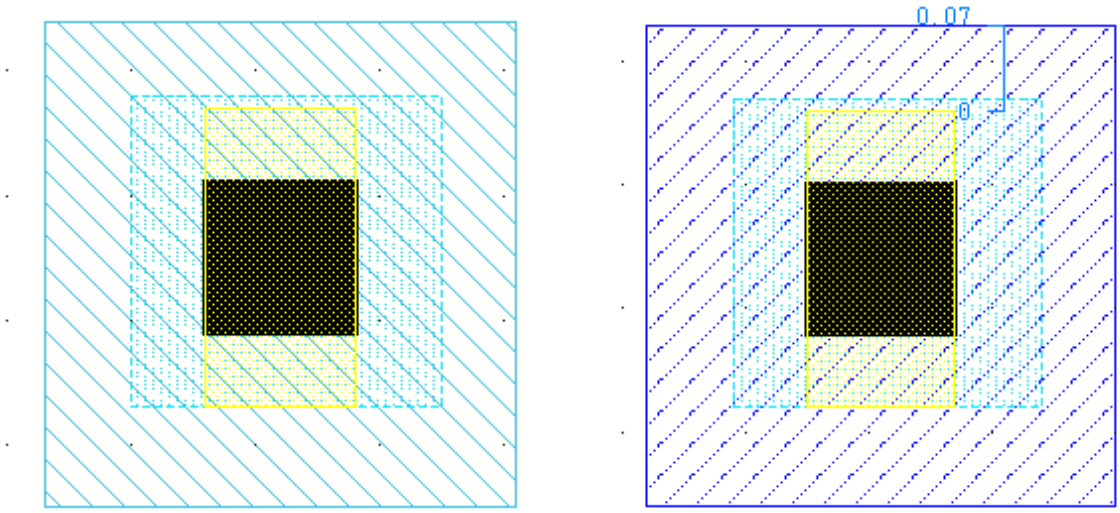

Figure No.04: P-substrate and NWELL contact

First the p-subtrate contact was made by placing the contact, oxide, Pimp layer and metal contact was created. Similarly, the NWELL was made just by replacing the pimp layer to nimp.

Discussion:

1. This experiment led to the creation of a layout view for the fundamental inverter in Virtuoso Layout Editor.
2. The same cell height from the cell library was maintained while using a full-custom IC design method.
3. Physical verification is the process of checking the generated layout once it has been created.
4. A scale was used to properly measure each item.
5. Minimum width and distance was maintained to avoid error.