Chittagong University of Engineering & Technology

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

NAME OF THE EXPERIMENT / REPORT

Design and Performance Analysis of an Inverter Using Cadence Virtuoso

COURSE NO : ETE 404

COURSE TITLE : VLSI Technology Sessional

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TERM : I

SECTION :

GROUP : G-2

Objectives:

- To familiarize with Cadence tools and library creation.
- To familiarize with inverter design and implementation.
- To familiarize with transient analysis and performance measurements.

Required Software:

1. Cadence

Design:

In this experiment, our goal was to design and analyze an inverter. For this purpose, I used the Cadence design software.

For this at first, I opened the Cadence Virtuoso and then created a library named 'touhidul_1808034' and attached to an existing library 'gpdk090' which stands for Generic PDK 90nm. Then after the library was created, for creating the schematic of the inverter, in CIW went to File and selected 'Cellview' from New. The form that appeared was filled with Library: touhidul_1808034, Cell: inverter, View: schematic, Type: schematic, Open with: Schematics L. After clicking OK a black window appeared.

For the instance creation, shortcut key 'i' was pressed. After that from gpdk090 library, nmos1v cell was selected and its schematic was added. Similarly, a pmos1v was also added. After successfully adding the schematics now to edit the properties the respective nmos and pmos was selected and shortcut key 'q' was pressed. The Total width of nmos was set to 240nm and pmos to 480nm. Similarly, the power nets 'vdd' and 'gnd' was added from the analogLib. Input and output pin were inserted by selecting Direction property as input for in and output for out. The input pin is the input to gate and output pin is the output of the NMOS and PMOS at the common node between drains.

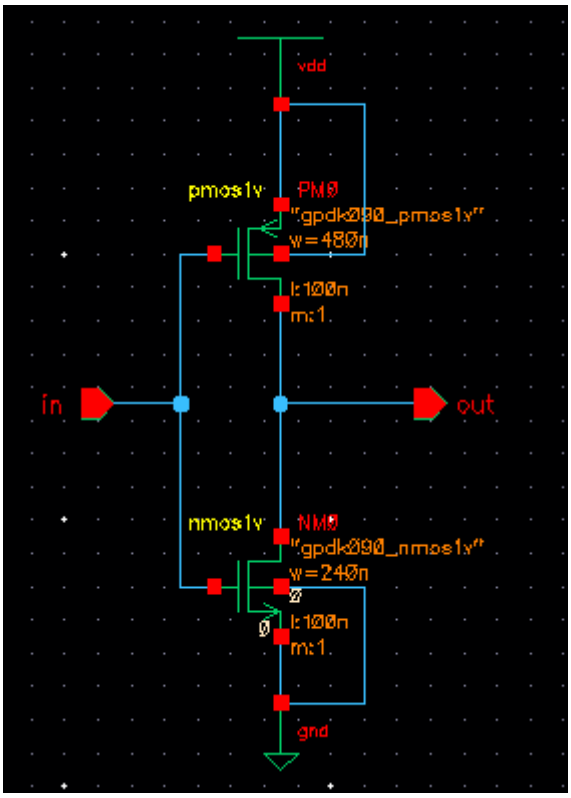

Figure No. 01: Schematic of inverter

After the schematic has been designed, it is time for simulation. For simulating, Analog Design Environment (ADE) L was used. At first the model library was selected by clicking on Setup > Model Libraries. 'gpdk090_mos.scs' was selected as the model file. From the section scroll bar 'TT_s1v' was selected to enable us use TT models of the MOS transistors. Then the input and output signal were defined from Setup > Stimuli. After defining the input and output appropriate values, transient mode of analysis

was selected. Then in ADE window Simulation > Netlist and Run was executed which resulted in the following output curve.

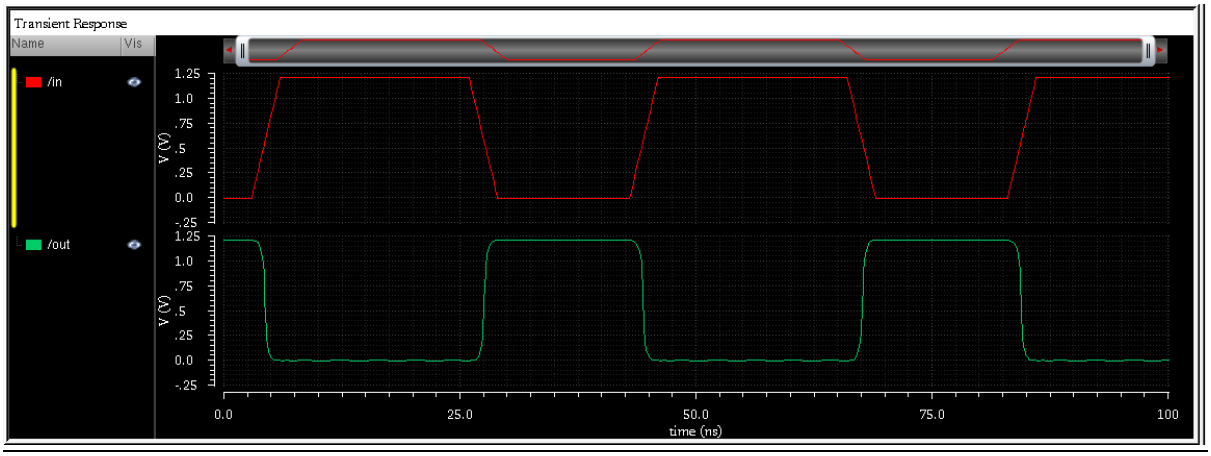

Figure No. 02: Output of the Inverter

In Figure No. 02, we can see that the output is the inverted form of the input which matches the theoretical concept of an inverter.

Waveform calculator was used to calculate the propagation delay, rise time and average power consumption. For calculation of the propagation delay, Executed Tools > Calculator in Virtuoso Visualization & Analysis XL window. Then selected VT('/in') at signal1 and VT('/out') for signal 2. By special function to delay the value were applied for further calculation. With threshold value of both signals as 0.6 the buffer icon was selected. The delay was 109.2E-12.

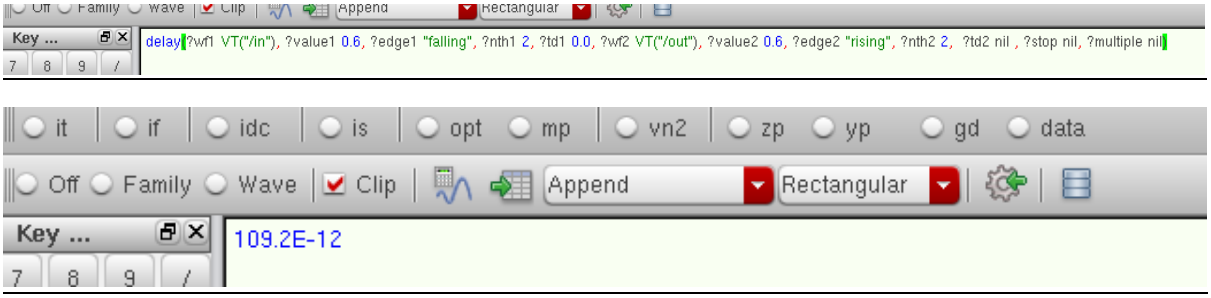

Figure No. 03: Propagation delay equation and result

Again, the calculation for the rise time was done and the output was found to be 709.9E-12.

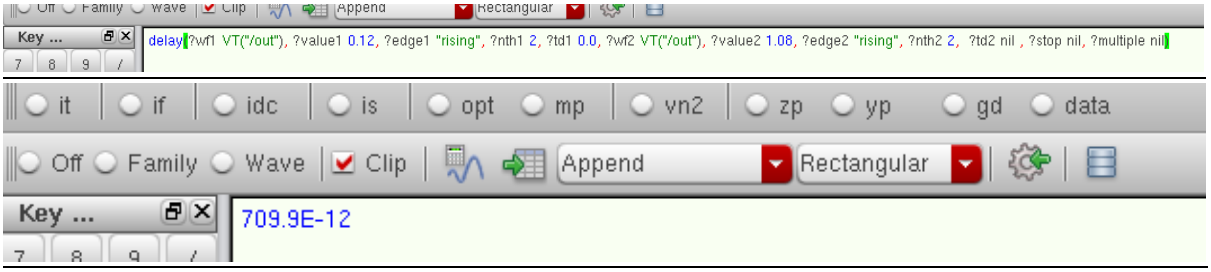

Figure No. 04: Rise Time equation and result

After that for power calculation, before running simulation selected the Outputs >Save All option in ADE L window. Then the circuit was simulated as usual. Next trans option was selected and power waveform was shown then, also by clicking output waveforms the average power was calculated 2.958E-6.

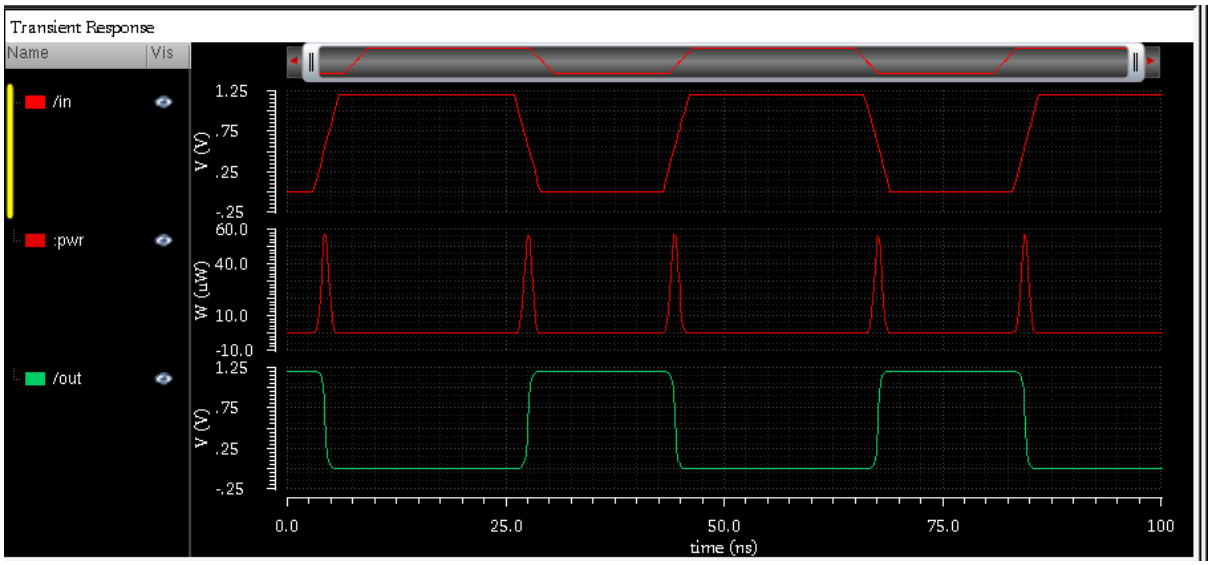

Figure No. 05: Power consumption graph

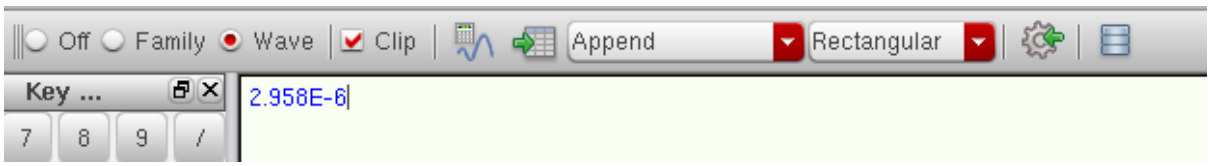

Figure No. 06: Average calculated power

Discussion:

1. Design of an inverter using NMOS and PMOS along with the performance analysis in Cadence Virtuoso was learnt in this experiment.
2. Connection of the wires were made carefully so that they do not touch each other and form cross connection.
3. Propagation delay was measured between the input and the output signal with 0.6V as threshold.
4. Rise time which is defined as the time required to reach from 10% to 90% of the signal, was also calculated.
5. For rise time calculation the edge number of input and output was kept same.
6. Power consumption graph was observed and the average power was also calculated.