Design and Analysis of 8x1 Multiplexer Using CMOS

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***Abstract*—The design and implementation of multiplexers (MUXes) using complementary metal-oxide-semiconductor (CMOS) technology play a vital role in modern digital circuitry. This paper presents a comprehensive study on the design of an 8x1 MUX using CMOS technology. The 8x1 MUX serves as a fundamental building block in digital systems, allowing the selection of one out of eight input signals based on control lines. The design process involves transistor level implementation of n-type metal-oxide-semiconductor (NMOS) and p-type metal-oxide-semiconductor (PMOS) transistors controlled by select lines, to determine the routing of input signals to the output. Simulations and performance evaluations are conducted by industry standard electronic design automation tools which demonstrates the successful operation of the CMOS 8x1 MUX design. The discussed design of 8x1 MUX shows the practical implementation of CMOS logic in digital circuits, offering insights into the design principles and considerations required for efficient signal routing.**

***Index Terms*—Multiplexer,Transistors, CMOS, NMOS, PMOS**

I. Introduction

The field of digital circuit design continues to evolve with advancements in semiconductor technology whic aims to achieve higher levels of integration, improved performances and lower power consumption. Multiplexers are essential components in digital systems that play an important role in signal routing and selection. Designers are empowered to create efficient and compact MUX designs with the help of complementary metal-oxide-semiconductor (CMOS) technology to fulfill the demands of modern digital circuits.

With this view, this paper introduces the design and implementation of an 8x1 MUX using CMOS technology. Multiplexers are versatile elements that allow a single output to be driven by one of several input lines based on control signals. The 8x1 MUX extends this functionality to select from eight different input sources, making it a crucial building block in various digital applications, including data routing, memory addressing, and control logic.

The use of CMOS technology in the design process offers advantages such as low power consumption,compatibility, and high noise immunity. The NMOS (n-type metal-oxide-semiconductor) and PMOS (p-type metal-oxide-semiconductor) transistors in the design enables the realization of efficient pass transistors that control signal routing through the MUX.

In the course of the paper, the fundamental principles of CMOS design and logic synthesis will be explored. Simulations and evaluations using industry-standard electronic design automation (EDA) tools will be conducted to verify the functionality and correctness of the designed 8x1 MUX. The results obtained from these simulations will highlight the successful implementation of the CMOS-based MUX, contributing to the broader understanding of digital circuit design using advanced semiconductor technologies.

II. Proposed Methodology

Multiplexers are used in almost all circuits of our daily usage such as routers and switches. This design approach includes designing of an inverter and connecting the NMOS and PMOS in suitable combination. There are 8 input lines and 3 select lines. The select lines can have eight different combinations which route the eight different inputs to the outputs. The circuit design is based on the Boolean output equation of the multiplexer.

$$Y = S0'S1'S2'D0 + S0'S1'S2D1 + S0'S1S2'D2 + S0'S1S2D3 + S0S1'S2'D4 + S0S1'S2D5 + S0S1S2'D6 + S0S1S2D7$$

A. Design Steps

1 First an inverter in design to invert the selection lines. For this an NMOS of width 120nm and PMOS of width 240nm was taken. The gate of the NMOS and PMOS was connected to the input. The source of PMOS was connected to the Vdd and source of NMOS to Gnd. The drain of PMOS and source of NMOS were connected with each other and output was taken form there. Fig. 1 shows the schematic of the inverter.

2 Then the selection lines of S0, S1 and S2 were fed to different inverter to calculate the inverted output. Fig.2 shows the schematic.

3 Now the PMOS transistors with width 240nm are connected in such a configuration where if there is AND operation PMOS are connected in parallel and for OR operation they are connected in series. The selection lines

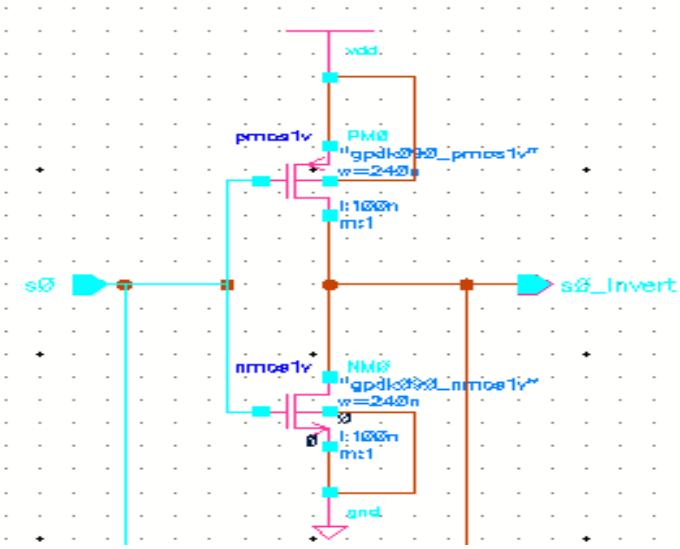


Fig. 1: Schematic of an inverter

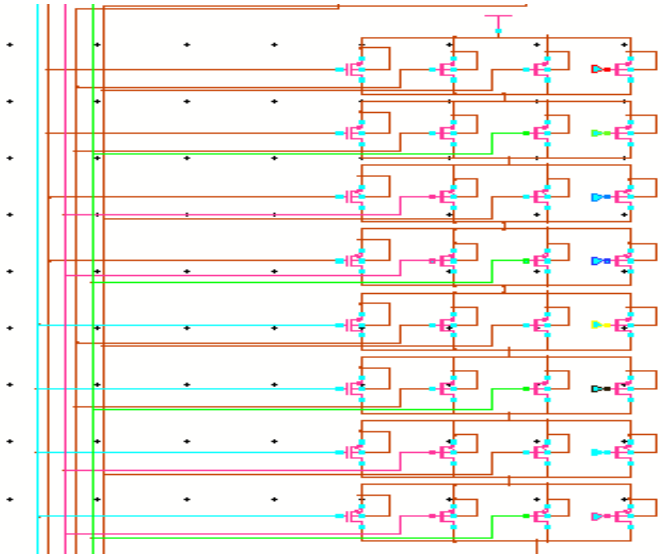


Fig. 3: Connection of the PMOS transistors

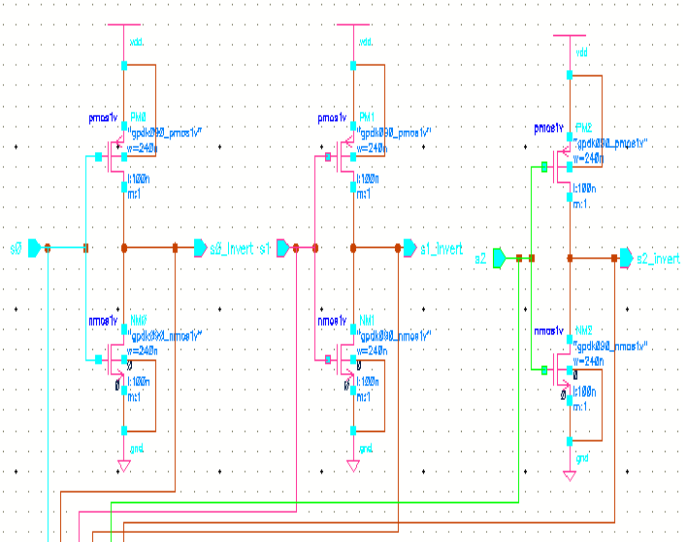


Fig. 2: Connection of the selection lines in the inverter

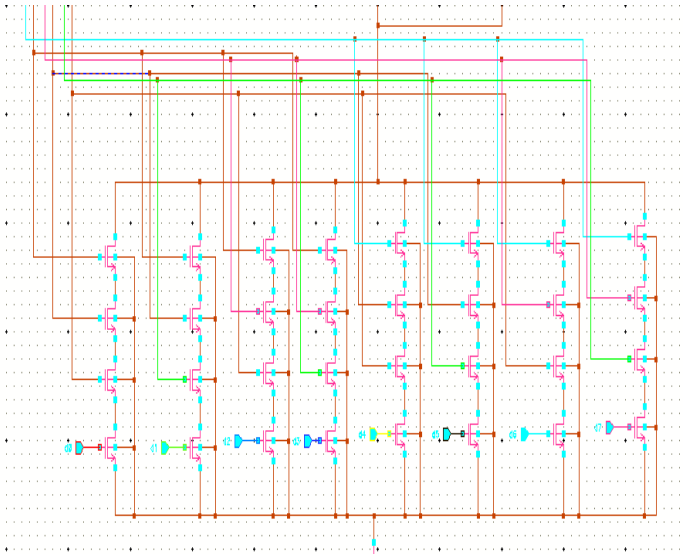


Fig. 4: Connection of the NMOS transistors

and the inputs from D0 to D7 are connected accordingly. Fig. 3 shows the final configuration.

4 Now the NMOS transistors with width 120nm are connected in such a configuration where if there is AND operation NMOS are connected in series and for OR operation they are connected in parallel. The selection lines and the inputs from D0 to D7 are connected accordingly. Fig. 4 shows the final configuration.

5 Now the PMOS configuration or pull up network and NMOS configuration or pull down network are connected. The output is taken from the connection point. The output is passed through another inverter because the implemented configuration results in an inverted output. Fig. 5 shows the overall schematic of the 8x1 MUX.

B. Stick Diagram

A stick diagram is a kind of diagram which is used to plan the layout of a transistor cell[1]. The stick diagrams uses ”sticks” or lines to represent the devices and conductors.

In stick diagram the crossing of poly-silicon with p-type and n-type material creates a PMOS and NMOS transistors. The red lines resemble poly-silicon, yellow means p-type, green means n-type, black means via connection, blue means metal and dashed brown means demarcation. The via connection are used in the junctions where two different type of materials connect with each other.

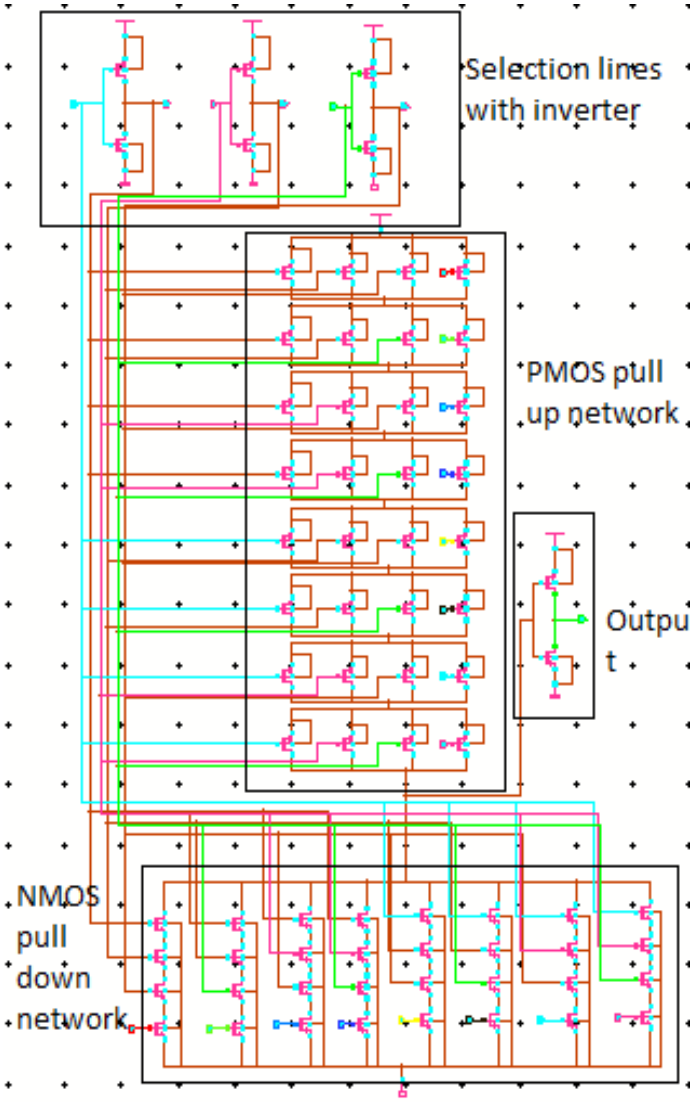


Fig. 5: Schematic of 8x1 MUX

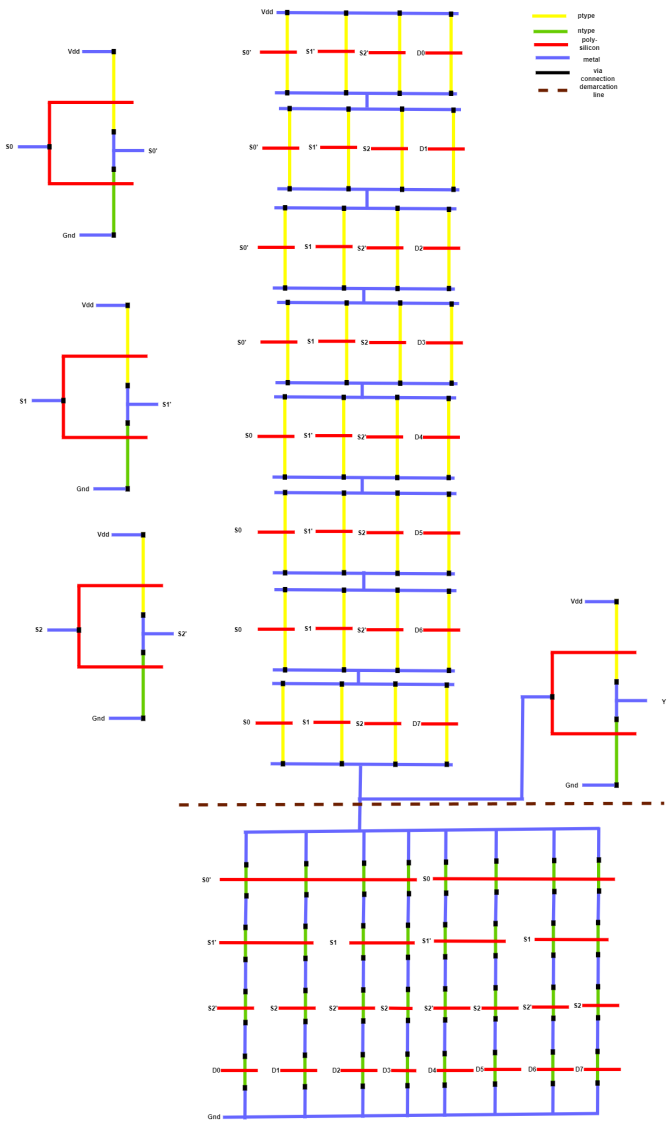


Fig. 6: Stick Diagram of 8x1 MUX

III. Result Analysis

A. Simulation Results

The simulation results shows the behaviour of the 8x1 MUX. In the figures it can be seen that for different combination of the selection lines different outputs are being displayed.

B. Truth Table

When the select line reads 000 then the input D0 is selected. In the similar way for combinations 001, 010, 011, 100, 101, 110, 111 the inputs D1, D2, D3, D4, D5, D6 and D7 are routed to the output. Table I shows the truth table for the all the combinations.

S0	S1	S2	Y
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

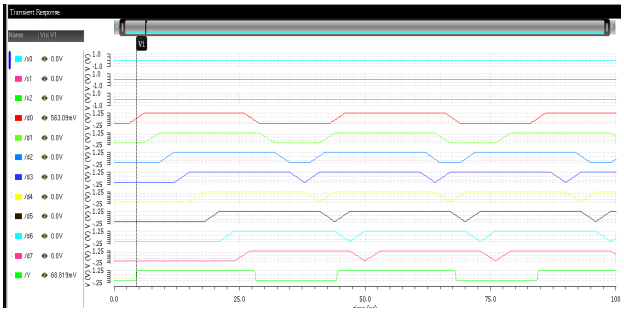
TABLE I: TRUTH TABLE

C. Delay

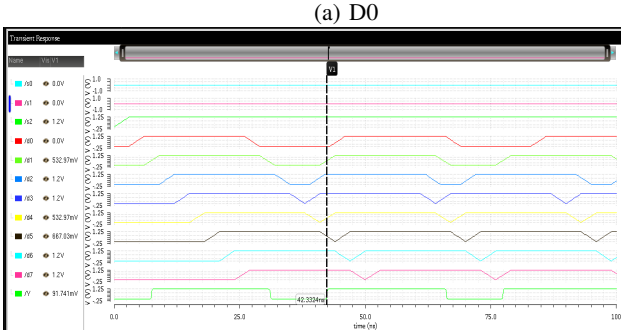
The time taken by a signal or electric pulse to propagate through a specific component, circuit or system [2]. Here the propagation delay of the MUX. Here the delay in between the output is calculated. The delay was found to be 128.6ps. Fig. 11 shows the output of the delay.

D. Power Calculation

The maximum power that is dissipated while the input rise from 0 to 1 or the rising edge is calculated from the waveform. The maximum power was found to be 49.9931 microWatt. Fig. 12 shows the power dissipation graph.

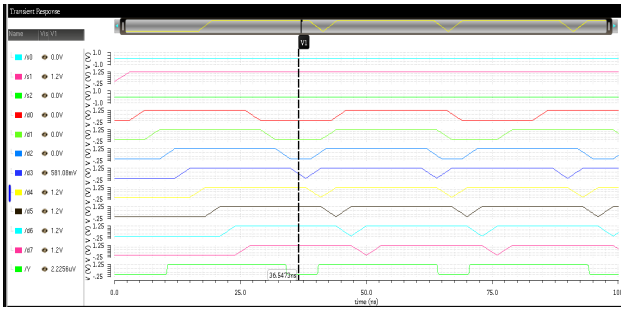


(a) D0

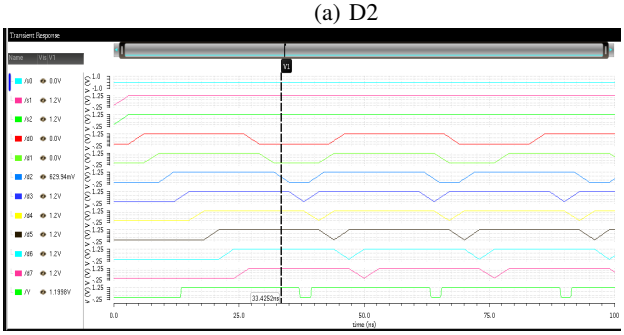


(b) D1

Fig. 7: Simulation Output results of 8x1 MUX

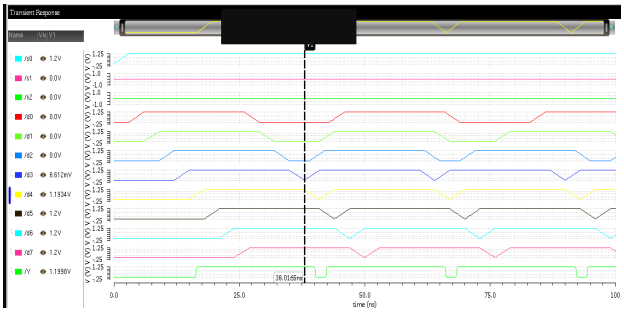


(a) D2

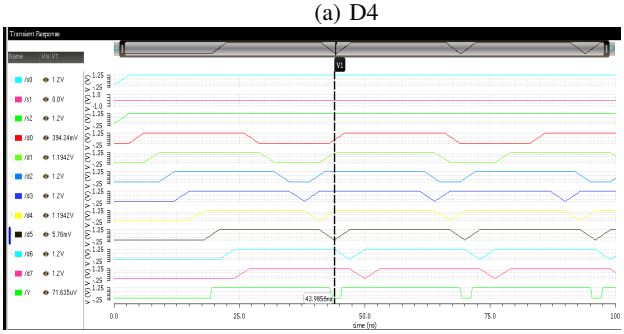


(b) D3

Fig. 8: Simulation Output results of 8x1 MUX

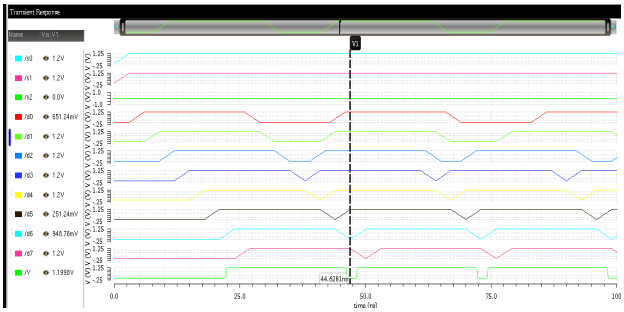


(a) D4

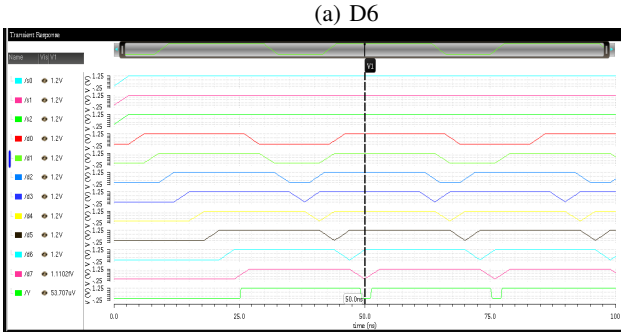


(b) D5

Fig. 9: Simulation Output results of 8x1 MUX



(a) D6



(b) D7

Fig. 10: Simulation Output results of 8x1 MUX

IV. Conclusion

The design and implementation of 8x1 MUX using CMOS technology has been successfully realized. Throughout the discussion we gained knowledge about transistor level design and analysis of results. The presented 8x1 MUX design shows the relation between logical functionality and physical realization. By leveraging both n-type metal-oxide-semiconductor (NMOS) and p-type metal-oxide-semiconductor (PMOS) transistors, we utilized the inherent advantages of CMOS technology to achieve a balance between power efficiency and high-performance signal routing.

Our exploration extended beyond theoretical discussions,

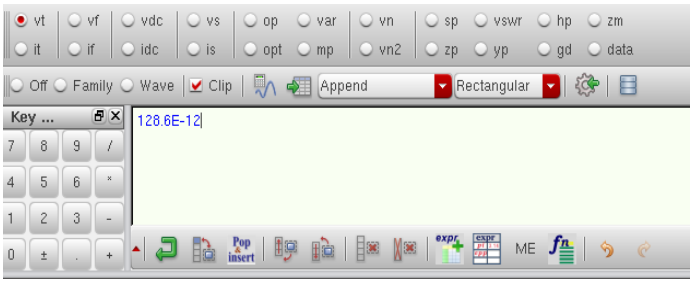


Fig. 11: Delay of 8x1 MUX

as we ventured into simulation and validation using industry-standard electronic design automation (EDA) tools. The simulation results provided evidence of the designed 8x1 MUX's accurate and reliable operation, reinforcing the theoretical concepts and design decisions that were crafted.

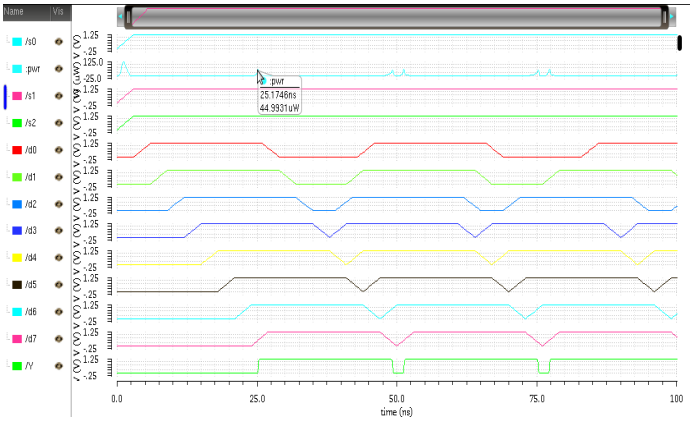


Fig. 12: Maximum Power dissipation of 8x1 MUX

REFERENCES

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2 What is propagation delay? [https://www.techtarget.com/searchnetworking/definition/propagation-delay]