Objective:

Our main goal is to sequentially display "CSE231.7G02ProJ" on Seven Segment display. It reflects that how much we have learned from digital logic design course. First of all we had to display "CSE231.7G02ProJ" by combinational circuit then implement that by sequential circuit .For that we have to implement mux in combination part and JK- flip flop in sequential part with IC 555.We have develop our skill very much by doing this project.

Theory:

Combinational circuit:

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer.


Memory Element:

Memory element A device that stores one item of information: if it has q stable states it is said to be q-ary, and if q = 2 it is said to be binary. The flip-flop is the most common type of memory element.
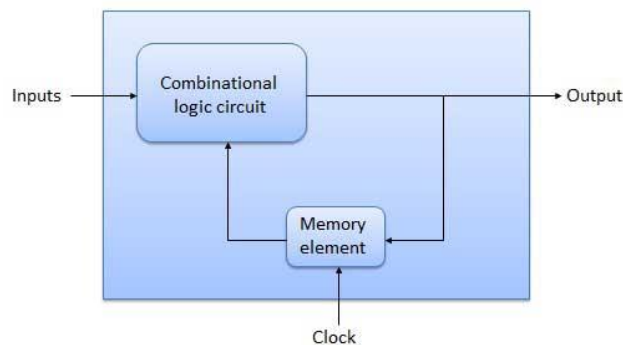
The JK Flip Flop:

Then the JK flip-flop is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time thereby eliminating the invalid condition seen previously in the SR flip flop circuit. Also when both the J and the K inputs are at

logic level "1" at the same time, and the clock input is pulsed "HIGH", the circuit will "toggle" from its SET state to a RESET state, or visa-versa. This results in the JK flip flop acting more like a T-type toggle flip-flop when both terminals are "HIGH".
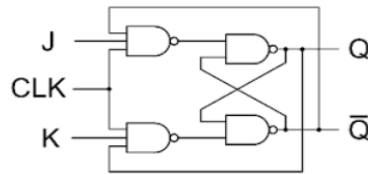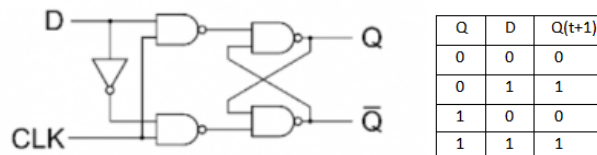

TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table: J-K flip-flop

D flipflop:

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Table: D flip-flop

A D-type flip-flop is a clocked flip-flop which has two stable states. A D-type flip-flop operates with a delay in input by one clock cycle. Thus, by cascading many D-type flip-flops delay circuits can be created, which are used in many applications such as in digital television systems.

T flipflop:

The name T flip-flop is termed from the nature of toggling operation. The major applications of T flip-flop are counters and control circuits. **T flip flop is modified form of JK-Flipflop** making it to operate in toggling region.

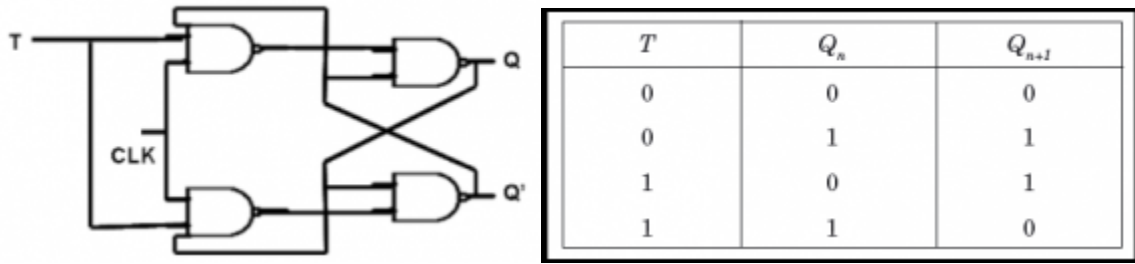| T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Table: T flip-flop

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active. Thus, T flip-flop is a controlled Bi-stable latch where the clock signal is the control signal.

Apparatus:

- 16:1 Mux IC 74150
- BCD 7 segment (Common Cathod)
- 3 input AND gate IC 4073
- 3 input OR gate IC 4075
- 2 input OR gate IC 7432
- NOT gate IC 7404 – 1
- Resistor 10k
- Timer IC 555
- Capacitor 22uF 16volt
- Jumper wire
- Battery 9V
- LM 2596 DC to DC (Bug)
- J-K flip flop IC 74107
- Breadboard

State diagram:
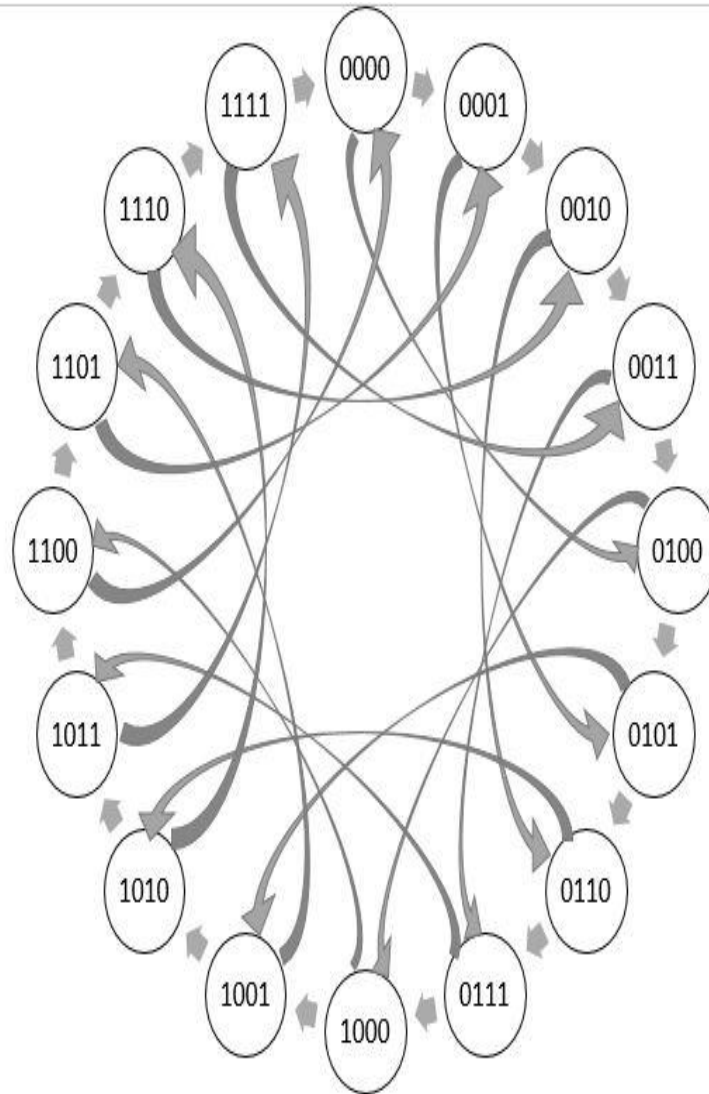
Truth table:

Combinational Part

		A	B	C	D	a	b	c	d	e	f	g	dot
0	J	0	0	0	0	1	1	1	1	1	0	0	1
1	C	0	0	0	1	1	0	0	1	1	1	0	1
2	S	0	0	1	0	1	0	1	1	0	1	1	1
3	E	0	0	1	1	1	0	0	1	1	1	1	1
4	2	0	1	0	0	1	1	0	1	1	0	1	1
5	3	0	1	0	1	1	1	1	1	0	0	0	1
6	1	0	1	1	0	0	1	1	0	0	0	0	1
7	.	0	1	1	1	0	0	0	0	0	0	0	1
8	7	1	0	0	0	1	1	1	0	0	0	0	1
9	G	1	0	0	1	1	0	1	1	1	1	0	1
10	0	1	0	1	0	1	1	1	1	1	1	0	1
11	2	1	0	1	1	1	1	0	1	1	0	1	1
12	P	1	1	0	0	1	1	0	0	1	1	1	1
13	r	1	1	0	1	0	0	1	0	1	0	1	1
14	0	1	1	1	0	0	0	1	1	1	0	1	1
15	x	1	1	1	1	x	x	x	x	x	x	x	x

Sequential part

	E	A	B	C	D	A(n)	B(n)	C(n)	D(n)	J-A	K-A	J-B	K-B	J-C	K-C	J-D	K-D	D-A	D-B	D-C	D-D	T-A	T-B	T-C	T-D
0	0	0	0	0	0	0	0	0	1	0	X	0	x	0	x	1	X	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	1	0	0	X	0	x	1	x	x	1	0	0	1	0	0	0	1	1
2	0	0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	X	0	0	1	1	0	0	0	1
3	0	0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1	0	1	0	0	0	1	1	1
4	0	0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	X	0	1	0	1	0	0	0	1
5	0	0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1	0	1	1	0	0	0	1	1
6	0	0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	X	0	1	1	1	0	0	0	1
7	0	0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1	1	0	0	0	1	0	1	1
8	0	1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	X	1	0	0	1	0	0	0	1
9	0	1	0	0	1	1	0	1	0	x	0	0	x	1	x	x	1	1	0	1	0	0	0	1	1
10	0	1	0	1	0	1	0	1	1	x	0	0	x	x	0	1	X	1	0	1	1	0	1	0	1
11	0	1	0	1	1	1	1	0	0	x	0	1	x	x	1	x	1	1	1	0	0	0	0	1	1

12	0	1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	X	1	1	0	1	0	0	0	1
13	0	1	1	0	1	1	1	1	0	x	0	x	0	1	x	x	1	1	1	1	0	0	0	1	1
14	0	1	1	1	0	0	0	0	0	x	1	x	1	x	1	0	X	0	0	0	0	1	1	1	0
15	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	X	x	x	x	x	x	x	x	x
16	1	0	0	0	0	0	1	0	0	0	x	1	x	0	x	0	X	0	1	0	0	0	1	0	0
17	1	0	0	0	1	0	1	0	1	0	x	1	x	0	x	x	0	0	1	0	1	0	1	0	0
18	1	0	0	1	0	0	1	1	0	0	x	1	x	x	0	0	X	0	1	1	0	0	1	0	0
19	1	0	0	1	1	0	1	1	1	0	x	1	x	x	0	x	0	0	1	1	1	0	1	0	0
20	1	0	1	0	0	1	0	0	0	1	x	x	1	0	x	0	X	1	0	0	0	1	1	0	0
21	1	0	1	0	1	1	0	0	1	1	x	x	1	0	x	x	0	1	0	0	1	1	1	0	0
22	1	0	1	1	0	1	0	1	0	1	x	x	1	x	0	0	X	1	0	1	0	1	1	0	0
23	1	0	1	1	1	1	0	1	1	1	x	x	1	x	0	x	0	1	0	1	1	1	1	0	0
24	1	1	0	0	0	1	1	0	0	x	0	1	x	0	x	0	X	1	1	0	0	0	1	0	0
25	1	1	0	0	1	1	1	0	1	x	0	1	x	0	x	x	0	1	1	0	1	0	1	0	0
26	1	1	0	1	0	1	1	1	0	x	0	1	x	x	0	0	X	1	1	1	0	0	1	0	0
27	1	1	0	1	1	0	0	0	0	x	1	x	1	x	1	x	1	0	0	0	0	1	0	1	1
28	1	1	1	0	0	0	0	0	1	x	1	x	1	0	x	1	X	0	0	0	1	1	1	0	1
29	1	1	1	0	1	0	0	1	0	x	1	x	1	1	x	x	1	0	0	1	0	1	1	1	1
30	1	1	1	1	0	0	0	1	1	x	1	x	1	x	0	1	X	0	0	1	1	1	1	0	1
31	1	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	X	x	x	x	x	x	x	x	x

Equation:

***D-FlipFlop*:**

$D_A = E'AB' + E'AC' + AB'C' + AB'C' + AB'D' + EA'B + BCD$

$D_B = E'BC' + EA'B' + EB'C' + E'B'CD + EB'D' + E'A'BD'$

$D_C = E'C'D + A'CD' + B'CD' + EA'C + ECD' + ABD$

$D_D = E'A'D' + E'B'D' + E'C'D' + EA'D + EB'CD + EABD'$

JK-FlipFlop:

$J_A = EA'B + BCD$

$K_A = BC + EB + ECD$

$J_B = EA' + EC' + ED' + E'CD$

$K_B = E + CD + AC$

$J_C = E'D + ABD$

$K_C = E'D + AD + E'AB$

$J_D = E'A' + E'B' + E'C' + EAB$

$K_D = AC + AB$

T-FlipFlop:

$T_A = EB + BCD + ABC + EACD$

$T_B = EA' + EC' + ED' + E'CD + ABC$

$T_C = E'D + ACD + ABD + E'ABC$

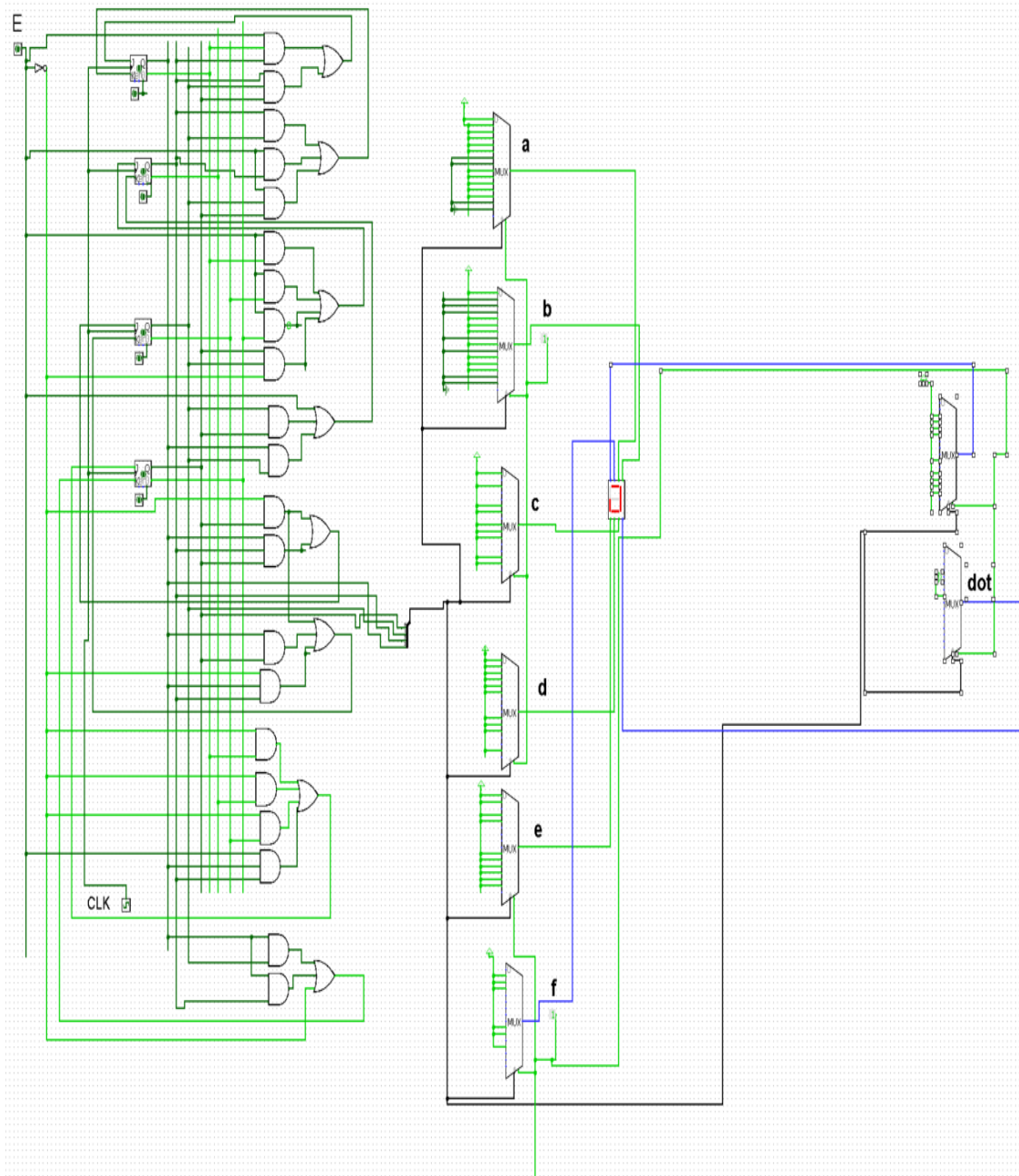$T_D = E'A' + E'B' + E'C' + ACD + EAB$

Logisim:

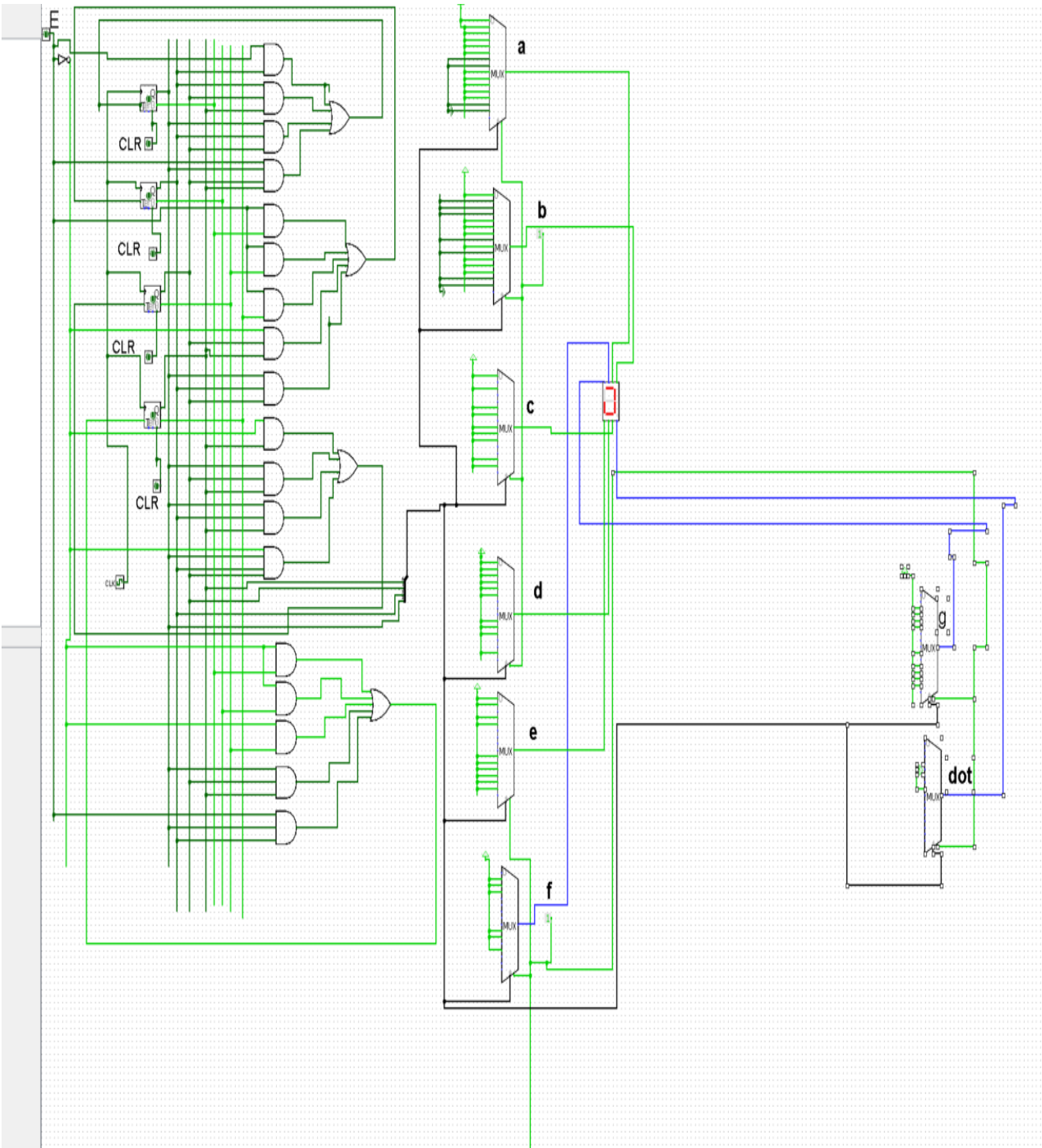**MUX:**
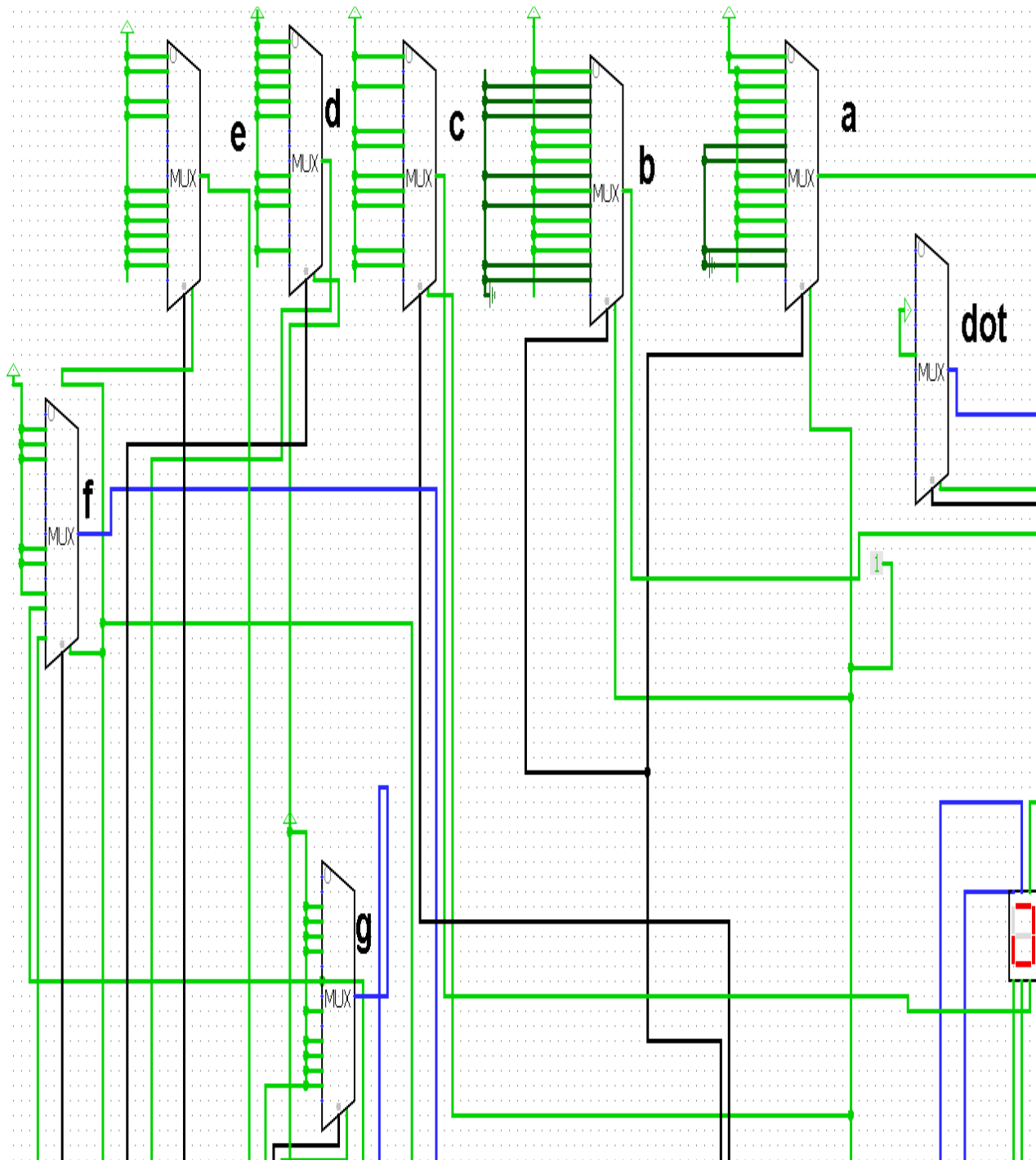
Basic Gate:
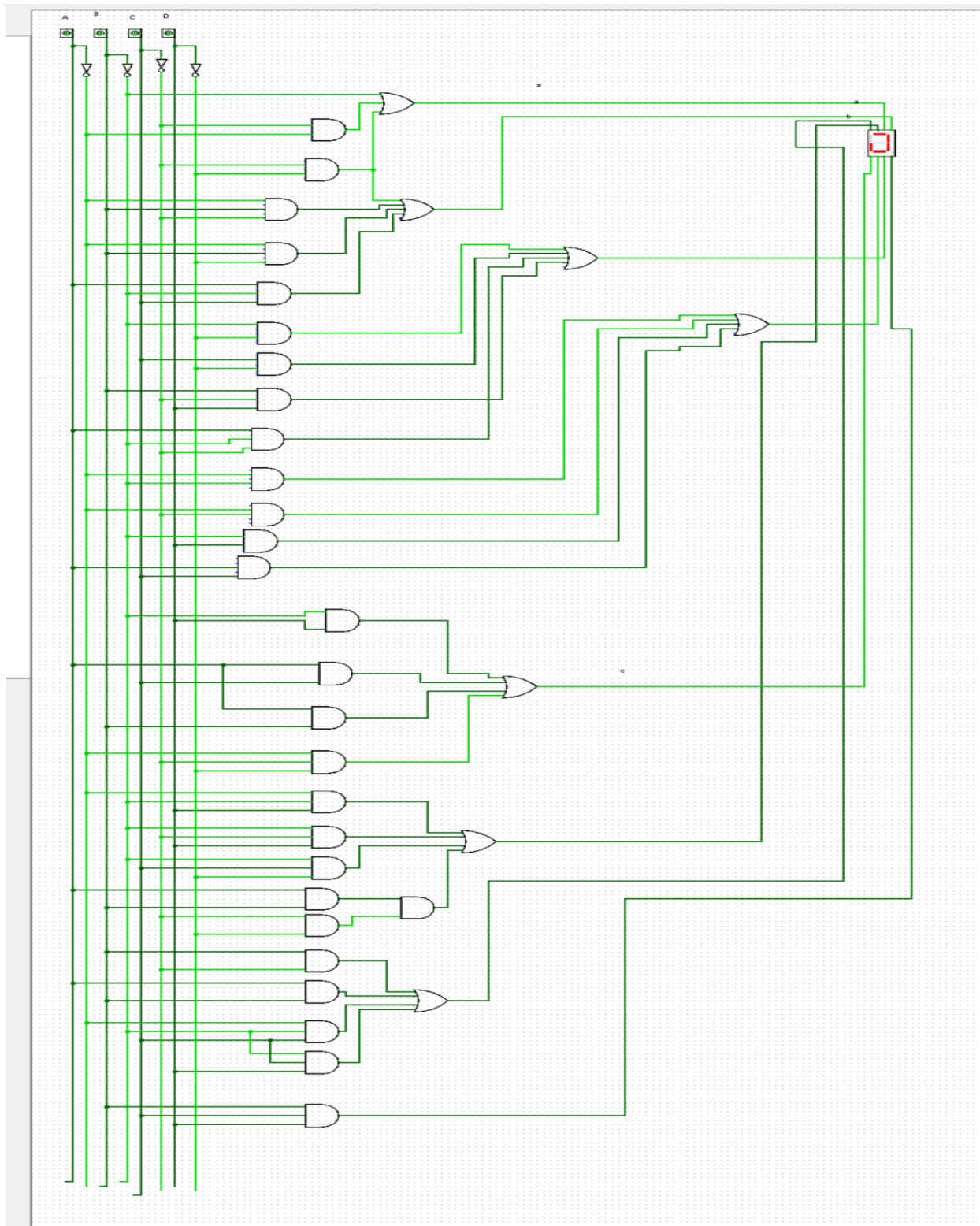
Decoder:
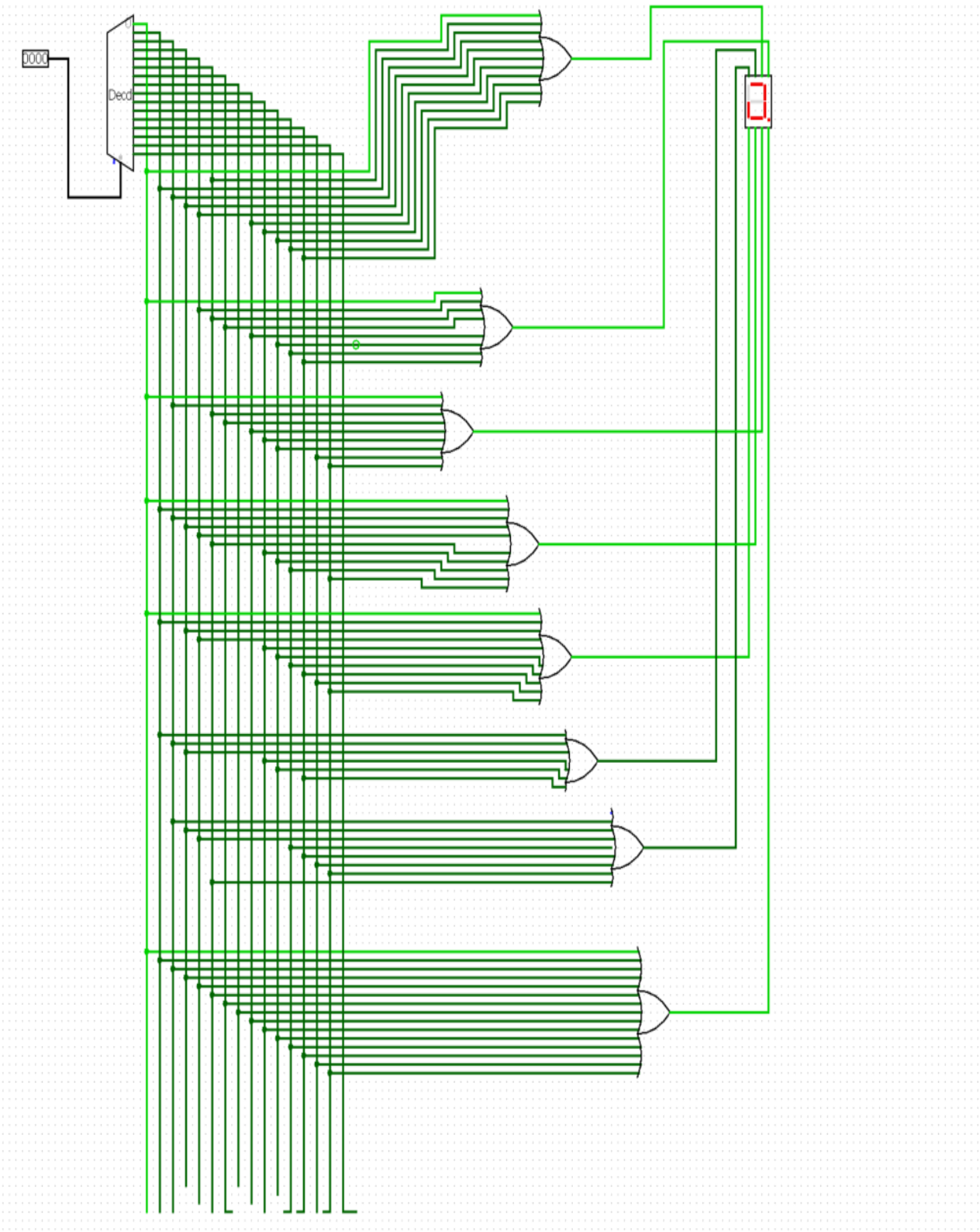
D Flip-Flop:
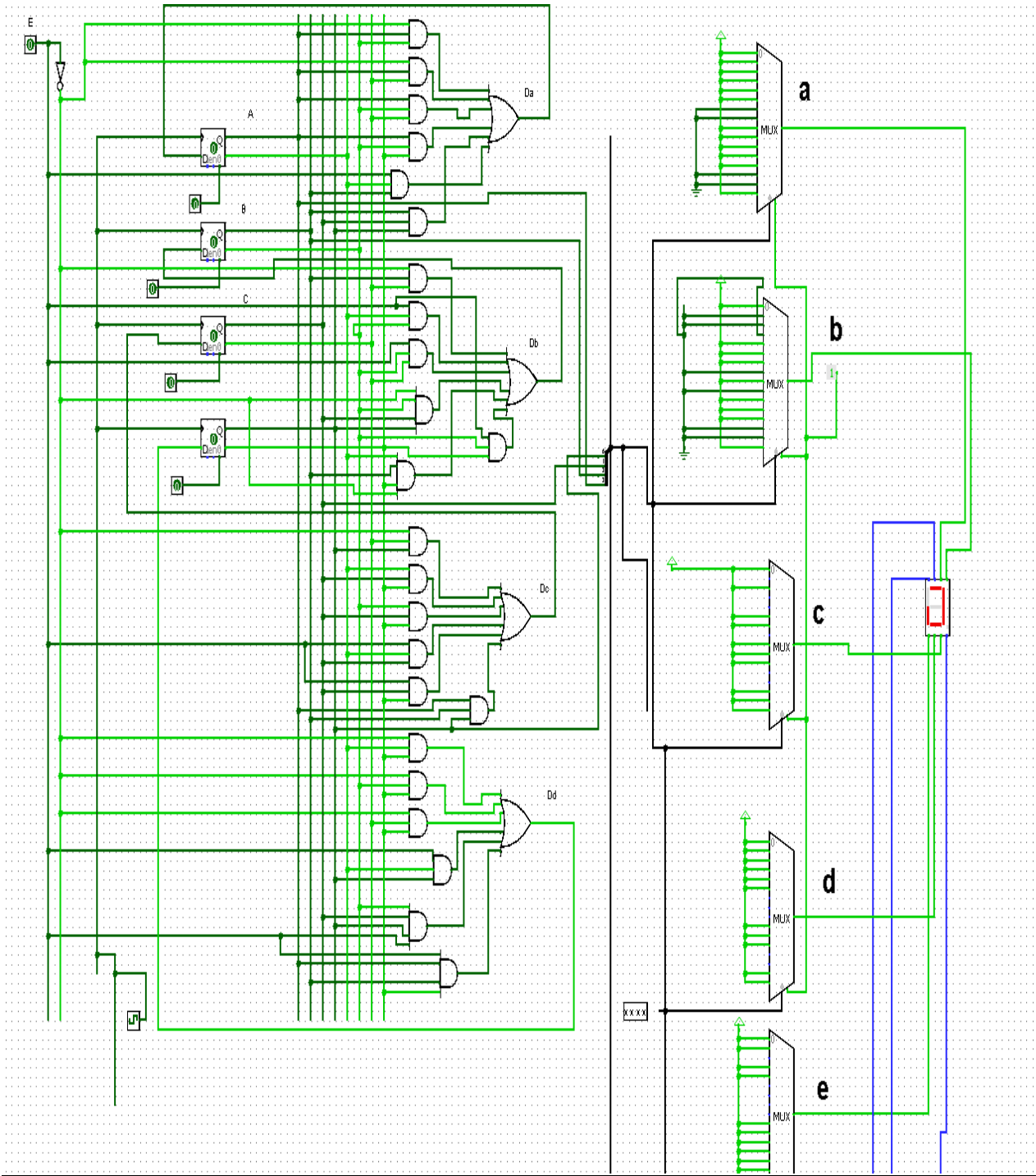
J-K Flip-Flop

T-Flip-Flop

Methodology:

1. First, we made the truth table of combinational part and implemented in Logisim.
2. Then we implemented the combinational part and made the 7-segment to print the accurate letters and number.
3. Then we made state table of sequential part.
4. Then we implemented the sequential part on Logisim and practically also.
5. Then we combined sequential with IC timer 555 and combinational implementations.

Success:

Our combinational part worked and showed result "CSE231.7G02ProJ" on 7-segment. But our sequential part didn't work fine and showed some of the letters and numbers sequentially of "CSE231.7G02ProJ".

Limitations and Problems:

We faced some of power supplying issues and IC complications. We supplied 5volts power in our project which sometimes showed weaker outcome. Due to our insufficient plans and programs, our budget costs got a pretty rise in amount.

Budget/cost estimation:

Item	Price	Unit	Item Cost
Bread Board	95	10	950
IC 7432	25.59	2	51.18
IC 7404	25.59	1	25.59
IC 7408	23.59	2	47.18
IC 7411	24.9	7	174.3
IC 74107	24.4	2	48.8
IC 74150	145.9	8	1167.2
IC 555	10.7	1	10.7
Seven Segment	9.85	1	9.85
Capacitor(22uf)	3.7	1	3.7
Jumper Wire	50	8	400
Resistor 10k	1.25	2	2.50
LED	1.31	4	5.24
		Total	2896.24

Project Photos:
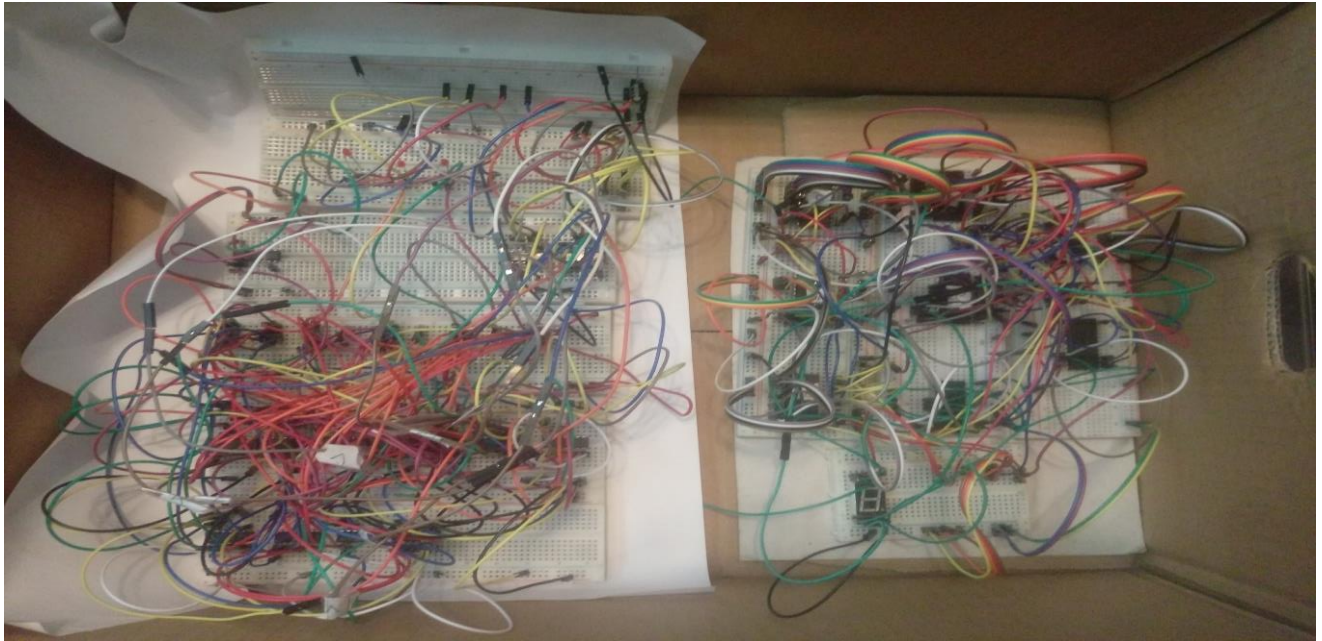
Discussion:

Through this project we learnt about many kinds of problems of digital logic design and now we know that how to solve those problems. Doing such kind of project make us more efficient to work. Now we have a clear idea about how seven segment, combinational circuit and sequential circuit works. Combinational circuit is combine of a,b,c,d to control the seven segment and display "CSE231.7G02ProJ". And in sequential circuit a,b,c,d is sequentially initialized from 0 to 15 and display "CSE231.7G02ProJ" on seven segment display. The sequential circuits and combinational circuits are been used in the displays such as boarding flights, bus stations, in weight machines, in weather forecast instruments etc.